A. Raja Ravi Venkat Sai

arrvsai@gmail.com — +91-7008247525
github.com/raviloggg — linkedin.com/in/a-raja-ravi-venkat-sai-324971233

Education

C V Raman Global University, Bhubaneswar Sept 2021 – Expected May 2025
B.Tech in Electronics and Communication Engineering GPA: 8.0
Cohen International School (CBSE, Class XII) Apr 2020 – Mar 2022
Percentage: 75%

Key Skills

Programming Languages: C, C++, MATLAB
Software/Tools: STM32CubeIDE, Autodesk Eagle, Cadence Virtuoso, Makerchip IDE
Frameworks/RTOS: FreeRTOS, Zephyr, Mbed OS
Expertise: Embedded Systems, IoT Development, Bare-metal Programming, FPGA/VLSI Design, Digital Signal Processing
Hardware: STM32, ESP32, RISC-V, SystemVerilog, TL-Verilog

Experience

Project Intern — IIT Bhubaneswar Sept 2025 – Present
- Developing RISC-V based IoT solutions for scalable, future-ready embedded systems.
- Designing and testing RISC-V modules with SystemVerilog for hardware implementation.

Winter Intern — IIT Bhubaneswar Nov 2024 – Dec 2024
- Built an FPGA-based Smart Padlock System for secure password validation using RISC-V.
- Applied open-source hardware tools (Makerchip IDE) for digital design and verification.

Summer Intern — East Coast Railways May 2025 – July 2025
- Worked on large-scale signal and telecommunication networks (OFC and LAN).
- Gained hands-on exposure to railway signaling systems ensuring safe and reliable operations.

Projects

RISC-V Based IoT Prototype (Ongoing)
- Prototyping a self-driving RC car to support differently-abled individuals using RISC-V and IoT.
- Implementing autonomous navigation features with real-time sensor integration.

FPGA-Based Smart Padlock System — IIT Bhubaneswar
- Designed a password-protected smart lock on FPGA using TL-Verilog.
- Integrated a RISC-V processor for secure input handling and authentication.
- Validated design through simulation and FPGA prototyping.

Signal Generation System using STM32
- Developed a signal generation system with STM32 using DAC, UART, and interrupts.
- Implemented lookup tables for sine, cosine, and triangular waveforms.
- Achieved precise waveform synthesis via ISR-based DAC output control.

Positions of Responsibility

Vice President — NSS, CV Raman Global University Sept 2025 – Present
- Leading NSS initiatives, coordinating volunteers, and organizing blood donation camps.

Core Member — Space Club, CV Raman Global University Sept 2025 – Present
- Achieved ASOC certification in satellite launch operations.
- Collaborated on research initiatives and hands-on space-tech activities.

Certifications

- IIT Bhubaneswar Internship: FPGA VLSI project on Smart Padlock with RISC-V integration.
- GIAN Short Course (IIT Bhubaneswar): Next-Generation Semiconductors – RISC-V, AI, and TL-Verilog (Feb 2025).
- Embedded C Internship (CGU): Training + mini-project on embedded programming.
- AI/ML Workshop by IOE: Hands-on exposure to ML models and AI applications.