# Day 5

**## Final step for RTL2GDS using tritinRoute and openSTA**

**The final step in Physical design would be routing and Design Rule check (DRC). Global and detailed routing was performed using tritinRoute . After that Static Timing Analysis was performed using openSTA. And the DRC checks was applied to ensure that layout matches he schematic and adheres to design rules.**

**### 1. Routing:**

Routing involves establishing the physical connections between various circuit elements (standard cells, macros, I/O pins) on a chip layout according to the netlist generated during the synthesis and placement phases. This step ensures that all the electrical connections are correctly implemented while adhering to design rules and optimizing for performance metrics like timing, power, and area. The path between one source and target should be the shortest and the same is explained by Lee algorithm.

#### Lee algorithm

It is an algorithm for maze routing, used to find paths for routing nets on a chip. It guarantees to find the shortest path between two points if one exists and is particularly useful for ensuring that routing respects design rules.

Till lab 4 we have executed the CTS, now we for executing routing, the first step would be to generate Power distribution network (PDN) by using following commands:

docker

.flow.tcl -interactive

package require openlane 0.9

prep design picorv32a tag $date (date should be retrieved by executing ls)

echo $::env(CURRENT\_DEF)

A screenshot of a computer

Description automatically generated

gen\_pdn

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Description automatically generated

Write about result

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Description automatically generated

Below image shows that PDN is generated successfully.

A screenshot of a computer

Description automatically generated

The resulting file 15-pdn.def contains the information from cts.def as well as the power distribution network.

Below image shows README.md file located in the configuration folder of the OpenLANE directory. One can refer to this file to understand about the various switches available for routing.

A close-up of a computer screen

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There are two types of routing, one is global routing and second is Detailed routing. For default, global routing is used. Command to run default routing:

*run\_routing*

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After executing the command run\_routing our slack values is reduce to 8.24. And since we are getting positive slack value, it implies that there is no timing violation in the layout.

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Now, the next step is to do post-routing STA analysis, which involves the extraction of parasitic effects (SPEF). The extraction of file needs to be done outside of OpenLANE. Under the results>>routing folder, resulting .spef file can be located.

A screenshot of a computer

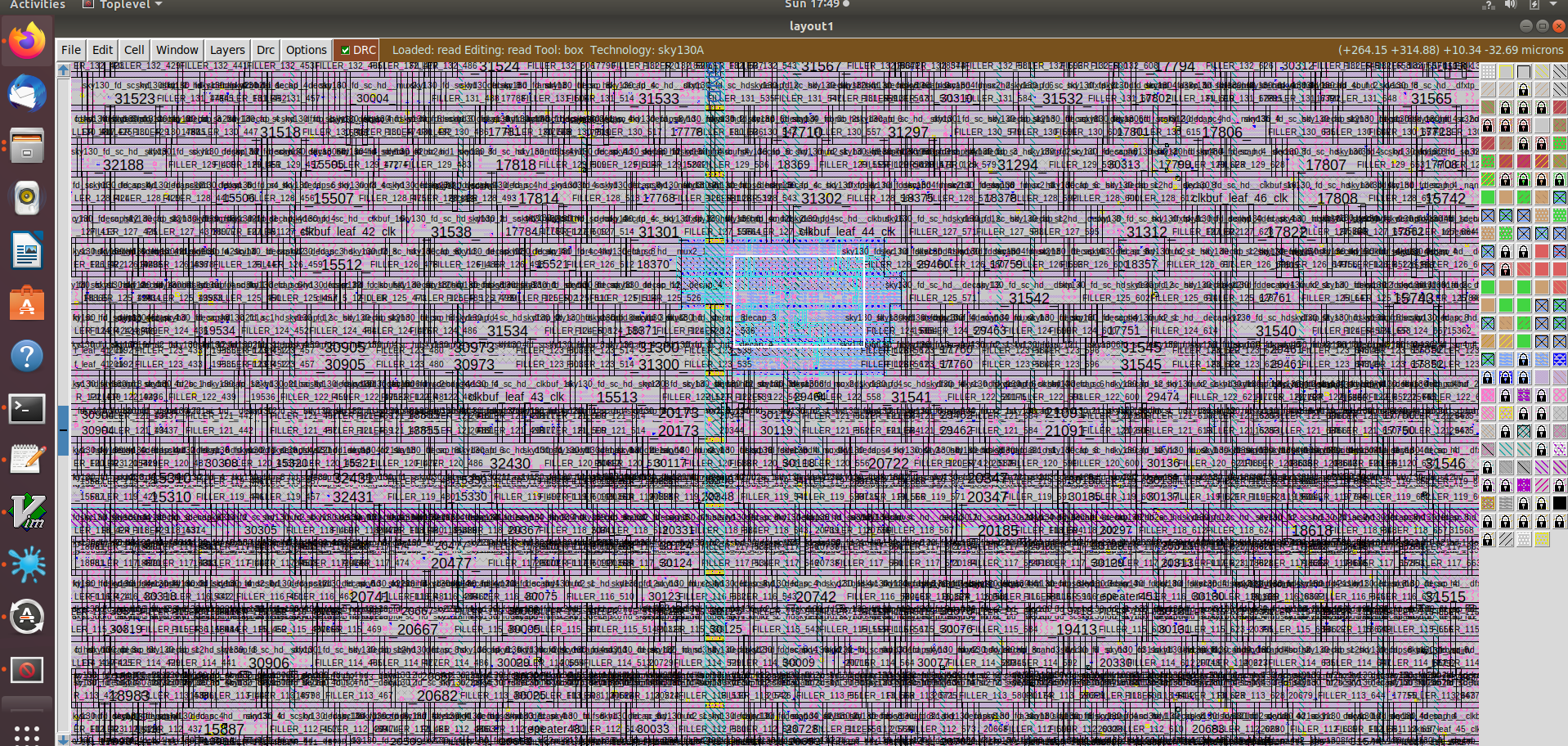
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This is the final generated layout after routing.

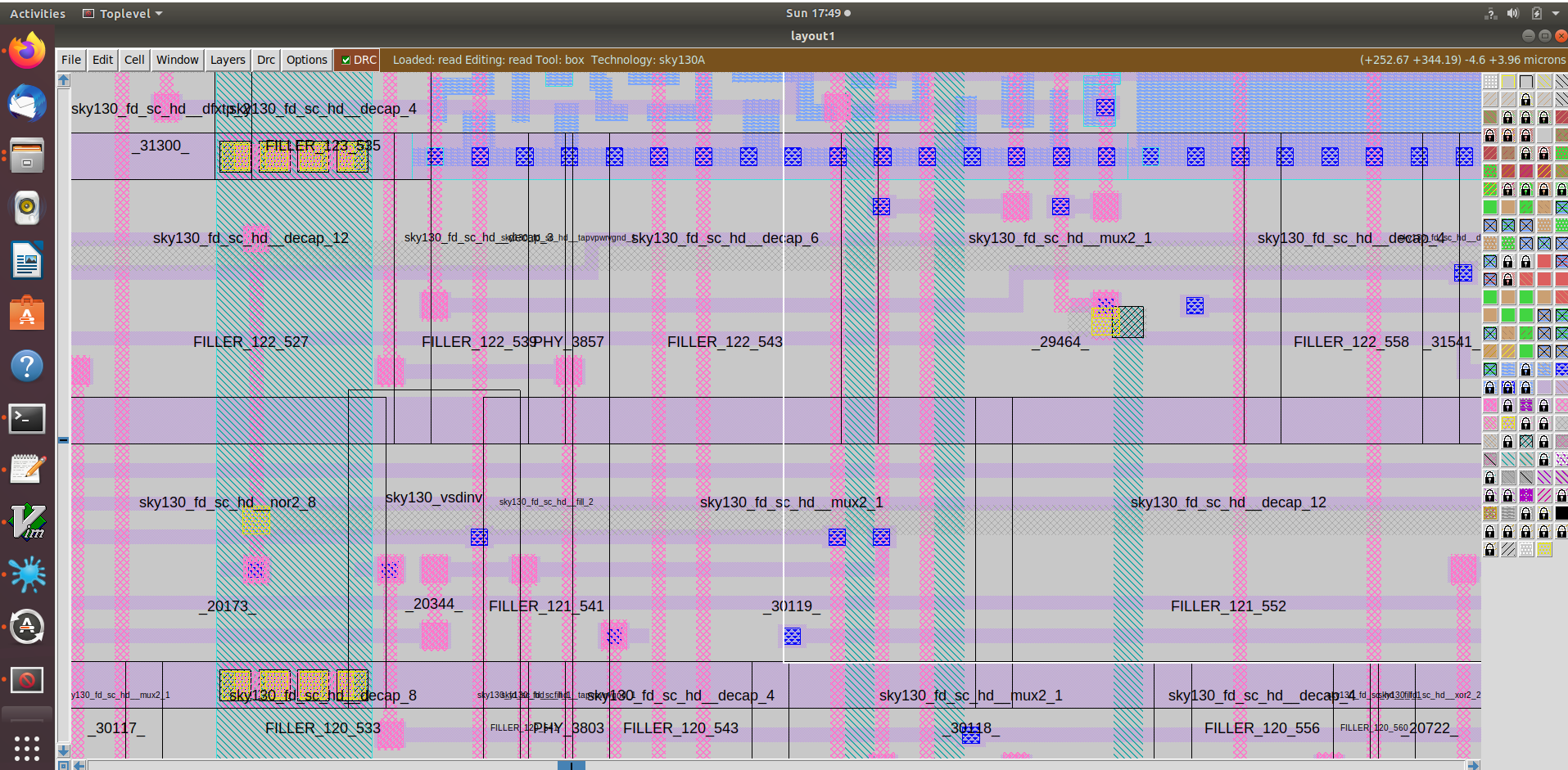
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Below image is the zoomed version of previous image.



Here we can easily see the routing between the macros and cell in the layout.



And, in the following image we can see routing through padding.

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So the final positive slack we are getting around 14 ns. Hence, there is no timing violation in the design. And our design will work perfectly.

