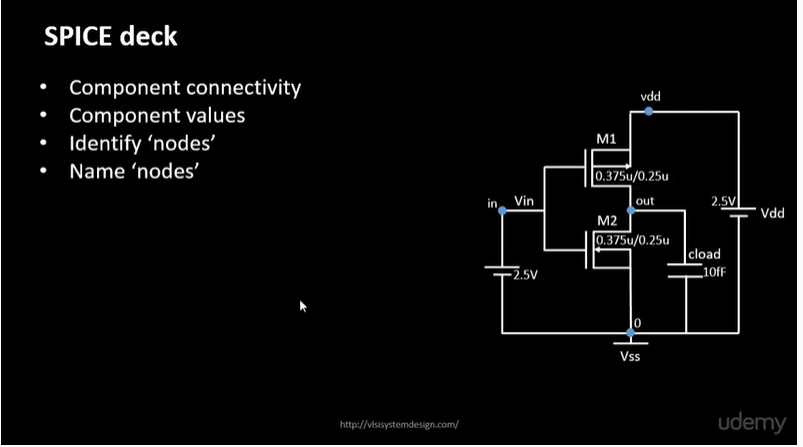
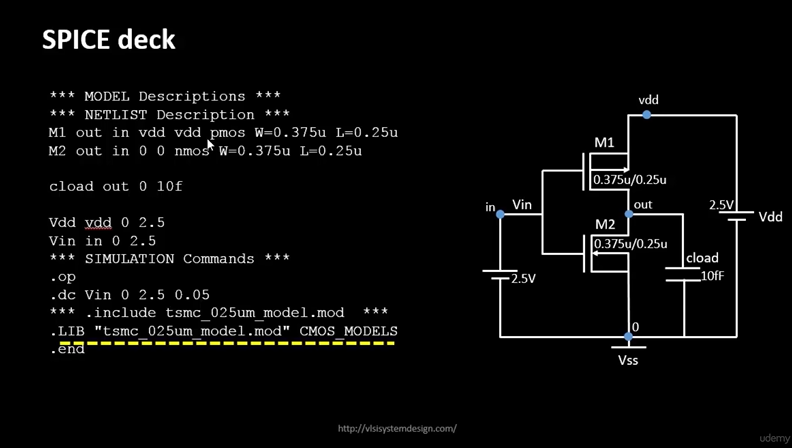
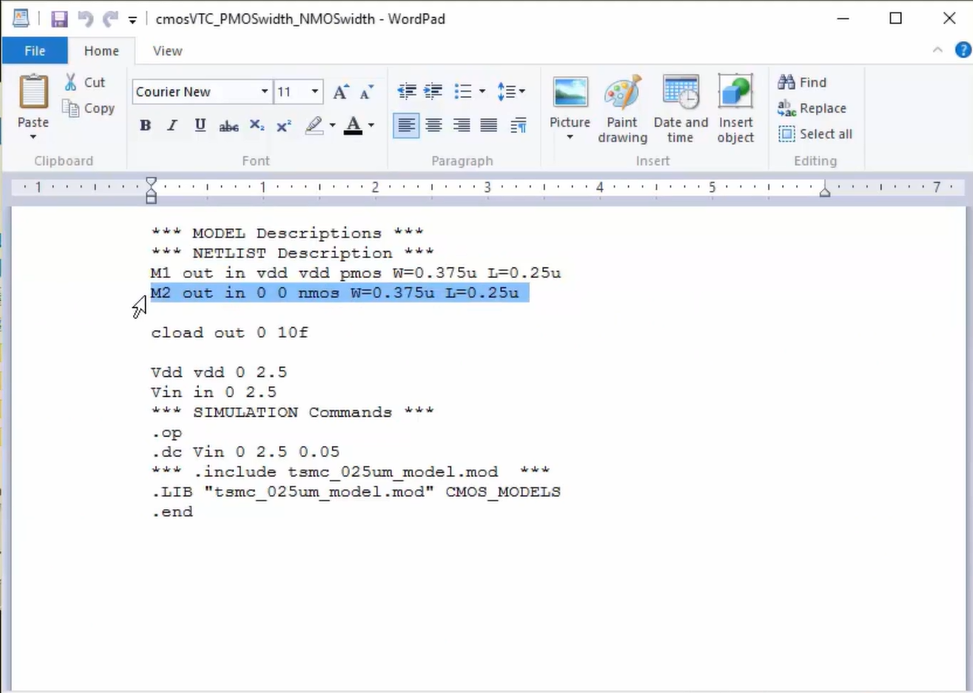
**DAY-3** **Design Library Using magic layout and Ng spice characterization.**

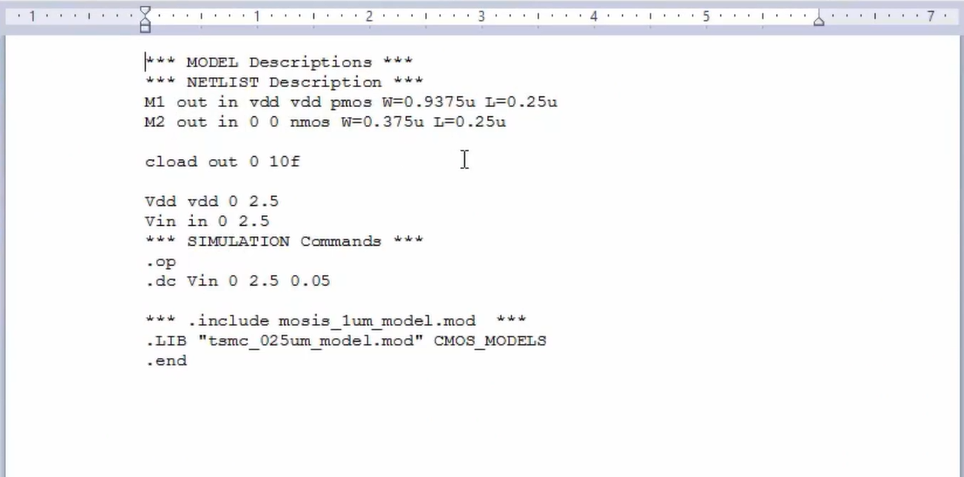
**L0 – SPICE DECK Creation for CMOS inverter**

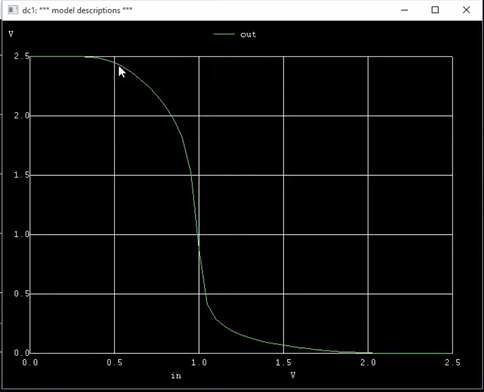
****creating a SPICE (Simulation Program with Integrated Circuit Emphasis) deck for a CMOS circuit involves defining the circuit components, their interconnections, and the simulation parameters.



**L1 – SPICE SIMULATION LAB FOR CMOS INVERTER**

1. When the width of the both n and p mos are same (wp =wn).
2. When width of n and p mos are not equal (wp = 2.5\*wn)



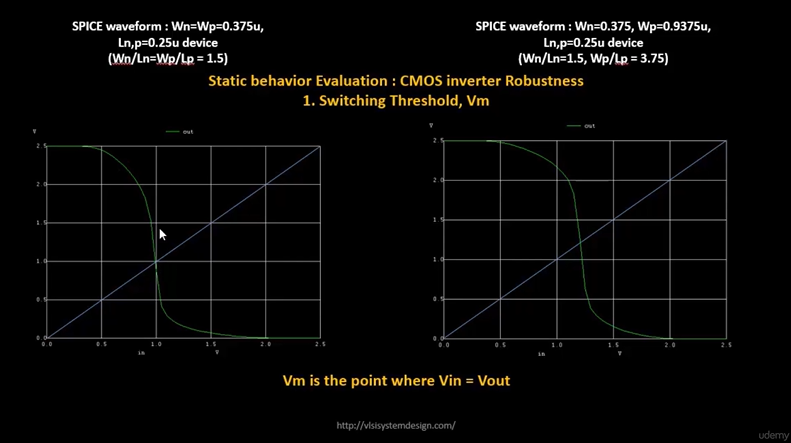
RESULTS OBTAINED –

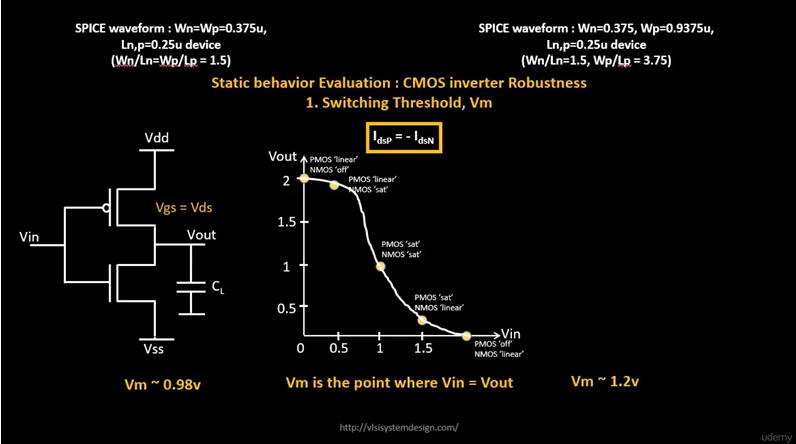
A graph on a black background

Description automatically generated

**L2 – SWITCHING THRESHOLD Vm**

The switching threshold 𝑉𝑚 of a CMOS inverter is the input voltage at which the output voltage is equal to the input voltage. At this point, the inverter is transitioning from one logic level to another (e.g., from high to low or low to high). The switching threshold is an important parameter because it defines the inverter's behaviour in terms of noise margin and signal integrity.

****



**L4 – Static and Dynamic simulation of CMOS inverter**

**A screenshot of a computer

Description automatically generated**

**L5 – LAB STEPS TO GIT CLONE vsdstdcelldesign**

1. Clone a custom inverter standard cell design from a GitHub repository.

**# Change directory to openlane**

cd Desktop/work/tools/openlane\_working\_dir/openlane

**# Clone the repository with custom inverter design**

git clone <https://github.com/nickson-jose/vsdstdcelldesign>

**# Change into repository directory**

cd vsdstdcelldesign

**# Copy magic tech file to the repo directory for easy access**

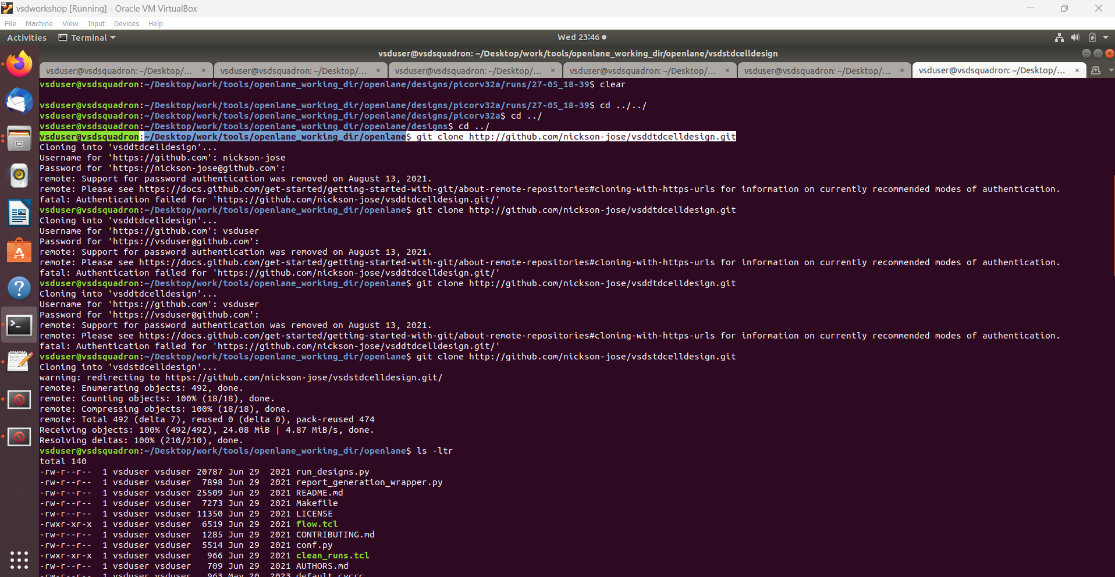
cp /home/vsduser/Desktop/work/tools/openlane\_working\_dir/pdks/sky130A/libs.tech/magic/sky130A.tech .

**# Check contents whether everything is present**

Ls -ltr

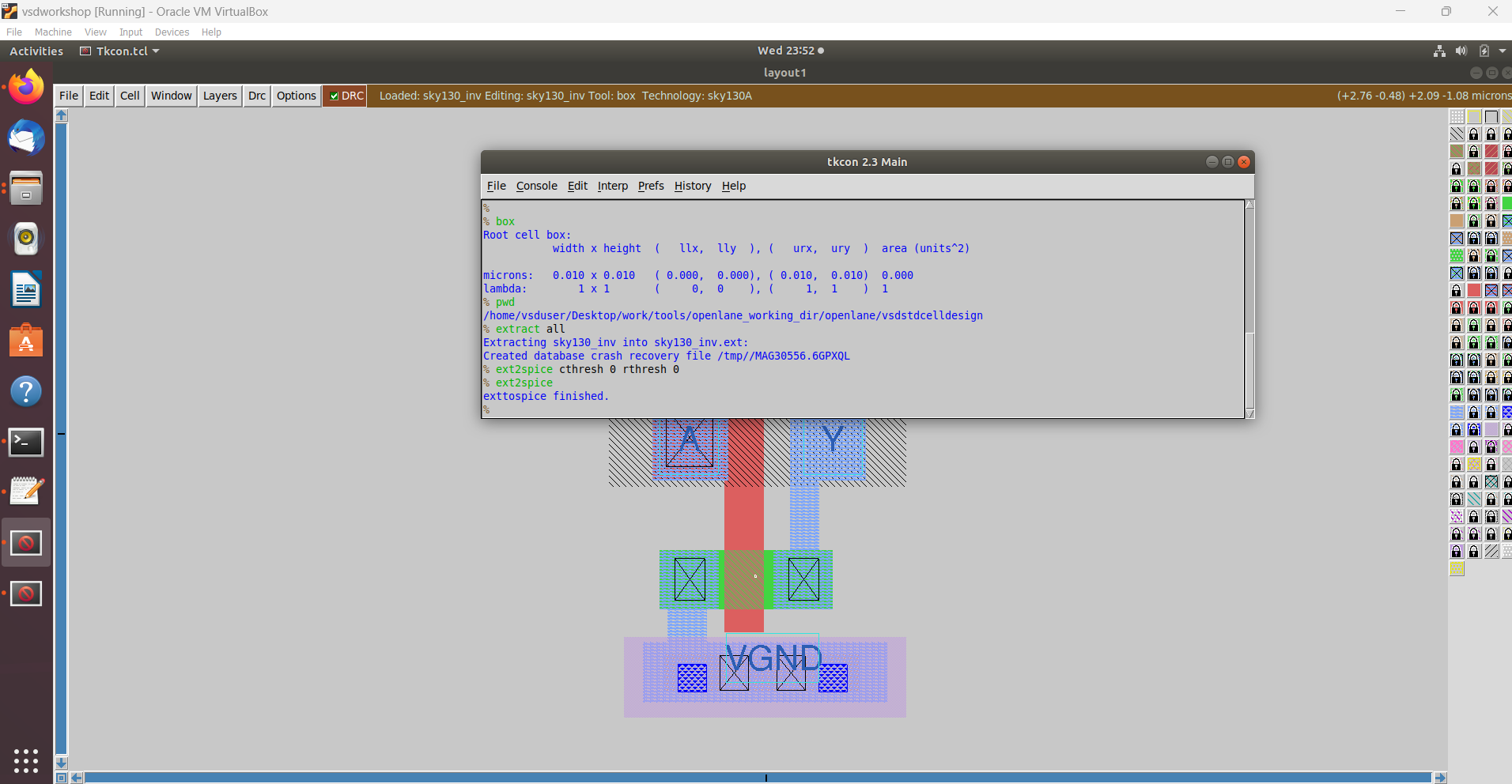
**# Command to open custom inverter layout in magic**

magic -T sky130A.tech sky130\_inv.mag &



1. Now we will load inverter layout in magic tool





1. SPICE extraction of an inverter using the Magic tool involves generating a SPICE netlist from the layout. **(#as shown in the above fig)**

**# Check current directory**

pwd

**# Extraction command to extract to .ext format**

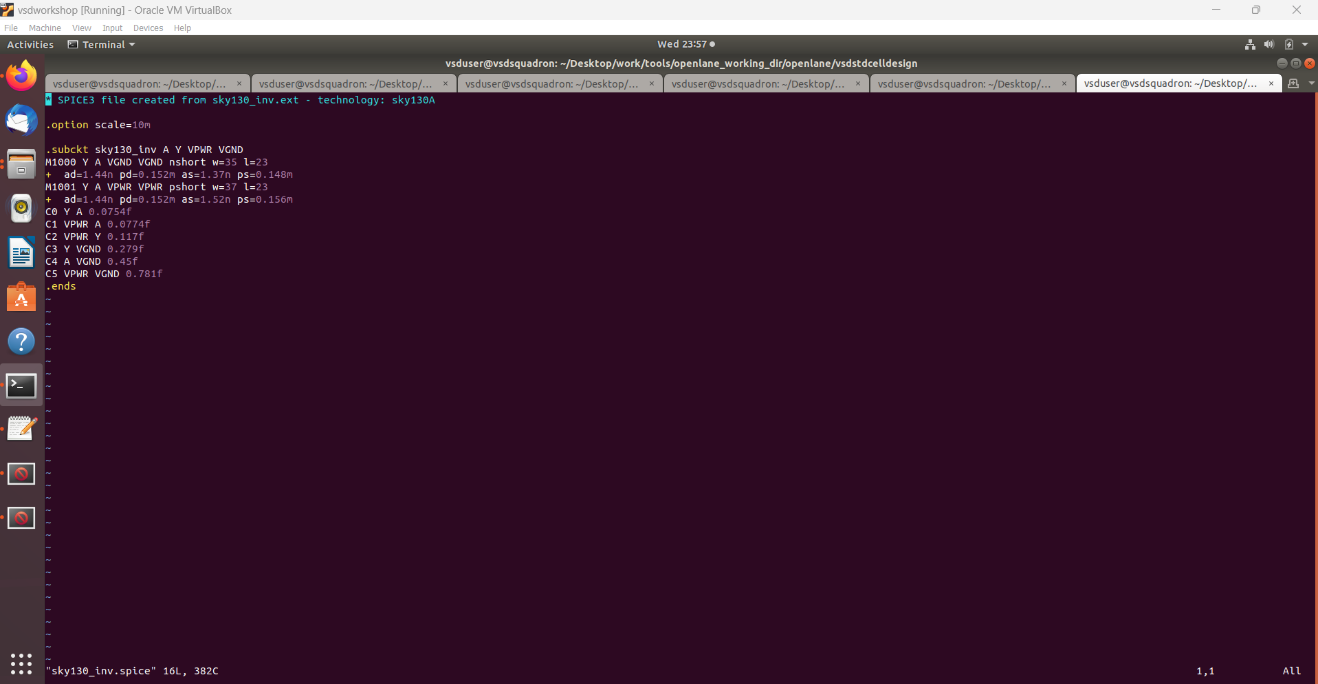
extract all

**# Before converting ext to spice this command enable the parasitic extraction also**

ext2spice cthresh 0 rthresh 0

**# Converting to ext to spice**

ext2spice

**# Here we used vim command to edit SPICE file**

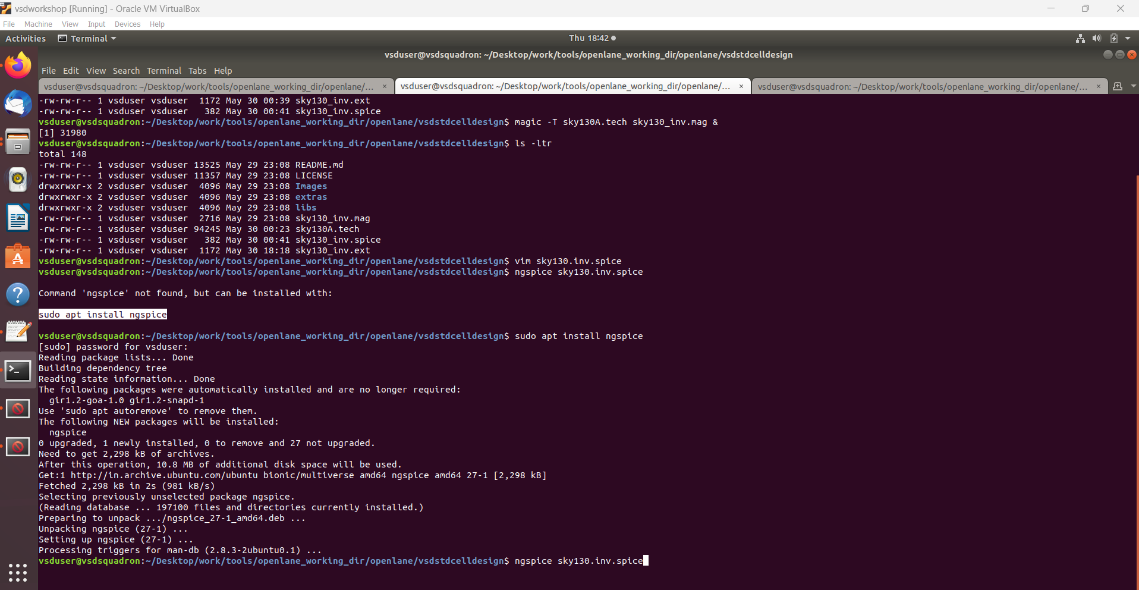
1. Post-layout ngspice simulations.

Here are the given commands to perform ngspice simulations

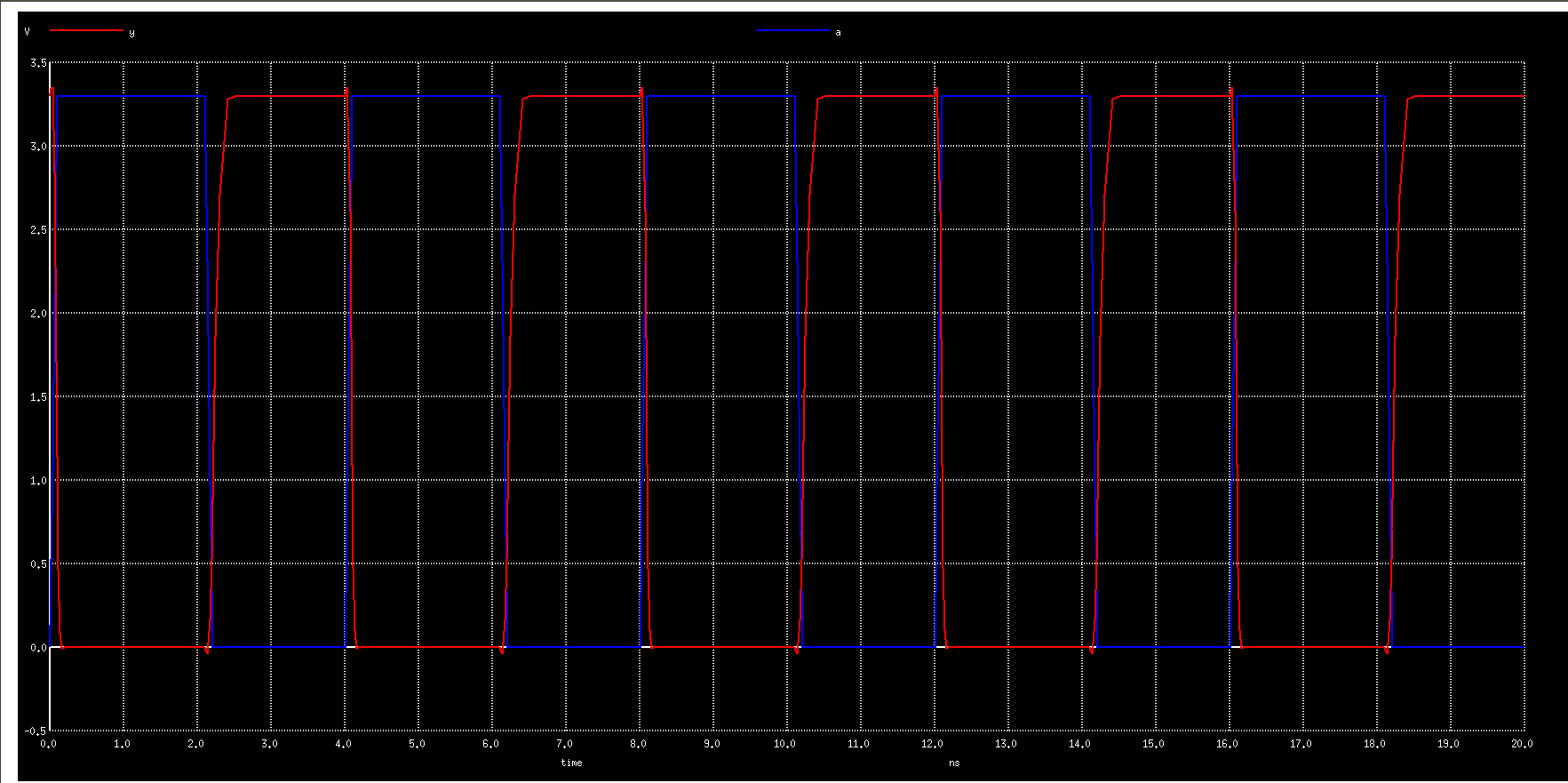
**# Command to directly load spice file for simulation to ngspice**

ngspice sky130\_inv.spice

**# Now that we have entered ngspice with the simulation spice file loaded we just have to load the plot**

plot y vs time a



Here I have given the screenshot of generated plot of O/P (a) vs O/P(y) -

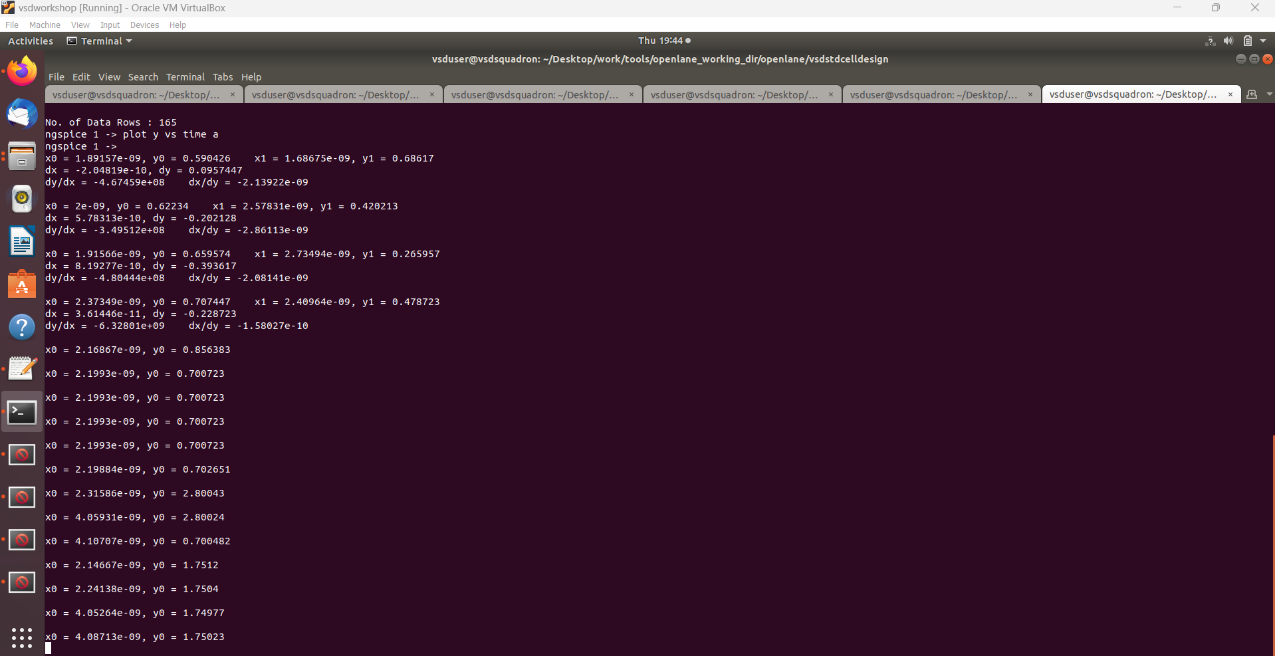
**ASSIGNMENT -1**

After getting plot we have to find out the value of 4 – parameter –

1. Rise Transition time.
2. Fall Transition time.
3. Fall cell delay.
4. Rise cell delay.

First let’s understand what are those delay means -

1. **Rise Transition time** - Rise transition time is the time it takes for a signal to transition from a low voltage level (typically 20% of the maximum value) to a high voltage level (typically 80% of the maximum value). It is a critical parameter in evaluating the speed and performance of digital circuits.
2. **Fall Transition time -** Fall transition time is the duration for a signal to change from a high voltage level (typically 80% of the maximum value) to a low voltage level (typically 20% of the maximum value). It is crucial for assessing the speed and performance of digital circuits.
3. **Fall cell delay –** Fall cell delay is the time it takes for a cell's output to transition from a high voltage level to a low voltage level after the input signal triggers the change.
4. **Rise cell delay -** Fall cell delay is the time interval between the input signal reaching a defined threshold and the output signal falling from a high to a low voltage level.



Inside the box we have desired values from the plot now we can calculate the delays –

X0 = 2.19884e-09 Y0 = 0.702651 X0’ = 2.31586e-09 Y0’ = 2.80043

**Rise Transition time(tr) = (X0’-X0) tr = 0.117 ns**

X0 = 4.05931e-09 Y0 = 2.80024 X0’ = 4.10707e-09 Y0’ = 0.700482

**Fall Transition time(tr) = (X0’-X0) tr = 0.0477 ns**

X0 = 2.14667e-09 Y0 = 1.7512 X0’ = 2.24138 Y0’ = 1.7504

**Rise cell delay (trc) = (X0’-X0) trc = 0.09471 ns**

X0 = 4.05264e-09 Y0 = 1.74977 X0’ = 4.08713e-09 Y0’ = 1.75023

**fall cell delay (tfc) = (X0’-X0) tfc = 0.035 ns**

1. **Identify issues in the Design Rule Check (DRC) section of the old Magic Tech file for the SkyWater process and correct them.**

Here are the following commands mentioned to download and view the corrupted skywater magic tech file –

**# Change to home directory**

cd

**# Command to download the lab files**

wget <http://opencircuitdesign.com/open_pdks/archive/drc_tests.tgz>

**# Since lab file is compressed command to extract it**

tar xfz drc\_tests.tgz

**# Change directory into the lab folder**

cd drc\_tests

**# List all files and directories present in the current directory**

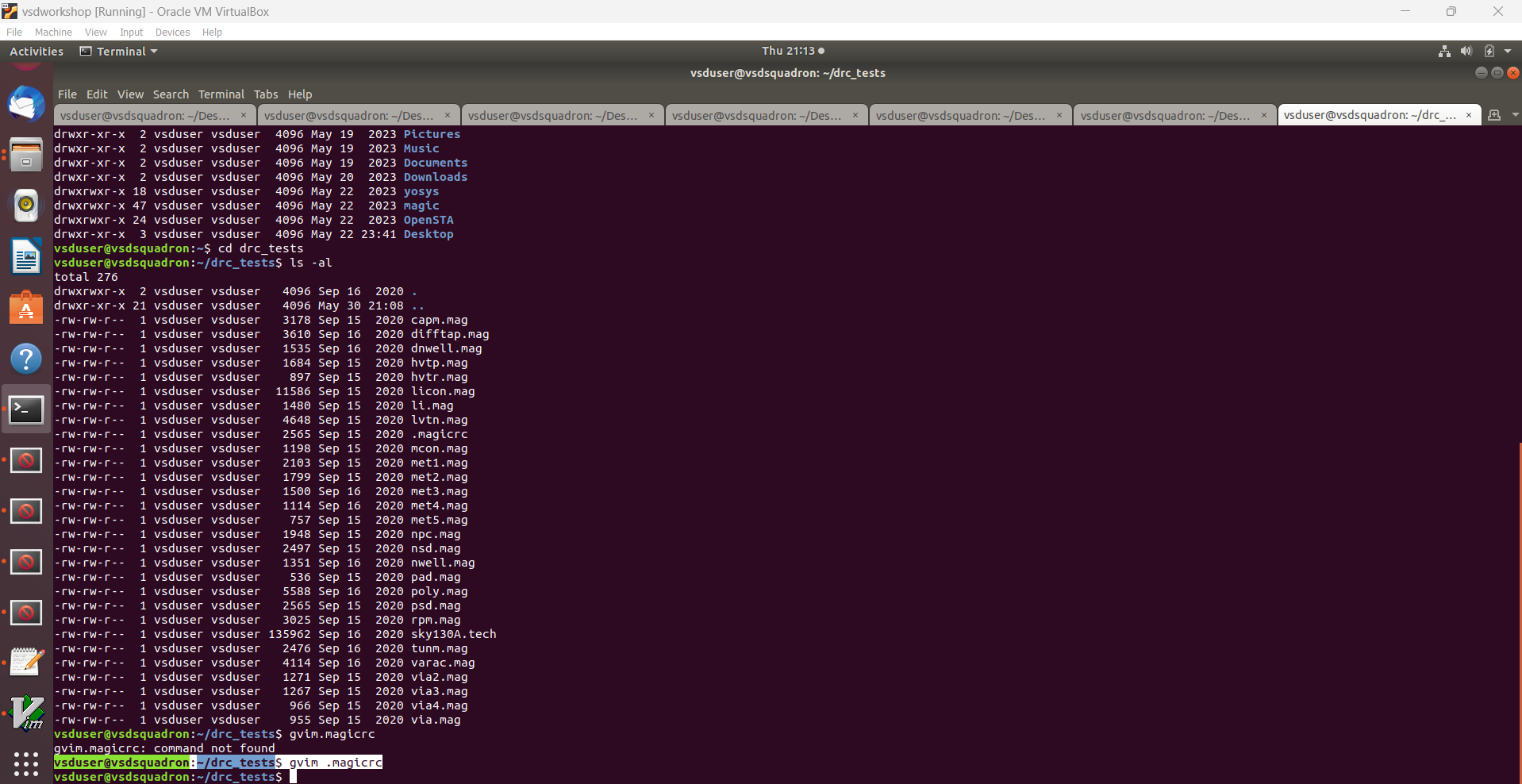
ls -al

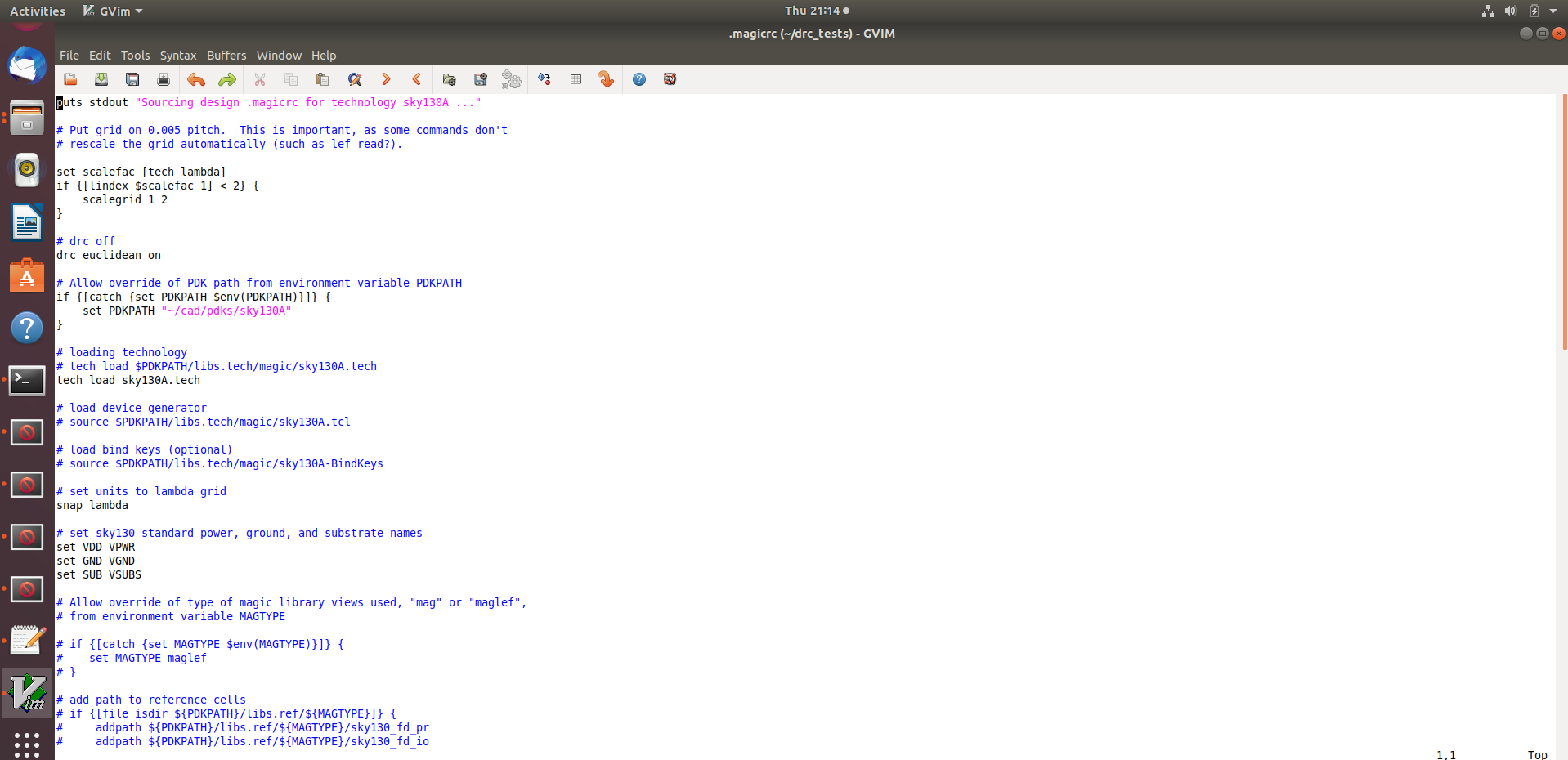
**# Command to view .magicrc file**

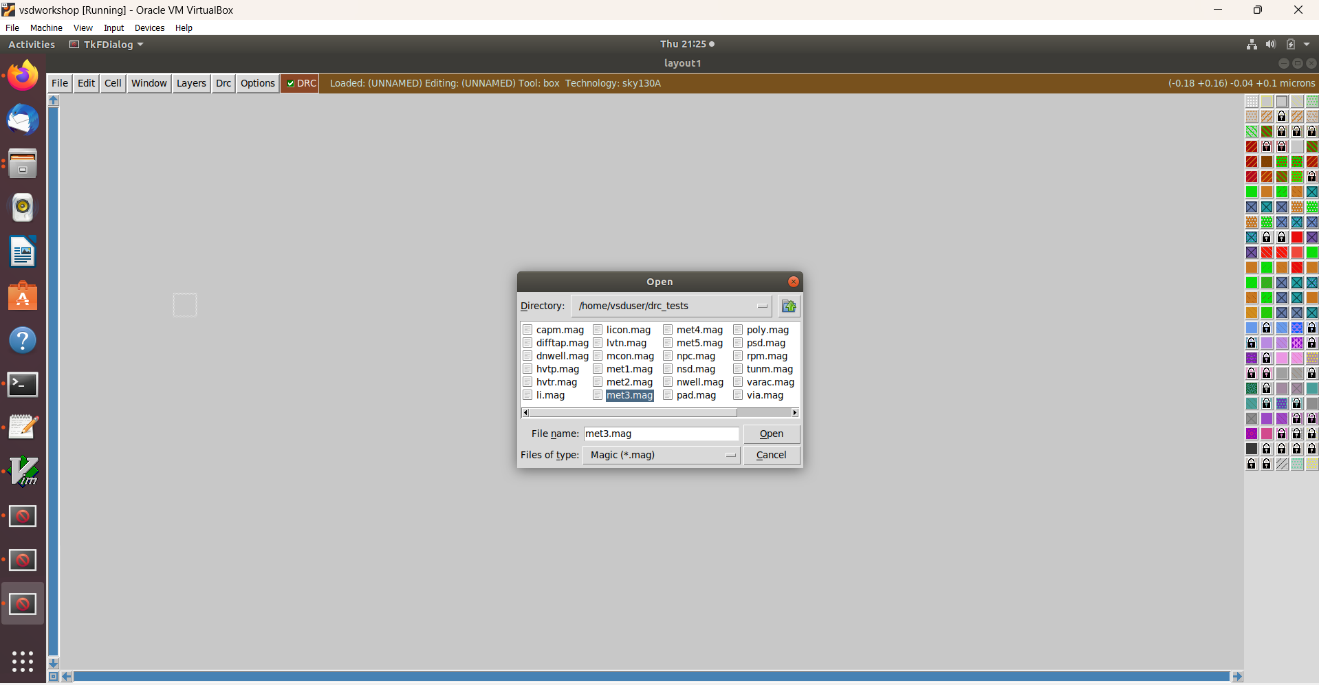
gvim .magicrc

**# Command to open magic tool in better graphics**

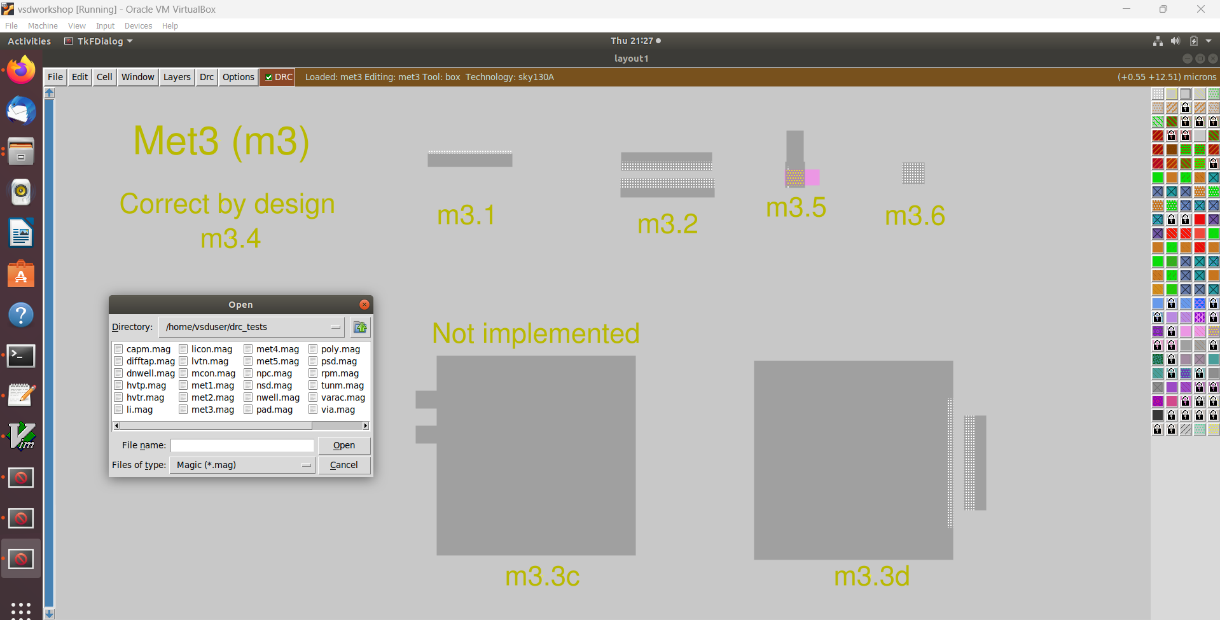
magic -d XR &



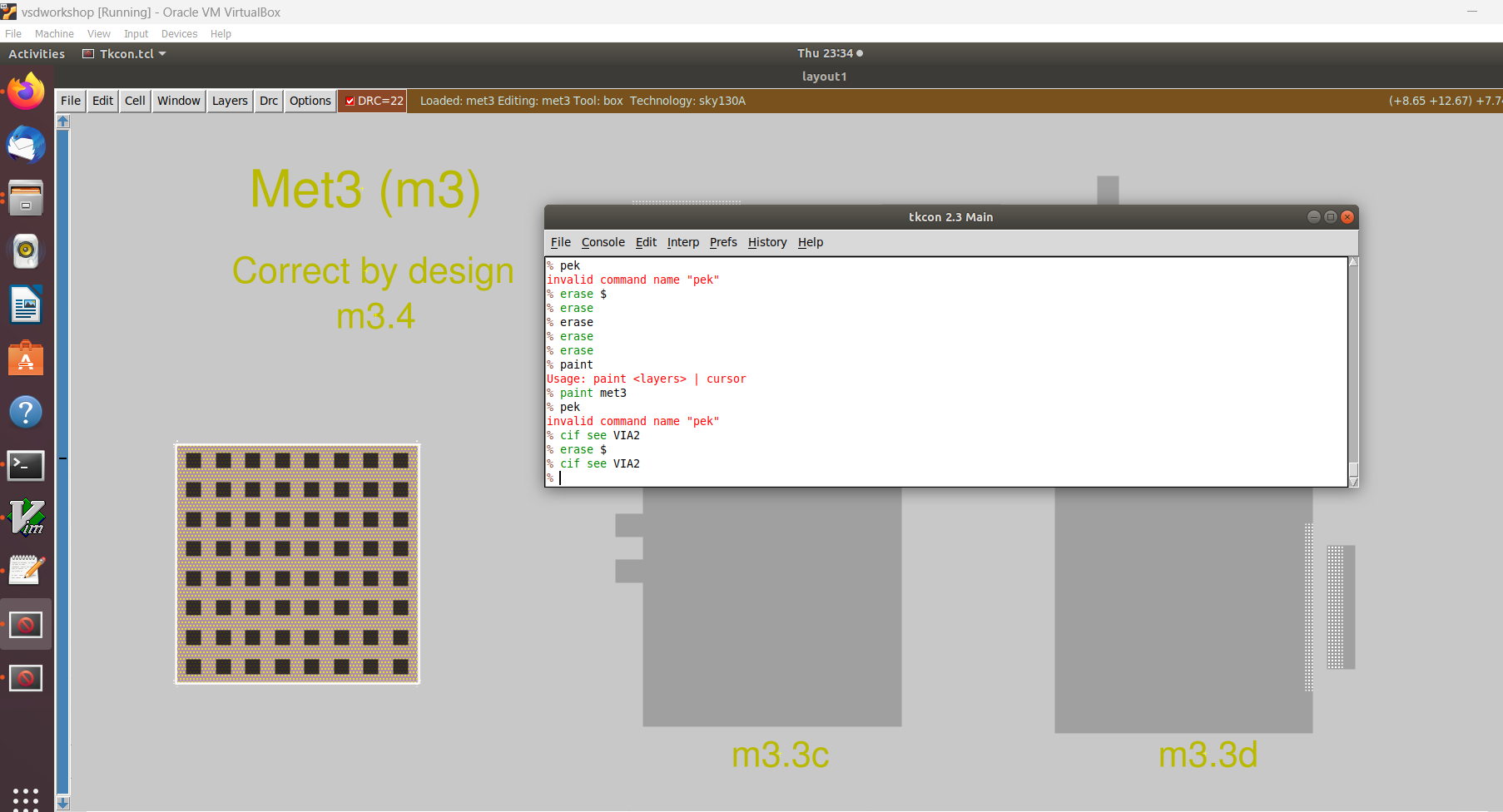
**.magicrc file**

open met3.mag file in magic tool as shown in below fig -

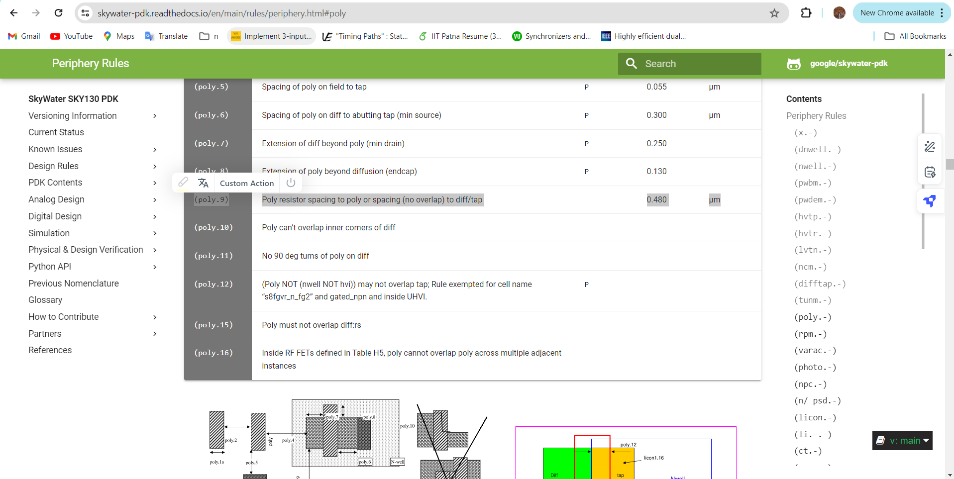
Different Layout and Different DRC as shown in below fig –

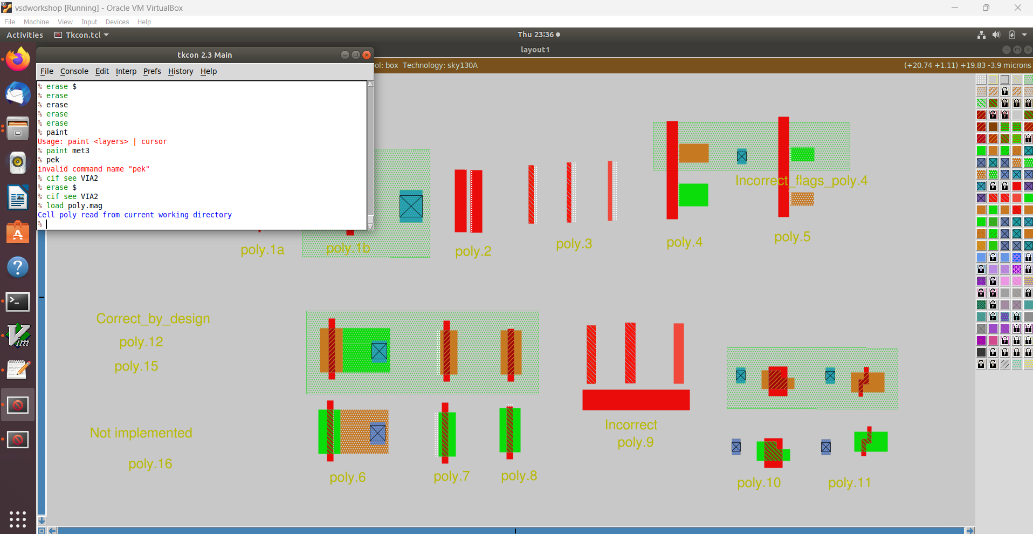


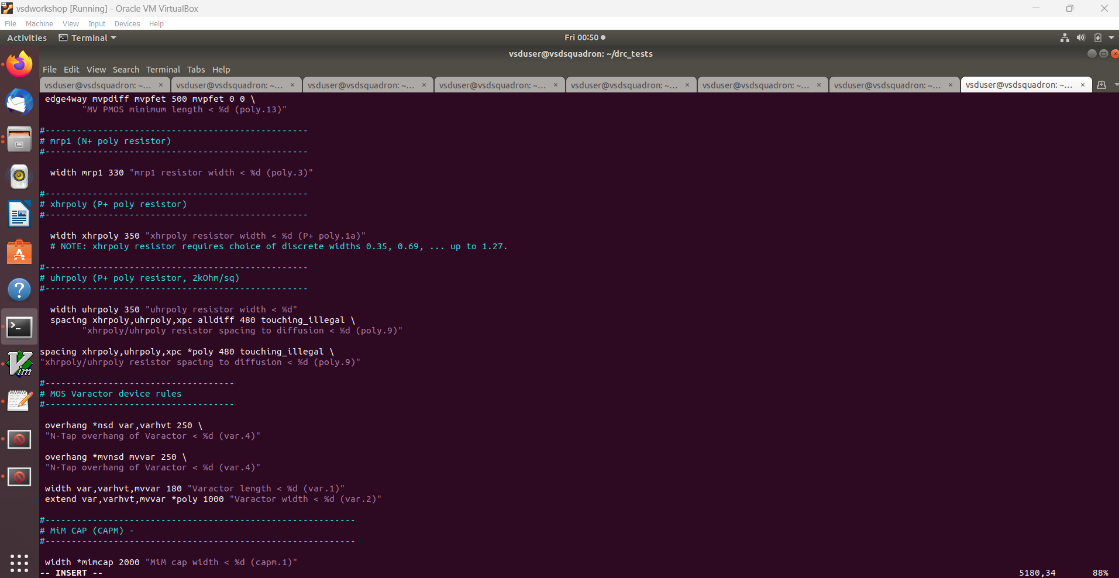
DRC for selected layout area -

VIA2 file -

Screenshot of poly rules and link is given below -

https://skywater- pdk.readthedocs.io/en/main/rules/periphery.html#poly

The difftap.2 rule is incorrectly implemented, resulting in no DRC violation even when the spacing is less than 0.42µm.

To update DRC new command is inserted using vim in sky130A.tech

**# Loading updated tech file**

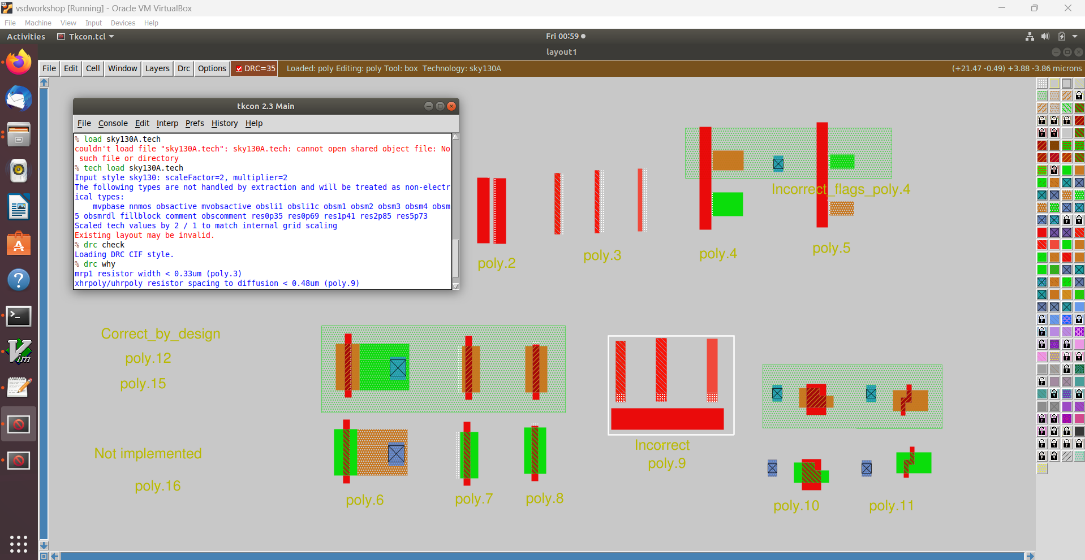
tech load sky130A.tech

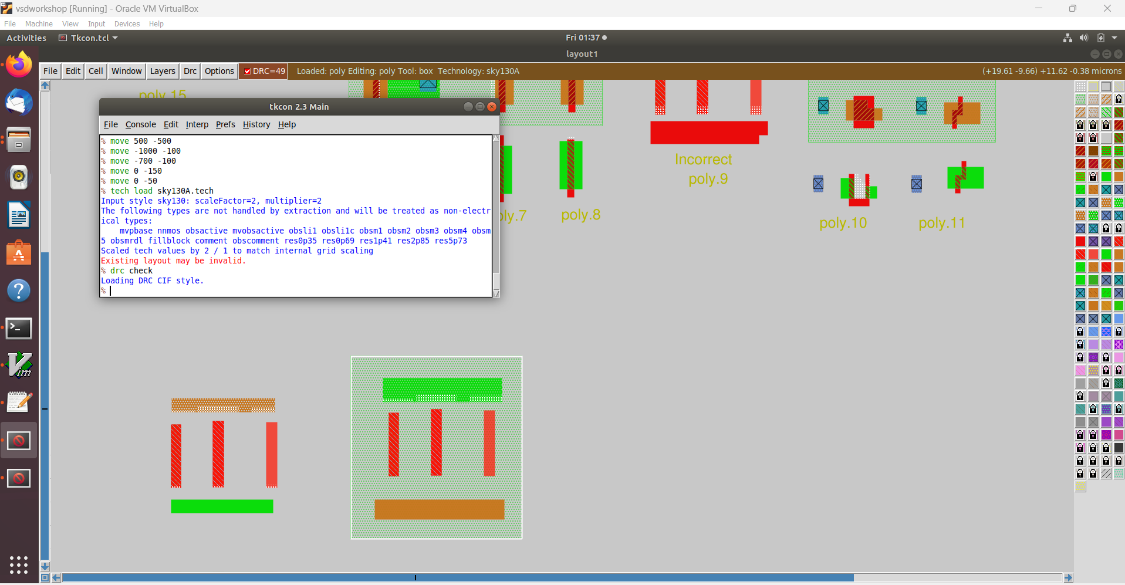
**# Must re-run drc check to see updated drc errors**

drc check

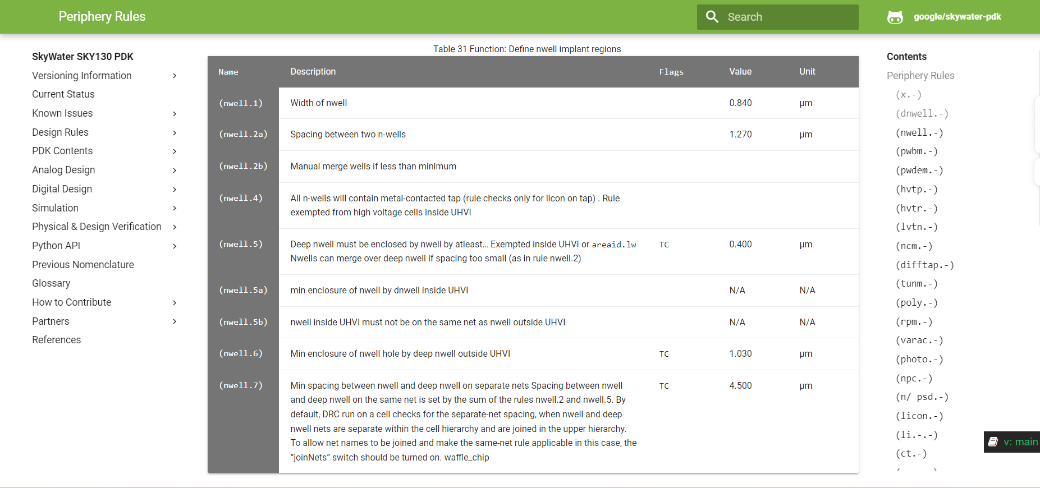
**# Selecting region displaying the new errors and getting the error messages**

drc why



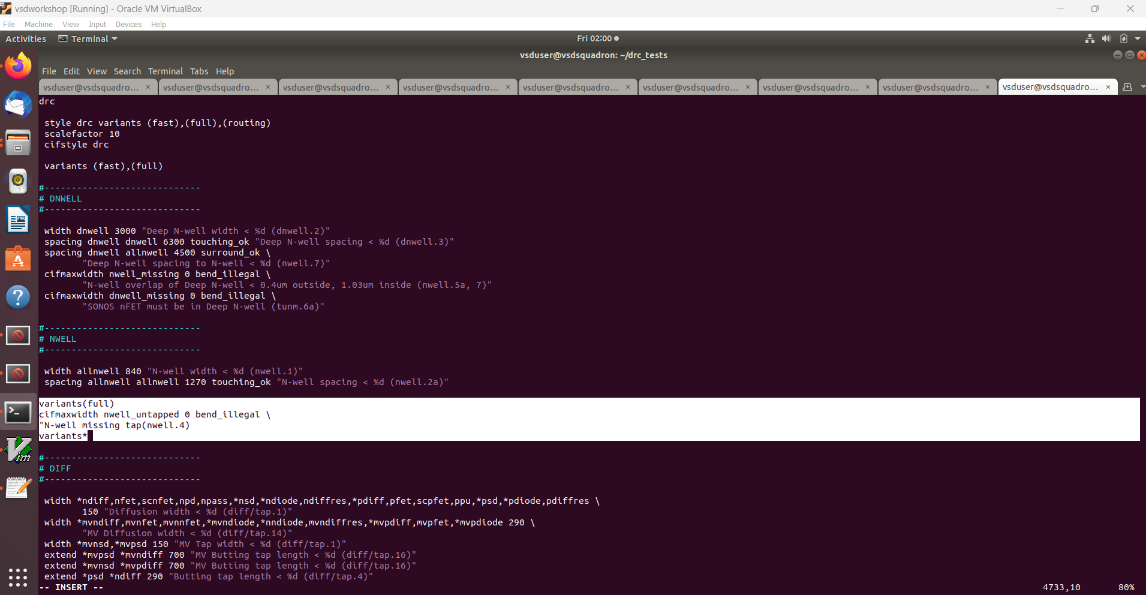


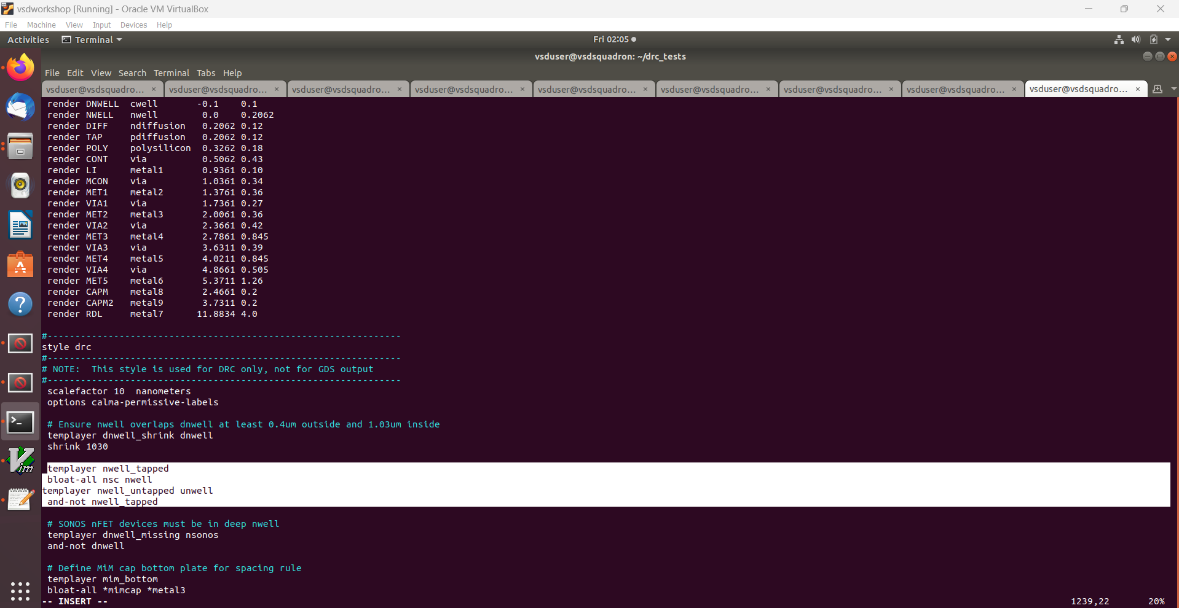
Incorrectly implemented nwell.4 complex rule correction –

These are the following nwell rule -

Incorrectly implemented nwell.4 rule no drc violation even though no tap present in nwell –

To update DRC new command is inserted in sky130A.tech file





Command to run in magic tkcon window –

**#Loading updated tech file**

tech load sky130A.tech

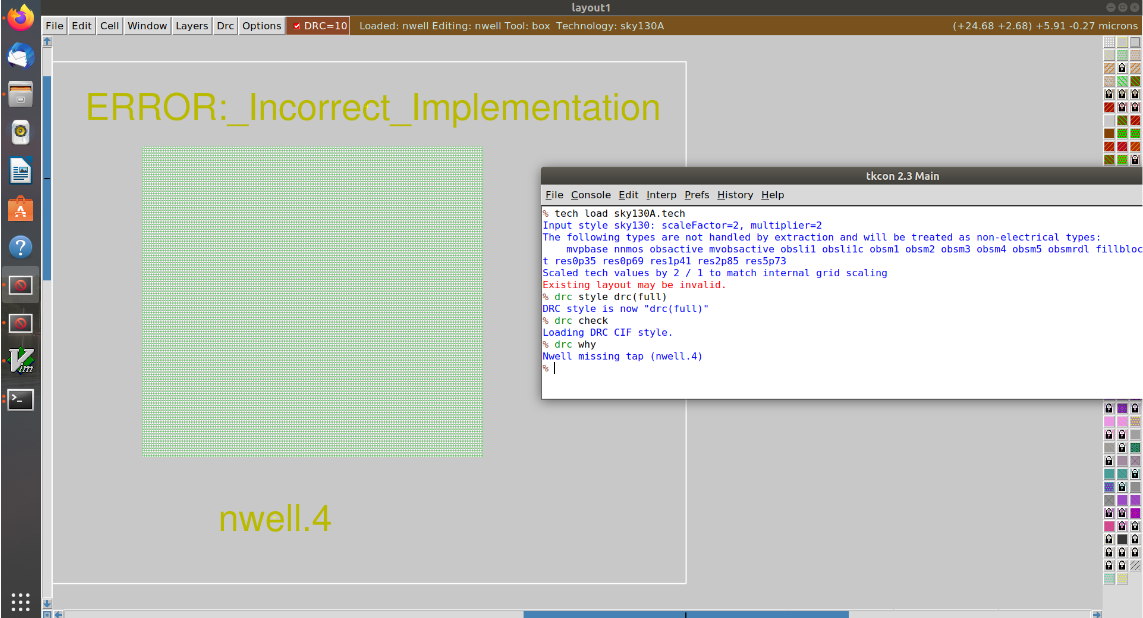
**#change drc style**

drc style drc(full)

**#check drc**

drc check

**#See errors in selecting area**

Drc why