# Logic Families

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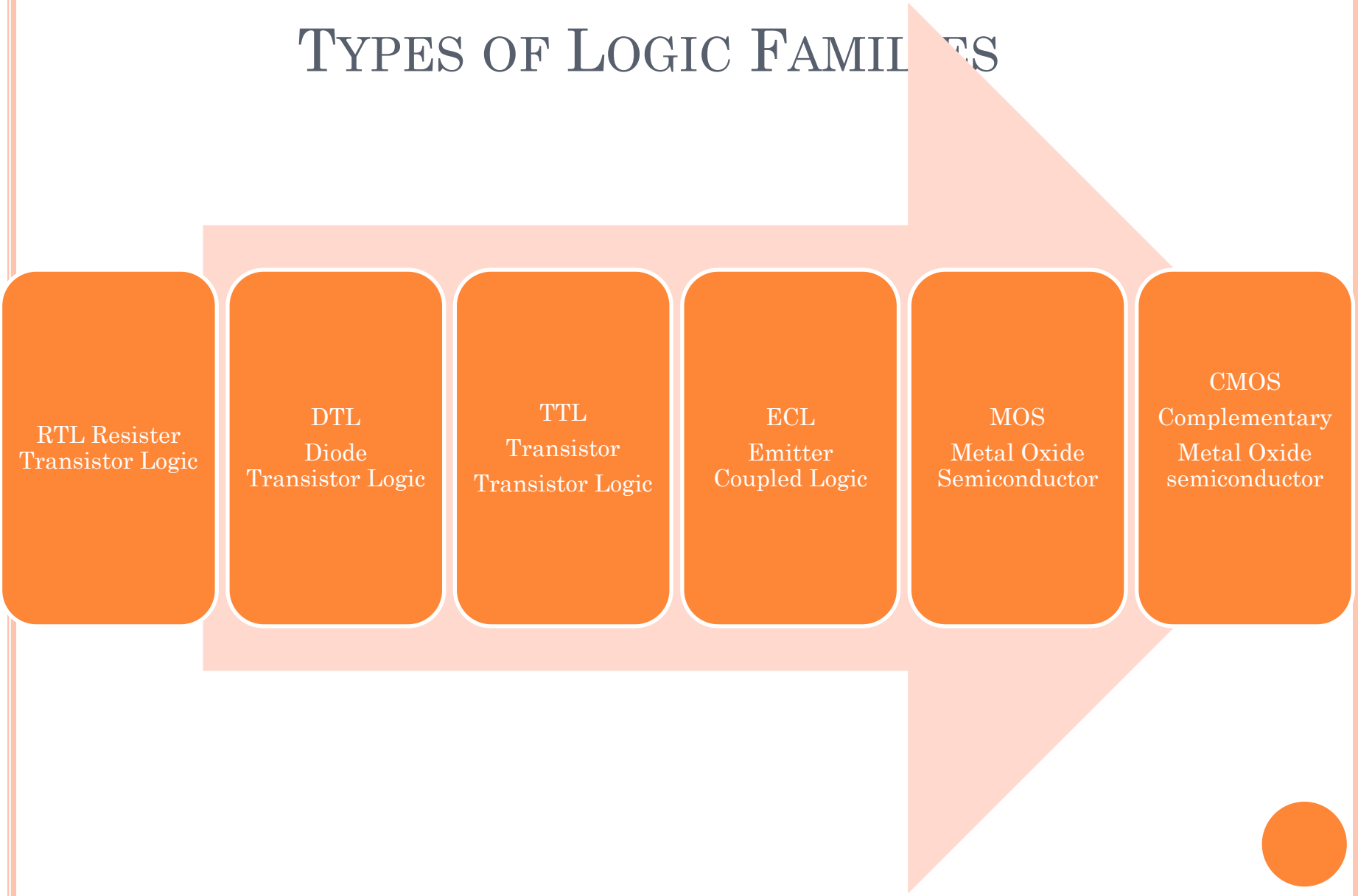
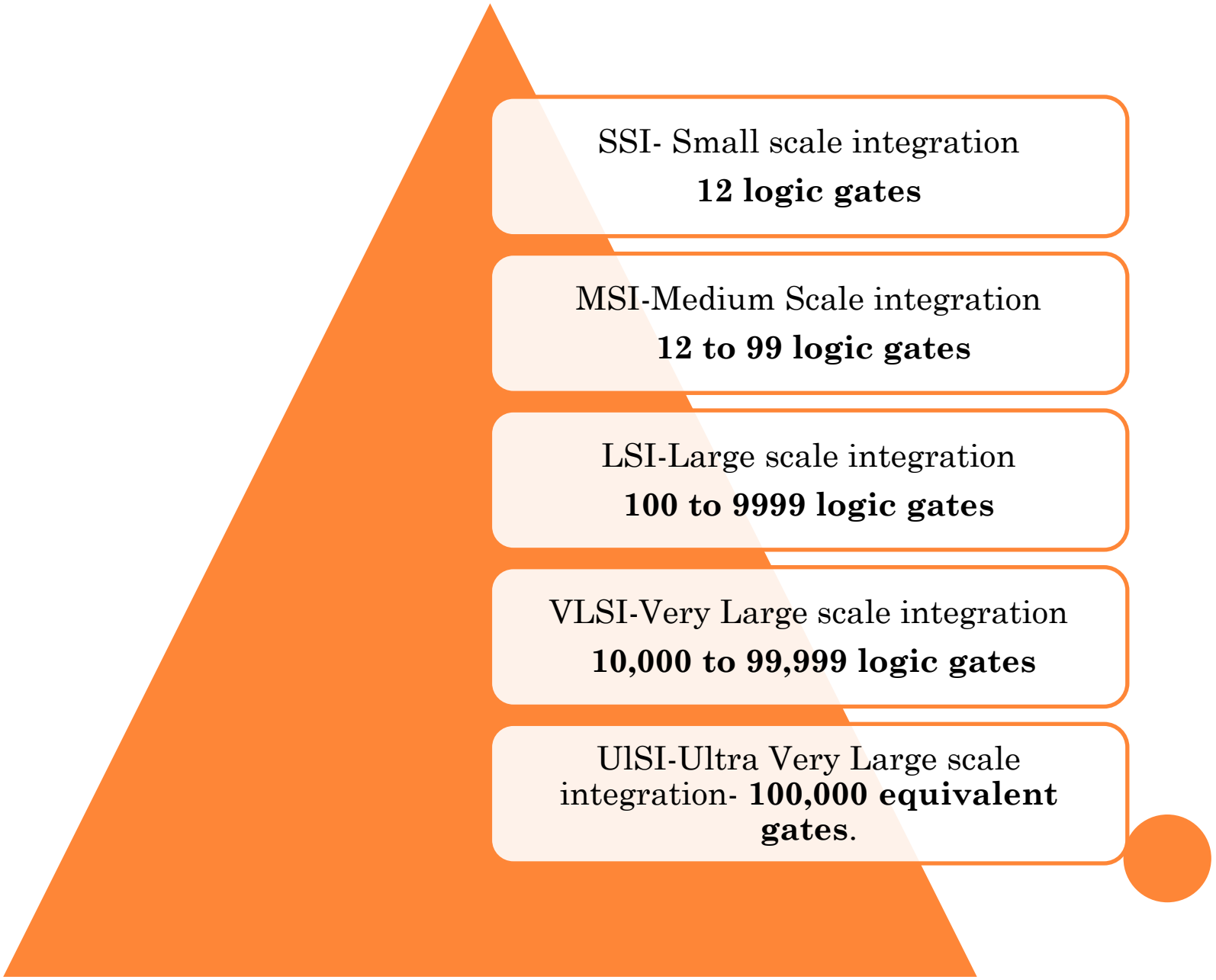
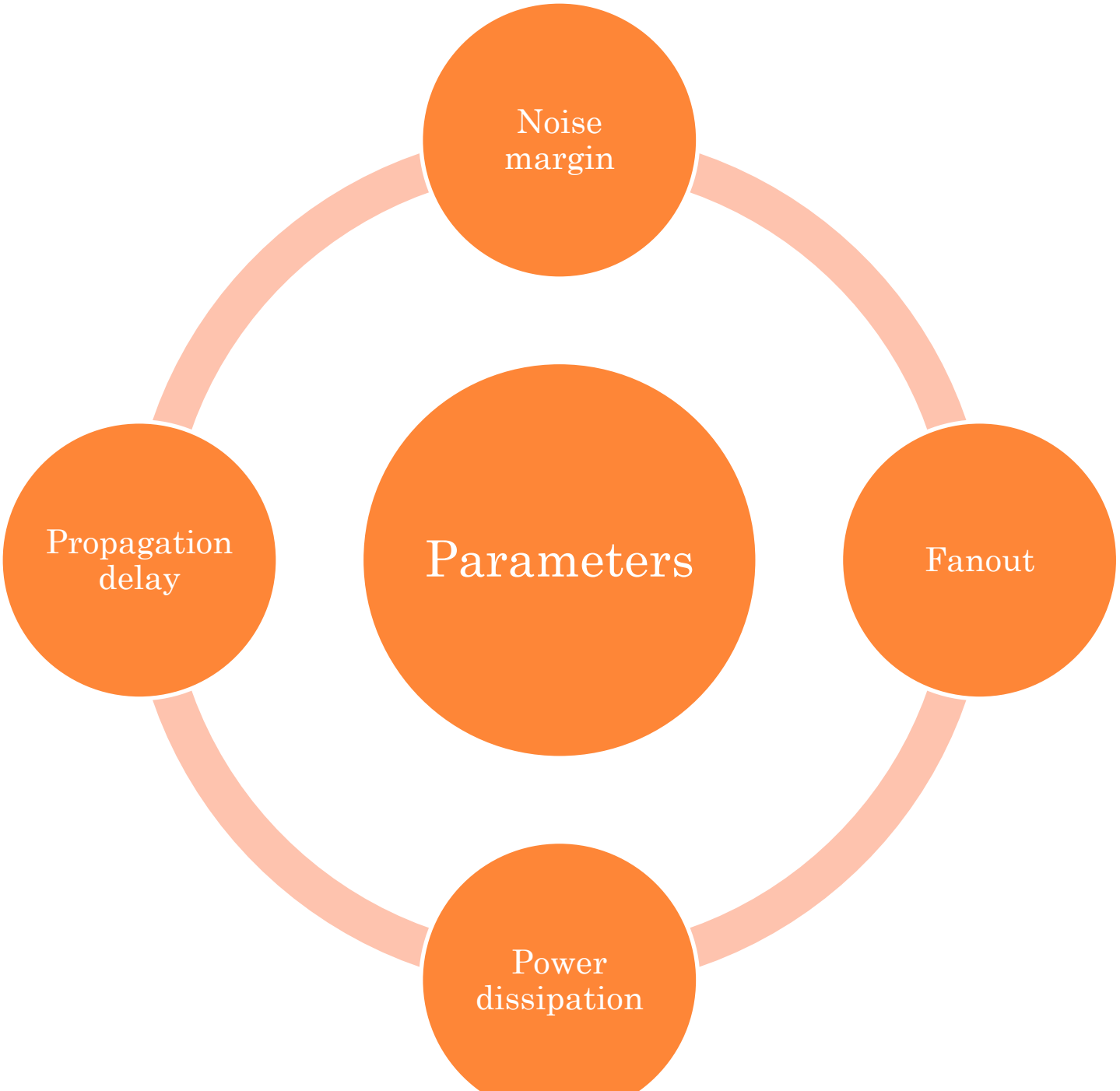
# Types of Logic Families



# TYPES OF PACKAGING




Noise margin
Propagation delay
Parameters
Fanout
Power dissipation

# Fan out {Number} {Desired: HIGH}

- Number of standard loads that can be connected to output of gate without degrading its normal operation
- Calculated from amount of current available. Ans is simply the **Ratio of output high current and input high current or Ratio of output low current or input low current.**
- Fan-in : Maximum number of inputs can be attached to a gate.

# Power dissipation { Milli-watt} Desired: Low

- Represents amount of power needed by the gate or in other words amount of power delivered to the gate.
- Given as product of voltage and average current
- **Measures in milliwatts.**
- For an IC with 4 logic gates, the overall power dissipation is sum of power dissipation of each gates.

# Noise margin { volts} Desired: High

- Represents the maximum noise voltage that can be added to an input signal of a digital gate, that does not affect the gate functioning.

# Propagation delay { nano-seconds} Desired: Low

- Average transition delay time for a signal to propagate from input to output when binary signal changes its value from 1 to 0 or 0 to 1.
- Calculated form input output waveforms.

## TTL

- most widely used families for small- and medium-scale devices
- operated from 5V supply
- noise immunity about 1 – 1.6 V

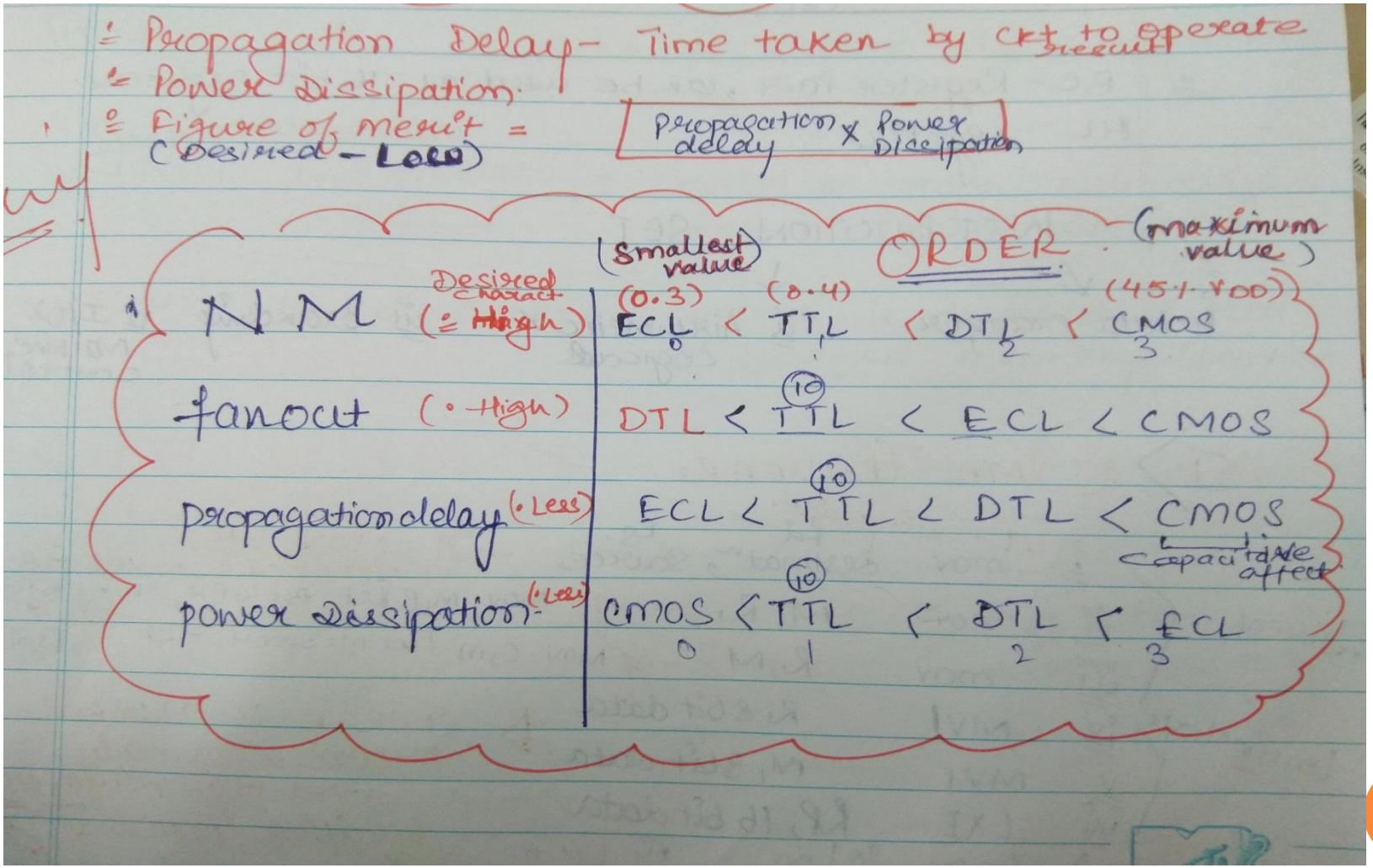
## ECL

- very fast operation - propagation delays of 1ns or less
- high power consumption 60 mW/gate
- low noise immunity of about 0.2-0.25 V
- but now largely replaced by high speed CMOS

## CMOS

- used family for large-scale devices
- high speed with low power consumption
- single supply of 5 – 15 V
- power consumption depends on speed

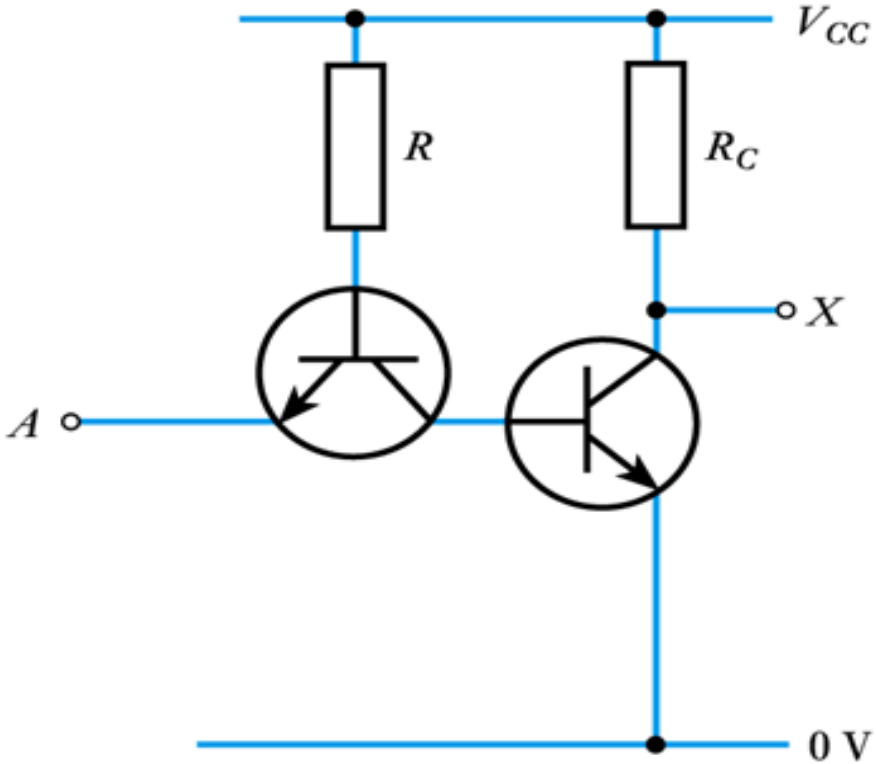
# COMPARISON OF DIFFERENT LOGIC FAMILIES



# Comparison continued…

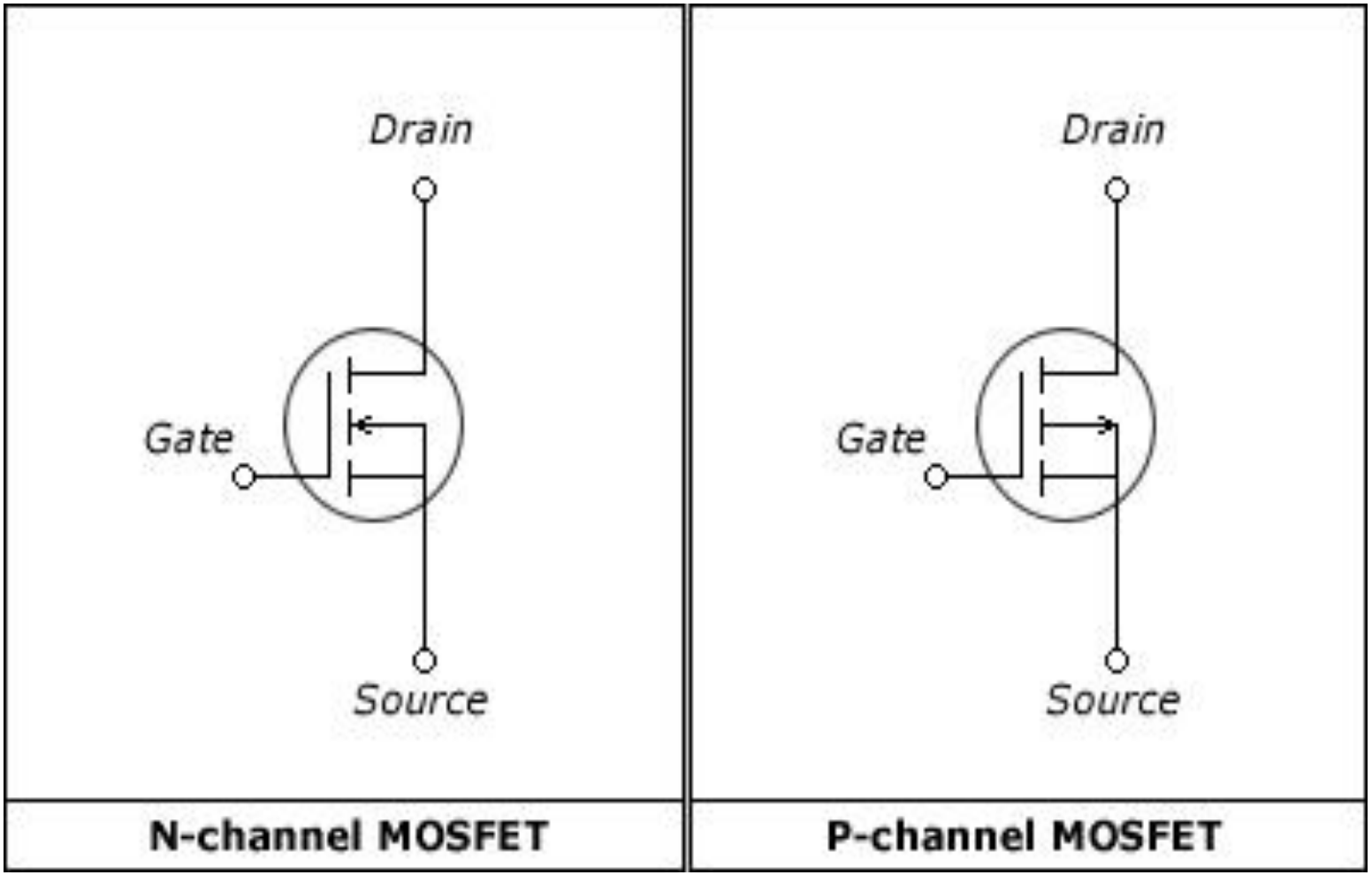
| Parameter | CMOS | TTL | ECL |
|---|---|---|---|
| Basic gate | NAND/NOR | NAND | OR/NOR |
| Fan-out | >50 | 10 | 25 |
| Power per gate (mW) | 1 @ 1 MHz | 1 - 22 | 4 - 55 |
| Noise immunity | Excellent | Very good | Good |
| $t_{PD}$ (ns) | 1 - 200 | 1.5 – 33 | 1 - 4 |

# Inverter circuit using TTL

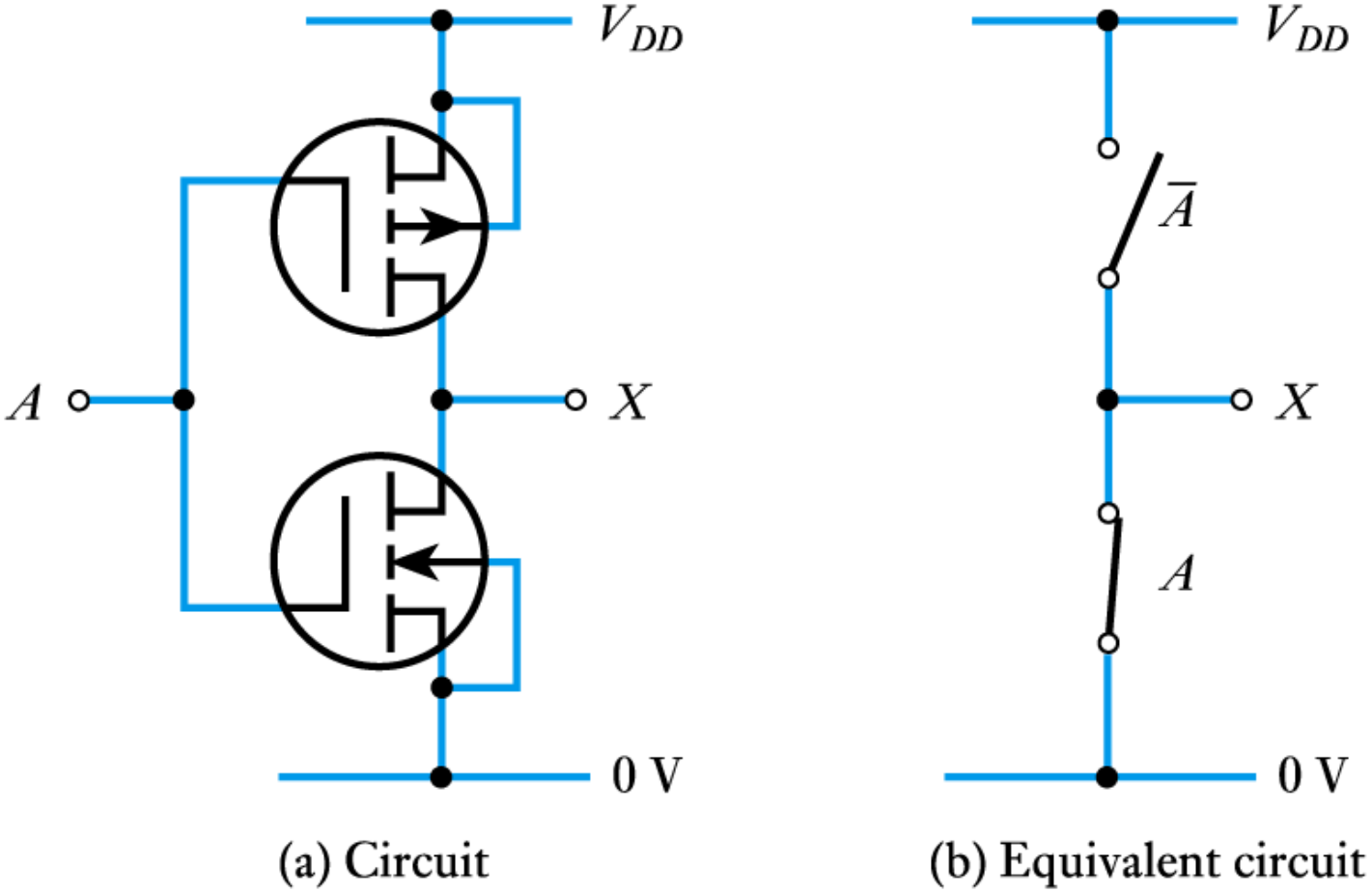



(a) A TTL inverter

# FET BASICS


Drain
Gate
Source
N-channel MOSFET
Drain
Gate
Source
P-channel MOSFET

# Inverter circuit using CMOS




(a) Circuit

(b) Equivalent circuit