

LOGIC FAMILIES

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TYPES OF LOGIC FAMILIES

RTL Resister
Transistor Logic

DTL
Diode
Transistor Logic

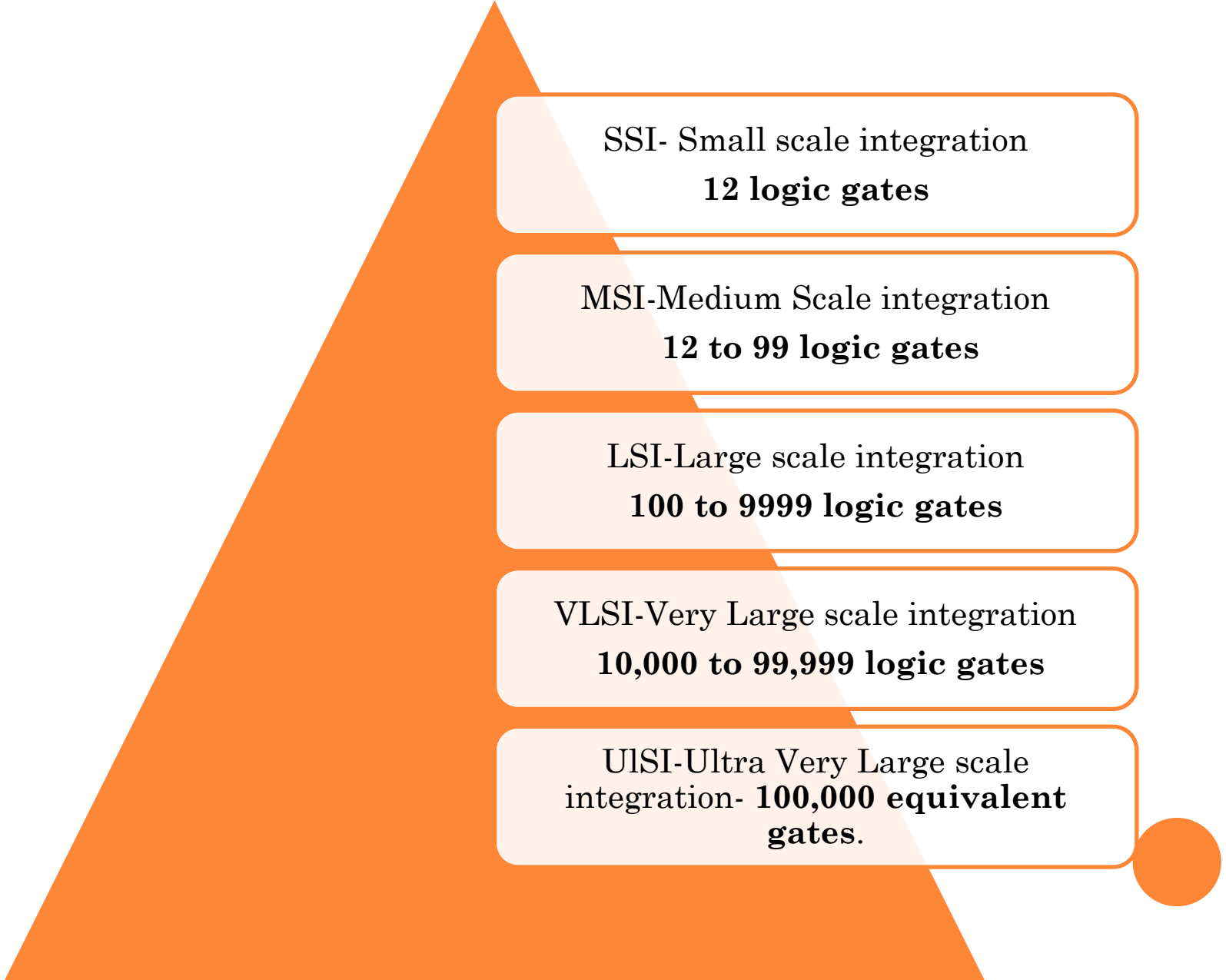
TTL
Transistor
Transistor Logic

ECL
Emitter
Coupled Logic

MOS
Metal Oxide
Semiconductor

CMOS
Complementary
Metal Oxide
semiconductor

TYPES OF PACKAGING



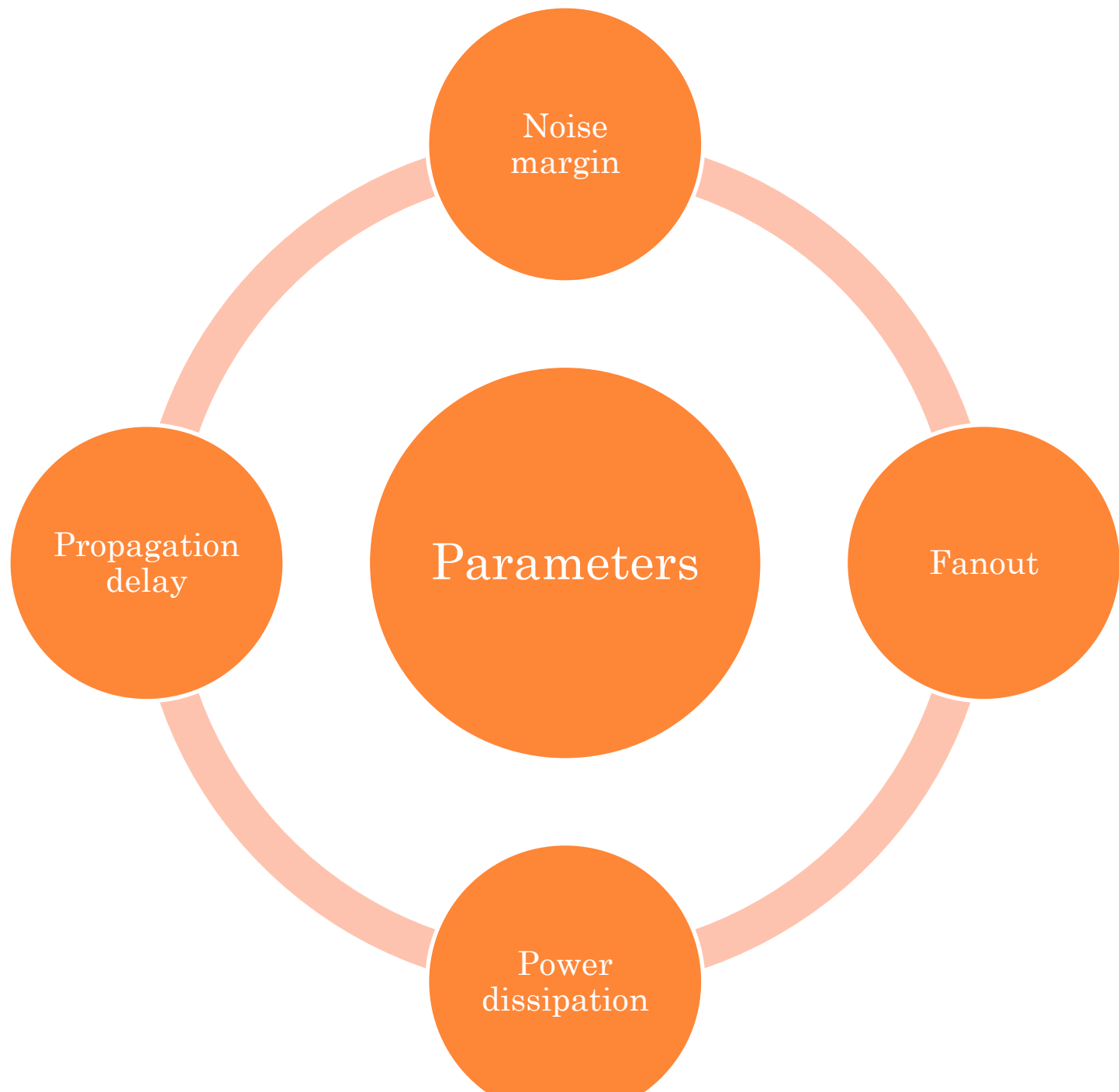
SSI- Small scale integration
12 logic gates

MSI-Medium Scale integration
12 to 99 logic gates

LSI-Large scale integration
100 to 9999 logic gates

VLSI-Very Large scale integration
10,000 to 99,999 logic gates

ULSI-Ultra Very Large scale
integration- **100,000 equivalent
gates.**



FAN OUT {NUMBER} {DESIRED: HIGH}

- Number of standard loads that can be connected to output of gate without degrading its normal operation
- Calculated from amount of current available. Ans is simply the **Ratio of output high current and input high current or Ratio of output low current or input low current.**
- Fan-in : Maximum number of inputs can be attached to a gate.



POWER DISSIPATION

{ MILLI-WATT }

DESIRED: LOW

- Represents amount of power needed by the gate or in other words amount of power delivered to the gate.
- Given as product of voltage and average current
- **Measures in milliwatts.**
- For an IC with 4 logic gates, the overall power dissipation is sum of power dissipation of each gates.



NOISE MARGIN { VOLTS} DESIRED: HIGH

- Represents the maximum noise voltage that can be added to an input signal of a digital gate, that does not affect the gate functioning.



PROPAGATION DELAY

{ NANO-SECONDS}

DESIRED: LOW

- Average transition delay time for a signal to propagate from input to output when binary signal changes its value from 1 to 0 or 0 to 1.
- Calculated from input output waveforms.



TTL

- most widely used families for small- and medium-scale devices
- operated from 5V supply
- noise immunity about 1 – 1.6 V

ECL

- very fast operation - propagation delays of 1ns or less
- high power consumption 60 mW/gate
- low noise immunity of about 0.2-0.25 V
- but now largely replaced by high speed CMOS

CMOS

- used family for large-scale devices
- high speed with low power consumption
- single supply of 5 – 15 V
- power consumption depends on speed

COMPARISON OF DIFFERENT LOGIC FAMILIES

= Propagation Delay - Time taken by ckt to operate

= Power Dissipation

= Figure of merit = $\frac{\text{Desired} - \text{Less}}{\text{Desired} - \text{Less}}$

Propagation delay \times Power Dissipation

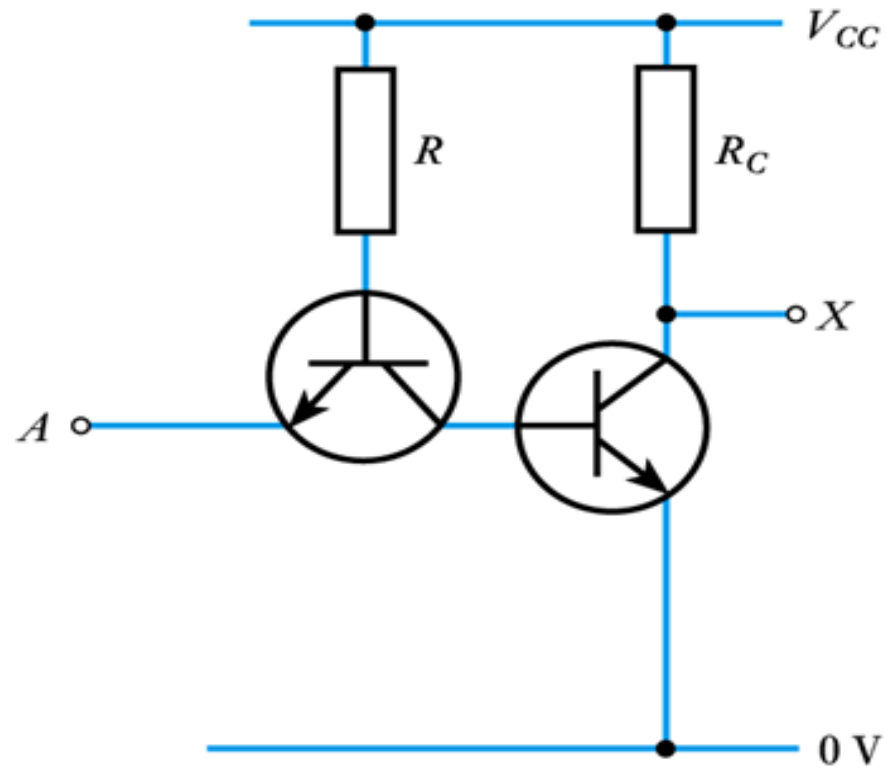
	Desired Characteristic (= High)	(Smallest value)	ORDER	(Maximum value)
NM	(= High)	(0.3)	ECL ₀ < TTL ₁ < DTL ₂ < CMOS ₃	(45-100)
fanout	(= High)	(10)	DTL < TTL < ECL < CMOS	
propagation delay	(= Less)	(10)	ECL < TTL < DTL < CMOS	Capacitive affect
power dissipation	(= Less)	(10)	CMOS ₀ < TTL ₁ < DTL ₂ < ECL ₃	

COMPARISON CONTINUED...

Parameter	CMOS	TTL	ECL
Basic gate	NAND/NOR	NAND	OR/NOR
Fan-out	>50	10	25
Power per gate (mW)	1 @ 1 MHz	1 - 22	4 - 55
Noise immunity	Excellent	Very good	Good
t_{PD} (ns)	1 - 200	1.5 – 33	1 - 4



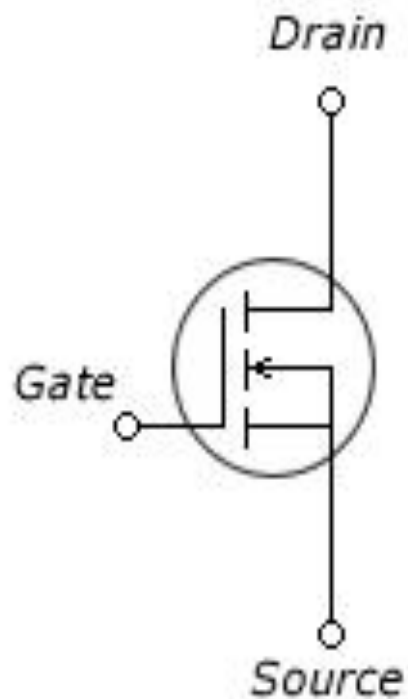
INVERTER CIRCUIT USING TTL



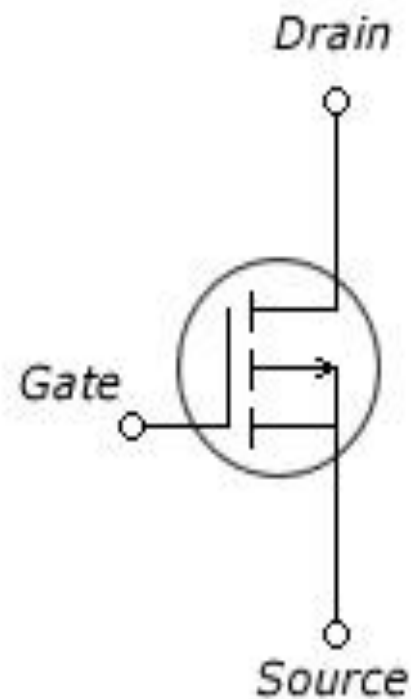
(a) A TTL inverter



FET BASICS



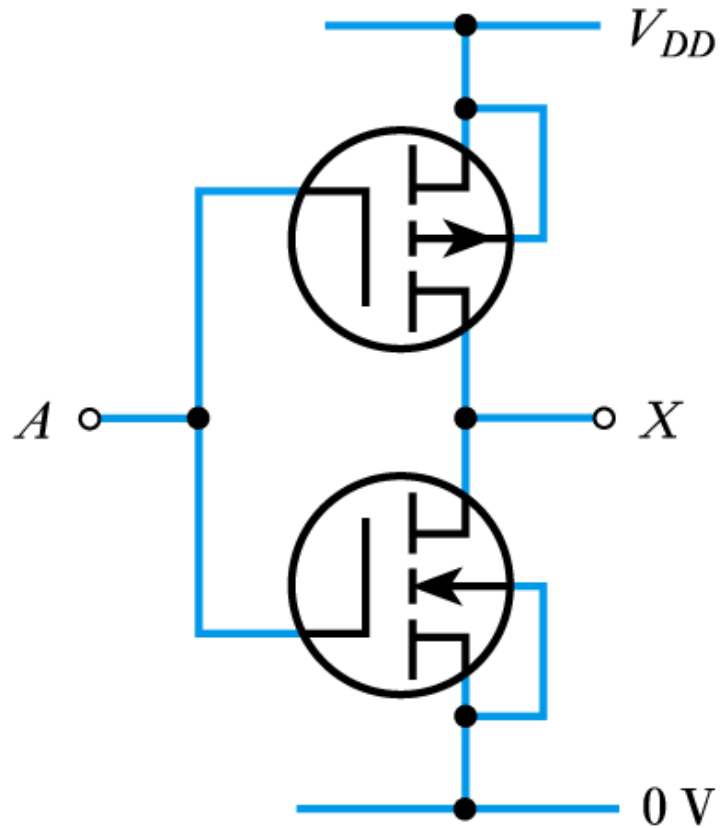
N-channel MOSFET



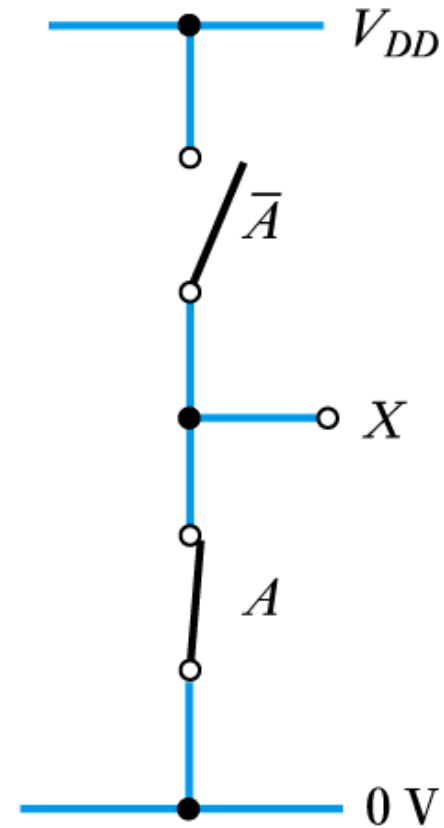
P-channel MOSFET



INVERTER CIRCUIT USING CMOS



(a) Circuit



(b) Equivalent circuit

