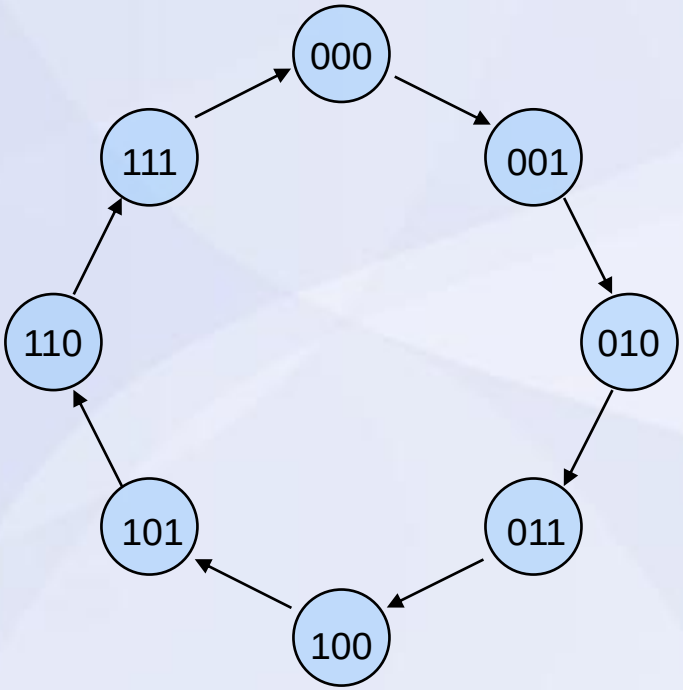
ECE 213 – Digital Electronics

Counters

3-bit Counter: State Diagram



Counters

Asynchronous Counters

(aka. Ripple Counters)

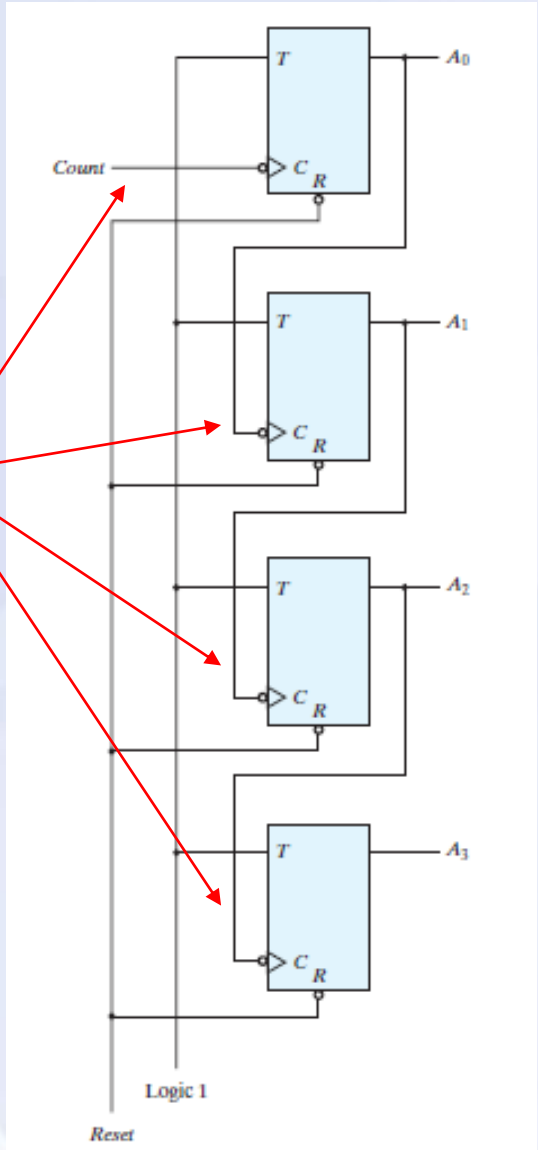
4-bit (up) Counter

- Let each bit in the counter be represented by the output of a flip-flop.

Count	A_3	A_2	A_1	A_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1

Count	A_3	A_2	A_1	A_0
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

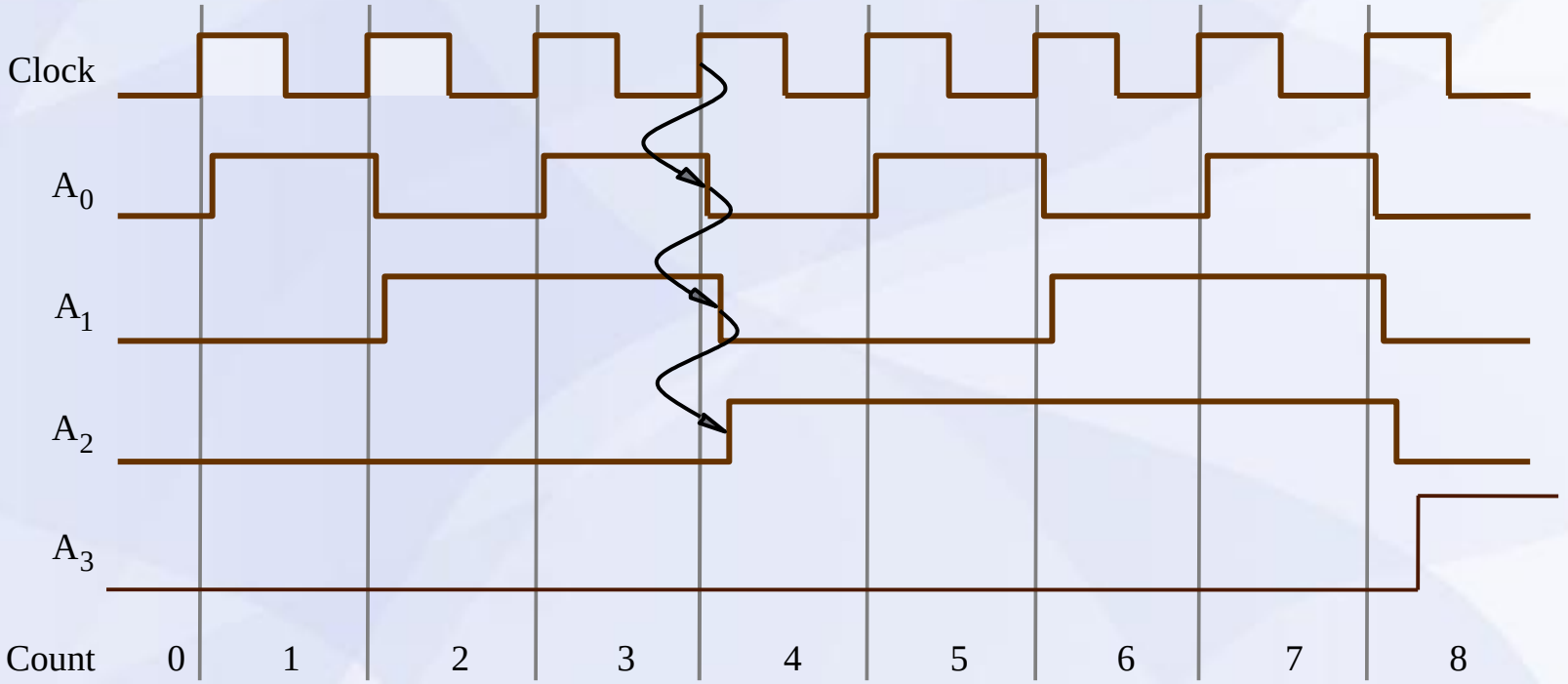
4-bit (up) Counter: T Flip-Flops



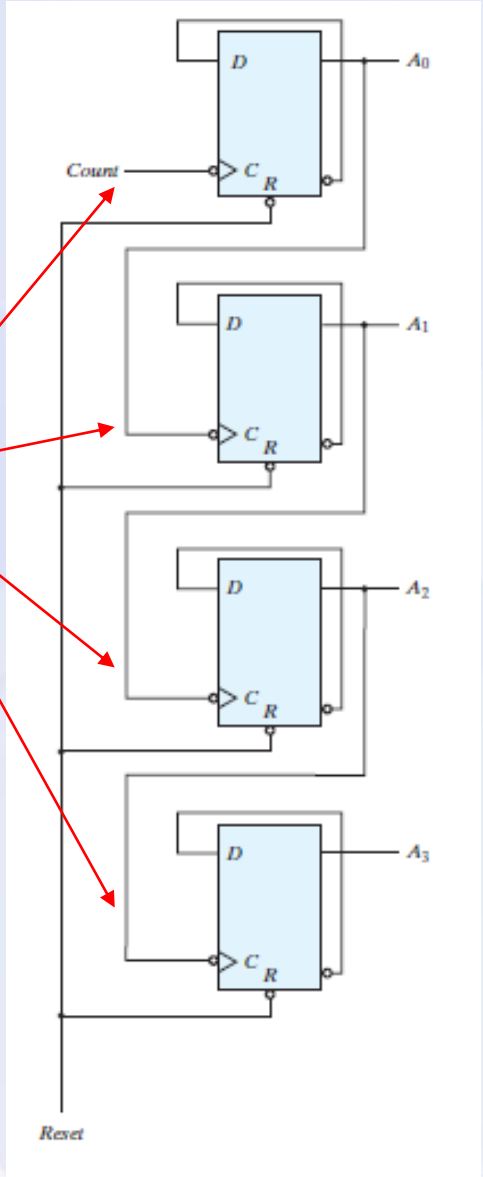
Counter does not use a common clock.

Asynchronous Counter

4-bit (up) Counter: T Flip-Flops



4-bit (up) Counter: D Flip-Flops



Counter does not use a common clock.

Asynchronous Counter

Counters

Synchronous Counters

4-bit (up) Counter

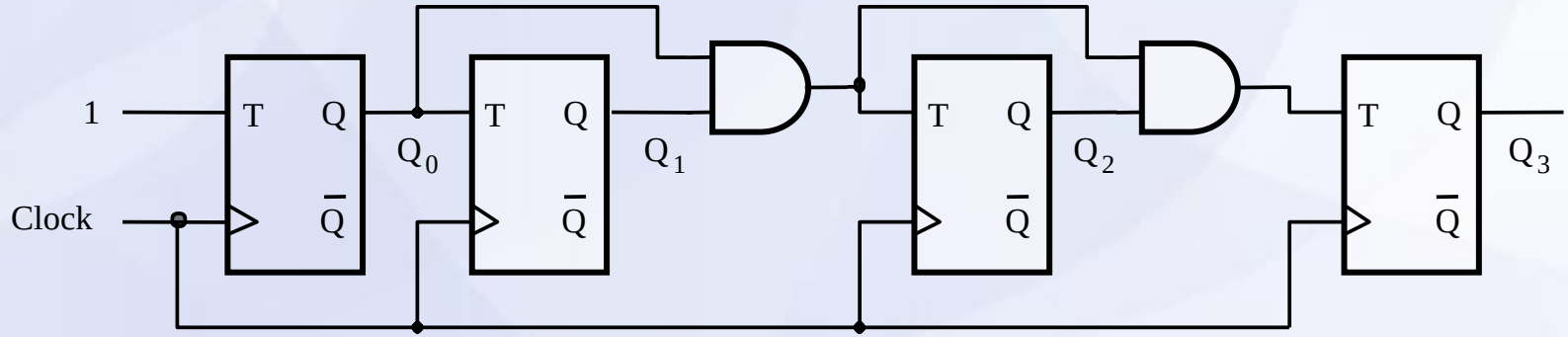
- As before, let each bit in the counter be represented by the output of a flip-flop.

Count	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1

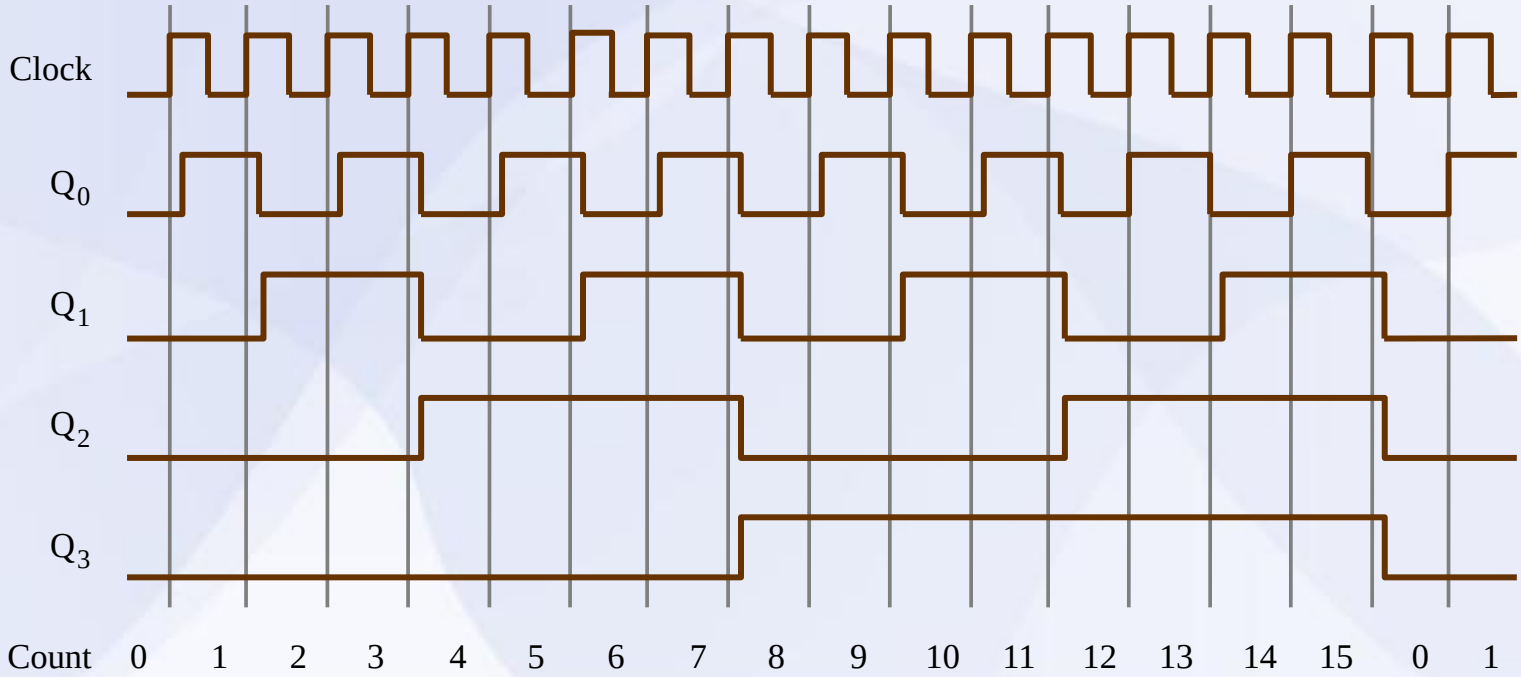
Count	Q_3	Q_2	Q_1	Q_0
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

4-bit (up) Counter: T Flip-Flops

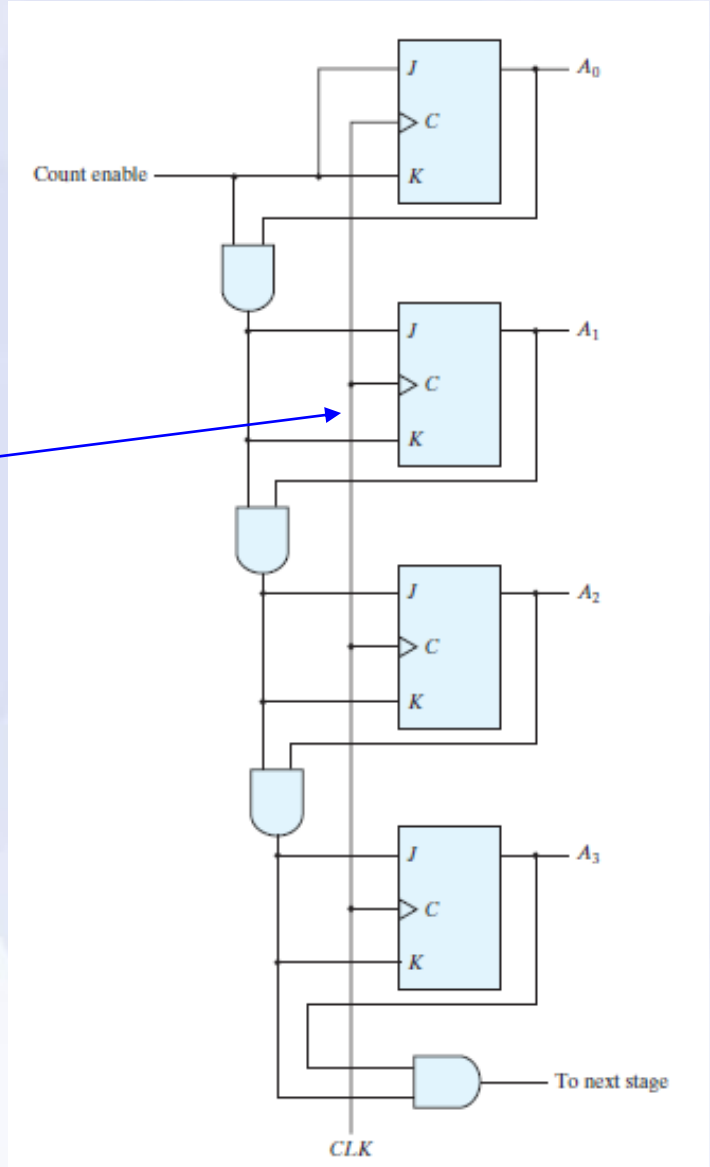
Synchronous Counter



Counter uses a common clock.



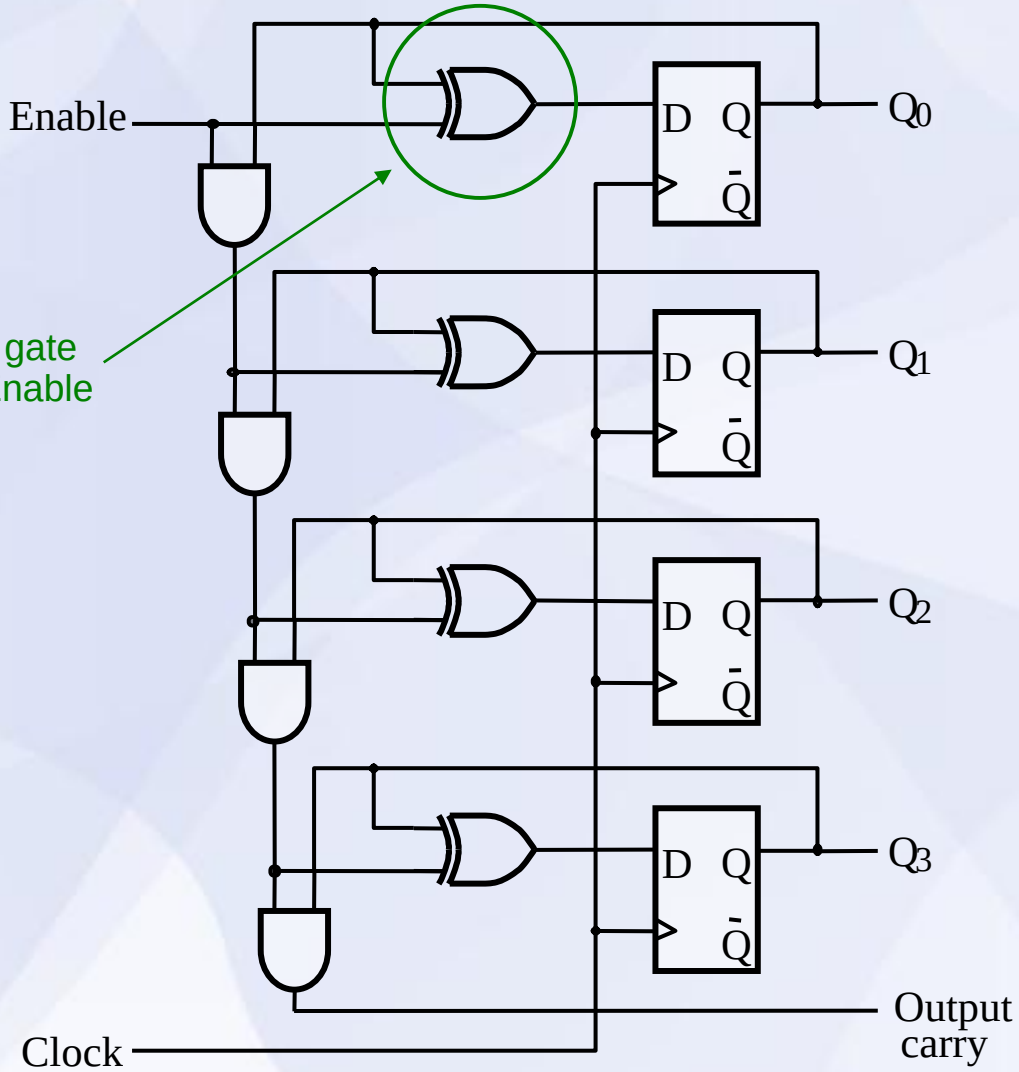
4-bit (up) Counter: JK Flip-Flops



Counter uses
a common clock.

Synchronous
Counter

4-bit Counter: D Flip-Flops

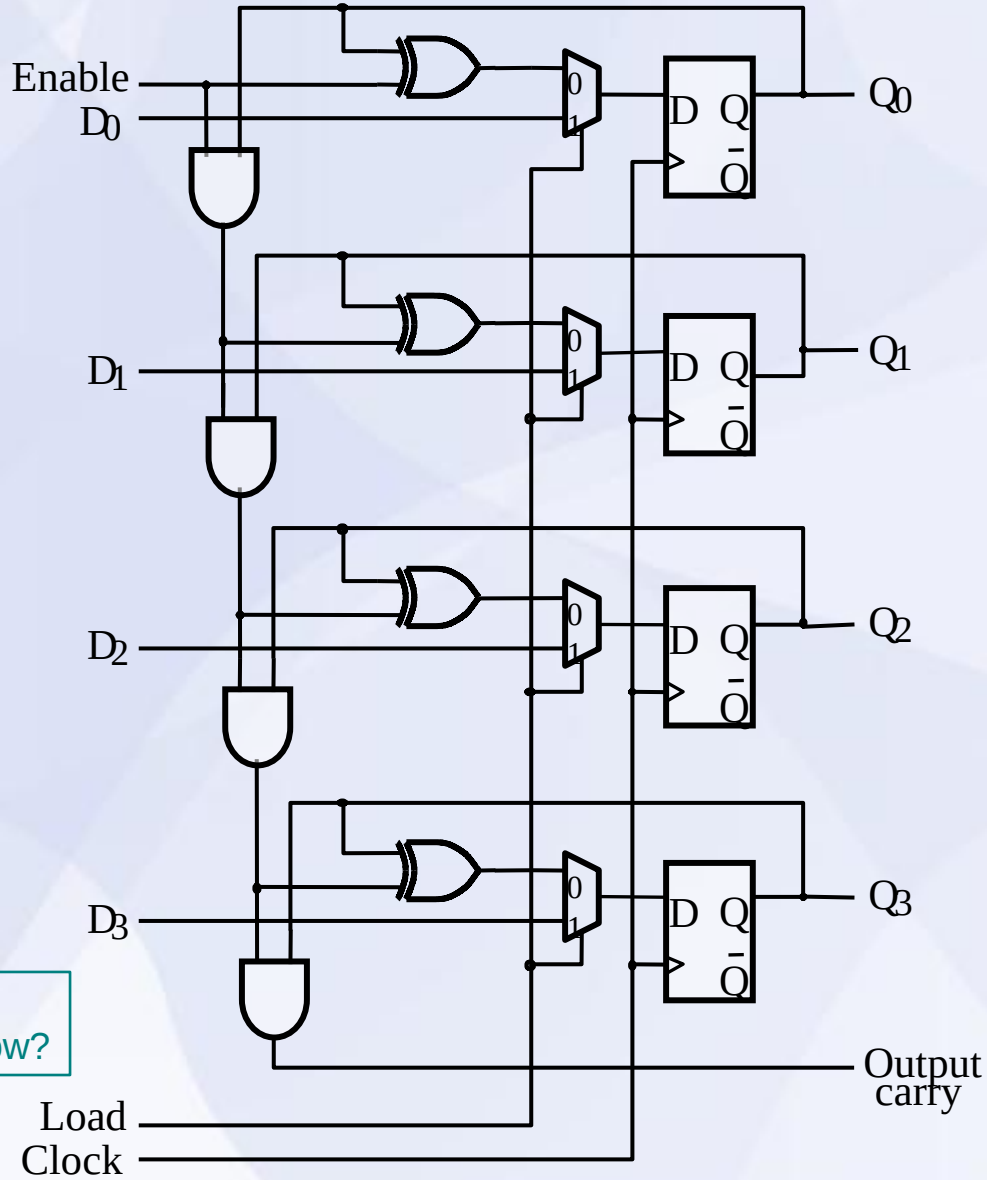


How does the XOR gate function when the Enable signal is a logic-1?

Synchronous Counters

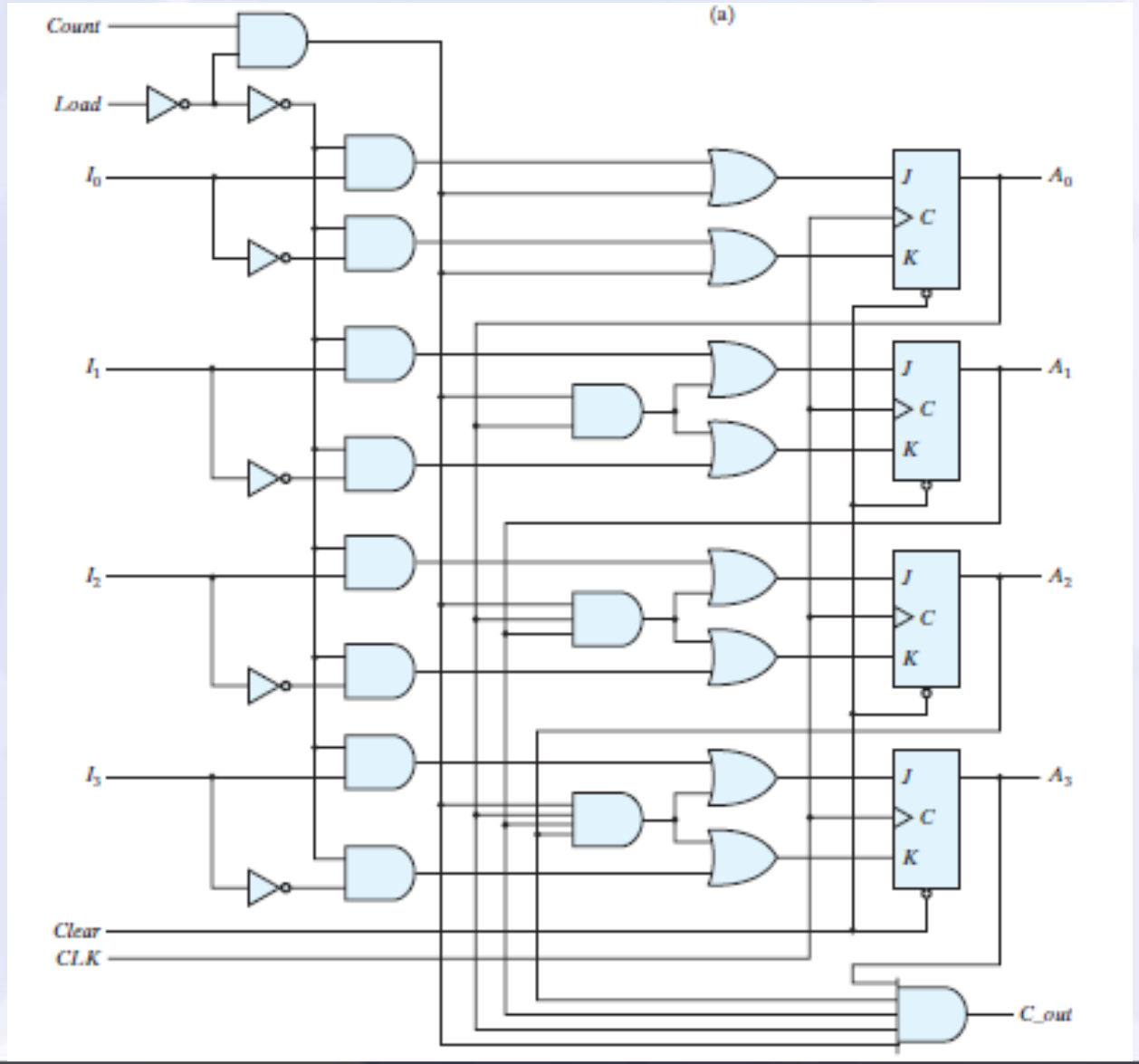
Binary Counter with Parallel Load

4-bit Counter with Parallel Load



Is the Load signal active-high or active-low?

4-bit Counter with Parallel Load

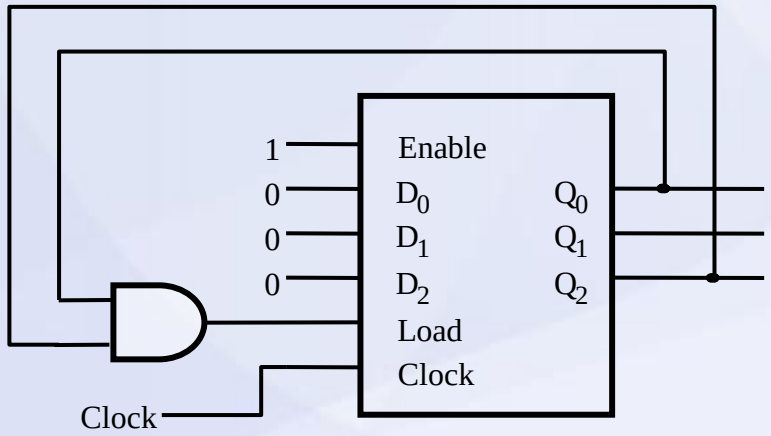


Synchronous Counters

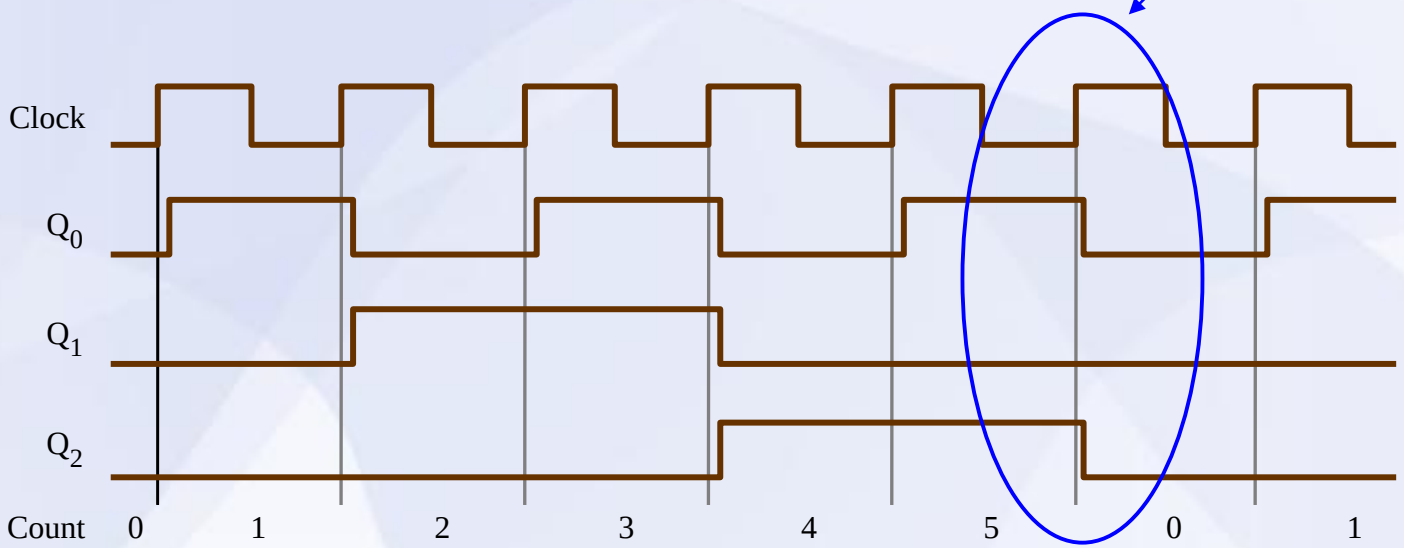
Modulo-6 Counter

Modulo-6 Counter: D Flip-Flops

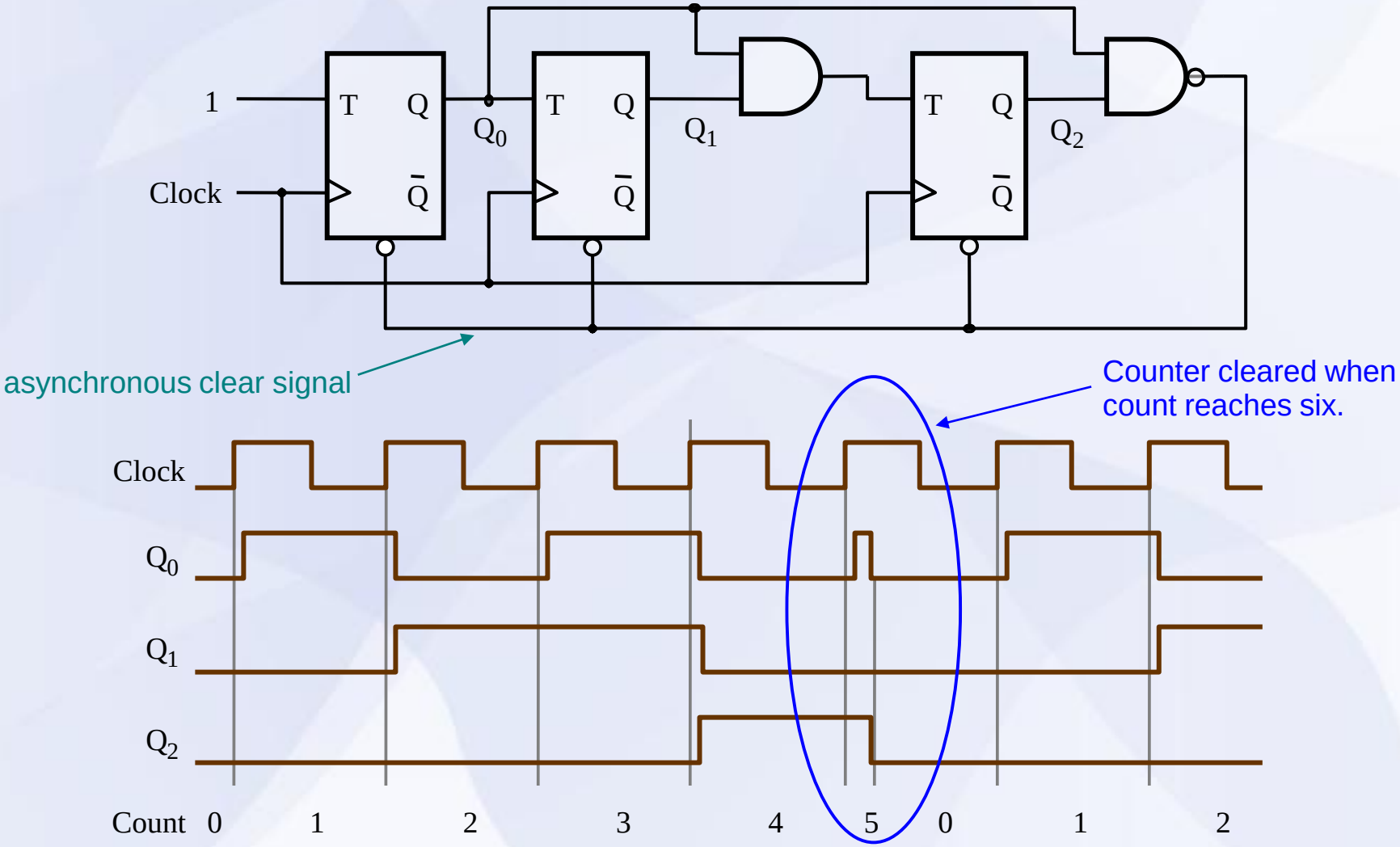
3-bit counter
with Parallel Load



Counter resets to zero
when count reaches six.



Modulo-6 Counter: T Flip-Flops

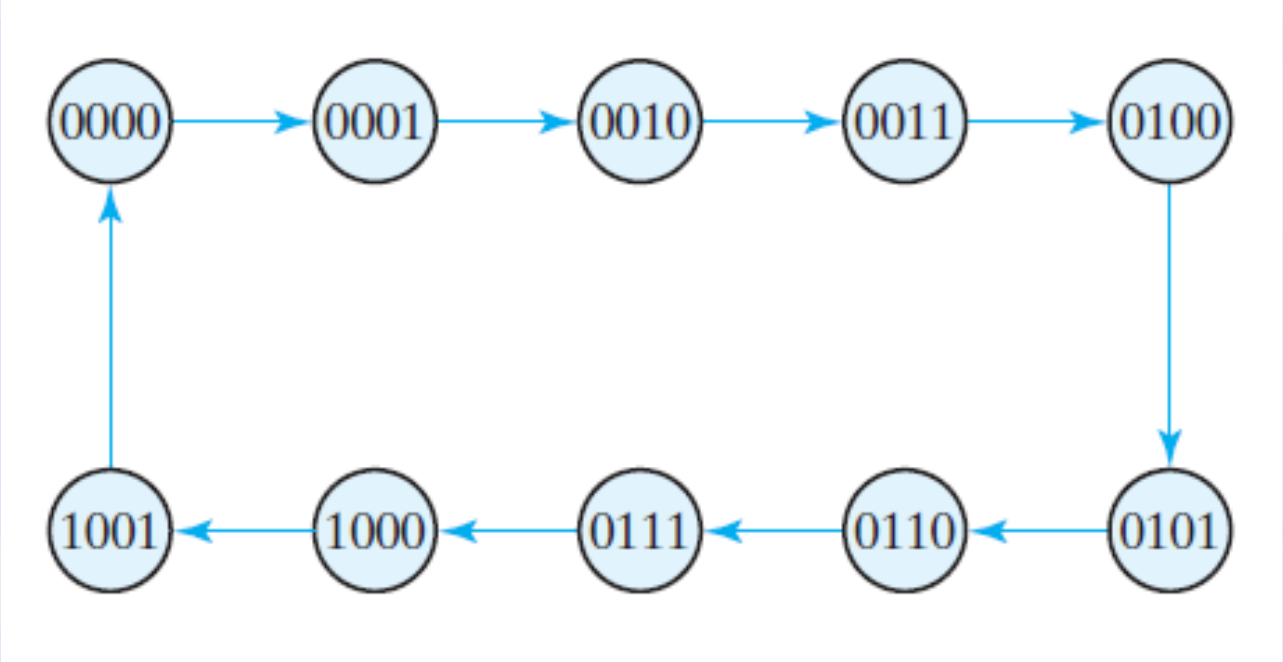


Counters

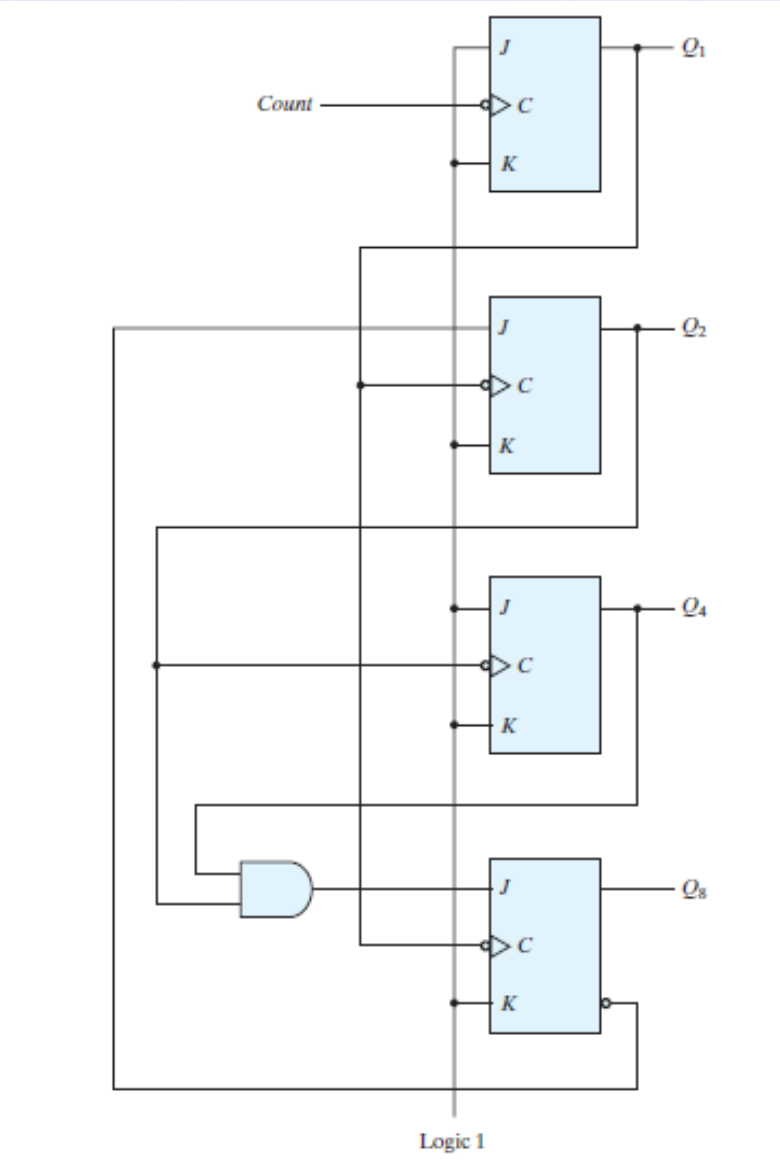
BCD (Decimal) Counter

(aka. Modulo-10 Counter)

BCD Counter: State Diagram

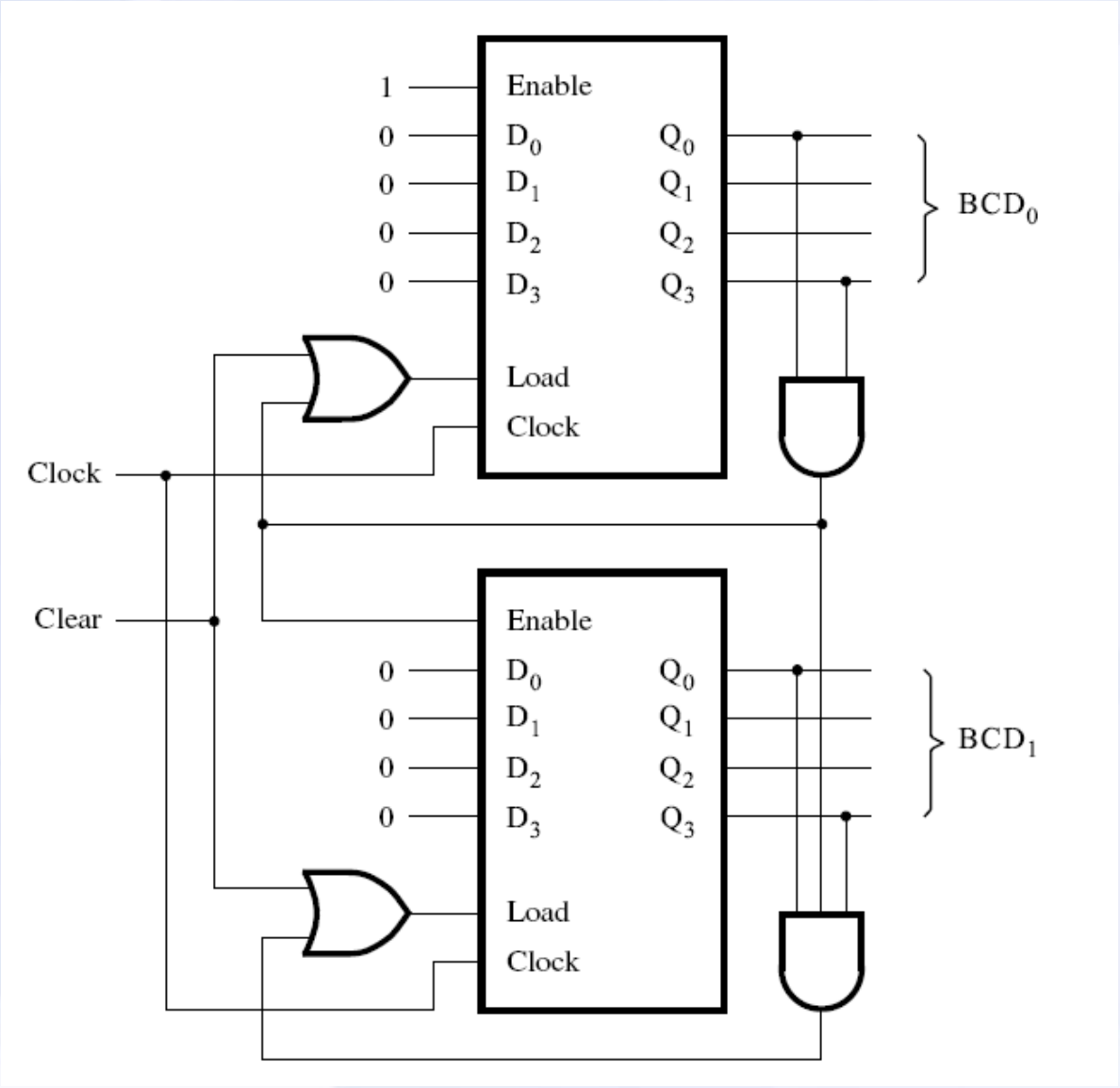


BCD Counter: JK Flip-Flops



Asynchronous Counter

BCD Counter: D Flip-Flops

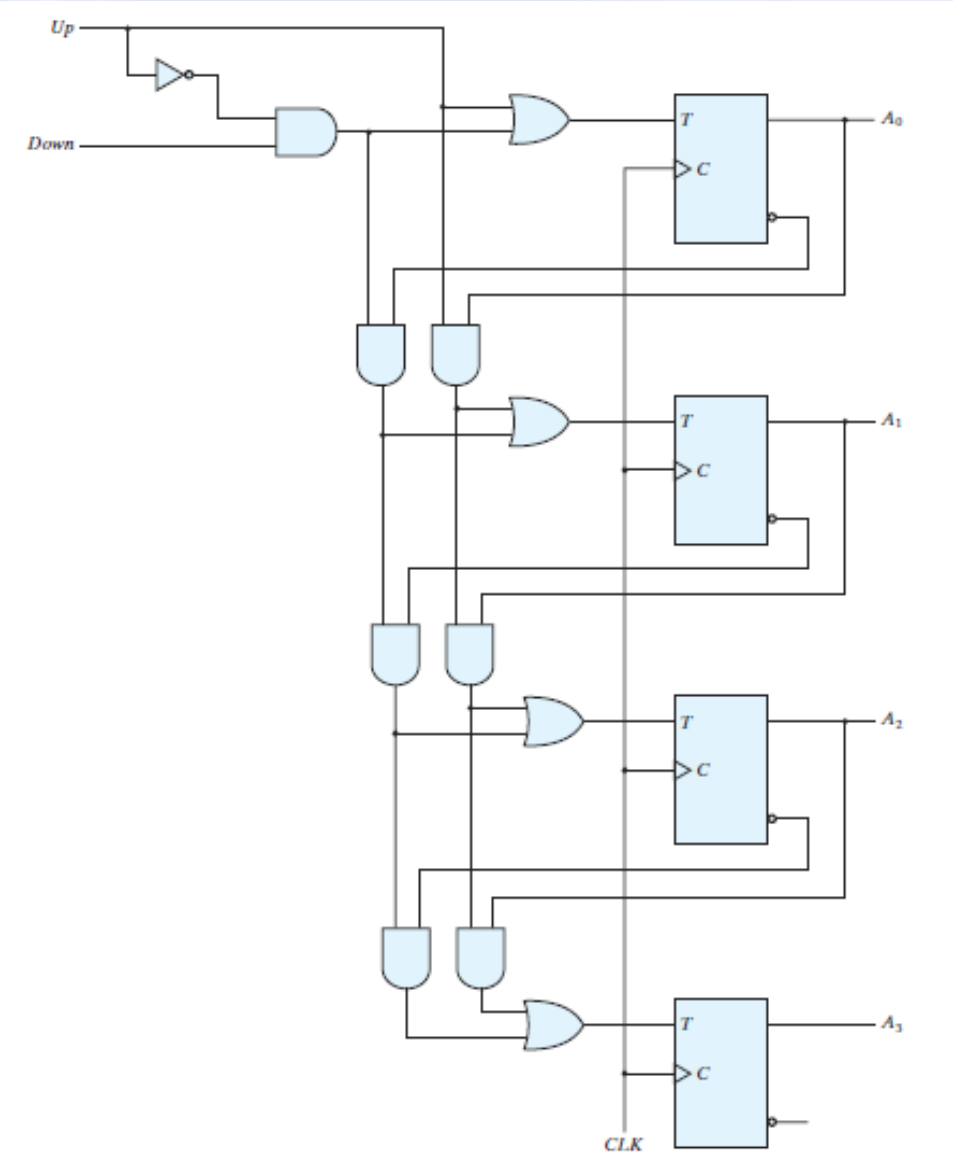


Synchronous Counter

Synchronous Counters

Up / Down Counter

4-bit Up / Down Counter



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