SUMIT SHARMA

Residence:- C1/104, Ambika Township, Dindoli, Surat(Guj.)

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CAREER OBJECTIVE

Dedicated professional seeking suitable position that would enable me to broaden my current skills and challenge my various abilities.

EDUCATION

DEGREE	YEAR	INSTITUTE	UNIVERSITY/BOARD	PERCENTAGE
B.TECH (ECE)	2019	B. K. BIRLA INSTITUTE OF ENGINEERING AND TECHOLOGY , PILANI	RAJASTHAN TECHNICAL UNIVERSITY	64% (1st Class)
12th	2014	EVER GREEN SR. SEC. SCHOOL	CBSE	68% (1st Class)
10th	2012	EVER GREEN SR. SEC. SCHOOL	CBSE	78% (1st Class)

ACHIVEMENTS

- **'C'** Certified at **National Cadet Corps.**
- 9 months Internship in **Physical Design at Incise Infotech Pvt. Ltd., Noida.**
- 2 months summer training in **VLSI at Incise Infotech Pvt. Ltd., Noida.**

CORE COMPETENCY

- Good knowledge of Digital Electronics
- Good knowledge in Linux command
- Basic knowledge of C and C++.
- Basic knowledge in Perl.
- Basic knowledge in TCL
- Basic knowledge in Verilog
- Good knowledge of ASIC flow (RTL to GDSII).
- Good knowledge of Physical Design(Floor Planning, Power Planning, Placement , CTS, Routing) .
- Good knowledge in STA (setup and hold time, slack , skew, slew, latency etc.).
- Good knowledge of MS Word, Power Point and MS Excel.

PROJECT DETAILS

Project 1:- Floor Planning of Rapid Adaption Kit

- Objective:- Floor Planning(Relative FloorPlan) , Power Grid Generation.
- Tool Used:- Cadence(Innovus 16.2)
- Design Description:-
  - Design mode:- 45nm
  - Instances:- 18228
  - Analysis mode:- Non-OCV
  - Metal Layers:- 9
- Problem Occurs :- Placing macros and in power generations.

Project 2:- Block Level Designing of USB

- Objective:- Floor Planning, Power Grid Generation, Placement, CTS, Routing, Timing analysis and verification.
- Tool Used :- Cadence(Innovus 16.2)
- Design Description:-
  - Design mode:- 90nm
  - Instances:- 18508
  - Analysis mode :- Non OCV
  - No. of Clocks:- 3
- Problem Occurs:- Fixing timing violation and fixing Connectivity violation.

Project 3:- Block level design of Dual Tone Multi Frequency (DTMF) 90nm technology.

- Objective :- To do the floorplanning, Powerplanning , placement , CTS ,routing , verify and report analysis of design.
- Tool used :- Cadence (Encounter & Innovus)
- Design description :-
  - Design mode: 90 nm.
  - Instances: 3243
  - Analysis mode : non OCV
  - No. of Clocks:17(1 reference clock ,16 generated clock)

Problem Occurs :- Macro placement, providing blockages, finding the width and spacing ofstripes, fixing timing violations, fixing geometry and other defects violation.

PERSONAL PROFILE

Name	:-	Sumit Sharma
Date of Birth	:-	3rd October 1995
Father Name	:-	Sushil Sharma
Sex	:-	Male
Languages known	:-	English, Hindi
Hobbies	:-	Reading, Writing, Travelling and Outdoor Games

DECLARATION

I hereby declare that all the information furnished above is true to the best of my knowledge.

Place: Surat
Date:

Sumit Sharma
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