SUMIT SHARMA

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CAREER OBJECTIVE

Dedicated professional seeking suitable position that would enable me to broaden my current skills and challenge my various abilities.

CORE COMPETENCY

- Good Knowledge of Digital Electronics(Logical gates, K-map, Flip-flops, Shift register, Counters).
- Good knowledge in Linux command:- mkdir, rmdir, cat, grep, vi editor, cp, mv ,head , tail , ls , pwd etc..
- Basic knowledge of C and C++.
- Basic Knowledge in Perl:- scalar, array, hashes, loop.
- Basic knowledge in TCL :- set, puts, loops (for, while, foreach) , conditional statements (if, if-else).
- Basic knowledge in Verilog(gate level, data flow, behavioral modeling).
- Good Knowledge of ASIC flow (RTL to GDSII).
- Good Knowledge of Physical Design(Floor Planning, Power Planning, Placement ,CTS, Routing) .
- Good Knowledge in STA (setup and hold time, slack , skew, slew, latency etc.).

PROJECT DETAILS

Project 1:- Block Level Designing of FSM Sequence Detector

- Objective:- Synthesis, Floor Planning, Power Grid Generation, Placement, CTS, Routing, Timing analysis and verification.
- Tool Used :- Cadence(Genus, Innovus 16.2)
- Design Description:-
  - Design mode:- 90nm
  - No. of standard cells:- 13
  - Instances:- 13
  - Analysis mode :- Non OCV
  - No. of Clocks:- 1
  - Frequency:- 152mhz
    - Problem Occurs:- Fixing timing violation and generating netlist.

Project 2:- Floor Planning of Rapid Adaption Kit

- Objective:- Floor Planning(Relative FloorPlan) , Power Grid Generation.
- Tool Used:- Cadence(Innovus 16.2)
- Design Description:-
  - Design mode:- 45nm
  - No. of standard cells:- 17886
  - No. of Macros:- 29
  - Instances:- 18228
  - Analysis mode:- Non-OCV
  - Metal Layers:- 9
- Problem Occurs :- Placing macros and in power generations.

Project 3:- Block Level Designing of USB

- Objective:- Floor Planning, Power Grid Generation, Placement, CTS, Routing, Timing analysis and verification.
- Tool Used :- Cadence(Innovus 16.2)
- Design Description:-
    - Design mode:- 90nm
    - No. of standard cells:- 18508
    - Instances:- 18508
    - Analysis mode :- Non OCV
    - No. of Clocks:- 3
    - Frequency:- 142.3mhz
    - Metal Layers:- 9
- Problem Occurs:- Fixing timing violation and fixing Connectivity violation.

Project 4:- Block level design of Dual Tone Multi Frequency (DTMF) 90nm technology.

- Objective :- To do the floorplanning, Powerplanning , placement , CTS ,routing , verify and report analysis of design.
- Tool used :- Cadence (Encounter & Innovus)
- Design description :-
    - Design mode: 90 nm.
    - No of standard cells: 3238
    - Instances: 3243
    - Analysis mode : non OCV
    - No. of Clocks:17(1 reference clock ,16 generated clock)
    - Metal layers: 9
- Problem faced :- Macro placement, providing blockages, finding the width and spacing ofstripes, fixing timing violations, fixing geometry and other defects violation.

ACHIVEMENTS

- ‘C’ certified at National Cadet Corps.
- 10 months Internship at Incise Infotech , Noida.

EDUCATION

DEGREE	YEAR	INSTITUTE	UNIVERSITY/BOARD	PERCENTAGE
B.TECH	2019	B.K.B.I.E.T	RTU	64%
12th	2014	E.G.P.S	CBSE	68%
10th	2012	E.G.P.S	CBSE	78%

PERSONAL PROFILE

Name :- Sumit Sharma
Date of Birth :- 03/10/1995
Father Name :- Sushil Sharma
Nationality :- Indian
Sex :- Male
Languages known :- English, Hindi.