ECE 385

Fall 2022

Experiment #1

Introductory Experiment: Static Hazards

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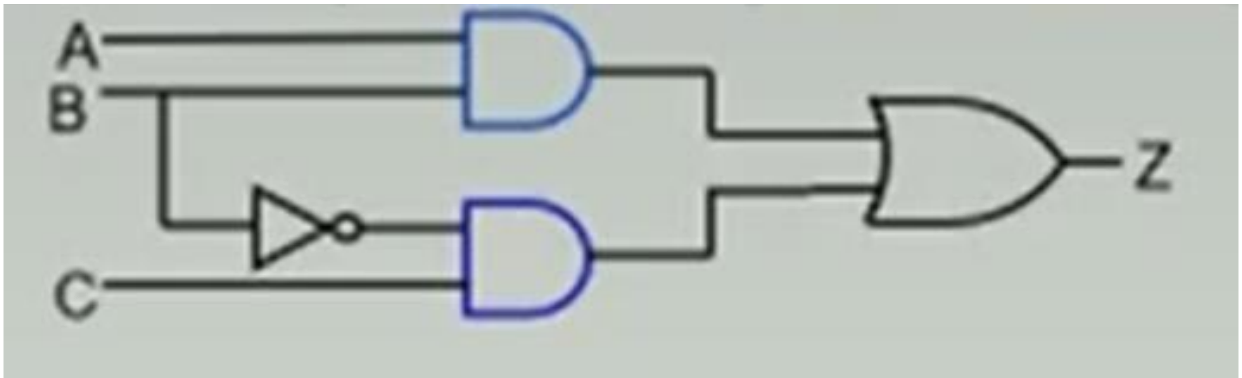
Introduction

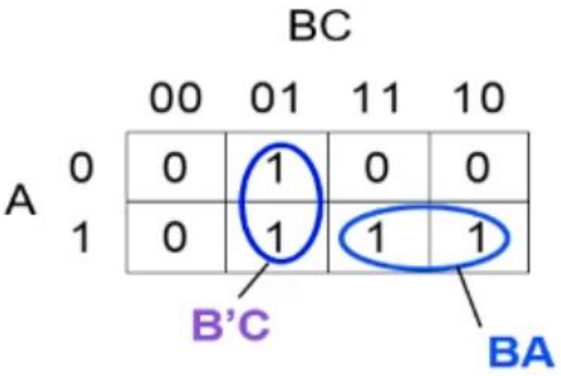
This lab demonstrates a glitch that may occur in digital circuits known as a static one hazard. A static 1 hazard is when an output of a digital circuit momentarily goes from a 1 to a 0 due to gate delays. Even a momentary drop and rise may damage the circuit or at least cause some sort of unexpected trouble. To get rid of this type of error, redundant logic is used. While this requires extra logic gates, this ensures that there is no point in time where there is an incorrect output from the circuit.

Written Description of Circuit

The first circuit is a 2 to 1 multiplexer circuit that has a Static 1 hazard. The circuit takes in three inputs, which are labeled A, B, and C. Input B is the input that allows for the circuit to mirror either input A or input C, depending on whether B is high or low. If B is high, then output Z matches input A, but when B is low, Z matches input C. Shown below is the logic diagram for the circuit using minimal SOP form.



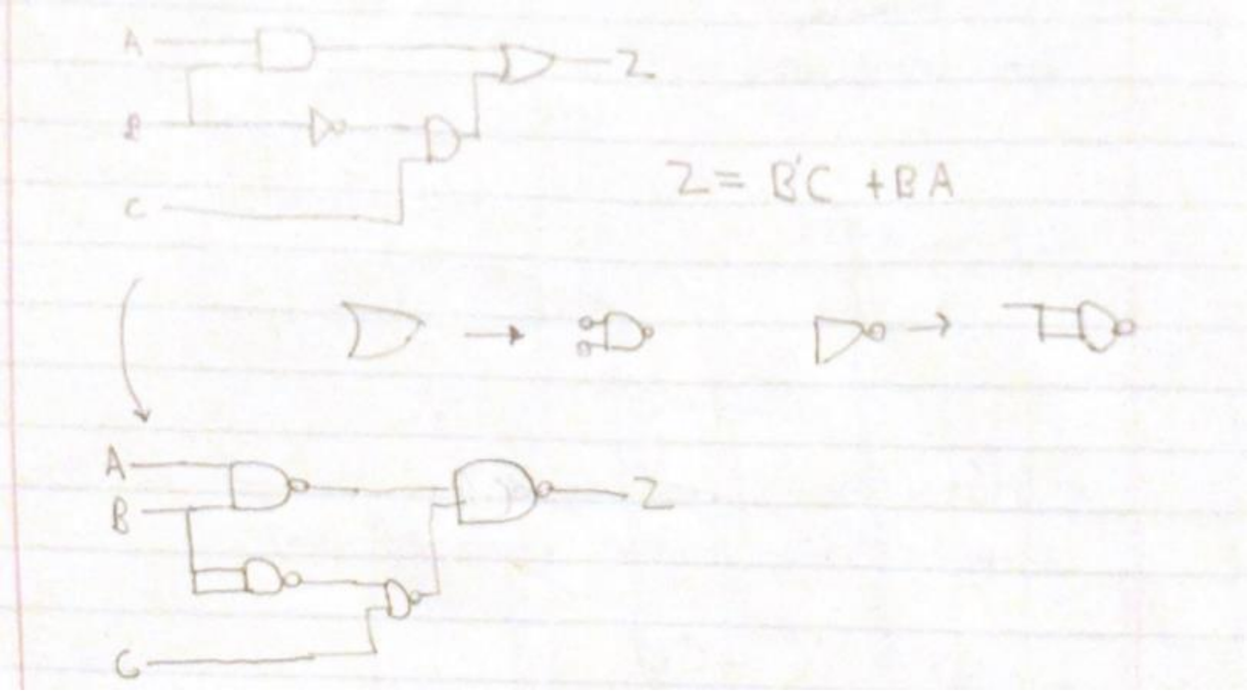
Below is the Karnaugh map for this circuit. The Karnaugh map shows how the 2-to-1 mux can be represented as **Z = B'C+BA**.



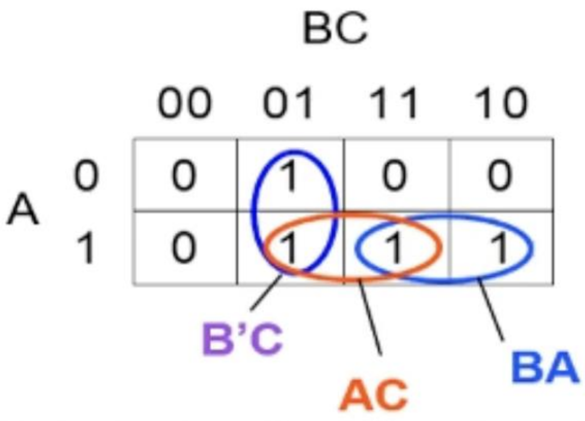
BC

A	00	01	11	10
0	0	1	0	0
1	0	1	1	1

To change the logic diagram so that it only consists of NAND gates, what you can do is use Demorgan’s Law on the OR gate at the right and change it to a NAND gate with inverted inputs. Those inverted inputs, represented by a hollowed circle, can be ‘attached’ to the two AND gates to turn them into NAND gates. The NOT gate can be turned into a NAND gate by shorting the two inputs for the NAND gate with one input. This process is visualized in the drawing below.

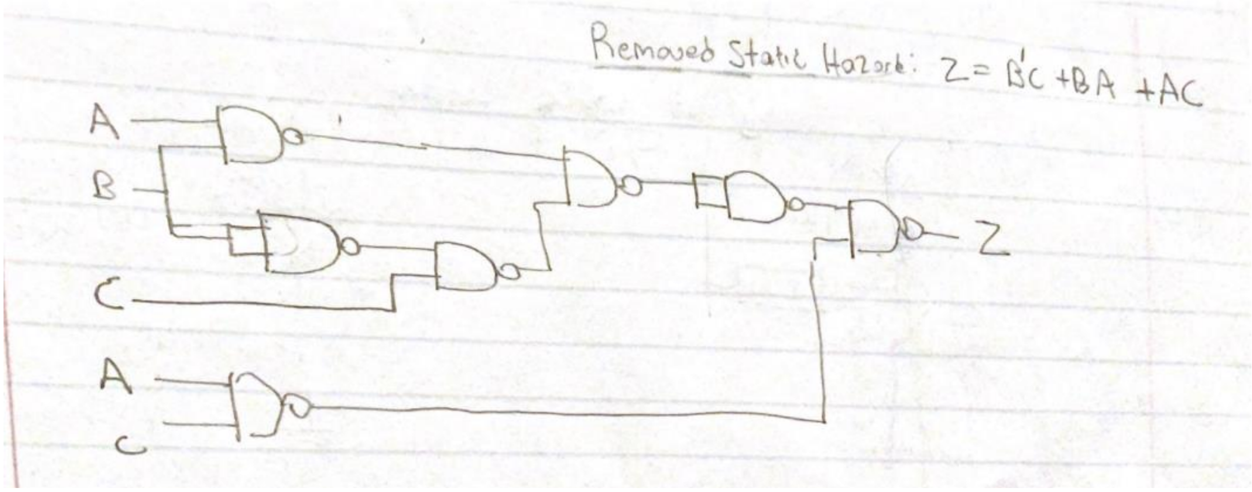


The 2-by-1 mux can be implemented using only four NAND gates, which is the exact amount of NAND gates in a 7400 IC. When implementing this, the problem of this circuit can be found when observing the output waveform when both A and C are high and B switches from high to low and the static 1 hazard appears. Now, what needs to be done is creating a new circuit that adds redundant logic that will ensure that the Static 1 hazard cannot appear. This is done by adding extra expressions to cover all adjacent minterms on the K map and re-implementing the circuit. The Karnaugh map shown below illustrates this process.



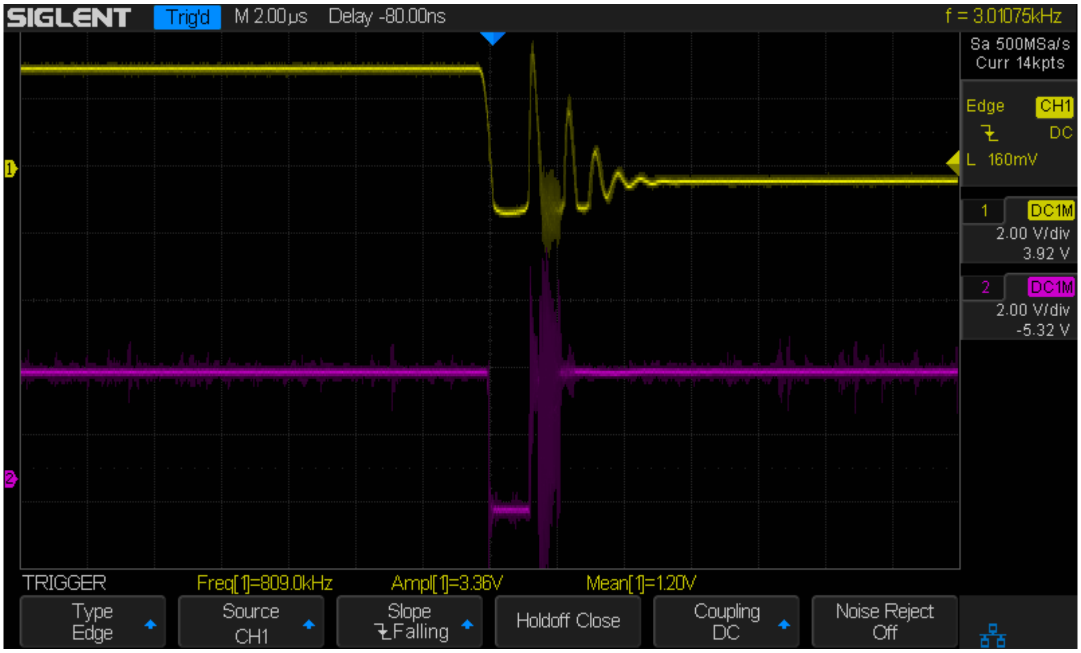
A \ BC	00	01	11	10
0	0	1	0	0
1	0	1	1	1

Now that this extra term is added, the function becomes **Z = B'C + BA + AC**. Now that this function is derived, we can create a new logic diagram using only NAND gates, and this time we are not expecting to see a Static 1 hazard. To implement using only NAND gates, we follow the same process as before (using Demorgan's Law) to make the switch from minimal SOP form to NANDs. Shown below is a drawing of the resulting logic diagram.



This circuit only requires 7 NAND gates, which means that only two 7400 ICs will be needed to implement this circuit. This can be confirmed by evaluating the waveforms of the output from before the static hazard is removed to after the static hazard is removed (old circuit vs. new circuit).

Before Static Hazard Removal (First Circuit)



M 2.00μs Delay -80.00ns f = 3.01075kHz

Sa 500MSa/s
Curr 14kpts

Edge CH1
DC
L 160mV

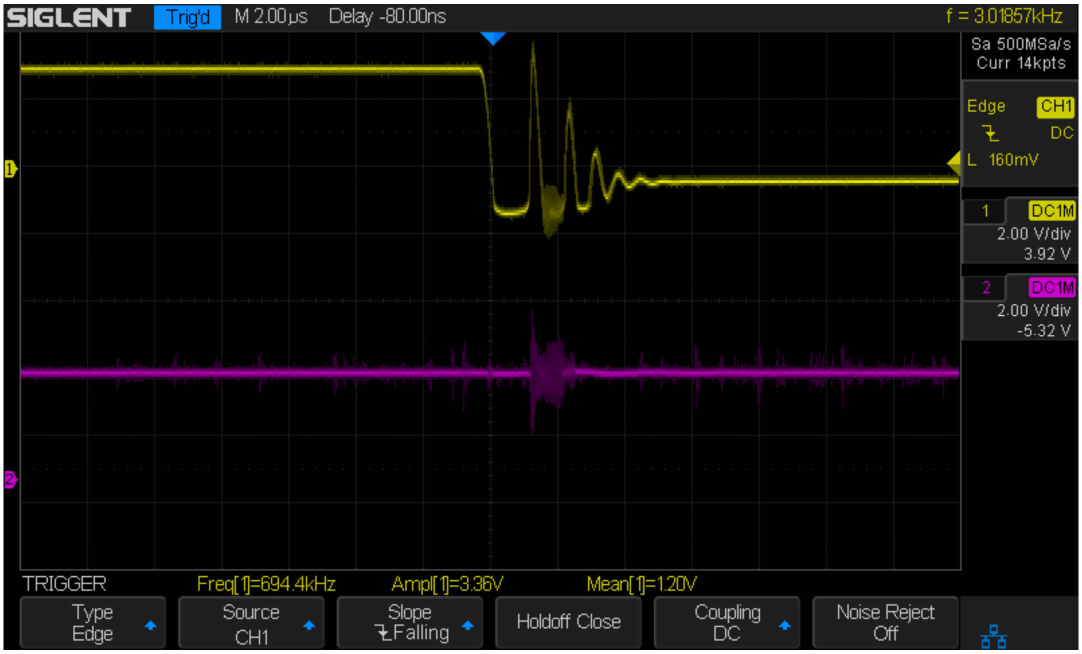
1 DC1M
2.00 V/div
3.92 V

2 DC1M
2.00 V/div
-5.32 V

Freq[1]=809.0kHz Ampl[1]=3.36V Mean[1]=1.20V

Type Edge | Source CH1 | Slope Falling | Holdoff Close | Coupling DC | Noise Reject Off

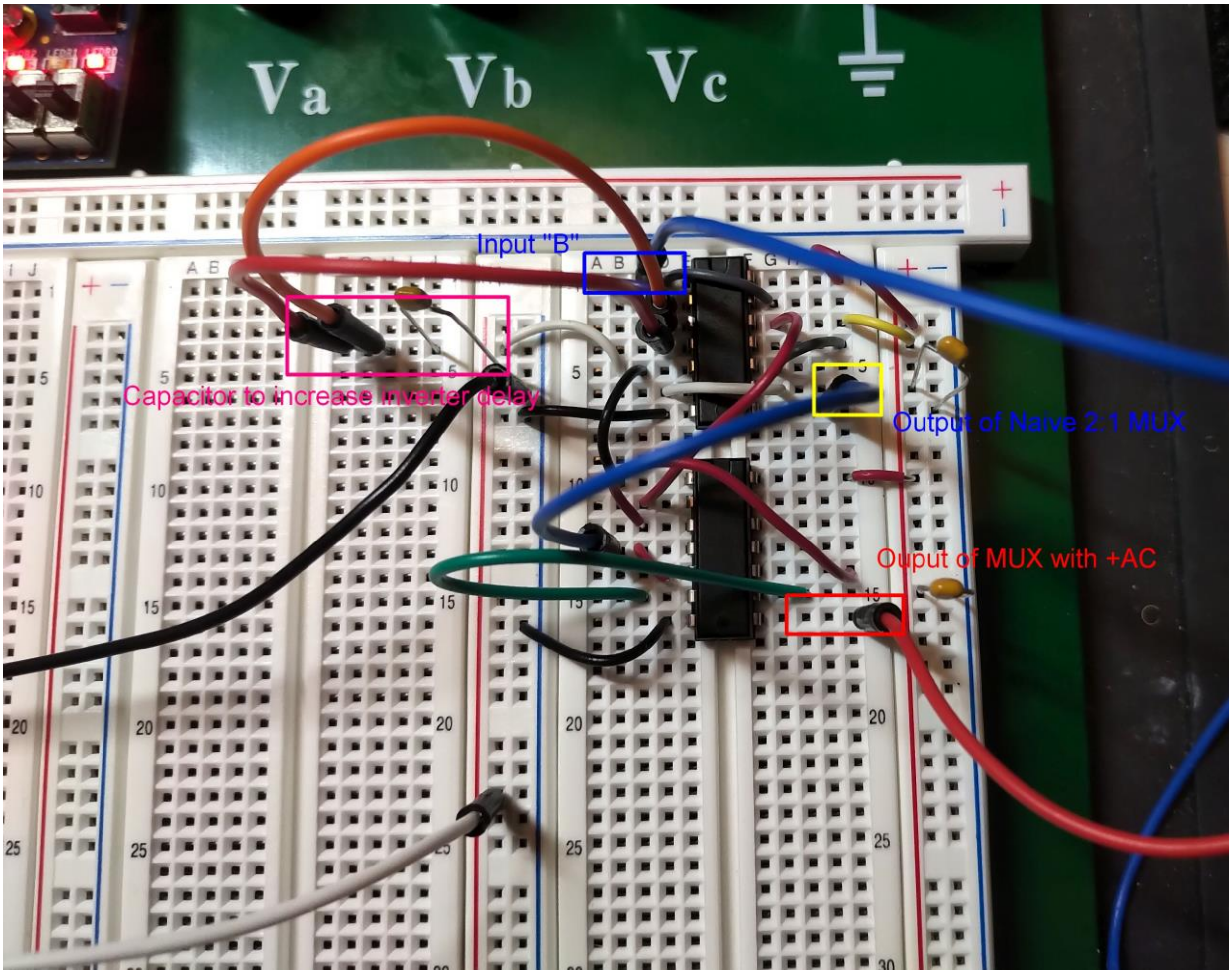
After Static Hazard Removal (New Circuit)



M 2.00µs
Delay -80.00ns
f = 3.01857kHz
Sa 500MSa/s
Curr 14kpts
Edge CH1
DC
L 160mV
1 DC1M
2.00 V/div
3.92 V
2 DC1M
2.00 V/div
-5.32 V
TRIGGER
Freq[1]=694.4kHz
Ampl[1]=3.36V
Mean[1]=1.20V
Type Edge
Source CH1
Slope Falling
Holdoff Close
Coupling DC
Noise Reject Off

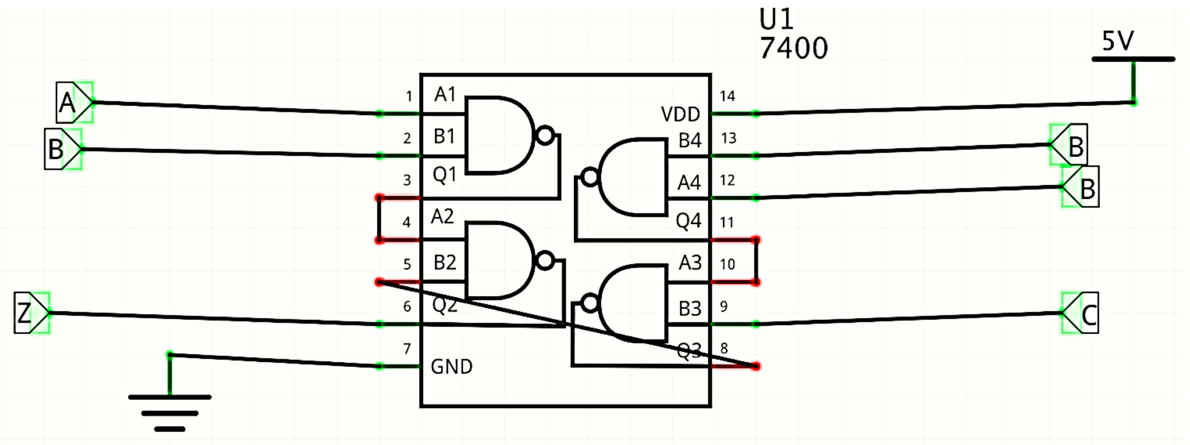
The first waveform shows a Static 1 hazard when the output momentarily drops to 0 and then comes back up to 1. This does not happen in the second waveform that uses the new circuit, and you can see that there is no drop on that waveform.

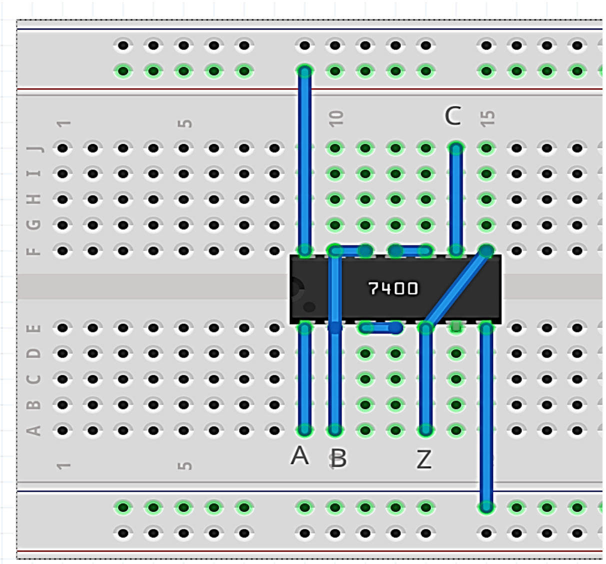
Below shows the actual implementation of the circuit without the static 1 hazard on a breadboard. Only two 7400 ICs were used and a capacitor was used to increase the inverter delay.



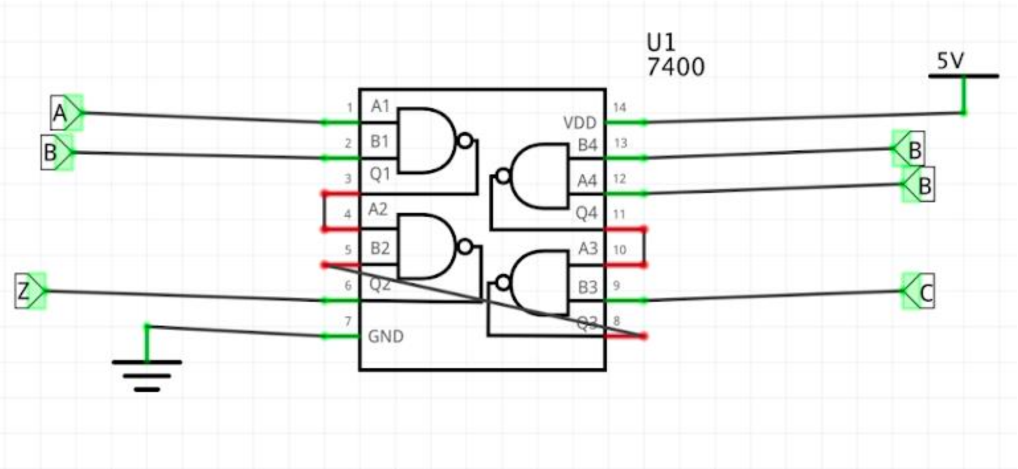
Component Diagrams

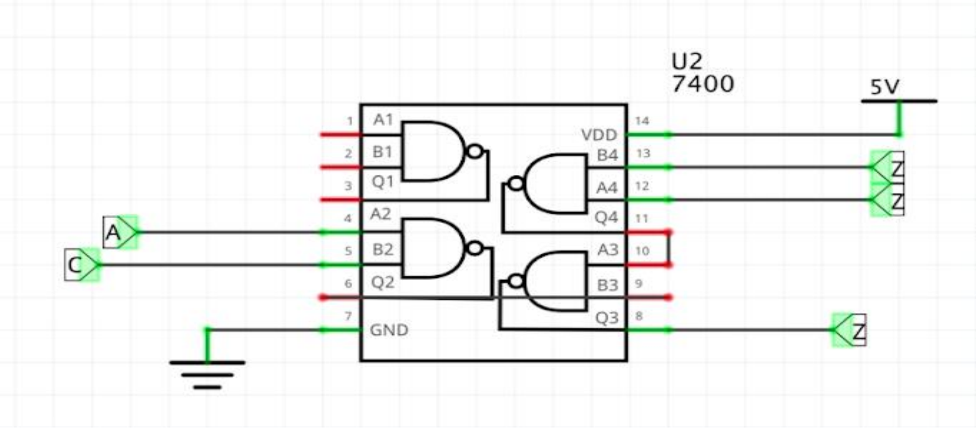
I used Fritzing to create all the diagrams for the implementation of the circuit using the 7400 IC. Below are the schematic and the breadboard views of the singular 7400IC with the inputs and the outputs connected to the IC as well as the wiring necessary for the circuit with the static 1 hazard.

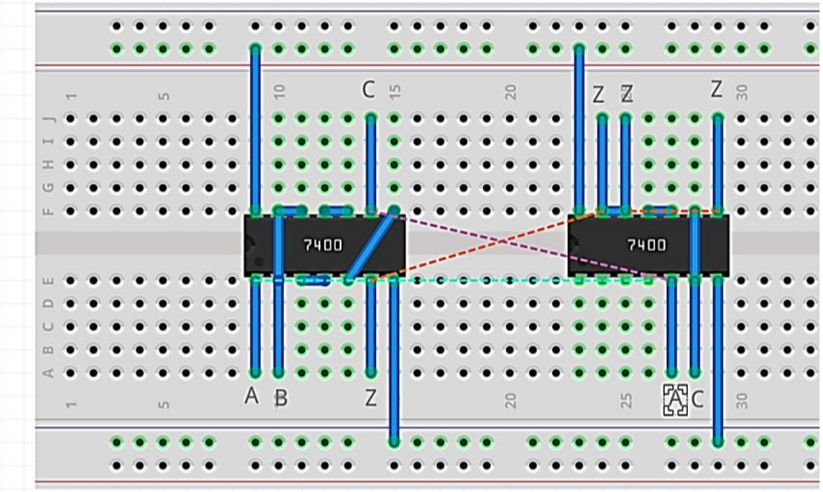




Below are the same screenshots but for the circuit without the static 1 hazard.



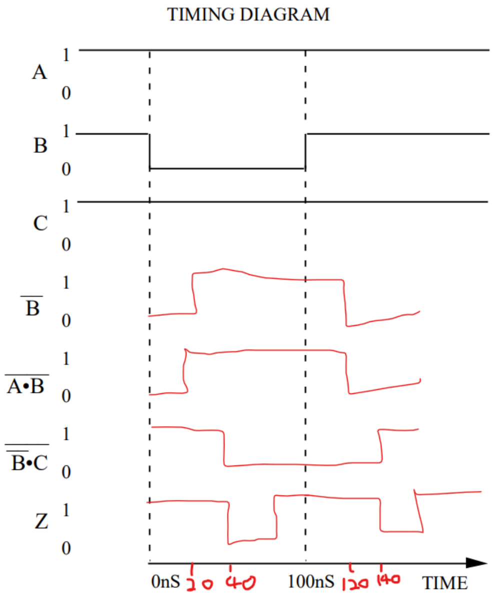




Prelab Questions

Some groups may not get a static hazard because the gate delay is not a value that is set in stone. The datasheet of the 7400IC may provide a value but it is possible that for the specific IC being used, there is a smaller gate delay than the manufacturer anticipates. The capacitor can be added to amplify the delay time so the waveform can clearly depict the momentary static 1 glitch from the first circuit.

Postlab Questions



1. It takes 60 ns for Z to stabilize because the path to Z would be 3 NAND gates for both the rising and falling edge of B. There are definitely glitches in Z, which can be seen from 40ns to 60ns, where Z momentarily drops to 0, since the top path would be shorter than the bottom path for the signal to get

to on the circuit with the static hazard. This means that you can see a momentary drop due to gate delays.

2. A mechanical switch is prone to allowing floating values to be inputted in the process of switching or pressing on a button. Using SR latches, this problem can be solved with a debouncer.

Conclusion

The lab was a great introduction to the content of the course and a great learning tool to understand static hazards and how to implement solutions to get rid of them. It also allows for a brief introduction to reading schematics and practicing how to understand the functionality of different ICs.

Since this lab was not conducted in person by me, I didn’t have any problems with the lab, however I can anticipate myself running into problems with the waveform generation or using the scope if I was to do this in person since I don’t have too much experience with scopes. I learned about debouncing switches after writing my answer to the second question in the post-lab, which asked about mechanical switches causing floating values which may not seem like too much of a problem until you try to implement your own circuit, which is also another potential difficulty I could’ve encountered if I actually worked on the lab in person.