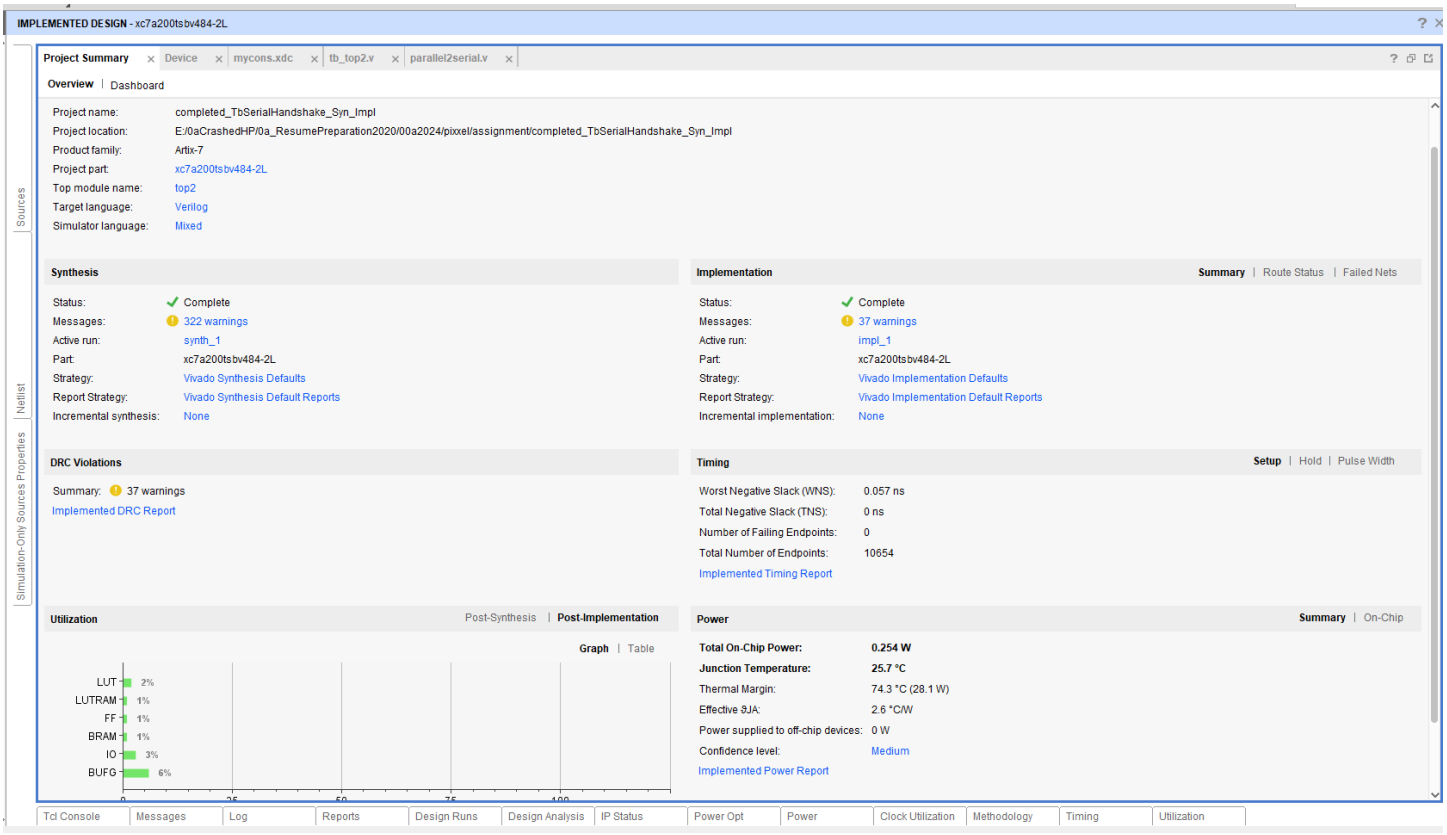
Improvements Made

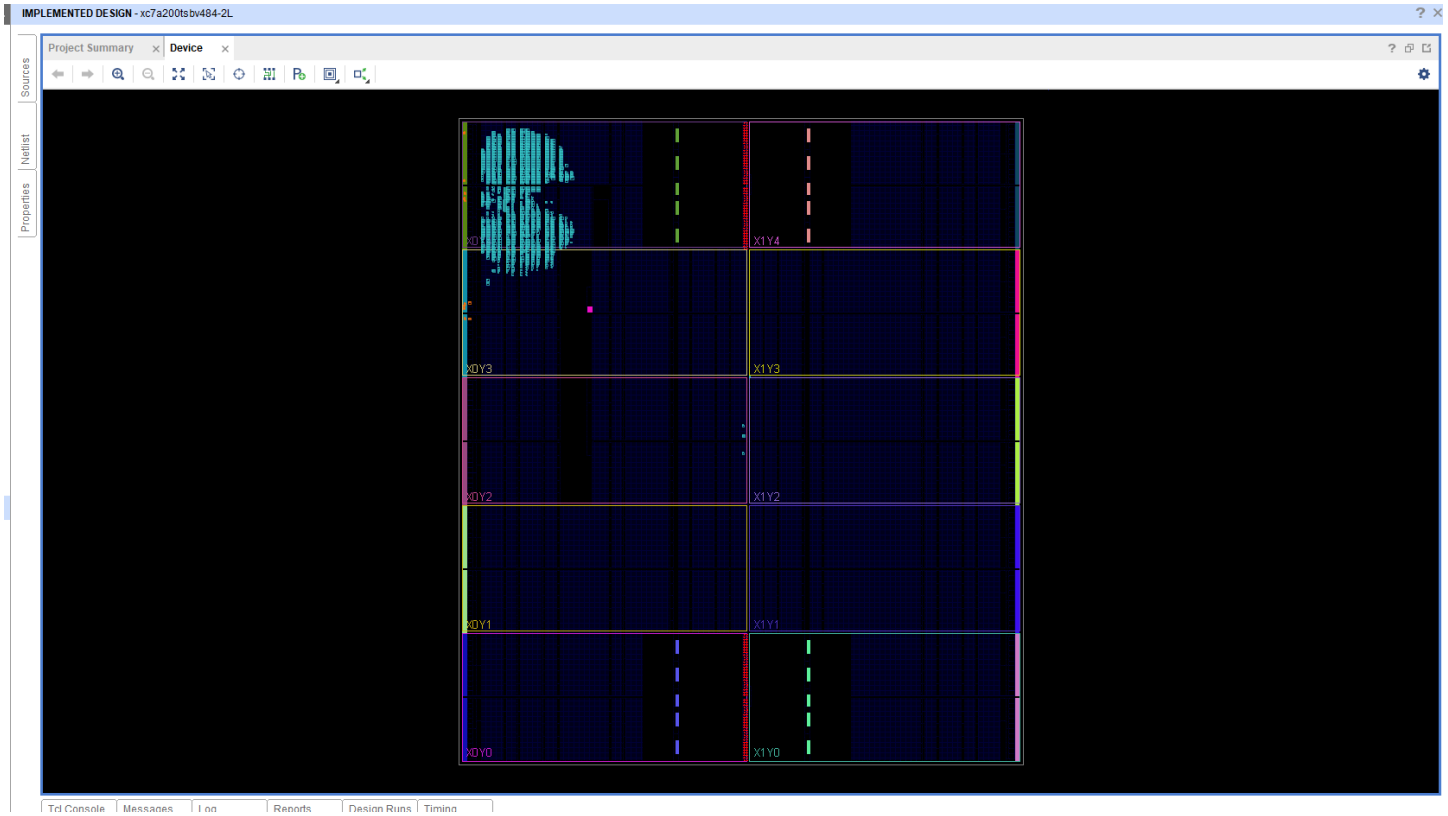
1. **Tested verified Serial Handshaking :** The testbench was modified to test serial handshaking properly, where serial ready in input goes to zero and back to 1 taking a random number of clock cycles.

2. **Removed unnecessary logic:** The parallel to serial module had a Primary input *serial_ready_in* → *serial_ready_in_t_Register*. This register was removed to facilitate proper handshaking with testbench. Also all the redundant combinational delays that were added to delay this path to make it pass hold timing were found unnecessary with better constraints and so were removed.

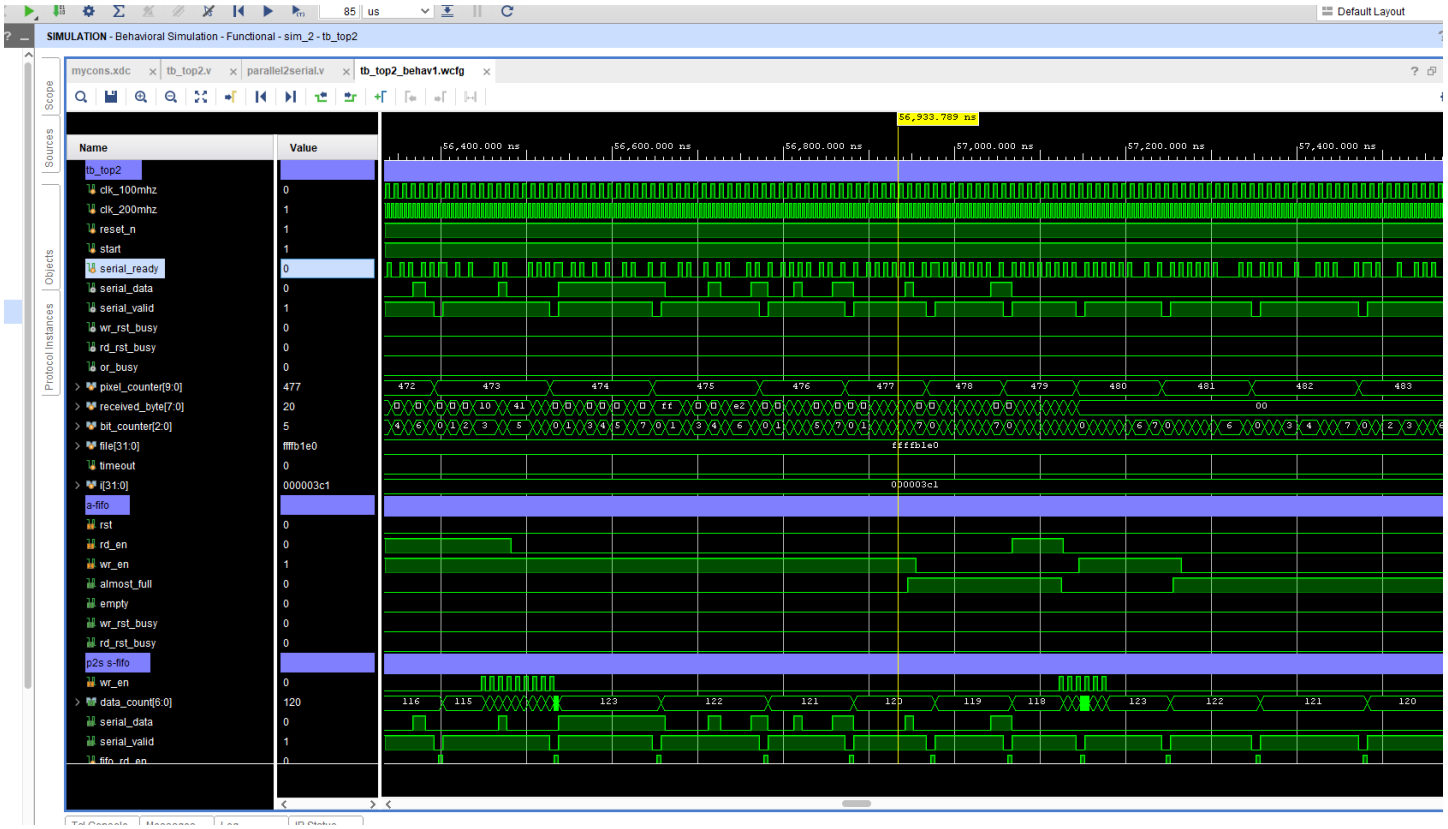
3. **The Design constraint file was improved** with better calculation for set input and set output delay. This resulted in avoiding setup or hold error with the serial ready in Pin or any other path. The design passed synthesis and implementation runs.

4. Currently the design works as Originally intended with **Serializer working at 200 Mhz** and properly handshaking with test bench. The design was synthesized and implemented successfully and the simulation was run at all steps. The waveform .wdb files for these simulations are in **Sim_waveforms** directory. The output pixel image data stream was verified to be correctly working after recreating the image with python script.

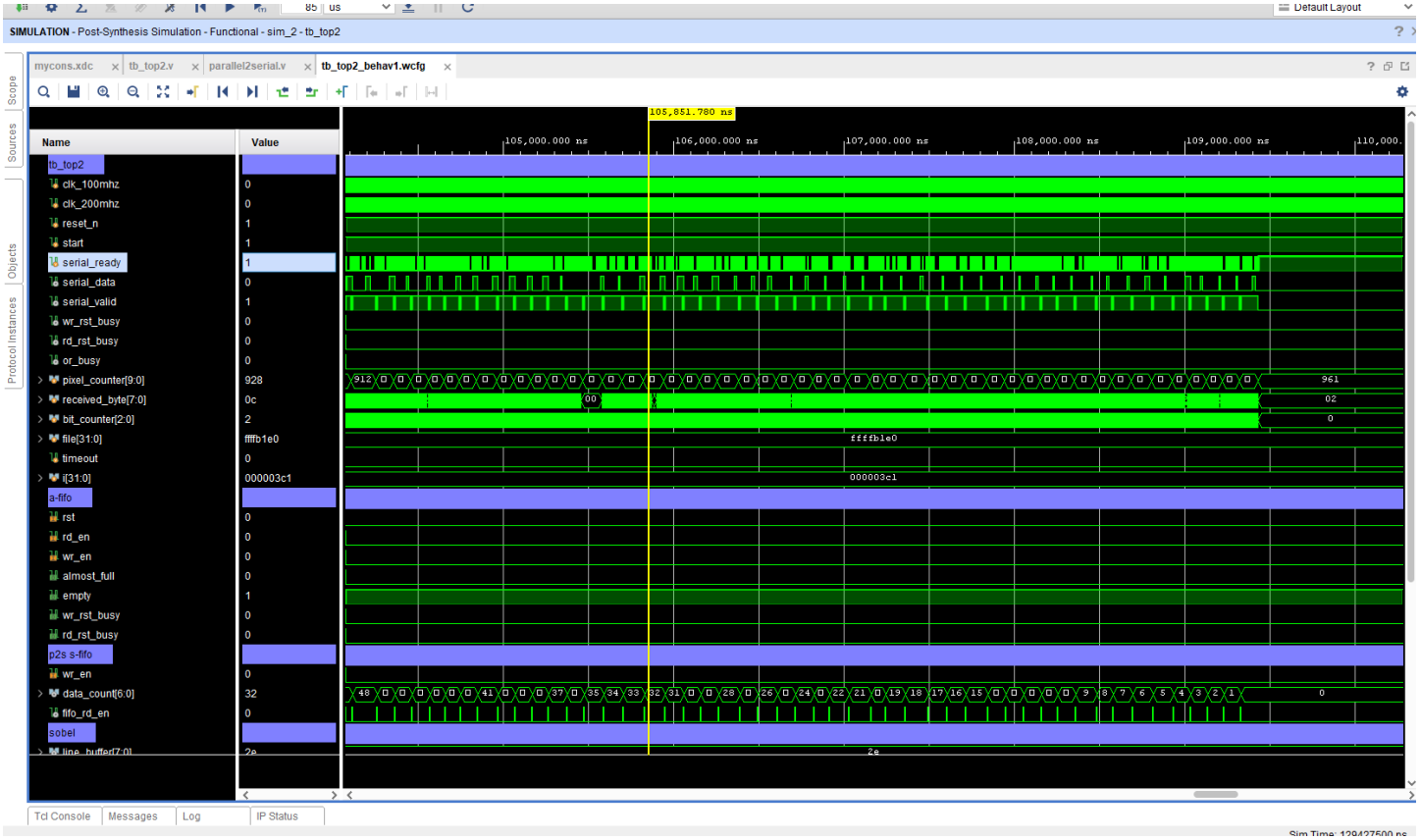




Sim behavioral



Sim synthesis



Sim implementation