Lebanese American University

Digital Systems Lab

Thursday's Section – 33

Final Project

Thursday, May 5, 2022

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Introduction:

In this project, we were asked to implement a project room management system. The system works based on two modes, normal and administration mode. To tackle it, we will be implementing a *Finite State Machine.* We will also be using multiple components in the FPGA, along with the PS/2 keyboard.

Project Description:

To design a project room management system, we would be decomposing it into two parts, the *normal* and *administrative* mode.

Normal Mode:

- The system starts with a waiting state for the user to enter their ID. It would show the relevant LCD display of "Door Locked Enter valid ID".
- Through the keyboard, the user would have to input the 9-digit ID, and whether the inputted ID is found to be one of the *five* predefined IDs, the user is granted access to the room. The LCD would display "Access Granted ID: *xxxxxxxxx*". Also, a green LED would blink every 0.5s for 5s.
- An else case would result if the user inputted a *wrong* ID, where the LCD would show "Access denied Try Again". A red LED would blink every 0.25s for 5s.
- Another case might arise if user inputted the *correct* ID, but the room was full. The LCD would display *Access denied Room is Full".*
- Finally, a button can be pressed to allow a person to leave the room.

Administrative Mode:

- To enter administrator mode, the user must press "*Alt+Ctrl+A"* simultaneously. The user has to input one of the predefined *admin* IDs to be granted access to this mode.
- If true, the LCD would display *Administrator Mode* where all green and red LEDs would blink in a certain pattern. If false, the system returns to *normal mode*.
- In the admin mode, the administrator is granted two options.
    1. Override the room capacity
    2. Add new IDs
- If the admin presses 1, they would be in the case of overriding the room capacity. After inputting the number of choice, they would have to confirm it, with the LCD showing "*Press enter to confirm num: xx*".
- If the admin presses 2, they would be in the case of adding a new ID to prompt more people into the room.
- If the inputted ID by the admin does *not* exist, it would save it, if it *does* exist, the system will ask the admin to input another one. The relevant sentences would be displayed on the LCD.

Since we are only two in the group, we were asked to implement only this part of the project

Finite State Machine:

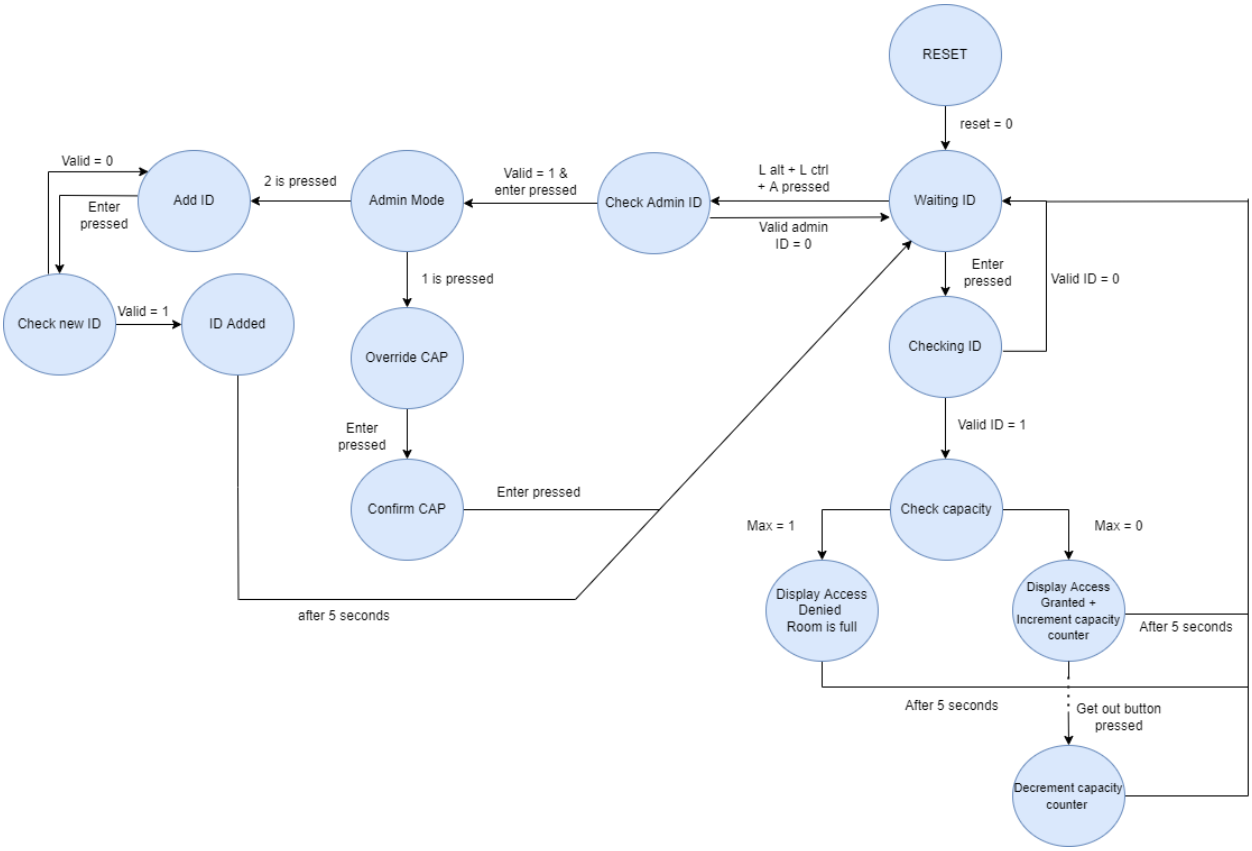

Figure 1: Finite State Machine

Explanation:

The above figure illustrates the *Finite State Machine (FSM)* that we followed and explained in the section above. However, it is important to note that one of states had to be developed further.

To explain this further, in the state "Admin Mode", we had to create a new state called "Admin Mode 2", which is not seen in the figure above, and that is to stop the LEDs from continuously blinking – they had to blink for *five* seconds. For them to stop blinking, we had to break from the "Admin Mode" state and go to the new one. In the new one, "Admin Mode 2", there, we are actually checking what option the admin prompted for – *override capacity or add new ID*.

** The codes can be found in a folder, attached to this document**

System Block Diagram:

The below figure further identifies the modules connected to our system:

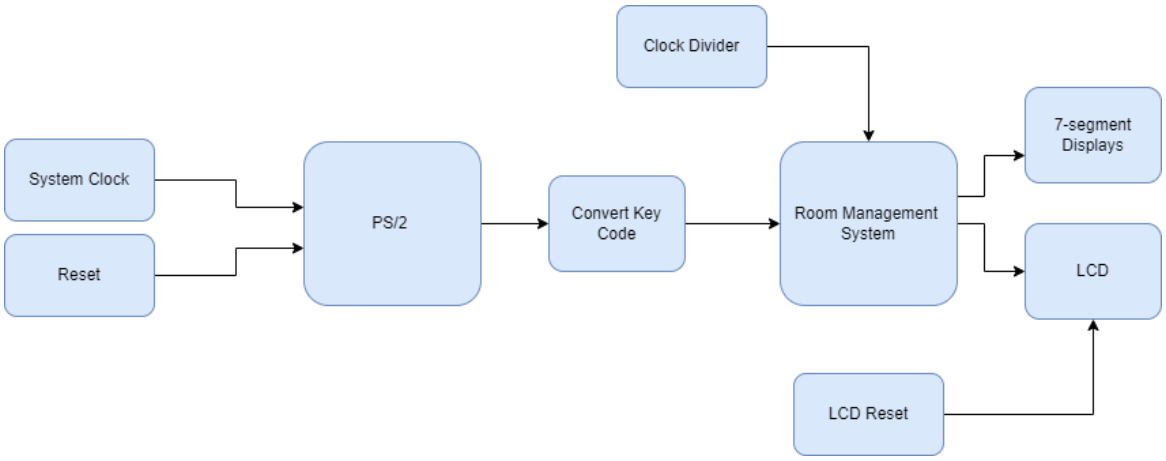

Figure 2: Block Diagram of the System

- The system clock – working at a 50MHz frequency, is fed into the system, along with the reset, that as the name suggests, resets it.
- A PS/2 module is instantiated to interface the FPGA with the keyboard.
- Next, a new module of our own is created that converts keyboard key codes to their hexadecimal value. For this project, we only used digits, 0 through 9.
- Our main block is the room management system block, where it loops through all the states defined earlier.
- It also includes a clock divider as one of its inputs for the push button to work properly. The problem that arose with the push button is that if it were to be pressed in the same process that is sensitive to the FPGA clock, it would register the input as multiple inputs. Therefore, we had to link it with a process that works on a slower clock using a clock divider. The output of this divider is a *five-second* clock (equivalent to the time of the state where the push button is being handled).
- Finally, the main output of our system is interfaced with the 7-segment displays and the LCD. The necessary instantiations for these two components are done.
  (Another block in our system that is worth mentioning is the LCD reset module whose job is to reset the LCD whenever a new input is written into it.)

Pin Assignment:

Finally, we assign the required pins as such:

	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
1	CLK	Bidir	PIN_G6	1	B1_N0	2.5 V (default)	
2	DAT	Bidir	PIN_H5	1	B1_N1	2.5 V (default)	
3	LCD_DATA[7]	Output	PIN_M5	1	B1_N2	2.5 V (default)	
4	LCD_DATA[6]	Output	PIN_M3	1	B1_N1	2.5 V (default)	
5	LCD_DATA[5]	Output	PIN_K2	1	B1_N1	2.5 V (default)	
6	LCD_DATA[4]	Output	PIN_K1	1	B1_N1	2.5 V (default)	
7	LCD_DATA[3]	Output	PIN_K7	1	B1_N1	2.5 V (default)	
8	LCD_DATA[2]	Output	PIN_L2	1	B1_N2	2.5 V (default)	
9	LCD_DATA[1]	Output	PIN_L1	1	B1_N2	2.5 V (default)	
10	LCD_DATA[0]	Output	PIN_L3	1	B1_N1	2.5 V (default)	
11	LCD_EN	Output	PIN_L4	1	B1_N1	2.5 V (default)	
12	LCD_RS	Output	PIN_M2	1	B1_N2	2.5 V (default)	
13	LCD_RW	Output	PIN_M1	1	B1_N2	2.5 V (default)	
14	LEDs_green[7]	Output	PIN_F17	7	B7_N2	2.5 V (default)	
15	LEDs_green[6]	Output	PIN_G21	7	B7_N1	2.5 V (default)	
16	LEDs_green[5]	Output	PIN_G22	7	B7_N2	2.5 V (default)	
17	LEDs_green[4]	Output	PIN_G20	7	B7_N1	2.5 V (default)	
18	LEDs_green[3]	Output	PIN_H21	7	B7_N2	2.5 V (default)	
19	LEDs_green[2]	Output	PIN_E24	7	B7_N1	2.5 V (default)	
20	LEDs_green[1]	Output	PIN_E25	7	B7_N1	2.5 V (default)	
21	LEDs_green[0]	Output	PIN_E22	7	B7_N0	2.5 V (default)	
22	LEDs_red[16]	Output	PIN_H15	7	B7_N2	2.5 V (default)	
23	LEDs_red[15]	Output	PIN_G16	7	B7_N2	2.5 V (default)	
24	LEDs_red[14]	Output	PIN_G15	7	B7_N2	2.5 V (default)	
25	LEDs_red[13]	Output	PIN_F15	7	B7_N2	2.5 V (default)	
26	LEDs_red[12]	Output	PIN_H17	7	B7_N2	2.5 V (default)	
27	LEDs_red[11]	Output	PIN_J16	7	B7_N2	2.5 V (default)	
28	LEDs_red[10]	Output	PIN_H16	7	B7_N2	2.5 V (default)	

	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
29	LEDs_red[9]	Output	PIN_J15	7	B7_N2	2.5 V (default)	
30	LEDs_red[8]	Output	PIN_G17	7	B7_N1	2.5 V (default)	
31	LEDs_red[7]	Output	PIN_J17	7	B7_N2	2.5 V (default)	
32	LEDs_red[6]	Output	PIN_H19	7	B7_N2	2.5 V (default)	
33	LEDs_red[5]	Output	PIN_J19	7	B7_N2	2.5 V (default)	
34	LEDs_red[4]	Output	PIN_E18	7	B7_N1	2.5 V (default)	
35	LEDs_red[3]	Output	PIN_F18	7	B7_N1	2.5 V (default)	
36	LEDs_red[2]	Output	PIN_F21	7	B7_N0	2.5 V (default)	
37	LEDs_red[1]	Output	PIN_E19	7	B7_N0	2.5 V (default)	
38	LEDs_red[0]	Output	PIN_F19	7	B7_N0	2.5 V (default)	
39	clock_in	Input	PIN_Y2	2	B2_N0	2.5 V (default)	
40	getOut	Input	PIN_M23	6	B6_N2	2.5 V (default)	
41	led_g	Output	PIN_E21	7	B7_N0	2.5 V (default)	
42	led_r	Output	PIN_G19	7	B7_N2	2.5 V (default)	
43	outID_1[6]	Output	PIN_AD17	4	B4_N2	2.5 V (default)	
44	outID_1[5]	Output	PIN_AE17	4	B4_N2	2.5 V (default)	
45	outID_1[4]	Output	PIN_AG17	4	B4_N2	2.5 V (default)	
46	outID_1[3]	Output	PIN_AH17	4	B4_N2	2.5 V (default)	
47	outID_1[2]	Output	PIN_AF17	4	B4_N2	2.5 V (default)	
48	outID_1[1]	Output	PIN_AG18	4	B4_N2	2.5 V (default)	
49	outID_1[0]	Output	PIN_AA14	3	B3_N0	2.5 V (default)	
50	outID_2[6]	Output	PIN_AA17	4	B4_N1	2.5 V (default)	
51	outID_2[5]	Output	PIN_AB16	4	B4_N2	2.5 V (default)	
52	outID_2[4]	Output	PIN_AA16	4	B4_N2	2.5 V (default)	
53	outID_2[3]	Output	PIN_AB17	4	B4_N1	2.5 V (default)	
54	outID_2[2]	Output	PIN_AB15	4	B4_N2	2.5 V (default)	
55	outID_2[1]	Output	PIN_AA15	4	B4_N2	2.5 V (default)	
56	outID_2[0]	Output	PIN_AC17	4	B4_N2	2.5 V (default)	

	Node Name	Direction	Location	I/O Bank	VREF Group	I/O Standard	Reserved
57	outID_3[6]	Output	PIN_AD18	4	B4_N1	2.5 V (default)	
58	outID_3[5]	Output	PIN_AC18	4	B4_N1	2.5 V (default)	
59	outID_3[4]	Output	PIN_AB18	4	B4_N0	2.5 V (default)	
60	outID_3[3]	Output	PIN_AH19	4	B4_N2	2.5 V (default)	
61	outID_3[2]	Output	PIN_AG19	4	B4_N2	2.5 V (default)	
62	outID_3[1]	Output	PIN_AF18	4	B4_N1	2.5 V (default)	
63	outID_3[0]	Output	PIN_AH18	4	B4_N2	2.5 V (default)	
64	outID_4[6]	Output	PIN_AB19	4	B4_N0	2.5 V (default)	
65	outID_4[5]	Output	PIN_AA19	4	B4_N0	2.5 V (default)	
66	outID_4[4]	Output	PIN_AG21	4	B4_N2	2.5 V (default)	
67	outID_4[3]	Output	PIN_AH21	4	B4_N2	2.5 V (default)	
68	outID_4[2]	Output	PIN_AE19	4	B4_N1	2.5 V (default)	
69	outID_4[1]	Output	PIN_AF19	4	B4_N1	2.5 V (default)	
70	outID_4[0]	Output	PIN_AE18	4	B4_N2	2.5 V (default)	
71	outID_5[6]	Output	PIN_V21	5	B5_N1	2.5 V (default)	
72	outID_5[5]	Output	PIN_U21	5	B5_N0	2.5 V (default)	
73	outID_5[4]	Output	PIN_AB20	4	B4_N0	2.5 V (default)	
74	outID_5[3]	Output	PIN_AA21	4	B4_N0	2.5 V (default)	
75	outID_5[2]	Output	PIN_AD24	4	B4_N0	2.5 V (default)	
76	outID_5[1]	Output	PIN_AF23	4	B4_N0	2.5 V (default)	
77	outID_5[0]	Output	PIN_Y19	4	B4_N0	2.5 V (default)	
78	outID_6[6]	Output	PIN_AA25	5	B5_N1	2.5 V (default)	
79	outID_6[5]	Output	PIN_AA26	5	B5_N1	2.5 V (default)	
80	outID_6[4]	Output	PIN_Y25	5	B5_N1	2.5 V (default)	
81	outID_6[3]	Output	PIN_W26	5	B5_N1	2.5 V (default)	
82	outID_6[2]	Output	PIN_Y26	5	B5_N1	2.5 V (default)	
83	outID_6[1]	Output	PIN_W27	5	B5_N1	2.5 V (default)	
84	outID_6[0]	Output	PIN_W28	5	B5_N1	2.5 V (default)	
85	outID_7[6]	Output	PIN_M24	6	B6_N2	2.5 V (default)	
86	outID_7[5]	Output	PIN_Y22	5	B5_N0	2.5 V (default)	
87	outID_7[4]	Output	PIN_W21	5	B5_N1	2.5 V (default)	
88	outID_7[3]	Output	PIN_W22	5	B5_N0	2.5 V (default)	
89	outID_7[2]	Output	PIN_W25	5	B5_N1	2.5 V (default)	
90	outID_7[1]	Output	PIN_U23	5	B5_N1	2.5 V (default)	
91	outID_7[0]	Output	PIN_U24	5	B5_N0	2.5 V (default)	
92	outID_8[6]	Output	PIN_G18	7	B7_N2	2.5 V (default)	
93	outID_8[5]	Output	PIN_F22	7	B7_N0	2.5 V (default)	
94	outID_8[4]	Output	PIN_E17	7	B7_N2	2.5 V (default)	
95	outID_8[3]	Output	PIN_L26	6	B6_N1	2.5 V (default)	
96	outID_8[2]	Output	PIN_L25	6	B6_N1	2.5 V (default)	
97	outID_8[1]	Output	PIN_J22	6	B6_N0	2.5 V (default)	
98	outID_8[0]	Output	PIN_H22	6	B6_N0	2.5 V (default)	
99	reset_clk	Input	PIN_AC28	5	B5_N2	2.5 V (default)	
100	reset_ps2	Input	PIN_AB28	5	B5_N1	2.5 V (default)	

Figure 3: Pin Assignment

Conclusion:

As a final project, we were asked to work with multiple components of the FPGA to create a project room management system. We had to use the PS/2 keyboard along with the FPGA to simulate what is required. We tackled this project using a design of *Finite State Machines*, where we laid out all the possible states of it and proceeded with the coding.