	Test 1 (mul.v)	Test 2 (full_adder.v)	Test 3 (counter.v)	Test 4 (RisingEdge_DFlipFlop.v)	Test 5 (divider.v)	All
Testbench Name	X	X	X	X	X	X
Clock & reset			X	X	X	X
Connect Parameters			X		X	X
Connect Inputs & outputs Ports	x	X	X	X	X	X
Terminate Simulation	x	X	X	X	X	X
Random Generation	x	X	X	X		X
Dump file (.vcd)	x	X	X	X	X	X
Time Scale	x	X	X	X	X	X
Initialize by zero	x	X	X	X	X	X
Resultant dumped on terminal	x	X	X	X	X	X
Declare Essential Parameters	x	X	X	X	X	X