DSD Final Project Scores (RISC-V)

1. Baseline

(1) Area: (um^2)

截圖:

(2) Total Simulation Time of given hasHazard testbench: (ns)

截圖:

(3) Area*Total Simulation Time: (um^2 * ns)

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

2. BrPred

(1) Total execution cycles of given I_mem_BrPred:

截圖:

(2) Total execution cycles of given I_mem_hasHazard:

截圖:

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um^2)

3. L2 Cache

(1) Average memory access time: (ns)

(2) Total execution time of given I_mem_L2Cache: (ns)

截圖:

4. Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um^2)

截圖:

(2) Total Simulation Time of given I_mem_compression: (ns)

截圖:

(3) Area*Total Simulation Time: (um^2 * ns)

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)