Computer Architecture Homework #3

Verilog RISC-V Decoder

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Due 2020/12/1 13:00 Tuesday (CEIBA, no late homework is allowed.)

1. Introduction

In this exercise, we ask you to write a RISC-V instruction decoder. Reading instructions one by one and decode the instruction type and format. After reading each instructions, you have to decode instructions and type.

We ask you to decode 23 instructions, "JAL, JALR, BEQ, BNE, LD, SD, ADDI, SLTI, XORI, ORI, ANDI, SLLI, SRLI, SRAI, ADD, SUB, SLL, SLT, XOR, SRL, SRA, OR, AND" and output instruction_type as below.

```
{JAL,JALR,BEQ,BNE,LD,SD,ADDI,SLTI,XORI,ORI,ANDI,SLLI,SRLI,SRAI,ADD,SUB,SLL,SLT,XOR,SRL,SRA,OR,AND};
```

Ex. For JAL we have to send {1'b1,22'b0} to instruction_type next cycle

Ex. ADDI: {6'b0, 1'b1, 16'b0}, AND: {22'b0, 1'b1}

Besides, instruction_format output should be like {R type, I type, S type, B type, J type}

Ex. ADDI(I type): {5'b01000} JAL(J type): {5'b00001}

Make sure you understand and check the instructions and it's answer in pattern folder.

2. Specification

The input/output pins are defined in Table1:

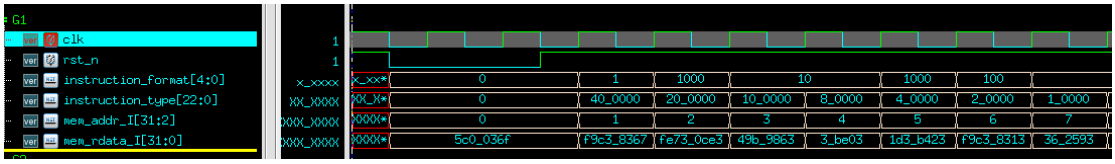
Tabel1 :I/O pins specification

Signal name	I/O	Bit width	Description
clk	I	1	Clock signal. Positive edge trigger.
rst_n	I	1	Active low **asynchronous** reset signal.
mem_addr_I	O	30	Output address of the instruction memory
mem_rdata_I	I	32	Instruction read from instruction memory
instruction_type	O	23	Decode and output which type of instruction
instruction_format	O	5	Decode and output R/I/S/B/J type

3. Timing Diagram for Memory

Below figure shows the timing diagram for our HW. After reset, rst_n is positive and you can start to send mem_addr_I. Then the testbench will give you mem_rdata_I instructions code. You have to decode it and output corresponding format and type.

We will check your instruction answer after your mem_addr_I is not zero. Don't stop counting up your mem_addr_I(Program Counter), just fetch instructions line by line.



4. Simulation Scripts

4.1 Sample Code: findmax

Circuit findmax.v finds the max and argmax value for eight continuous inputs. Visit folder sample/findmax and run the following script.

ncverilog testfixture.v findmax.v +access+r

4.2 Sample Code: matvec2x2

Circuit matvec2x2.v computes matrix-vector multiplication Ax. In this sample, the size of matrix A is 2x2 and the size of vector x is 2x1. Visit folder sample/matvec2x2 and run the following script.

ncverilog testfixture.v matvec2x2.v +access+r +define+tb1 +notimingchecks

4.3 RTL-SYN Read the README.txt

4.4 Debug

Use program nWave to view the simulated signals. This will be very helpful for this exercise.

nWave &

5. Files

- The deadline for this exercise is 13:00, Dec. 1th. Your work should be submitted in a compressed file following the naming convention, HW3_yourID.zip (for example, HW1_b07901999.zip). The file should look like: **(5% penalty for wrong format)** There's a 10% penalty for incorrect upload format. No late submission is accepted.
  - HW3_yourID.zip
    - HW3_yourID/
      - CHIP.v (RTL file)
      - CHIP_syn.v (synthesized gate-level netlist)
      - CHIP_syn.ddc (Design database generated by Synopsys

Design Compiler)

- CHIP_syn.sdf (Pre-layout gate-level sdf)
- yourID.pdf (Report)

6. Grading Criteria

Don't try to pass your code by modifying decoder_tb.v except cycle time. We will check by our testbench. We encourage you to generate testing file by RARS.

Plagiarism is prohibited!

Item	Description
RTL correctness(20%)	Your CHIP.v should give correct answer.
RTL tb(hidden) (20%)	Additional test case besides the provided files
Gate level no latch(20%)	There are no latches in your gate level.
Gate-level correctness (20%)	Your CHIP_syn.v should give correct answer.
Report (20%)	Snapchat: 1. RTL(Pass) 2. SYN(Pass) 3. no latch 4. Timing report → report_timing 5. Area report → report_area Please describe how you design this circuit and what difficulties you encountered when working on this exercise. (Please write down your Verilog experiences.)

Ref:

RTL:

```
Success! Execution 23                    10000                    10000
Success! Execution 23   00000000000000000001  00000000000000000001
=========================================The RTL result is PASS=========================================
```

SYN:

```
Success! Execution 20   00000000000000000001000  00000000000000000001000
Success! Execution 21                    10000                    10000
Success! Execution 21   00000000000000000100  00000000000000000100
Success! Execution 22                    10000                    10000
Success! Execution 22   00000000000000000010  00000000000000000010
Success! Execution 23                    10000                    10000
Success! Execution 23   00000000000000000001  00000000000000000001
=========================================The SYN result is PASS=========================================
```

No latch:

```
Inferred memory devices in process
        in routine CHIP line 76 in file
                '/home/raid7_2/user08/r08016/Test_HW3/v1_2/CHIP.v'.
===============================================================================
|     Register Name      |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|  instruction_type_reg  | Flip-flop |  23   |  Y  | N  | Y  | N  | N  | N  | N  |
| instruction_format_reg | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
|         PC_reg         | Flip-flop |  32   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/user08/r08016/Test_HW3/v1_2/CHIP.db:CHIP'
Loaded 1 design.
Current design is 'CHIP'.
Current design is 'CHIP'.
```

Timing report:

```
CHIP              tsmc13_wl10           slow

Point                                   Incr       Path
-----------------------------------------------------------
clock CLK (rise edge)                   0.00       0.00
clock network delay (ideal)             0.50       0.50
input external delay                    0.10       0.60 f
mem_rdata_I[3] (in)                     0.02       0.62 f
U65/Y (CLKINVX8)                        0.03       0.66 r
U69/Y (AND3X8)                          0.09       0.75 r
U43/Y (NOR3BX4)                         0.11       0.86 r
U66/Y (BUFX16)                          0.09       0.96 r
U121/Y (NAND3X8)                        0.09       1.05 f
U175/Y (NOR3X1)                         0.20       1.25 r
instruction_type_reg_10_/D (DFFRX1)     0.00       1.25 r
data arrival time                                  1.25

clock CLK (rise edge)                   1.00       1.00
clock network delay (ideal)             0.50       1.50
clock uncertainty                      -0.10       1.40
instruction_type_reg_10_/CK (DFFRX1)    0.00       1.40 r
library setup time                     -0.15       1.25
data required time                                 1.25
-----------------------------------------------------------
data required time                                 1.25
data arrival time                                 -1.25
-----------------------------------------------------------
slack (MET)                                        0.00
```

Area report:

```
****************************************
Report : area
Design : CHIP
Version: N-2017.09-SP2
Date   : Fri Nov 13 23:57:26 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CE

Number of ports:                          153
Number of nets:                           438
Number of cells:                          354
Number of combinational cells:            290
Number of sequential cells:                63
Number of macros/black boxes:               0
Number of buf/inv:                        134
Number of references:                      48

Combinational area:            3376.128590
Buf/Inv area:                  1363.012206
Noncombinational area:         2393.333981
Macro/Black Box area:             0.000000
Net Interconnect area:        32993.498932

Total cell area:               5769.462571
Total area:                   38762.961503
```