DSD Final Project Scores (MIPS)

1. Baseline

(1) Area: (um2)

截圖:

```
Total cell area:                311107.958699
Total area:                    2486719.108540
```

=> 311107.958699 μm^2

(2) Total Simulation Time of given hasHazard testbench: (ns)

截圖: (nb = 16)

```
------------------------- Simulation FINISH !!-------------
================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================
stall cycle:   179,  process cycle:  2113
total cycle number:        2292
Simulation complete via $finish(1) at time 5753750 PS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
```

=> 5753.75 ns

(3) Area*Total Simulation Time: (um2 * ns)

=> 1,790,037,417.36 $\mu m^2 \times ns$

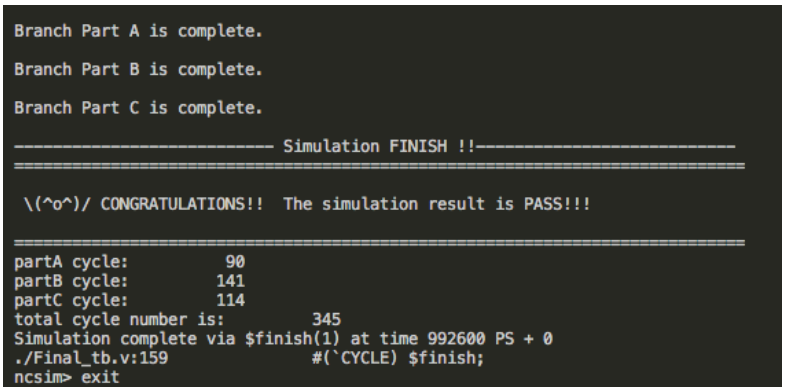
(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

=> 2.5 ns

2. BrPred

(1) Total execution cycles of given I_mem_BrPred:

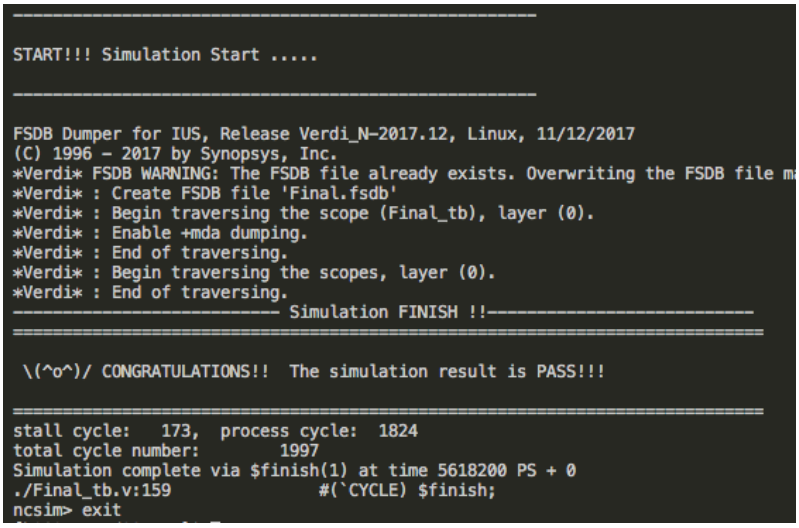
截圖: (nb_notBr = 10, nb_interBr = 20, nb_Br = 30)



=> 345 個 cycle

(2) Total execution cycles of given I_mem_hasHazard:

截圖: (nb = 16)



=> 1997 個 cycle

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um2)

=> 14,045.985096 μm^2

3. L2 Cache

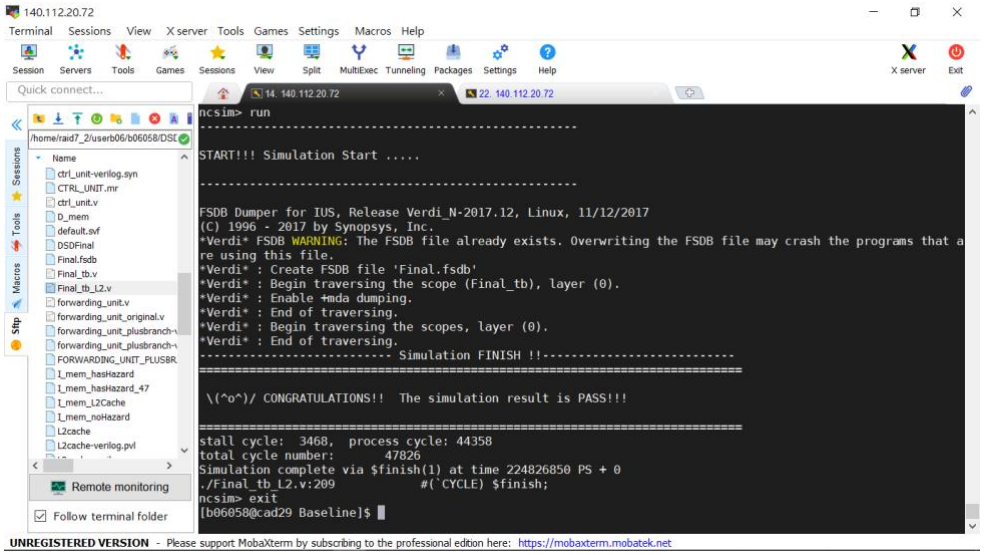
(1) Average memory access time: (ns)

I cache:1.00136*4.7=4.706(ns)

D cache:1.314*4.7=6.176(ns)

(2) Total execution time of given I_mem_L2Cache: (ns)

截圖: sdc 檔用 3.9 合成，final_tb 4.7ns 過



4. MultDiv

(1) Area of MultDiv (Total area of MultDiv minus baseline design, two design clock cycle need to be same): (um2)

=> 22,838.516852 μm^2

(2) Total execution time of given I_mem_MultDiv: (ns)

=> 2140.6 ns

(3) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

=> 2.8 ns