

DSD Final Project Scores (MIPS)

1. Baseline

(1) Area: (um²)

截圖:

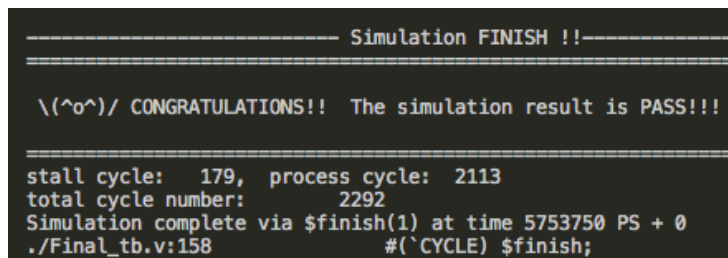


Total cell area:	311107.958699
Total area:	2486719.108540

=> 311107.958699 μm^2

(2) Total Simulation Time of given hasHazard testbench: (ns)

截圖: (nb = 16)



```
----- Simulation FINISH !!-----  
\\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!  
-----  
stall cycle: 179, process cycle: 2113  
total cycle number: 2292  
Simulation complete via $finish(1) at time 5753750 PS + 0  
./Final_tb.v:158 #(`CYCLE) $finish;
```

=> 5753.75 ns

(3) Area*Total Simulation Time: (um² * ns)

=> 1,790,037,417.36 $\mu m^2 \times ns$

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

=> 2.5 ns

2. BrPred

(1) Total execution cycles of given I_mem_BrPred:

截圖: (nb_notBr = 10, nb_interBr = 20, nb_Br = 30)

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Branch Part A is complete.
Branch Part B is complete.
Branch Part C is complete.

===== Simulation FINISH !!=====

\\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

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partA cycle:      90
partB cycle:     141
partC cycle:     114
total cycle number is: 345
Simulation complete via $finish(1) at time 992600 PS + 0
./Final_tb.v:159          #(`CYCLE) $finish;
ncsim> exit
```

=> 345 個 cycle

(2) Total execution cycles of given I_mem_hasHazard:

截圖: (nb = 16)

```
=====

START!!! Simulation Start .....

=====

FSDB Dumper for IUS, Release Verdi_N-2017.12, Linux, 11/12/2017
(C) 1996 - 2017 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file m
*Verdi* : Create FSDB file 'Final.fsdb'
*Verdi* : Begin traversing the scope (Final_tb), layer (0).
*Verdi* : Enable +mda dumping.
*Verdi* : End of traversing.
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.

===== Simulation FINISH !!=====

\\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!!

=====

stall cycle: 173, process cycle: 1824
total cycle number: 1997
Simulation complete via $finish(1) at time 5618200 PS + 0
./Final_tb.v:159          #(`CYCLE) $finish;
ncsim> exit
```

=> 1997 個 cycle

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um²)

=> 14,045.985096 μm^2

3. L2 Cache

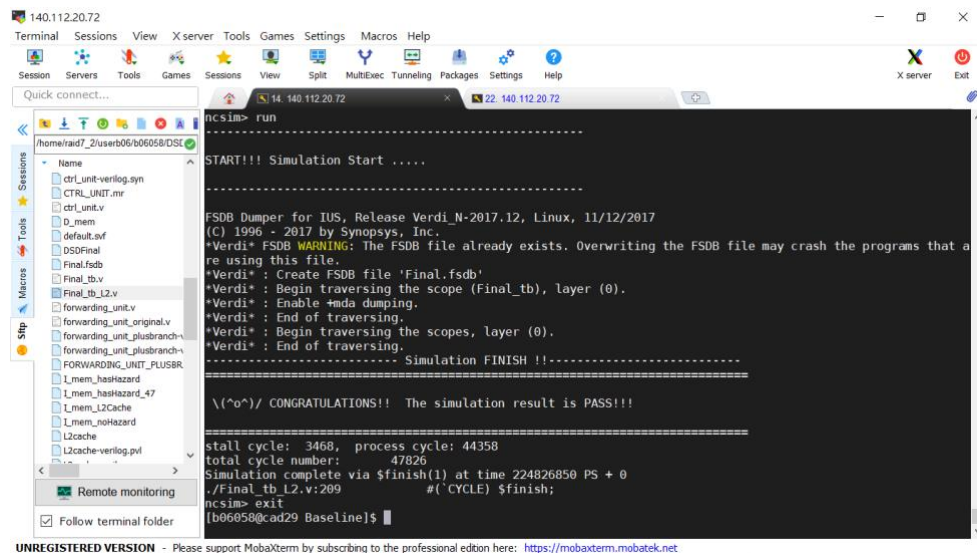
(1) Average memory access time: (ns)

$$\text{I cache: } 1.00136 \times 4.7 = 4.706(\text{ns})$$

$$\text{D cache: } 1.314 \times 4.7 = 6.176(\text{ns})$$

(2) Total execution time of given I_mem_L2Cache: (ns)

截圖: sdc 檔用 3.9 合成，final_tb 4.7ns 過



```
ncsim> run
START!!! Simulation Start .....
FSDB Dumper for IUS, Release Verdi_N-2017.12, Linux, 11/12/2017
(C) 1996 - 2017 by Synopsys, Inc.
*Verdi* FSDB WARNING: The FSDB file already exists. Overwriting the FSDB file may crash the programs that are using this file.
*Verdi* : Create FSDB file 'Final.fsdb'
*Verdi* : Begin traversing the scope (Final_tb), layer (0).
*Verdi* : Enable #mda dumping.
*Verdi* : End of traversing.
*Verdi* : Begin traversing the scopes, layer (0).
*Verdi* : End of traversing.
..... Simulation FINISH !!.....
\\(^o^)/ CONGRATULATIONS!! The simulation result is PASS!!
=====
stall cycle: 3468, process cycle: 44358
total cycle number: 47826
Simulation complete via $finish(1) at time 224826850 PS + 0
./Final_tb_L2.v:209 #( 'CYCLE) $finish;
ncsim> exit
[b06058@cad29 Baseline]$
```

4. MultDiv

(1) Area of MultDiv (Total area of MultDiv minus baseline design, two design clock cycle need to be same): (um²)

$$\Rightarrow 22,838.516852 \mu\text{m}^2$$

(2) Total execution time of given I_mem_MultDiv: (ns)

$$\Rightarrow 2140.6 \text{ ns}$$

(3) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

$$\Rightarrow 2.8 \text{ ns}$$