Answer No 1

x XOR (y OR z) = (x XOR y) OR (x XOR z)

is not valid for all x, y, z.

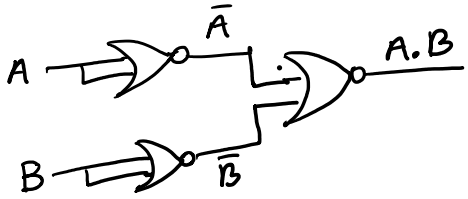
Here is the truth table.

x	y	z	y OR z	x XOR (y OR z)	x XOR y	x XOR z	(x XOR y) OR (x XOR z)
0	0	0	0	0	0	0	0
0	0	1	1	1	0	1	1
0	1	0	1	1	1	0	1
0	1	1	1	1	1	1	1
1	0	0	0	1	1	1	1
1	0	1	1	0	1	0	1
1	1	0	1	0	0	1	1
1	1	1	1	0	0	0	0

We can see that, when x = 1, y = 0, z = 1 and x = 1, y = 1, z = 0 both equations are giving different output. So, Equation is not valid.

Answer No 2

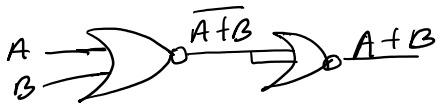
a) AND gate



b) Truth table

A	B	A NOR A	B NOR B	(A NOR A) NOR (B NOR B)	A AND B
0	0	1	1	0	0
0	1	1	0	0	0
1	0	0	1	0	0
1	1	0	0	1	1

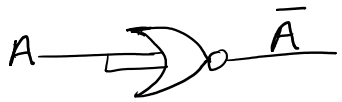
c) Or gate



d) Truth table

A	B	A NOR B	(A NOR B) NOR (A NOR B)	A OR B
0	0	1	0	0
0	1	0	1	1
1	0	0	1	1
1	1	0	1	1

e) Not gate



f) Truth table

A	A NOR A	NOT A
0	1	1
1	0	0

Answer no 3.

The next state will be as follows:

B0 = 0

B1 = 0

B2 = 0

B3 = 0

In a 4-bit synchronous counter, the next state is determined by the current state and the clock signal. In binary counting, since the current state is 111, when incrementing from 1111, we carry over to the next significant bit. Therefore, the next state after 1111 (decimal 15) is 0000 (decimal 0), completing one full cycle of counting.

Answer No 4

a) Truth table for V

A	B	C	V
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

b) Express V as a Sum of Products:
V= A'BC+ AB'C+ABC

c) Simplify V
V= A'BC+ AB'C+ABC
V= A'BC + AB'C+ ABC + ABC (Idempotent law: A+A =A)
V= A'BC + ABC + AB'C+ ABC
V= BC(A+A') + AC(B+B')
V= BC (1) + AC (1) (Inverse law: A+A' =1, B+B'=1)
V= AC+BC

d) Simplified circuit for V.