A Novel Fault Detection Circuit for Short-circuit Faults of IGBT

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***Abstract* — This paper proposed a novel fault detection circuit comparing the gate voltage of IGBT. The proposed scheme is operated to protect IGBT under short-circuit faults such as hard switch-fault (HSF). The proposed circuit consists of two parts. One is the difference generator which generates a difference between a gate voltage and an input voltage. The other is the short-circuit fault detector using a charged voltage of capacitor for short-circuit fault detection.**

The feasibility of the proposed short-circuit detecting scheme is verified by simulation results.

I. INTRODUCTION

As power electronics technology has been improved with a fast development of power semiconductor devices, their applications have been broadly founded in various electrical areas. Among several power semiconductor devices, an Insulated Gate Bipolar Transistor (IGBT) is a power switch widely found in many power electronics applications, due to its several advantages. Comparing to other semiconductor switches, the IGBT is known as a common selection in a high voltage/high current applications [1].

However, one critical issue of the IGBT is its weak ruggedness of the short-circuit condition. IGBT's fault is categorized into two cases: Fault Under Load (FUL) and Hard Switching Fault (HSF). In a single leg of an inverter, for example, FUL is the case when the IGBT located at a top side causes a short-circuit condition. Reversely, the short-circuit condition caused by the bottom IGBT is defined to HSF. In order to protect IGBTs, most gate drivers are designed to generate turn-off signals. However, in spite of turn-off signals by gate drivers, IGBTs experience an excessive voltage spike because of trapped energy in the circuit stray inductance. As a result, some of them may blow-up and the protection fails. In order to improve the reliability by the protection, it is important to reduce trapped energy by a fast gate turn-off signal as possible. Therefore, the protection circuit of the IGBT needs fast fault detection within a very fast time, i.e. few micro-second, and optimal fault remedial action.

Various approaches have been proposed and studied to protect IGBT based on the measurement of the collector voltage, the collector current, the gate voltage, or the induced voltage across the emitter stray inductance [4-9].The de-saturation technique [4-6], which is a common method used to identify a fault situation using a sensing diode detects the collector voltage under short-circuit faults. This method has disadvantages that require blanking time caused delayed fault detection and a high voltage diode. The current mirror technique [7-9] using emitter resistor, sense IGBT or CT can detect both over current and short-circuit faults. These methods have been introduced widely and used in the field of IGBT inverter. However, it is difficult to be integrated as a gate drive IC because of the addition of high power resistor and high voltage diode. These protection circuits have higher cost, larger configuration, and lower performance at transient. The technique using the induced voltage across the stray inductance between the Kelvin emitter and the power emitter[10] does not have any noise issue or no blanking time is required. However, it is difficult to calculate the correct stray inductance and perform the protection circuit.

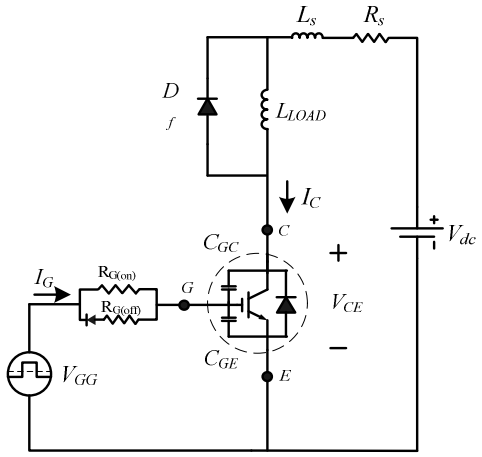

Fig. 1. Diode-clamped inductive load(DCIL).

To overcome these problems, this paper proposes a novel fault detection circuit for short-circuit faults of IGBT. The proposed fault detection circuit is achieved based on the measurement of the gate voltage which is differently

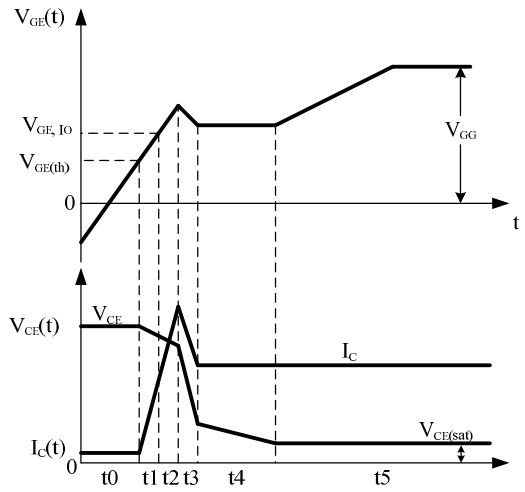

Fig. 2. Turn-on switching characteristic of IGBT under normal condition.

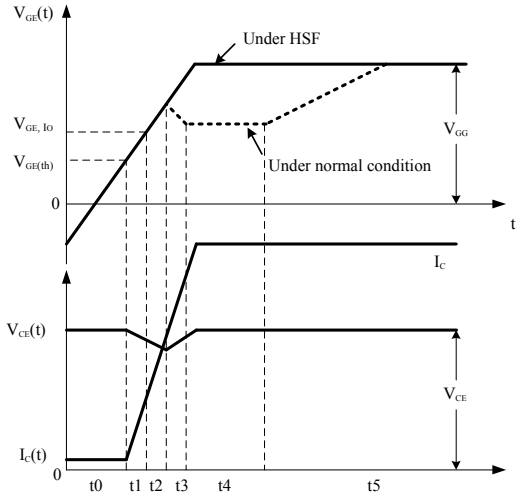

Fig. 3. Turn-on switching characteristic of IGBT under HSF

presented according to short-circuit faults. The proposed circuit consists of two parts. One is the difference generator, which generates a difference between a gate voltage and an input gate voltage. The other is the short-circuit fault detector using integrator and comparator by op-amps. The proposed fault detection circuit doesn't require the connection between main power circuit and detection circuit.

This paper is organized as follows. Section II introduces the general turn-on characteristics of IGBT. In Section III, a proposed scheme for detecting short-circuit faults using both difference generator and short-circuit fault detector is introduced. The feasibility of the proposed fault detection circuit is verified by simulation results in Section IV. Finally, in Section V conclusion is drawn.

II. Turn-on Switching Characteristics of IGBT

A. Turn-on Switching characteristic under Normal Condition

As shown in Fig. 1, the diode clamped inductive load (DCIL) circuit is configured to examine switching transient state characteristic of IGBT. L_S and R_S represent stray inductance and resistance of circuit, respectively. The stray inductance L_S and resistance R_S are considered to reflect the effect when the short-circuit fault occurs. R_S is used to model the slight fall in voltage across the device when it is turned on. For DCIL, the device is turned on with full bus voltage V_{dc} across it. V_{dc} is normally chosen to be 60% of the device voltage rating.

Generally, the turn-on switching characteristic of IGBT under normal condition is shown in Fig. 2. These waveforms can be applied to both inverter and chopper circuit using inductive load and reflects the effects of diode recovery and stray inductance.

Turn-on transient state of IGBT under normal condition is divided into five regions (t_0~t_5).

t_0 region : The gate current I_G charges parasitic input capacitance C_{GE} and C_{GC}, and then gate voltage V_{GE} rises to$V_{GE(th)}$. Waveform of increasing V_{GE} if shown to be linear, a practical V_{GE} exponentially increases with time constant of $R_G(C_{GE}+C_{GC})$ and is given by

$$V_{GE}(t) = V_{GA}\left(1-e^{[t/R_G(C_{GE}+C_{GV})]}\right) \tag{1}$$

In this region, V_{CE} which is between collector and emitter maintains to input voltage V_{GG} because collector current I_C does no flow through IGBT.

t_1 region : V_{GE} increases exponentially passing $V_{GE(th)}$ and as V_{GE} continues to increase, I_C begins to increase and reaches full load current I_0. In t_1 and t_2 region, V_{CE} decreases due to the induced voltage which is the value related with stray inductance L_S and di_C/dt, while I_C rises continuously due to a reverse recovery current of freewheeling diode.

t_2 and t_3 region : A reverse recovery current of freewheeling diode starts to show. This current starts to decrease at beginning t_3 region. At this time, voltage across the freewheeling diode increases, while V_{CE} fall. When C_{GC} has small value and V_{dc} is high, V_{CE} comes to be decreased rapidly. In t_2 region, C_{GC} absorbs and discharges the current from the gate drive and the discharge current from C_{GE}. At the end of t_3 region, reverse recovery time of the diode comes to be closed.

t_4 region : I_G is charging C_{GC}, and V_{GE} maintains $V_{GE(I_0)}$, and I_C maintains full load current I_0, while V_{CE} falls at a rate $(V_{CG}+-V_{GE(I_0)})/(R_GC_{GC})$.

t_5 region : V_{GE} increases again until V_{GG} with time constant of $R_G(C_{GE}+C_{GC,miller})$. $C_{GC,\text{miller}}$ is the C_{GC} that rose from low V_{CE} due to the miller effect. In this region, V_{CE} slowly diminishes to the collector-to-emitter on-state voltage and becomes completely saturated.

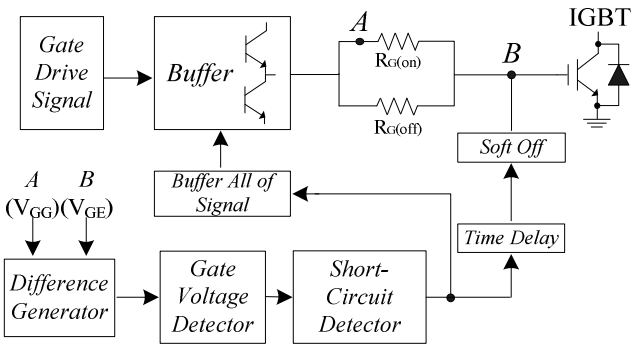

Fig.4. Block diagram of the proposed scheme.

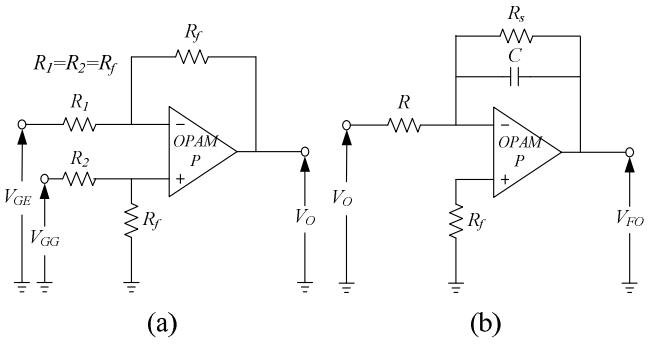

Fig. 5. Two parts of the proposed fault detection circuit.

B. Turn-on Switching Characteristic under Short-Circuit Fault

As shown in Fig. 2, it can easily be known that V_{GE} should be constant due to the miller effect in t3 and t4 regions as explained at chapter above. Short-circuit faults of IGBT can be divided into two different types which are the HSF and FUL according to fault conditions. Fig. 3 shows gate voltage waveform under HSF. As shown in Fig. 3, constant V_{GE} at any turn-on regions cannot find the miller effect under the HSF condition in t3 and t4 regions because V_{CE} should not be changed under HSF condition. V_{GE} rises differently in t3 and t4 regions, compared with the normal condition. V_{GE} with the slope of initial charged C_{GE} rises to V_{GG}. Consequently, the HSF fault of IGBT is detected by comparing V_{GG} and V_{GE} when the short-circuit faults occur.

III. Proposed Fault Detection Circuit

The proposed fault detection circuit consists of two parts. One is the difference generator for detecting difference between V_{GG} and V_{GE}. The other is the short-circuit fault detector that integrates the generated difference between V_{GG} and V_{GE}. Two parts have general differential input subtractor and integrator using an op-amp. If the short-circuit fault detector identify HSF, the gate voltage is clamped to reduce short-circuit fault current. And then, the gate voltage is slowly turned off to reduce the over voltage of V_{CE} due to the falling rate I_C and stray inductance. Fig. 4 shows the block diagram of the proposed fault detection circuit with soft turn-off configuration.

A. Difference Generator

Fig. 5(a) shows the difference generator which consists of differential input subtractor using an op-amp and resistors. In order to detect short-circuit fault, the difference generator receives two input voltage which are output voltage V_{GG} of buffer and the gate voltage V_{GE}. The output voltage V_0 of difference generator for difference between V_{GG} and V_{GE} can be expressed as

$$V_0 = \frac{R_f}{R_1}(V_{GG} - V_{GE}) \tag{2}$$

The output voltage V_0 distinguishes clearly because the gate voltage waveform differently appears in short-circuit fault and normal operation.

B. Short-Circuit Fault Detector

Fig. 5(b) shows the short-circuit fault detector which consists of integrator using an op-amp, resistors and a capacitor. In order to identify V_0 of difference generator, the short-circuit fault detector has integral circuit which detect difference between V_{GG} and V_{GE}. As shown in Fig. 5(b), the output voltage V_{F0} of short-circuit fault detector with general integrator integrates difference between V_{GG} and V_0. V_{F0} is given by

$$V_{F0} = -\frac{1}{CR}\int_0^t V_0\,dt \tag{3}$$

When the short-circuit fault occurs, the voltage time across difference generator has a short. Thus, the output voltage V_{F0} of the integrator becomes lower than that of normal condition. If V_{F0} is lower than reference voltage, this phenomena distinguishes the short-circuit fault operation compared with normal condition.

C. Overall structure of the proposed circuit

The overall structure of the proposed circuit for short-circuit faults of IGBT is shown in Fig. 6. The input voltage of *OP3* which is equal to output voltage through difference generator and short-circuit fault detector is compared with the fault reference voltage. Since the integration value always is equal in initial transient state, the proposed schematic circuit supplements additional circuits, which measure rise of V_{GE} to V_{GG}. As shown in Fig. 6, *OP4* is performed for this acquirement.

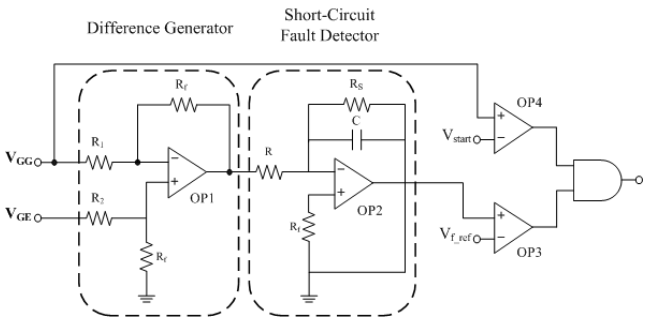

Fig.6. Proposed schematic circuit

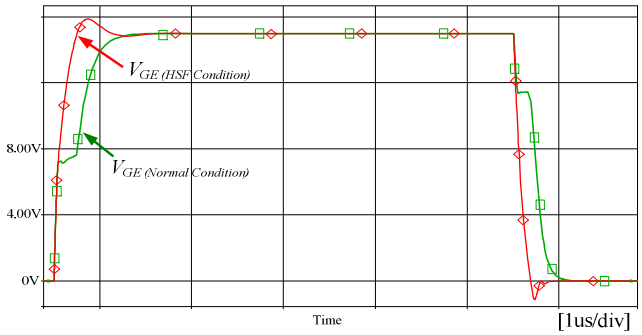

Fig. 8. Gate voltage waveforms at turn-on transient under normal and HSF condition.

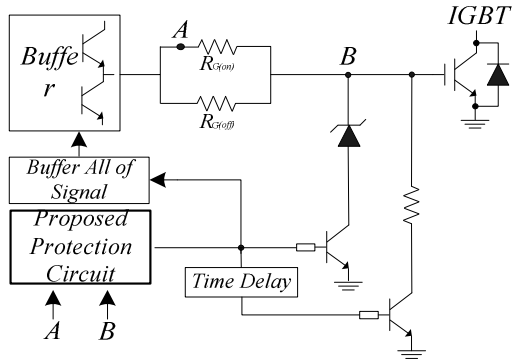

Fig. 7. Gate drive with the proposed protection circuit.

The proposed IGBT gate drive with detection circuit for short-circuit faults is shown in Fig. 7. When any fault situation are occurred under the operation of IGBT, it is necessary to detect it, and then gate voltage clamp is obligated to reduce a fault current of IGBT. And more, IGBT has to be softly turned off to reduce surge voltage due to the effect of stray inductance and di_c/dt. The soft off block is introduced in Fig. 4. When the output state of proposed protection circuit is high, gate voltage is clamped by zener diode. At the same time, both switches of a buffer are turned off. And then, after a short time delay, gate voltage is softly turned off by a high resistor.

VI. Simulation Results

In order to verify a novel short-circuit detection circuit, simulations are performed by using ORCAD simulator using the DCIL circuit as shown in Fig. 1. Table I shows the parameters used for simulation. Fig. 8 shows the gate voltage waveforms at turn-on transient under normal and HSF condition. There is no miller effect region under HSF condition in Fig. 8. Fig. 9 shows V_{GE}, V_{GG}, V_0, V_{F0}, and V_{ref} waveforms with proposed protection circuit under normal and HSF condition. As shown in Fig. 9, the output voltage V_0 for difference between V_{GG} and V_{GE} has differently the values.

TABLE I.
PARAMETERS FOR SIMULATION

Parameters	Symbols	Values
DC-link Voltage	V_{dc}	300 [V]
Load Inductance	L_{LOAD}	2 [mH]
Stray Inductancet	L_s	50 [nH]
Stray Resistance	R_s	150 [mΩ]
Gate Voltage	V_{GG}	15 [V]
Gate Resistor	R_G	100 [Ω]

The output voltage V_{FO} across short-circuit fault detector under normal operation is relatively lower than V_{F0} under HSF condition. If the V_{F0} is a lower value than V_{ref} to identify short-circuit fault under HSF condition, the short-circuit fault detector should decide on the short-circuit fault, and then V_{fault_signal} is generated. After short-circuit fault detection, the gate voltage V_{GE} by gate voltage clamp decreases and then is softly turn off to protect IGBT as shown in Fig. 9(b). Fig. 10 show collector current I_C and V_{CE} between collector and emitter when the short-circuit fault under HSF condition which is with protection circuit and without it. As shown in Fig 10, it can be known that short-circuit peak current and overshoot voltage of IGBT happen differently at the turn-off time. If there is with protection circuit under HSF condition, I_C becomes quickly drop due to V_{GE} decrease by voltage clamp after short-circuit fault detection. Therefore, when IGBT turns off, I_C and over voltage of V_{CE} with protection circuit is much lower than without it. From the detailed investigation of the simulation results, the feasibility is fully verified.

VII. Conclusion

This paper represents a novel short-circuit detecting scheme comparing the gate voltage of IGBT under HSF. The proposed protection circuit consists of both difference generator, which generates a difference between a gate voltage and an input voltage, and the short-circuit fault detector which integrate difference between input voltage

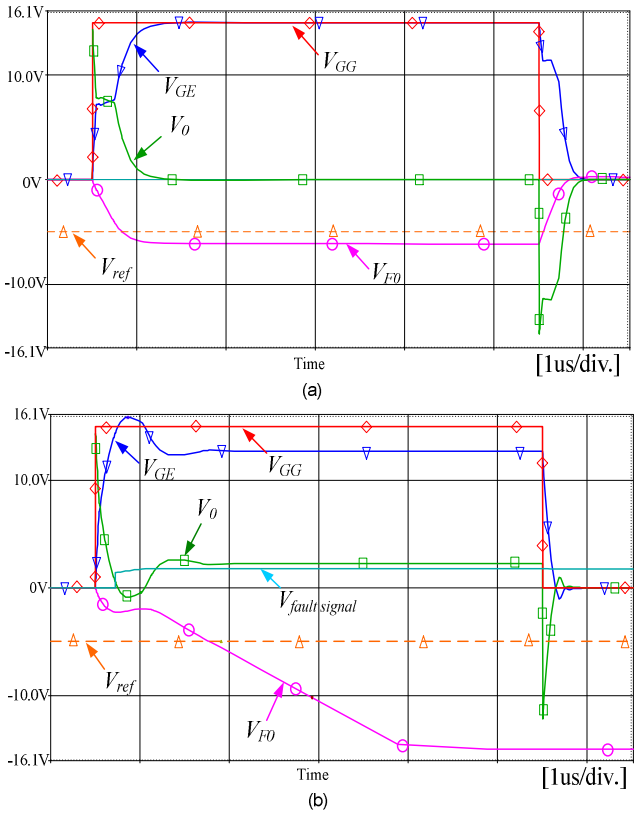

Fig. 9. Operating waveforms with protection circuit. (a) normal condition. (b) HSF condition.

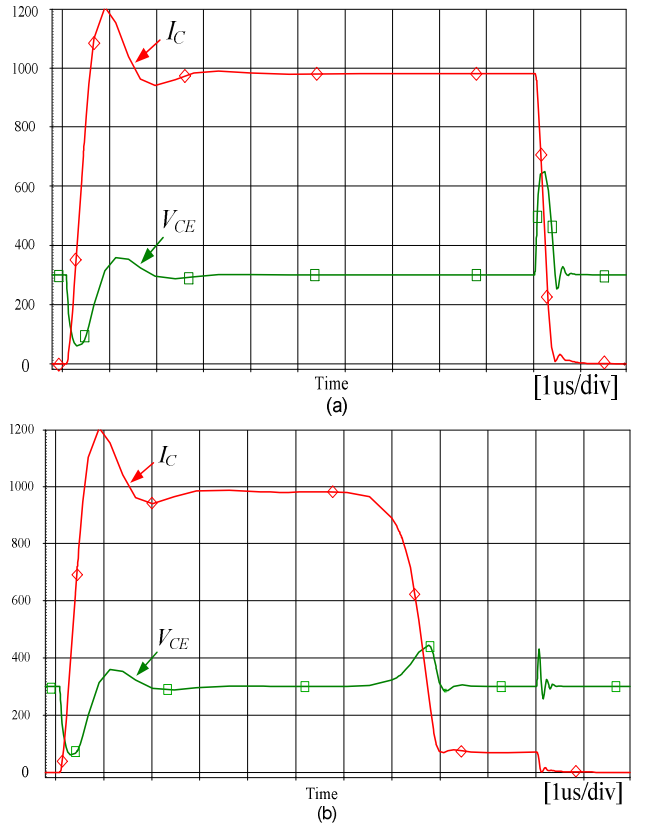

Fig. 10. Operating waveforms under HSF. (a) without protection circuit. (b) with protection circuit.

and output voltage of difference generator.

The proposed fault detection circuit can be conveniently integrated in one gate drive IC or HVIC due to the configuration of logic and low voltage components. The feasibility of the proposed protection circuit is verified by simulation results.

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