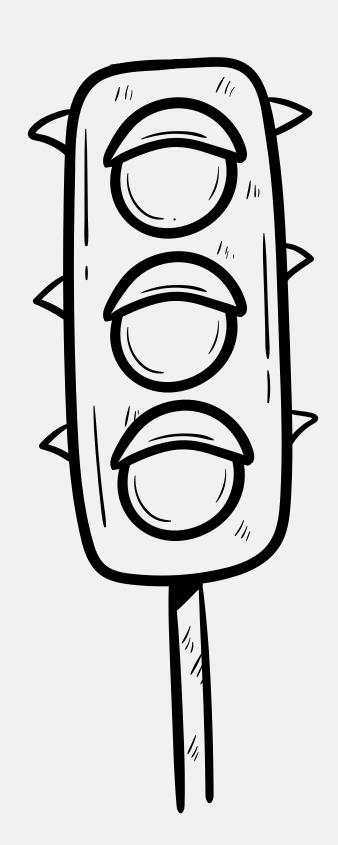
Traffic Light

Logic Design for a T-Junction Traffic light system.



The Problem

Traffic jams



Accidents



Long commute time



Goals

01

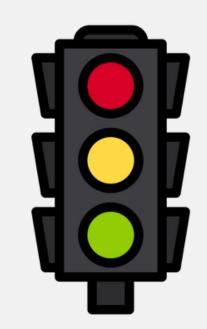
interrupts the heavy traffic at intersections to allow other vehicles or pedestrians to cross it.

02

help in reducing the severity and frequency of various types of accidents or crashes. 03

help in providing a continuous movement of traffic at a certain speed in a given route or way.





Before Trafic light With Traffic light

Common traffic jams

Continuous flow of traffic

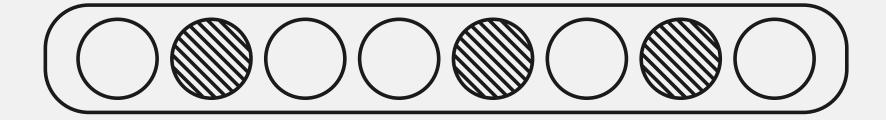
Very high risk of accidents

Very little accidents

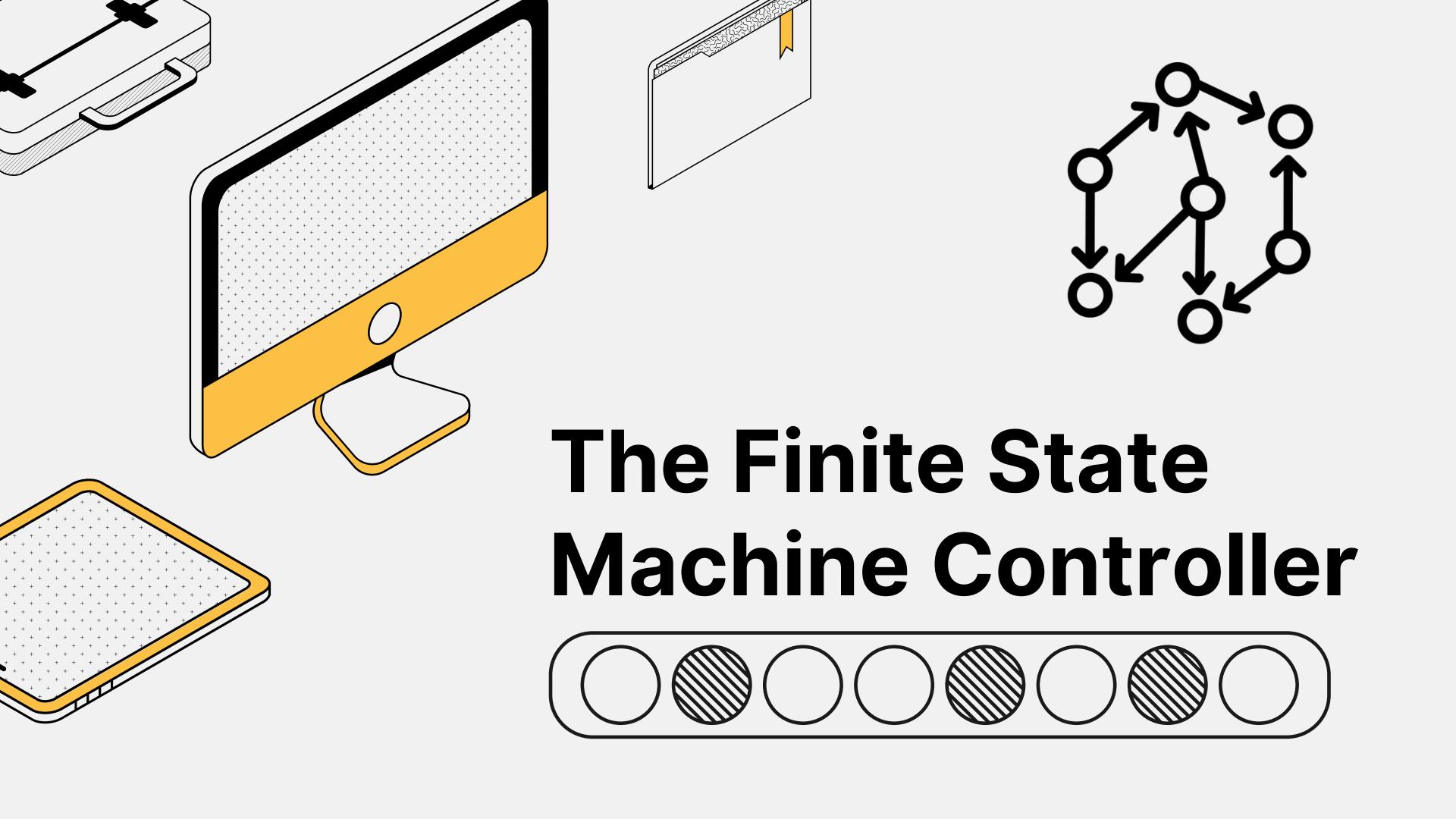
Longer commute times

Shorter commute times

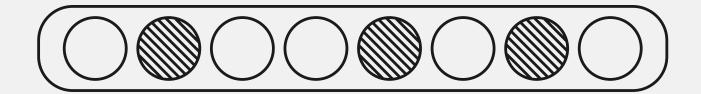
Design model

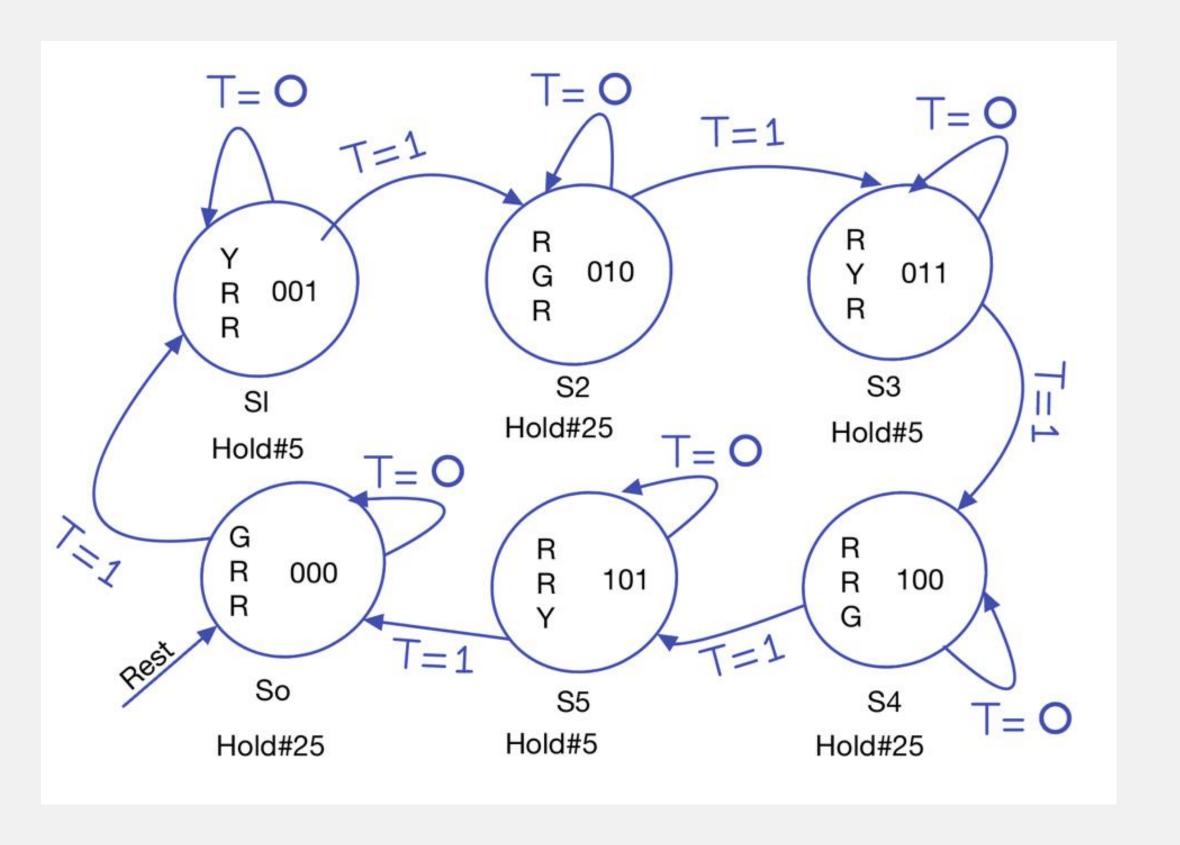






State Table Diagram



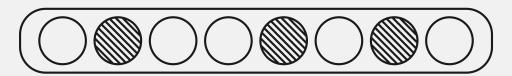


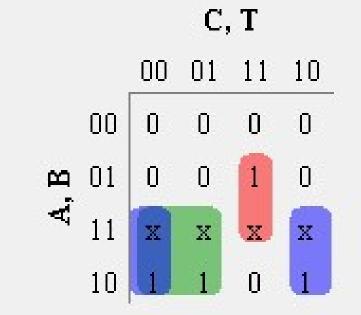
StateTable

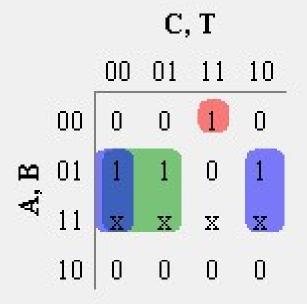
State	encoding	P1	P2	Р3	Delay
S0	000	Green	Red	Red	25 sec
S1	001	Yellow	Red	Red	5 sec
S2	010	Red	Green	Red	25 sec
S3	011	Red	Yellow	Red	5 sec
S4	100	Red	Red	Green	25 sec
S5	101	Red	Red	Yellow	5 sec

	present state	•	Input	Next State				
а	b	С	Т	a^	b^	c^		
0	0	0	0	0	0	0		
0	0	0	1	0	0	1		
0	0	1	0	0	0	1		
0	0	1	1	0	1	0		
0	1	0	0	0	1	0		
0	1	0	1	0	1	1		
0	1	1	0	0	1	1		
0	1	1	1	1	0	0		
1	0	0	0	1	0	0		
1	0	0	1	1	0	1		
1	0	1	0	1	0	1		
1	0	1	1	0	0	0		

Next State

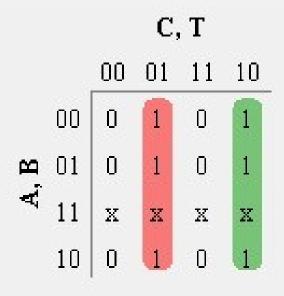






$$a^* = BCT + A\overline{C} + A\overline{T}$$

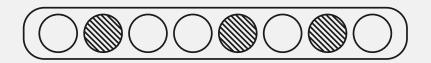
$$b^{-} = \overline{A}\overline{B}CT + B\overline{C} + B\overline{T}$$

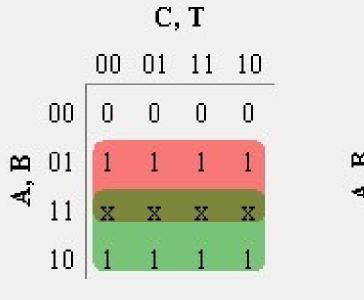


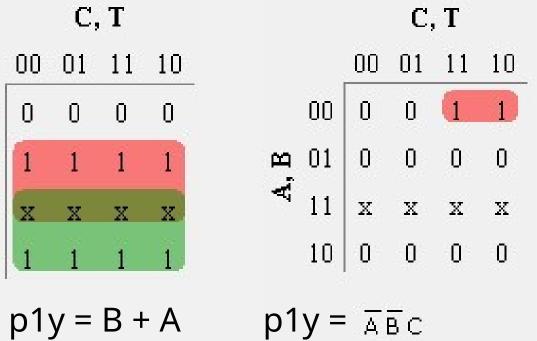
$$C^{=} \overline{C}T + C\overline{T}$$

	Inp	out	Output				
а	b	С	Т	p1r	p1y	p1g	
0	0	0	0	0	0	1	
0	0	0	1	0	0	1	
0	0	1	0	0	1	0	
0	0	1	1	0	1	0	
0	1	0	0	1	0	0	
0	1	0	1	1	0	0	
0	1	1	0	1	0	0	
0	1	1	1	1	0	0	
1	0	0	0	1	0	0	
1	0	0	1	1	0	0	
1	0	1	0	1	0	0	
1	0	1	1	1	0	0	

signal 1



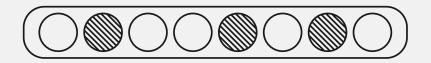


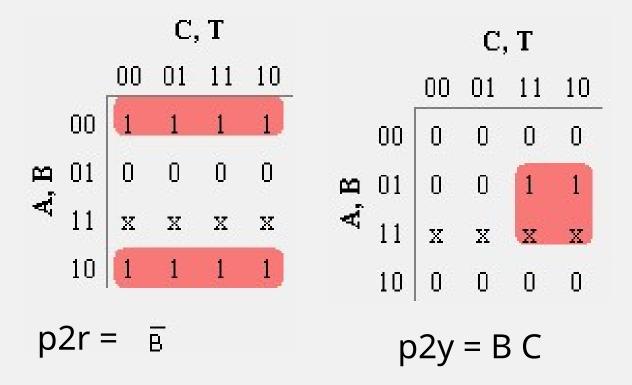


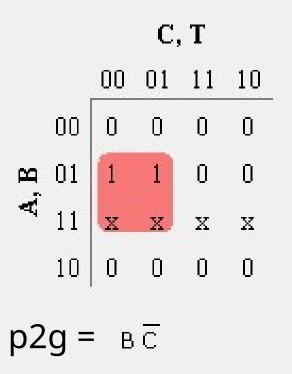
$$p1g = \overline{A}\overline{B}\overline{C}$$

	Inp	out	Output					
а	b	С	Т	p1r	p1y	p1g		
0	0	0	0	1	0	0		
0	0	0	1	1	0	0		
0	0	1	0	1	0	0		
0	0	1	1	1	0	0		
0	1	0	0	0	0	1		
0	1	0	1	0	0	1		
0	1	1	0	0	1	0		
0	1	1	1	0	1	0		
1	0	0	0	1	0	0		
1	0	0	1	1	0	0		
1	0	1	0	1	0	0		
1	0	1	1	1	0	0		

signal 2

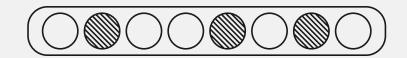


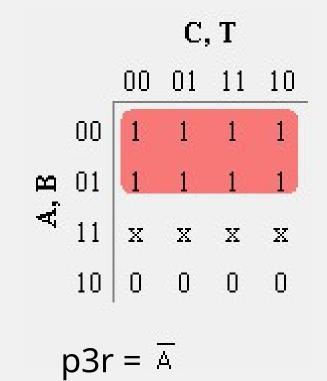


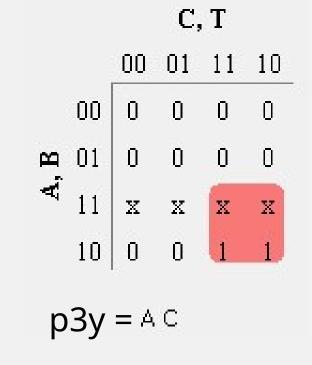


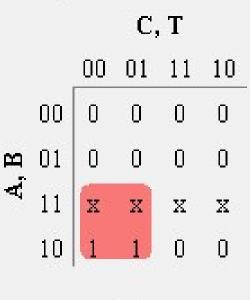
	Inp	out	Output				
а	b	с Т		p1r	p1y	p1g	
0	0	0	0	1	0	0	
0	0	0	1	1	0	0	
0	0	1	0	1	0	0	
0	0	1	1	1	0	0	
0	1	0	0	1	0	0	
0	1	0	1	1	0	0	
0	1	1	0	1	0	0	
0	1	1	1	1	0	0	
1	0	0	0	0	0	1	
1	0	0	1	0	0	1	
1	0	1	0	0	1	0	
1	0	1	1	0	1	0	

signal 3





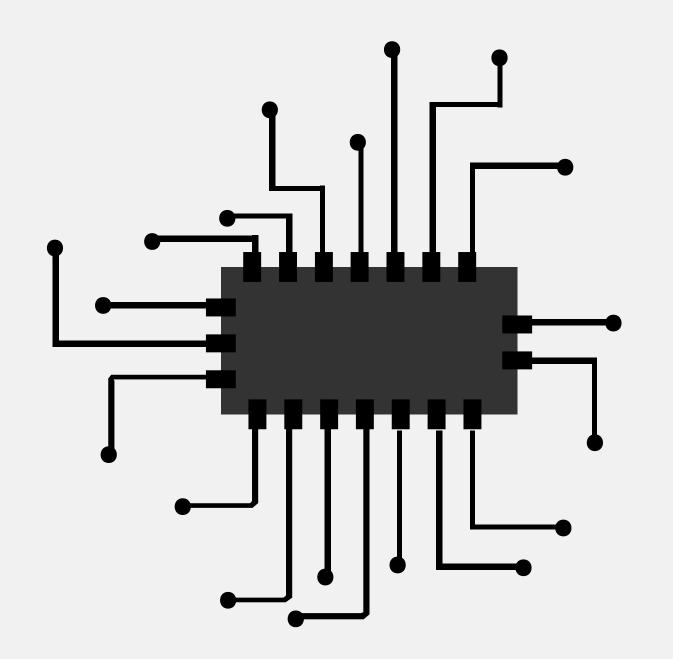




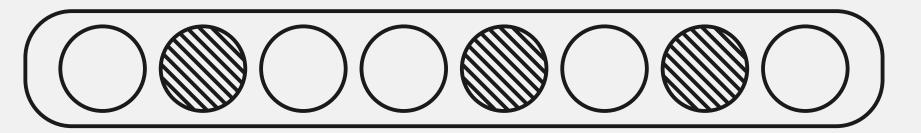
Truth Table



pres	sent st	ate	Input	Nε	ext Sta	ite		output				fl	flip flop					
а	b	С	Т	a^	b^	С^	p1r	р1у	p1g	p2r	p2y	p2g	p3r	рЗу	p3g	d1	d2	d3
0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1
0	0	0	1	0	0	1	0	0	1	1	0	0	1	0	0	0	0	1
0	0	1	0	0	0	1	0	1	0	1	0	0	1	0	0	0	1	0
0	0	1	1	0	1	0	0	1	0	1	0	0	1	0	0	0	1	0
0	1	0	0	0	1	0	1	0	0	0	0	1	1	0	0	0	1	1
0	1	0	1	0	1	1	1	0	0	0	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1	0	1	0	0	1	0	0
0	1	1	1	1	0	0	1	0	0	0	1	0	1	0	0	1	0	0
1	0	0	0	1	0	0	1	0	0	1	0	0	0	0	1	1	0	1
1	0	0	1	1	0	1	1	0	0	1	0	0	0	0	1	1	0	1
1	0	1	0	1	0	1	1	0	0	1	0	0	0	1	0	0	0	0
1	0	1	1	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0

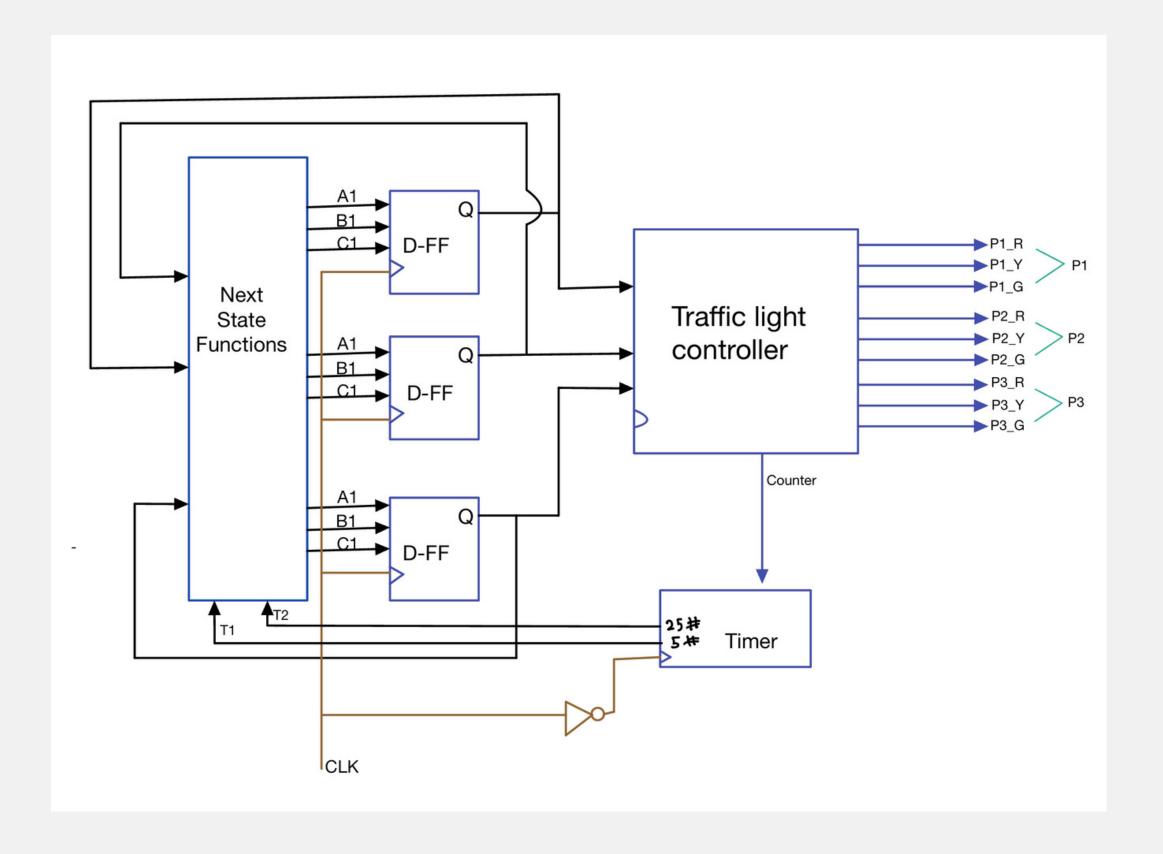


Circuit & data bath



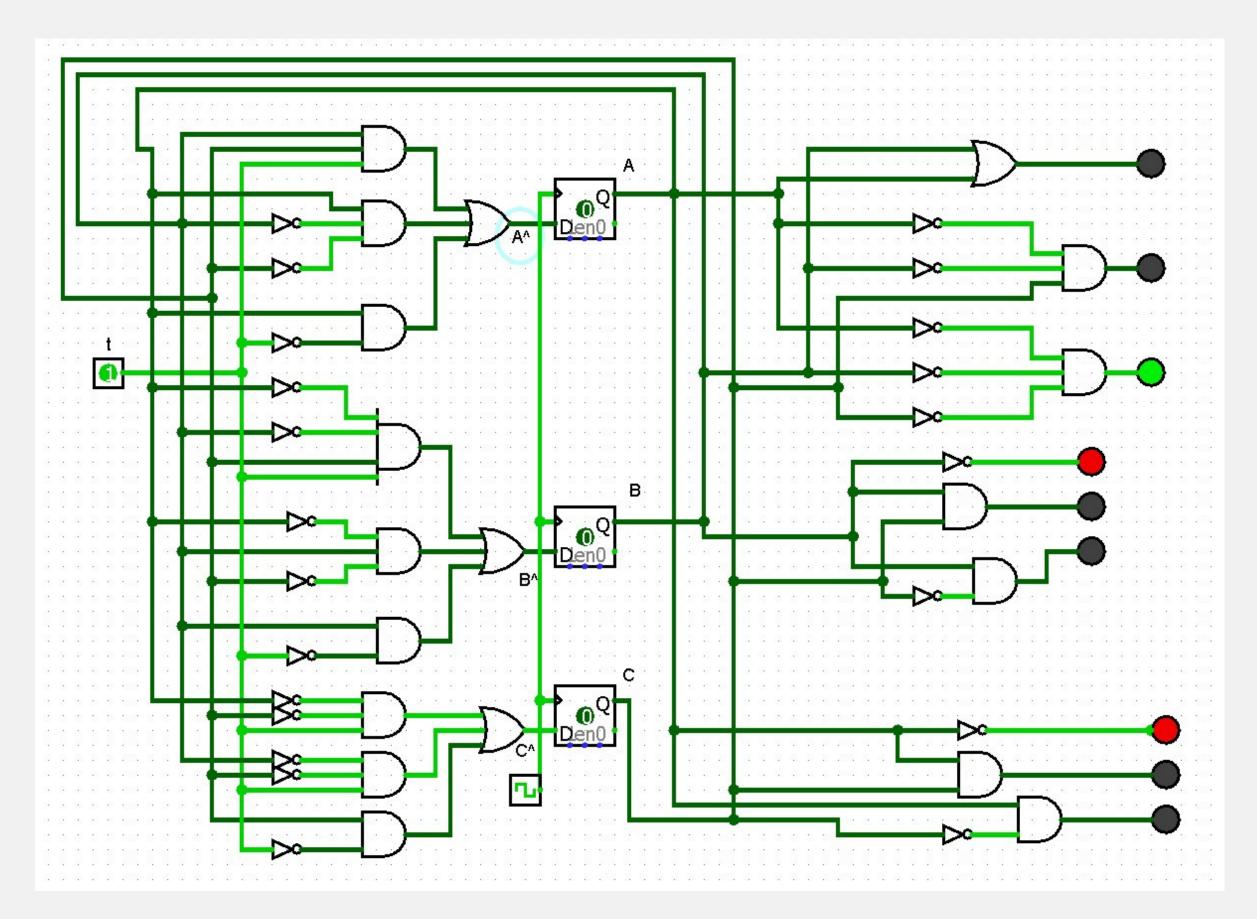
Data Path





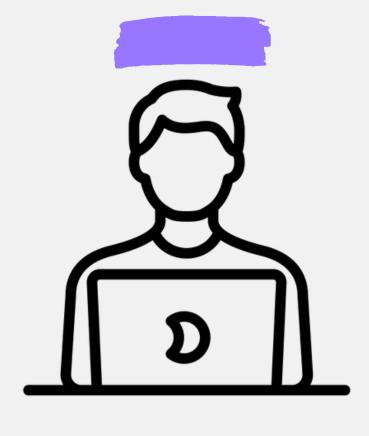
Logic Design





Meet the Group







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THANK YOU!

Do you have any questions for us?