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1   -- NAME: Owen Bailey
2   -- COURSE AND SECTION: CE 1901 031
3   -- FILE: ORBFA.vhd
4   -- DESCRIPTION: Implements a full adder using a with-select statement
5
6   -- include IEEE standard logic signal library
7   library ieee;
8   use ieee.std_logic_1164.all;
9
10  -- describe full adder symbol
11  entity ORBFA is
12     port(
13        ABCIN: in std_logic_vector(2 downto 0); -- input bits in vector form
14        S: out std_logic; -- sum
15        COUT: out std_logic -- carry out
16     );
17  end entity ORBFA;
18
19  -- describe signal path using with/select mux
20  architecture MULTIPLEXER of ORBFA is
21     begin
22        -- sum bit: low for everything except when only one bit is active or all bits are
    active
23        with ABCIN select
24           S <=  '1' when B"001",
25                 '1' when B"010",
26                 '1' when B"100",
27                 '1' when B"111",
28                 '0' when others;
29
30        -- carry bit: high for everything except when all bits are low or only one bit is
    active
31        with ABCIN select
32           COUT <= '0' when B"000",
33                   '0' when B"001",
34                   '0' when B"010",
35                   '0' when B"100",
36                   '1' when others;
37
38     end architecture MULTIPLEXER;
39
```