Constraint Exercise 1-5

Write the SystemVerilog code for the following items:

1) Create a class `Exercise1` containing two variables, 8-bit `data` and 4-bit `address`. Create a constraint block that keeps `address` to 3 or 4.

2) In an `initial` block, construct an `Exercise1` object and randomize it. Check the status from randomization.

3) Modify the solution for `Exercise1` to create a new class `Exercise2` so that:

1. `data` is always equal to 5
2. Probability of `address = 4'd0` is 10%
3. Probability of `address` being between [1:14] is 80%
4. Probability of `address = 4'd15` is 10%

4) Demonstrate its usage by generating 100 new `data` and `address` values and check for error.

5) Create 3 “static” counters c1-c3 within the class and use post_randomize to update their value:

c1 counts number of instances where 0 was generated

c2 counts ……1-14 were generated

c3 counts ……15 was generated

Use a “final” block to print the value of the counters.

Lab Exercise part 1:

- Solve Exercise 1-5 in class
- EVERYONE must submit their codes/reports to Moodle by the end of the lecture today (11:00am).
- Even if you are working in groups, please submit the same report, and clearly mention the team members.
- What to submit: the full SystemVerilog code.