

Exercise 3: Code Coverage

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Course: Verification Design

1. In arbitr_tb.v and arbiter.v what is the code coverage in the code?

Score: almost 94%

Line: 100%

Toggle: almost 91%

We knew the score by applying this commands in the server terminal:

- I. Open arbitr_tb.v and run it with these coverage options then debug it.
 - o **vcs -cm_tgl mda -lca -cm line+cond+fsm+tgl+path -debug_all arbiter_tb.v**

```
if [ -x ../simv ]; then chmod -x ../simv; fi
g++ -o ../simv -Wl,-rpath-link=:/ -Wl,-rpath=$ORIGIN/simv.daidir/ -Wl,-rpath=../simv.daidir/ -Wl,-rpath=$ORIGIN/simv.daidir/scsim.db.dir -m32 -m32 -rdynamic 6
4054_archive_1.so _csrc0.so _csrc0.so _rmapats_mop.o _rmapats.o _rmar.o _rmar.nd.o _rmar_llvm_0_1.o _rmar_llvm_0_0.o /Disk2/eda/synopsys/2017-18/RHELx86/
VCSMX_2017.12-1/linux/lib/libzerofree.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libvcsim.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017
.12-1/linux/lib/liberrorinf.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libnpsmalloc.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib
/libvcs.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libvcsnew.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libvcsprofile.so /Di
sk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libreader_common.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libBA.a /Disk2/eda/synopsys/20
17-18/RHELx86/VCSMX_2017.12-1/linux/lib/libcunlative.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/vcs_tls.o -Wl,-whole-archive /Disk2/eda/synopsys/2
017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libvcsucl.so -Wl,-no-whole-archive /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/vcs_save_restore_new.o
/Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/cvtype-stubs_32.a -ldl -lc -lm -lpthread -ldl
../simv up to date
CPU time: .203 seconds to compile + .026 seconds to elab + .169 seconds to link
[12010507@vls112 vcs_tutorial]$ ./simv -cm line+cond+fsm+tgl
Chronologic VCS simulator copyright 1991-2017
Contains Synopsys proprietary information.
Compiler version N-2017.12-1; Runtime version N-2017.12-1; May 13 10:58 2024

VCS Coverage Metrics Release N-2017.12-1 Copyright (c) 1991-2017 by Synopsys Inc.
sfinish called from file "arbiter_tb.v", line 67.
sfinish at simulation time 59

-----
VCS Coverage Metrics: during simulation line, cond, FSM, tgl was monitored
-----

Coverage status: End of All Coverages ...

VCS Simulation Report
Time: 59
CPU Time: 0.440 seconds; Data structure size: 0.0Mb
Mon May 13 10:58:28 2024
[12010507@vls112 vcs_tutorial]$ dve -cov &
[1] 64746
[12010507@vls112 vcs_tutorial]$ gedit arbitr_tb.v &
[2] 65035
[12010507@vls112 vcs_tutorial]$
** (gedit:65035): WARNING **: Set document metadata failed: Setting attribute me
tadata:gedit-spell-language not supported

** (gedit:65035): WARNING **: Set document metadata failed: Setting attribute me
tadata:gedit-encoding not supported

** (gedit:65035): WARNING **: Set document metadata failed: Setting attribute me
tadata:gedit-spell-language not supported

** (gedit:65035): WARNING **: Set document metadata failed: Setting attribute me
tadata:gedit-encoding not supported

** (gedit:65035): WARNING **: Set document metadata failed: Setting attribute me
tadata:gedit-spell-language not supported

** (gedit:65035): WARNING **: Set document metadata failed: Setting attribute me
tadata:gedit-encoding not supported

** (gedit:65035): WARNING **: Set document metadata failed: Setting attribute me
tadata:gedit-spell-language not supported
```

- II. Take the executable file generated by the VCS Simulator then run simulation with its coverage options

- o **simv -cm line+cond+fsm+tgl+path**

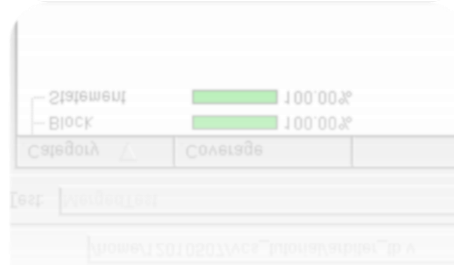
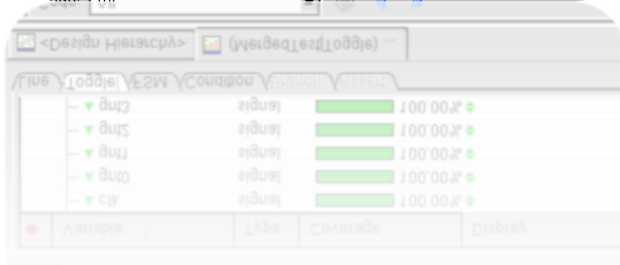
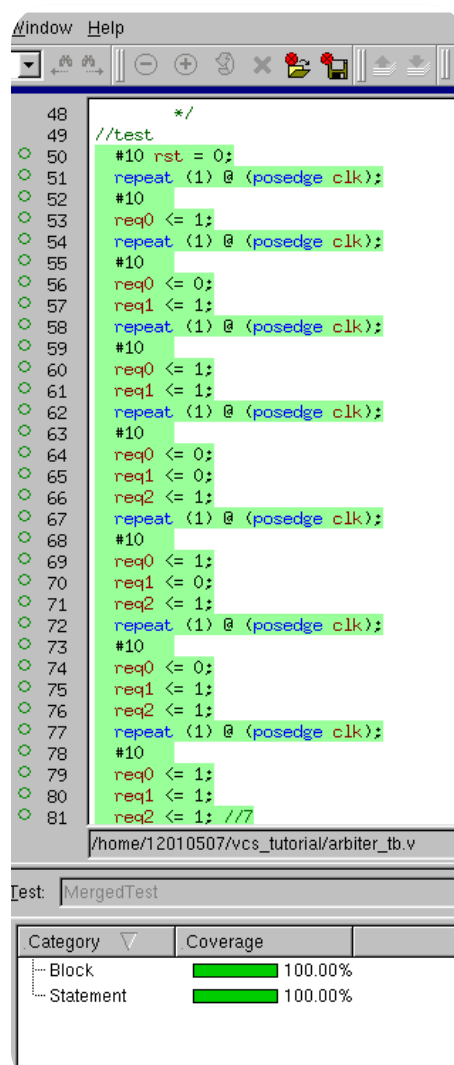
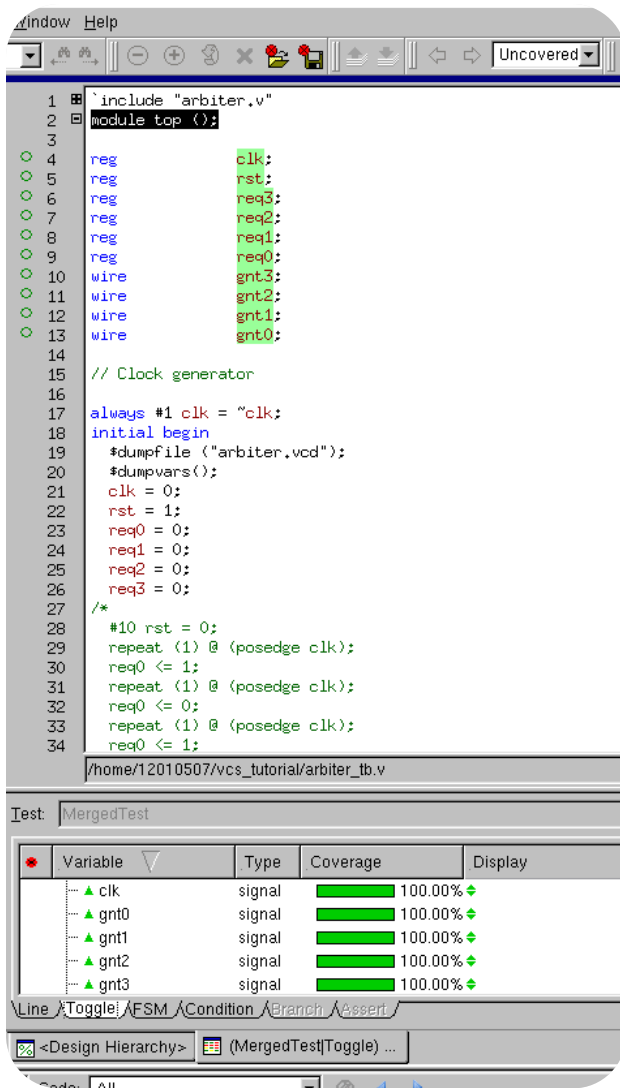
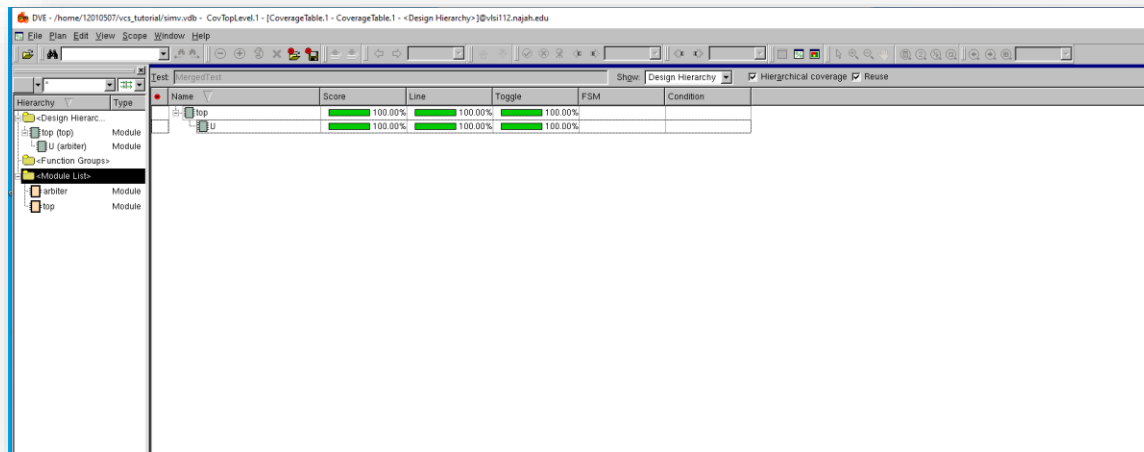
III. Open simulation database in design version environment

- **dve -cov**

```

[1] 4 12010507@vlsi12-vcs_mtor:
r[or]-[SE] Syntax error
Following verilog source has syntax error :
'arbiter_tb.v', 49: token is '#'
#10 rst = 0;
^
warnings
error
Pu time: .117 seconds to compile
5)+ Done dve -cov
12010507@vlsi12 vcs_tutorial$
* (gedit:65035): WARNING **: Set document metadata failed: Setting attribute me
adata:gedit-spell-language not supported
* (gedit:65035): WARNING **: Set document metadata failed: Setting attribute me
adata:gedit-encoding not support vcs -cm_tgl mda -lca -cm line+cond+fs+tgl -de
ug_al arbiter_tb.v
arning-[UNKNW OPTVIM] Unknown option passed
Ignoring unknown option '-debug_al' passed to 'vcs' and continuing
compilation.
Chronologic VCS (TM)
Version N-2017.12-1 -- Mon May 13 11:26:45 2024
Copyright (c) 1991-2017 by Synopsys Inc.
ALL RIGHTS RESERVED
his program is proprietary and confidential information of Synopsys Inc.
nd may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.
arning-[UNKNOPT] Unknown option found
Option 'xllcflags=' is unknown. It is being ignored. Try vcs -help for
supported options.
arning-[LCA_FEATURES_ENABLED] Usage warning
LCA features enabled by '-lca' argument on the command line. For more
information regarding list of LCA features please refer to Chapter "LCA
features" in the VCS/VCS-MX Release Notes
arsing design file 'arbiter_tb.v'
arsing included file 'arbiter.v'.
ack to file 'arbiter_tb.v'.
op Level Modules:
top
o Timescale specified
CS Coverage Metrics Release N-2017.12-1 Copyright (c) 1991-2017 by Synopsys Inc
tarting vcs inline pass...
module and 0 UDP read.
recompiling module top
m -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
d -m elf_i386 -shared -o ../..../simv.daidir//_csrc0.o so objs/amcQw.d.o
m -f _csrc0.so
f [ -x ../simv ]; then chmod -x ../simv; fi
++ -o ../simv -Wl,-rpath-link=-Wl,-rpath=$ORIGIN'/simv.daidir/ -Wl,-rpat
=/simv.daidir/ -Wl,-rpath=$ORIGIN'/simv.daidir/scsim.db.dir -m32 -m32 -rdyn
Warning-[UNKNW OPTVIM] Unknown option passed
Ignoring unknown option '-debug_all-debug_acc+all+dmptf' passed to 'vcs' and
continuing compilation.
Chronologic VCS (TM)
Version N-2017.12-1 -- Mon May 13 10:31:33 2024
Copyright (c) 1991-2017 by Synopsys Inc.
ALL RIGHTS RESERVED
This program is proprietary and confidential information of Synopsys Inc.
and may be used and disclosed only as authorized in a license agreement
controlling such use and disclosure.
Warning-[UNKNOPT] Unknown option found
Option 'xllcflags=' is unknown. It is being ignored. Try vcs -help for
supported options.
Warning-[LCA_FEATURES_ENABLED] Usage warning
LCA features enabled by '-lca' argument on the command line. For more
information regarding list of LCA features please refer to Chapter "LCA
features" in the VCS/VCS-MX Release Notes
Warning-[DBGACC_REG] '-debug_region' without '-debug_access'
'-debug_region' can only be used in conjunction with '-debug_access'.
'-debug_region' is ignored.
Please recompile using the '-debug_access<options>' switch and incremental
options as required. Recommended options are '-debug_access' for
post-process debug, '-debug_access+lass' for testbench debug, and
'-debug_access+all' for all debug capabilities. Refer the VCS user guide
for more granular options for debug control under the switch '-debug_access'
and refer to '-debug_region' for region control.
Parsing design file 'arbiter_tb.v'
Parsing included file 'arbiter.v'.
Back to file 'arbiter_tb.v'.
Top Level Modules:
top
No Timescale specified
VCS Coverage Metrics Release N-2017.12-1 Copyright (c) 1991-2017 by Synopsys Inc.
Starting vcs inline pass...
l module and 0 UDP read.
recompiling module top
rm -f _csrc*.so pre_vcsobj_*.so share_vcsobj_*.so
if [ -x ../simv ]; then chmod -x ../simv; fi
rm -o ../simv -Wl,-rpath-link=-Wl,-rpath=$ORIGIN'/simv.daidir/ -Wl,-rpath=$ORIGIN'/simv.daidir/scsim.db.dir -m32 -m32 -rdynamic obj
/amaCw.d.o 26620 archive_1.so SIM_1.o rmpats.mop.o rmpats.o rmar.o rmar.nd.o rmar.llvm_0.1.o rmar.llvm_0.0.o /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libzerofsof
rt.stubs.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libvirsim.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/liberrorinf.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libnpsmloc.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libbprof.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libbreader.common.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libB.a /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libbucnative.so /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/vcs.tls.o -Wl,-whole-archive /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/libvcsucli.so -Wl,-no-whole-archive /Disk2/eda/synopsys/2017-18/RHELx86/VCSMX_2017.12-1/linux/lib/ctype-stubs_32.a -ldl -lc -lm -lpthread -ldl
CPU time: .177 seconds to compile + .197 seconds to elab + .193 seconds to link

```



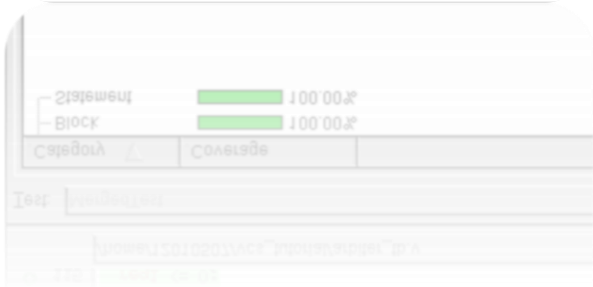
```
Window Help
[Icons] [Uncov]

82 repeat (1) @ (posedge clk);
83 #10
84 req0 <= 0;
85 req1 <= 0;
86 req2 <= 0;
87 req3 <= 1;
88 repeat (1) @ (posedge clk);
89 #10
90 req0 <= 1;
91 req1 <= 0;
92 req2 <= 0;
93 req3 <= 1;
94 repeat (1) @ (posedge clk);
95 #10
96 req0 <= 0;
97 req1 <= 1;
98 req2 <= 0;
99 req3 <= 1;
100 repeat (1) @ (posedge clk);
101 #10
102 req0 <= 1;
103 req1 <= 1;
104 req2 <= 0;
105 req3 <= 1;
106 repeat (1) @ (posedge clk);
107 #10
108 req0 <= 0;
109 req1 <= 0;
110 req2 <= 1;
111 req3 <= 1;
112 repeat (1) @ (posedge clk);
113 #10
114 req0 <= 1;
115 req1 <= 0;
```

/home/12010507/vcs_tutorial/arbiter_tb.v

Test: MergedTest

Category ▾	Coverage
Block	100.00%
Statement	100.00%



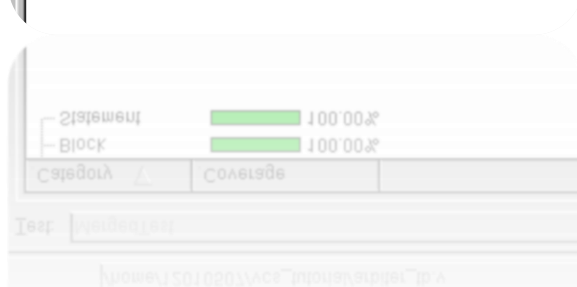
```
Window Help
[Icons]

127 req1 <= 1;
128 req2 <= 1;
129 req3 <= 1;
130
131 repeat (1) @ (posedge clk);
132 // finish test
133 #20 rst = 1;
134 repeat (1) @ (posedge clk);
135 req0 <= 1;
136 repeat (1) @ (posedge clk);
137 req0 <= 0;
138 repeat (1) @ (posedge clk);
139 req0 <= 1;
140 req1 <= 1;
141 repeat (1) @ (posedge clk);
142 req2 <= 1;
143 req1 <= 0;
144 repeat (1) @ (posedge clk);
145 req3 <= 1;
146 req2 <= 0;
147 repeat (1) @ (posedge clk);
148 req3 <= 0;
149 repeat (1) @ (posedge clk);
150 req0 <= 0;
151 repeat (1) @ (posedge clk);
152 #60 #finish;
153 end
154
155 // Connect the DUT
156 arbiter U (
157     clk,
158     rst,
159     req3,
160     req2,
```

/home/12010507/vcs_tutorial/arbiter_tb.v

Test: MergedTest

Category ▾	Coverage
Block	100.00%
Statement	100.00%



- what did we do is simply that we analyze the test bench and found out that we have four inputs plus the clk and reset signals then we added the missed test cases for them
- **req0->req3, 4 inputs**

0000 → 1111 so we have 16 test case without the reset

You can find them in the test bench

Count Value	8	4	2	1	Weighted Values
	Q3	Q2	Q1	Q0	Outputs
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	