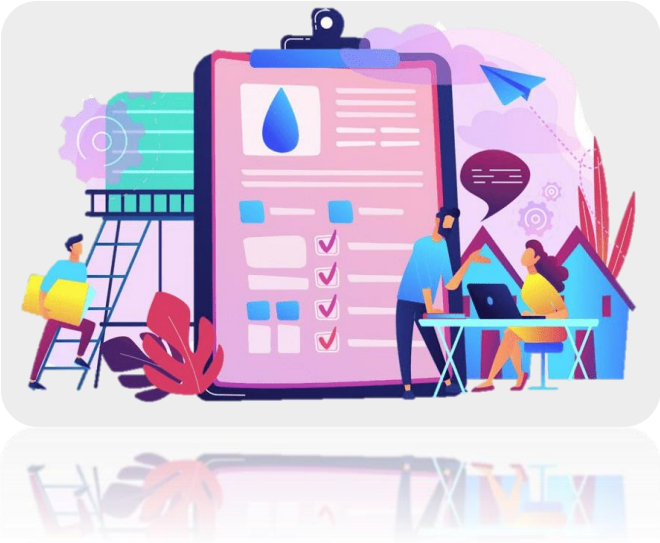

Exercise 3: Code Coverage

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Supervisor: Dr. Suliman Abu Kharmeh

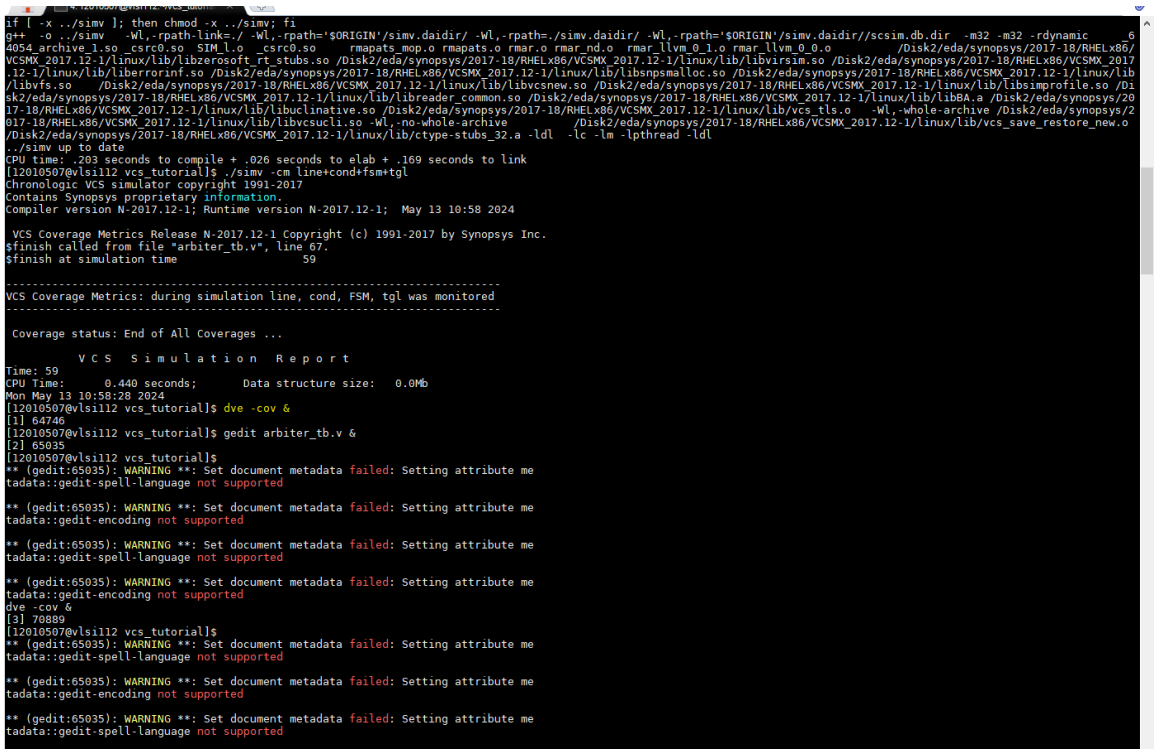
Course: Verification Design

1. In arbitr_tb.v and arbiter.v what is the code coverage in the code?

Score: almost 94% Line: 100% Toggle: almost 91%

We knew the score by applying this commands in the server terminal:

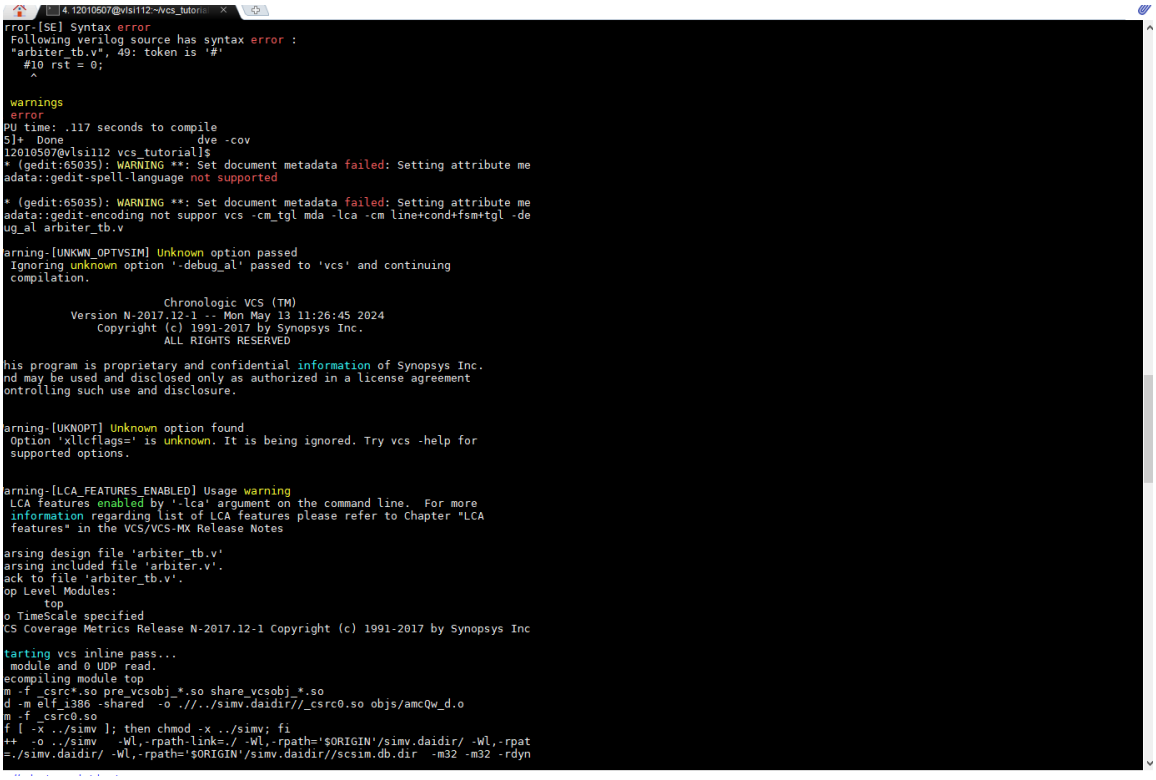
I. Open arbiter_tb.v and run it with these coverage options then debug it.
   - **vcs -cm_tgl mda -lca -cm line+cond+fsm+tgl+path -debug_all arbiter_tb.v**

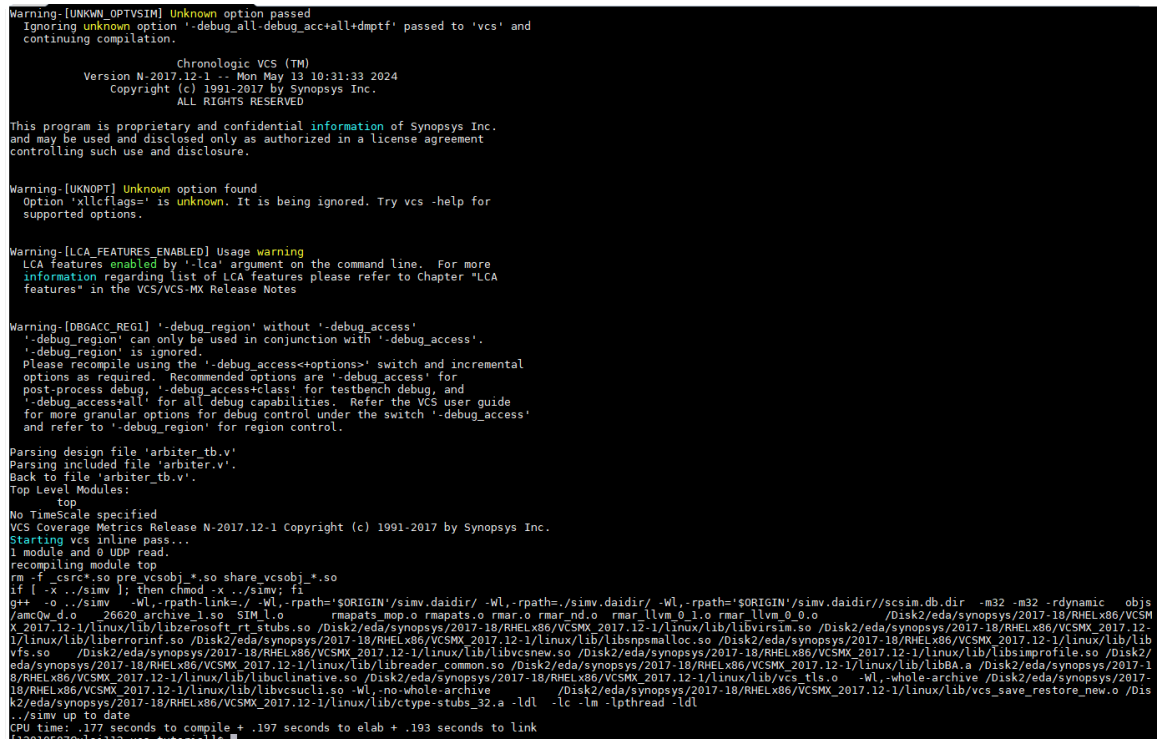


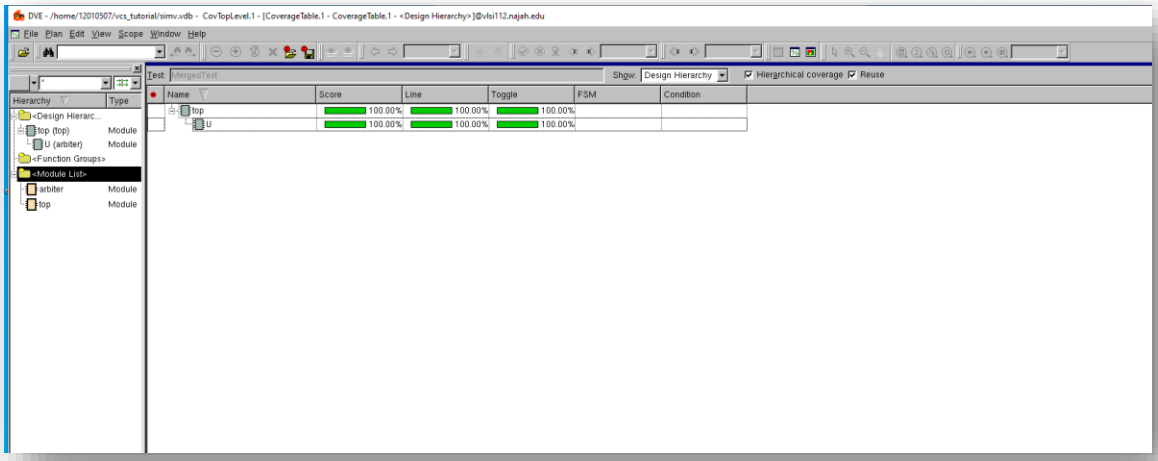
II. Take the executable file generated by the VCS Simulator then run simulation with its coverage options
   - **simv -cm line+cond+fsm+tgl+path**

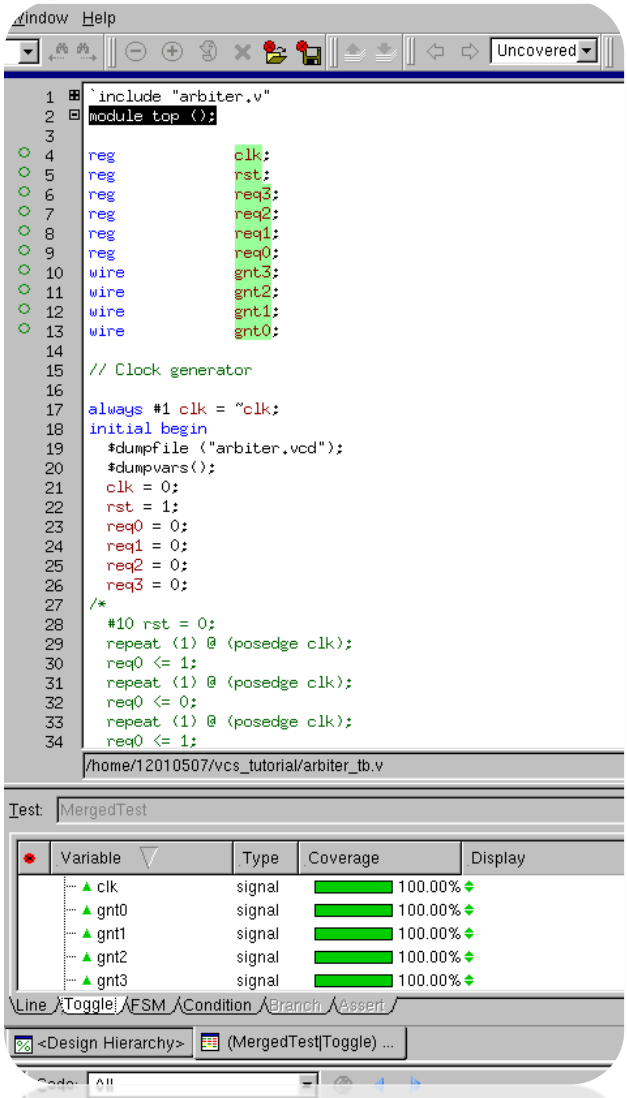
III. Open simulation database in design version environment

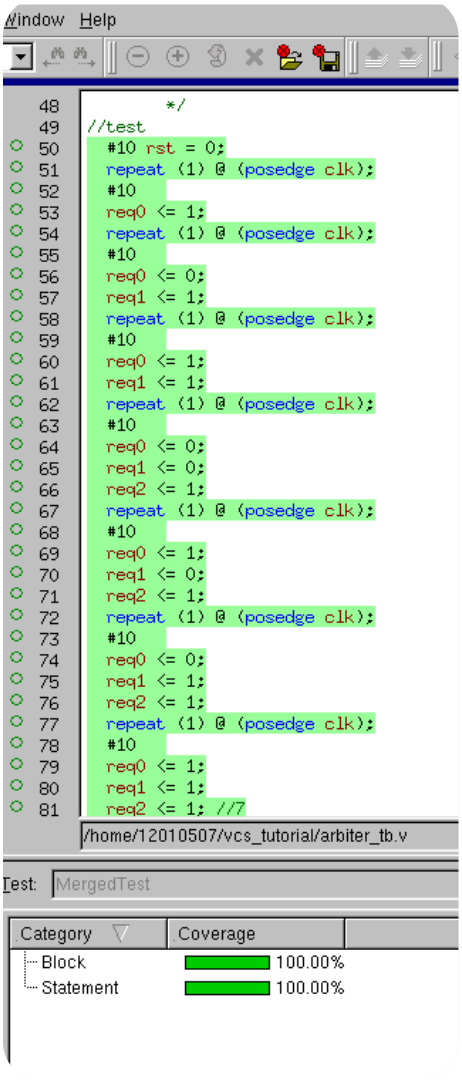
- **dve –cov**

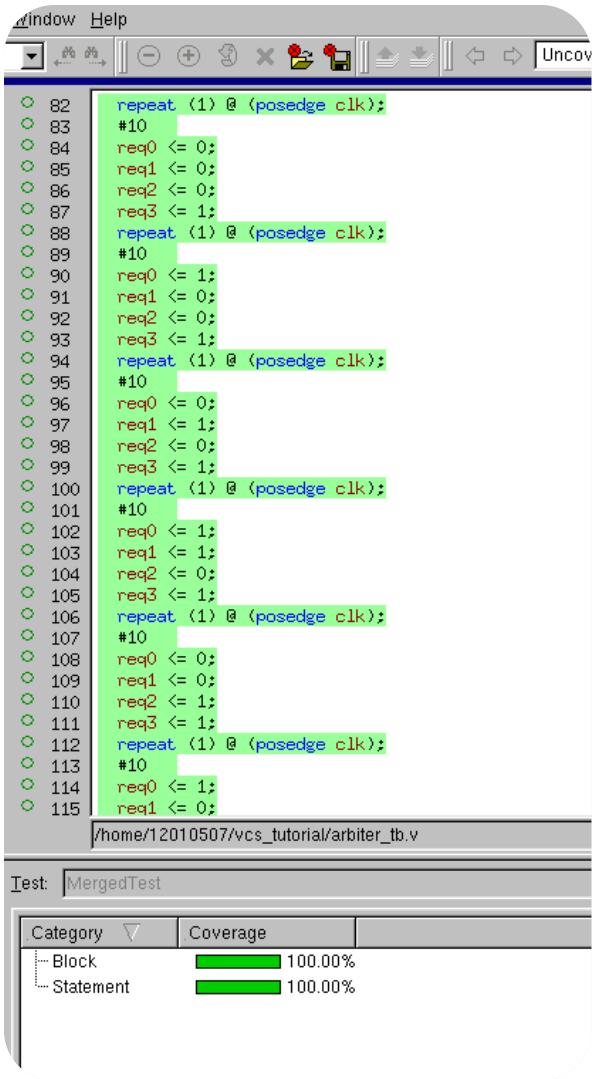


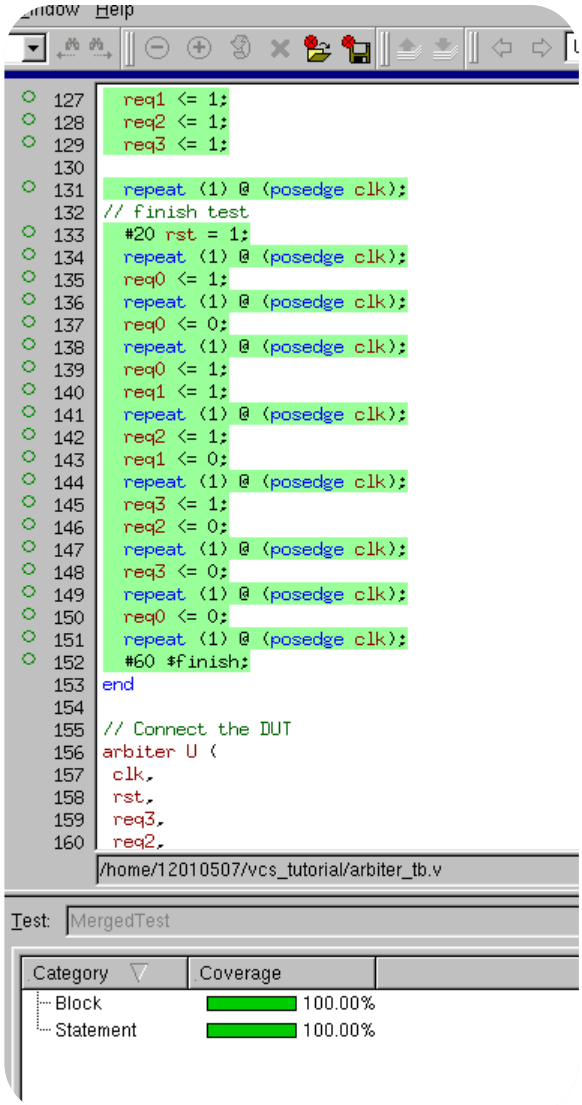



DVE - /home/12010507/vcs_tutorial/simv.vdb - CovTopLevel.1 - [CoverageTable.1 - CoverageTable.1 - <Design Hierarchy>]@vlsi112.najah.edu
File Plan Edit View Scope Window Help
Test: MergedTest
Show: Design Hierarchy
Hierarchical coverage
Reuse
Hierarchy
Type
<Design Hierarc...
top (top)
Module
U (arbiter)
Module
<Function Groups>
<Module List>
arbiter
Module
top
Module
Name
Score
Line
Toggle
FSM
Condition
top
100.00%
U
100.00%


Window Help
Uncovered
1 `include "arbiter.v"
2 module top ();
3
4 reg clk;
5 reg rst;
6 reg req3;
7 reg req2;
8 reg req1;
9 reg req0;
10 wire gnt3;
11 wire gnt2;
12 wire gnt1;
13 wire gnt0;
14
15 // Clock generator
16
17 always #1 clk = ~clk;
18 initial begin
19 $dumpfile ("arbiter.vcd");
20 $dumpvars();
21 clk = 0;
22 rst = 1;
23 req0 = 0;
24 req1 = 0;
25 req2 = 0;
26 req3 = 0;
27 /*
28 #10 rst = 0;
29 repeat (1) @ (posedge clk);
30 req0 <= 1;
31 repeat (1) @ (posedge clk);
32 req0 <= 0;
33 repeat (1) @ (posedge clk);
34 req0 <= 1;
/home/12010507/vcs_tutorial/arbiter_tb.v
Test: MergedTest
Variable
Type
Coverage
Display
clk signal 100.00%
gnt0 signal 100.00%
gnt1 signal 100.00%
gnt2 signal 100.00%
gnt3 signal 100.00%
Line
Toggle
FSM
Condition
Branch
Assert
<Design Hierarchy>
(MergedTest|Toggle) ...


Window Help
48 */
49 //test
50 #10 rst = 0;
51 repeat (1) @ (posedge clk);
52 #10
53 req0 <= 1;
54 repeat (1) @ (posedge clk);
55 #10
56 req0 <= 0;
57 req1 <= 1;
58 repeat (1) @ (posedge clk);
59 #10
60 req0 <= 1;
61 req1 <= 1;
62 repeat (1) @ (posedge clk);
63 #10
64 req0 <= 0;
65 req1 <= 0;
66 req2 <= 1;
67 repeat (1) @ (posedge clk);
68 #10
69 req0 <= 1;
70 req1 <= 0;
71 req2 <= 1;
72 repeat (1) @ (posedge clk);
73 #10
74 req0 <= 0;
75 req1 <= 1;
76 req2 <= 1;
77 repeat (1) @ (posedge clk);
78 #10
79 req0 <= 1;
80 req1 <= 1;
81 req2 <= 1; //7
/home/12010507/vcs_tutorial/arbiter_tb.v
Test: MergedTest
Category
Coverage
Block 100.00%
Statement 100.00%


Window Help
Uncov
82 repeat (1) @ (posedge clk);
83 #10
84 req0 <= 0;
85 req1 <= 0;
86 req2 <= 0;
87 req3 <= 1;
88 repeat (1) @ (posedge clk);
89 #10
90 req0 <= 1;
91 req1 <= 0;
92 req2 <= 0;
93 req3 <= 1;
94 repeat (1) @ (posedge clk);
95 #10
96 req0 <= 0;
97 req1 <= 1;
98 req2 <= 0;
99 req3 <= 1;
100 repeat (1) @ (posedge clk);
101 #10
102 req0 <= 1;
103 req1 <= 1;
104 req2 <= 0;
105 req3 <= 1;
106 repeat (1) @ (posedge clk);
107 #10
108 req0 <= 0;
109 req1 <= 0;
110 req2 <= 1;
111 req3 <= 1;
112 repeat (1) @ (posedge clk);
113 #10
114 req0 <= 1;
115 req1 <= 0;
/home/12010507/vcs_tutorial/arbiter_tb.v
Test: MergedTest
Category Coverage
Block 100.00%
Statement 100.00%


Window Help
127 req1 <= 1;
128 req2 <= 1;
129 req3 <= 1;
130
131 repeat (1) @ (posedge clk);
132 // finish test
133 #20 rst = 1;
134 repeat (1) @ (posedge clk);
135 req0 <= 1;
136 repeat (1) @ (posedge clk);
137 req0 <= 0;
138 repeat (1) @ (posedge clk);
139 req0 <= 1;
140 req1 <= 1;
141 repeat (1) @ (posedge clk);
142 req2 <= 1;
143 req1 <= 0;
144 repeat (1) @ (posedge clk);
145 req3 <= 1;
146 req2 <= 0;
147 repeat (1) @ (posedge clk);
148 req3 <= 0;
149 repeat (1) @ (posedge clk);
150 req0 <= 0;
151 repeat (1) @ (posedge clk);
152 #60 $finish;
153 end
154
155 // Connect the DUT
156 arbiter U (
157 clk,
158 rst,
159 req3,
160 req2,
/home/12010507/vcs_tutorial/arbiter_tb.v
Test: MergedTest
Category Coverage
Block 100.00%
Statement 100.00%

- what did we do is simply bthat we analyze the test bench and founbd out that w have four inputs plus the clk and reset signals then we added the missed test cases for them
- **req0->req3, 4 inputs**

0000 → 1111 so we have 16 test case without the reset

You can find them in the test bench