SYNOPSIS SENTAURUS TCAD FOR SEMICONDUCTOR DEVICE SIMULATION

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WELCOME & SCOPE

- **Includes…**

✓Semiconductor device modeling basics

✓Hands-on insight into Synopsys TCAD

✓Career/research applications of TCAD

- **It is not…**

× a replacement for formal device physics coursework

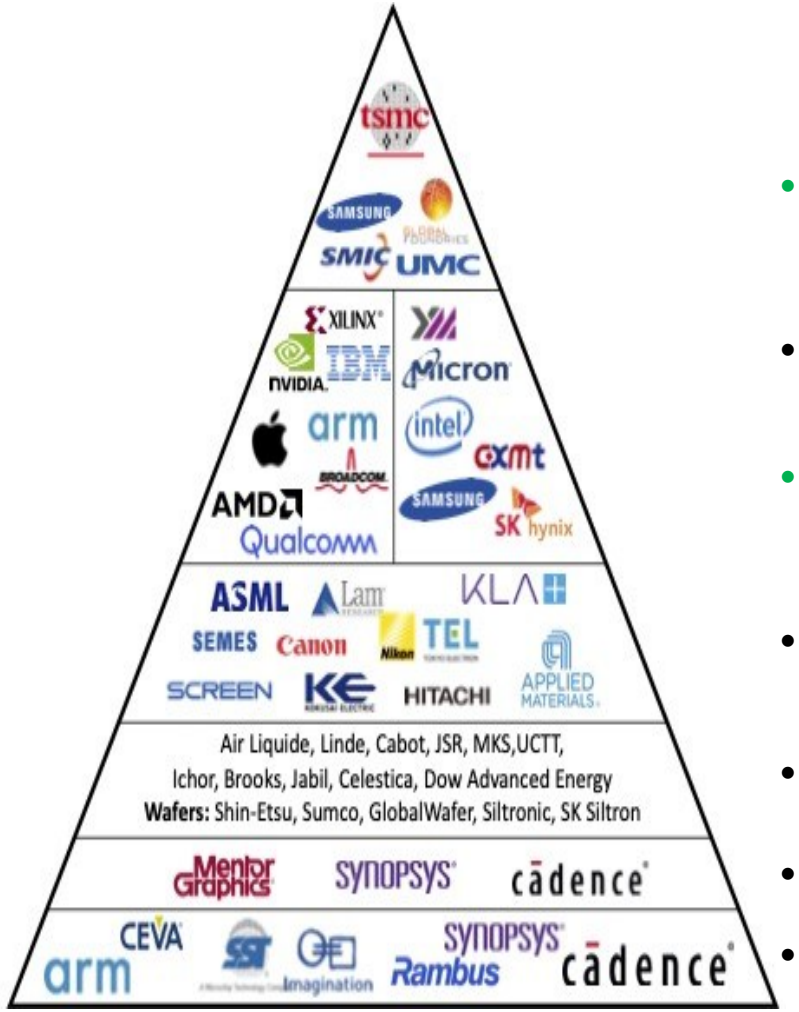
× a full TCAD training course

× a certification program

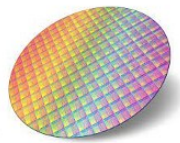
× an advanced/complex device simulation resource

- **Become familiar of Synopsys TCAD and get an overview of the tool and the resources for making a TCAD skillset**
- **Leveraging TCAD modeling skill for career development – securing higher study positions, Industry roles, etc.**

SEMICONDUCTOR SUPPLY CHAIN



- Chip Foundries



OSAT service providers

- Integrated Device Manufacturers (IDMs) (right-segment)
- "Fabless" Chip Companies (left-segment)

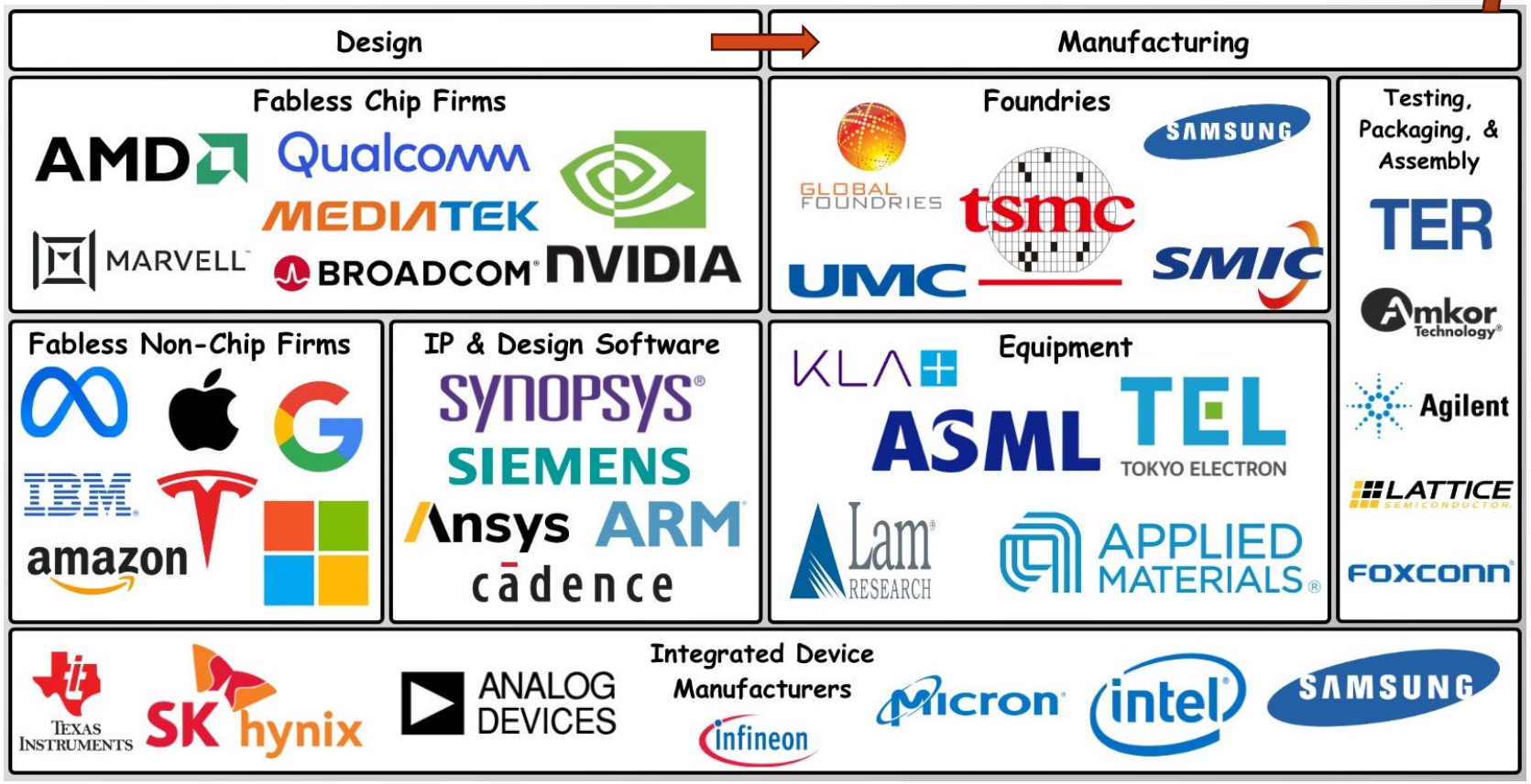
- Wafer Fab Equipment (WFE)
  Make the Chips
- Specialized Materials and Chemicals

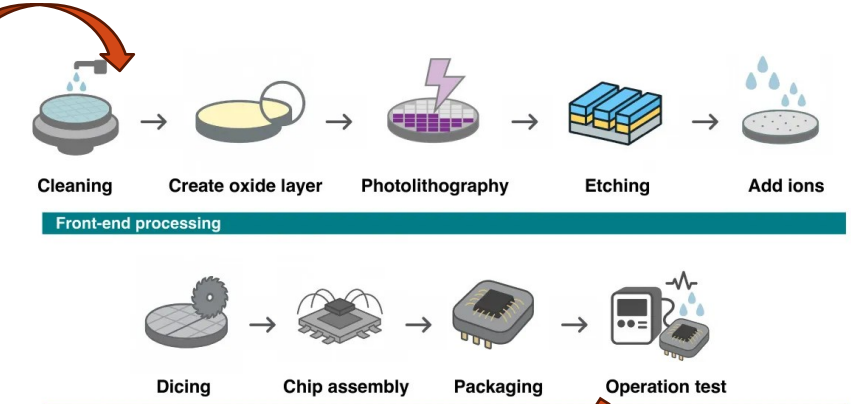
- Electronic Design Automation (EDA) Tools
- Chip Intellectual Property (IP) Cores

Bottom-up approach

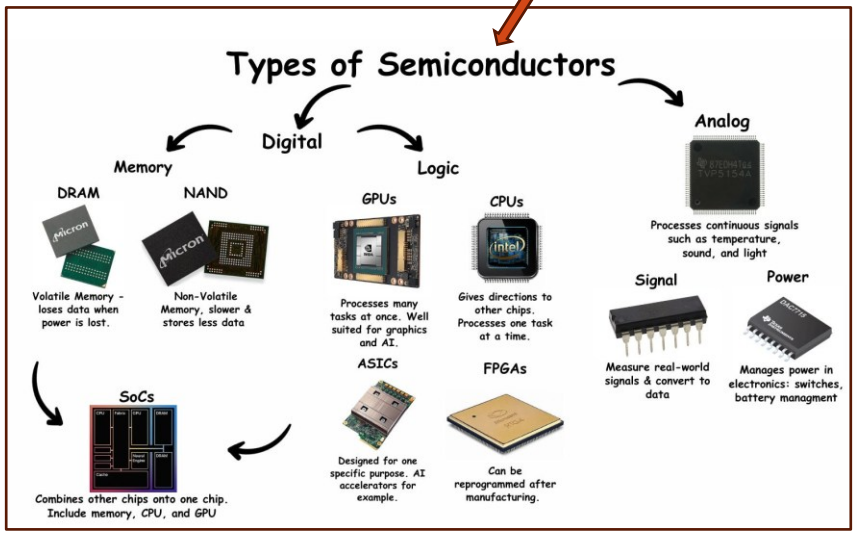
Credits: The Semiconductor Ecosystem Explained by Prof. Steve Blank on 02-06-2022; Semiconductor Value Chain – globally distributed ecosystem by Rokon Zaman 12-07-2023

SEMICONDUCTOR ECOSYSTEM





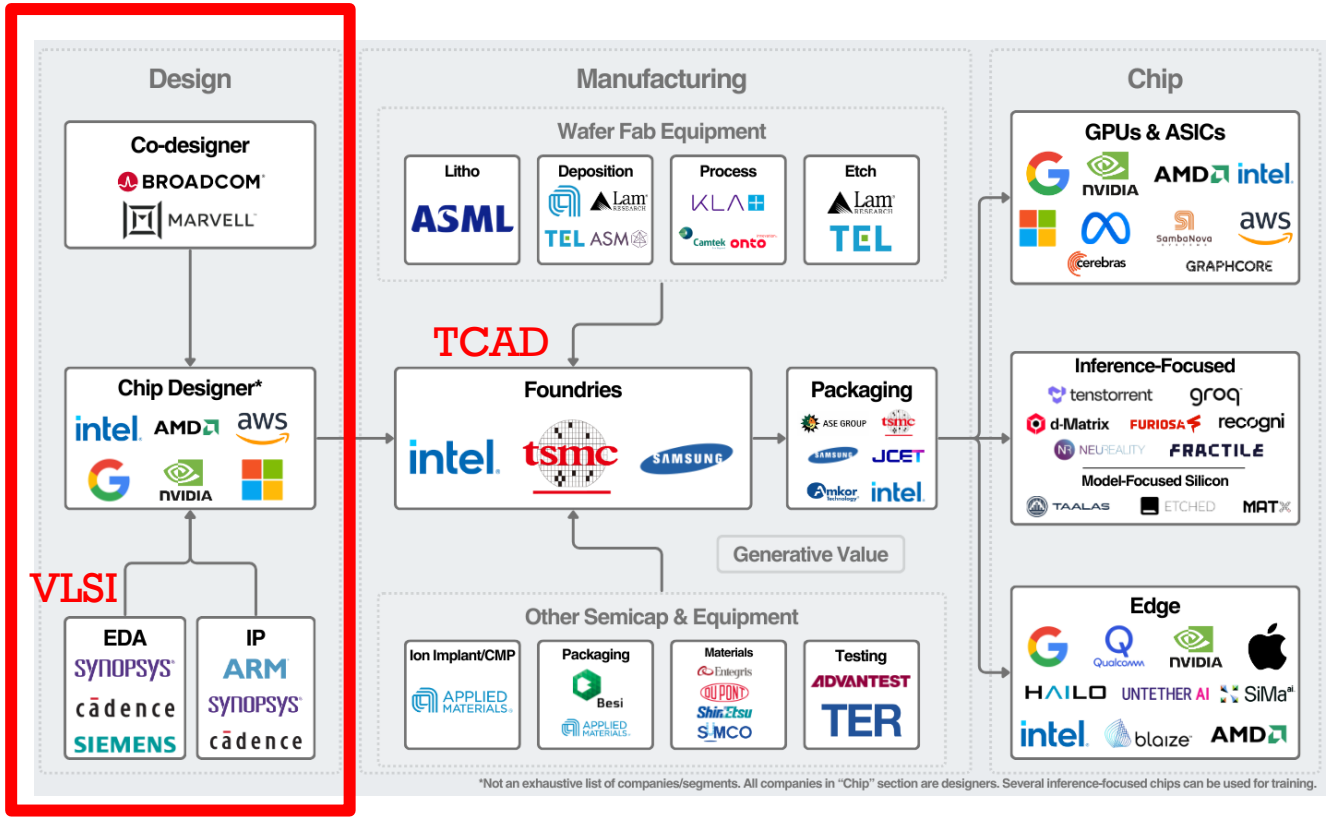
Front End: Wafer fabrication
Back End: Packaging & Testing

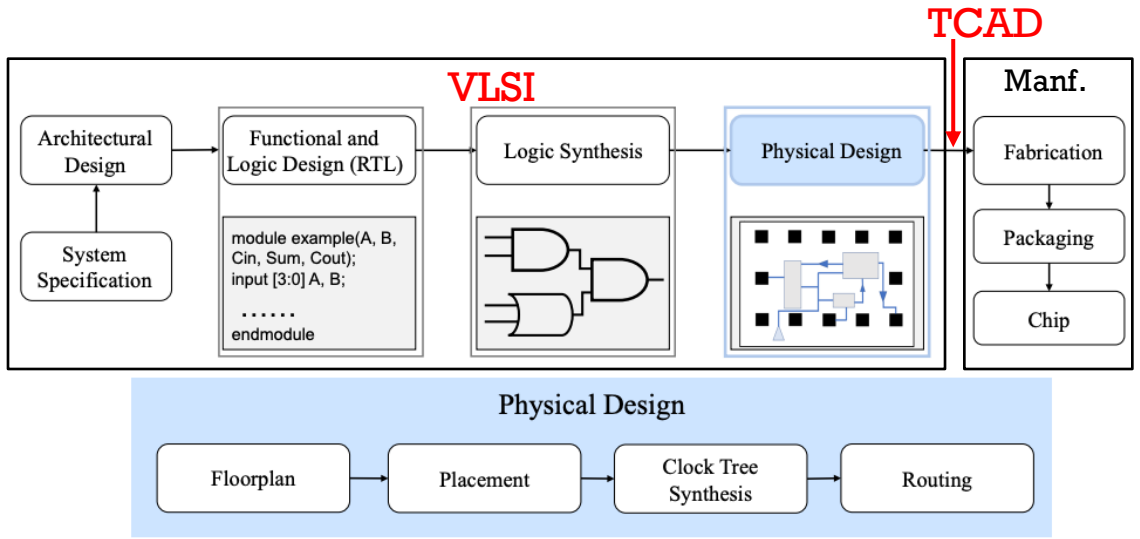


All these semiconductors are **packaged!**

Credits: **An Overview of the Semiconductor Industry** by Eric Flaningam on 11-16-2023 (left, right-bottom); Rapidus Inc. (Right-top)

ELECTRONIC DESIGN AUTOMATION (EDA) VS. TCAD (TECHNOLOGY COMPUTER-AIDED DESIGN)





Modern chip design process.

VLSI	TCAD
Circuit & system design	Device physics & process simulation
RTL → Layout → Tape-out	Doping, lithography, etching, I–V
Tools: Cadence, Synopsys (EDA)	Tools: Sentaurus, Silvaco (Device)
Used by IC designers	Used by device/process engineers
Output: Chip layout (GDSII)	Output: Device physics & profiles

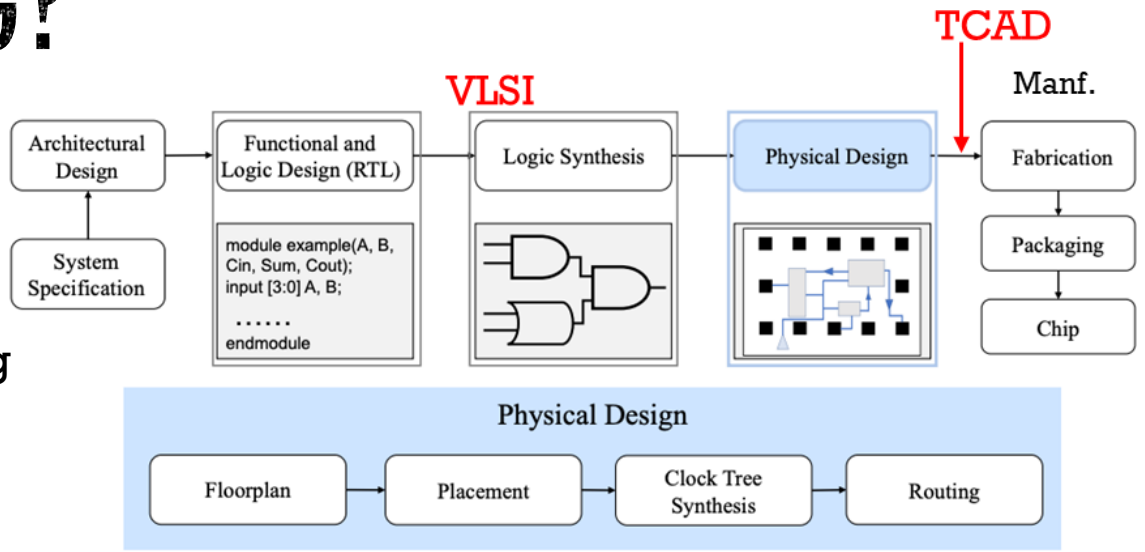
- When you see **EDA (Electronic Design Automation)** mentioned, it **almost always refers to VLSI / chip design, not TCAD**
- **VLSI users** - design companies (NVIDIA, Qualcomm, Broadcom, Intel, AMD, Marvell, etc.)
- **TCAD users –** *foundries (Intel, TSMC, Samsung, GlobalFoundries, etc.)

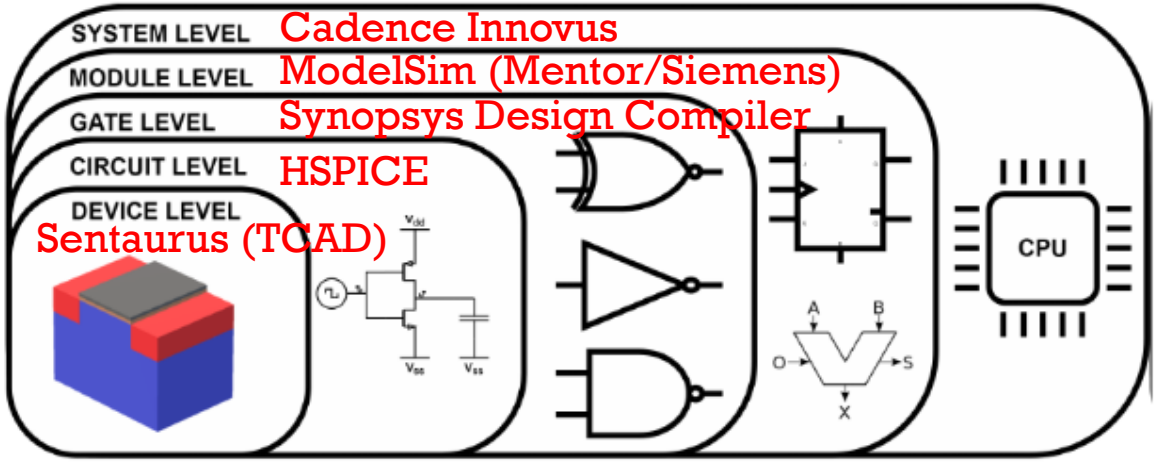
*Foundries = companies that own and operate the wafer fabrication plants (fabs)

Credits: **An Overview of the Semiconductor Industry** by Eric Flaningam on 11-16-2023 (left); Wang et al. arXiv:2407.15026v1 (2024) (right-top)

WHY USE TCAD MODELING?

- TCAD Modeling Benefits
  - 💰 Cost saving vs. actual fabrication
  - ✅ Check device feasibility before tape-out
  - 🔬 Understand physics beyond experimental probing
  - ⚙️ Optimize doping, geometry, and process conditions
- Industry Applications
  - Transistor scaling: FinFET, GAAFET, TFET
  - Power devices: IGBT, MOSFET, SiC/GaN HEMTs
  - Optoelectronics: LED, photodiode, solar cells
- Popular TCAD Solutions
  - **Synopsys Sentaurus** / TCAD (industry gold standard)
  - **Silvaco ATLAS**
  - COMSOL Multiphysics (general-purpose)
  - In-house proprietary simulators

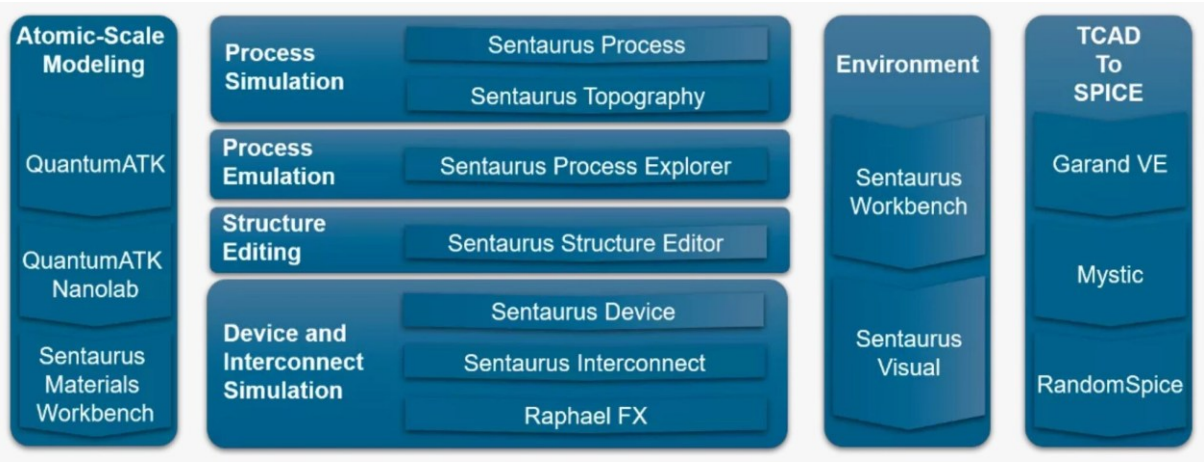


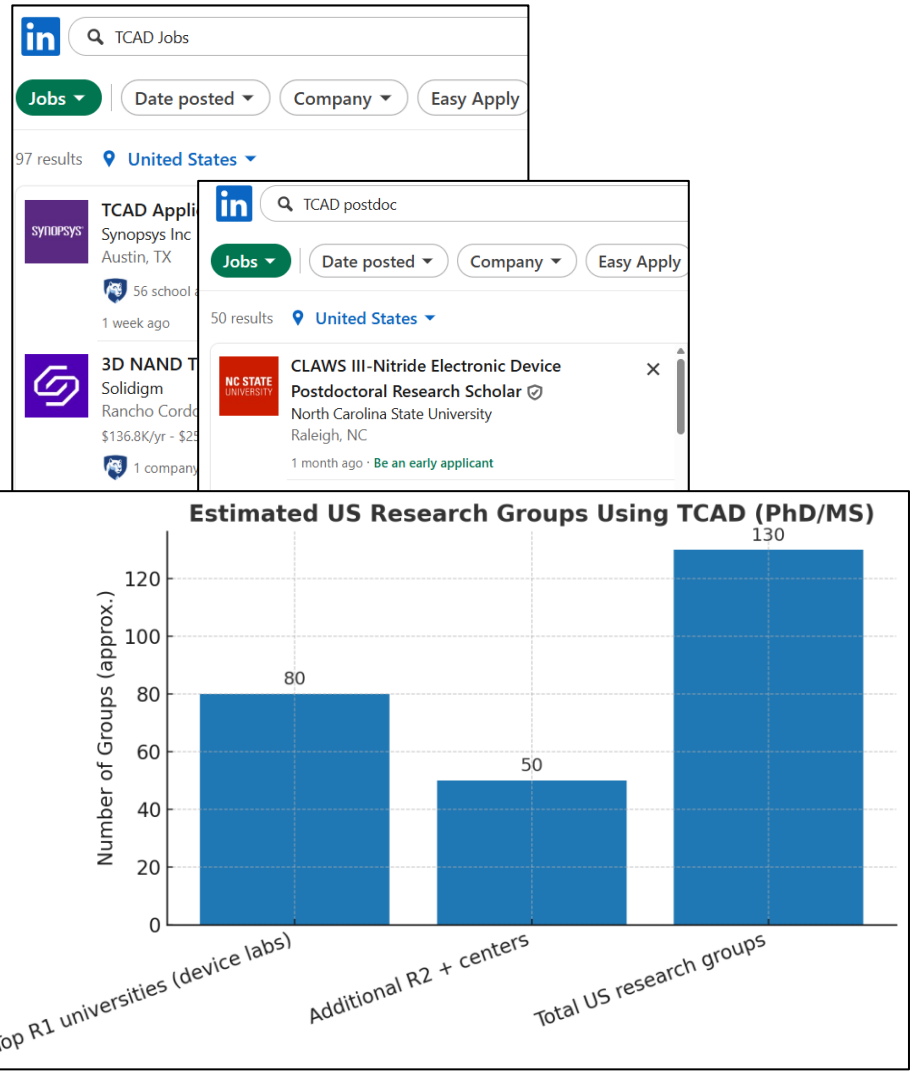


Credits: Wang et al. arXiv:2407.15026v1 (2024) (right-top); Talha Furkan Canan – PhD Dissertation (right-bottom)

WHY SYNOPSYS SENTAURUS TCAD?

- Strengths
  - 🌎 Widely used in academia & industry
  - 🔗 Integrates process + device simulation
  - 📚 Extensive materials library
  - ⚡ Links with circuit simulation
- Career Benefits
  - 🎓 PhD → device modeling & semiconductor physics
  - 🏭 Jobs → foundries & fabless (Intel, TSMC, Samsung, GlobalFoundries, Applied Materials, Lam Research)
  - 👷 Roles → TCAD Engineer, Device Modeling Engineer, Process Integration Engineer, R&D Engineer





as of August 16, 2025

Credits: University of Glasglow/Asen Asenov

SENTAURUS TCAD WORKFLOW

SEditor → SDevice → SVisual

Structure – Source, Drain, Gate, Contact

Doping

Meshing

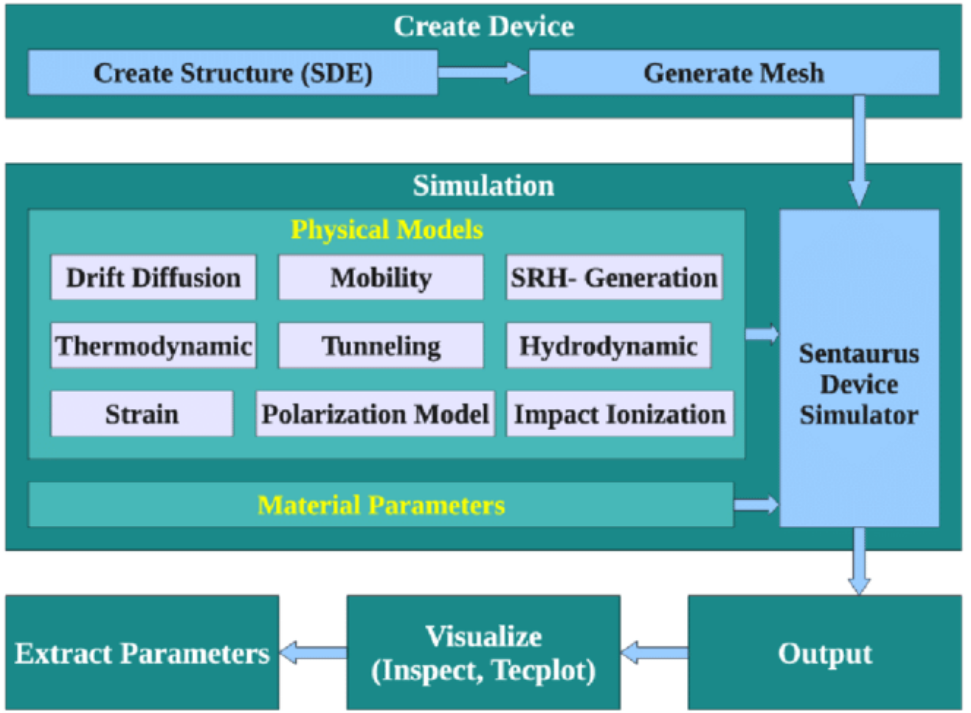
Part 1 – Structure (SEditor):
- Define geometry (2D MOSFET, FET, diode).
- Specify regions (source, drain, channel, oxide).
- Boundary conditions.

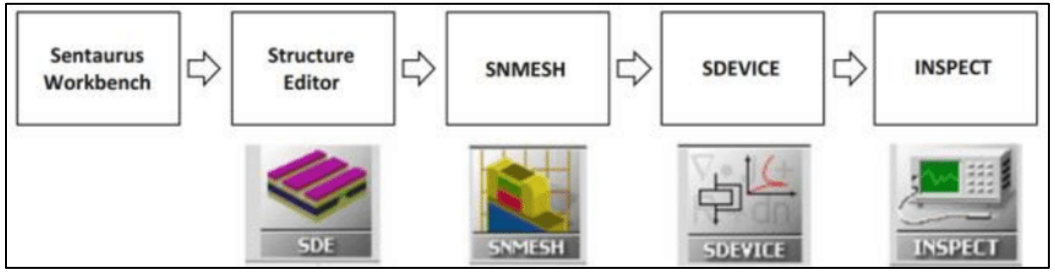
Part 2 – Doping:
- Uniform vs Gaussian profiles.
- Realistic implant/diffusion vs quick uniform doping.

Part 3 – Meshing:
- Importance of mesh density near junctions/interfaces.
  - Coarse mesh → faster, less accurate.
  - Fine mesh → accurate, slower.

Part 4 – Device (SDevice):
- Set biasing (Vds, Vgs).
- Choose physical models (mobility, recombination, quantum corrections).
- Run simulation.

Part 5 – Results (SVisual):
- Plot I_D–V_G, I_D–V_D.
- Check band diagrams, carrier density, field distribution.
- Debugging tips (convergence errors, unrealistic results).





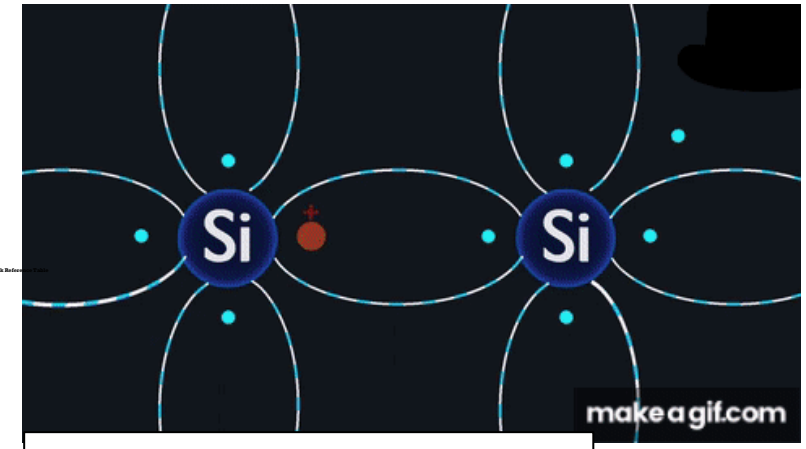
From SWorkbench (connecting all together), used to automate repetitive process

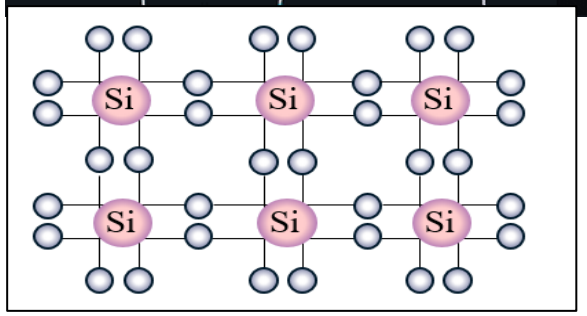
Credits: Wu et al. 3D TCAD Simulation for CMOS Nanoeletronic Devices (Springer, 2018) (right-top); Talha Furkan Canan – PhD Dissertation (right-bottom)

SEMICONDUCTOR MATERIALS

Intrinsic Semiconductor (no-doping)

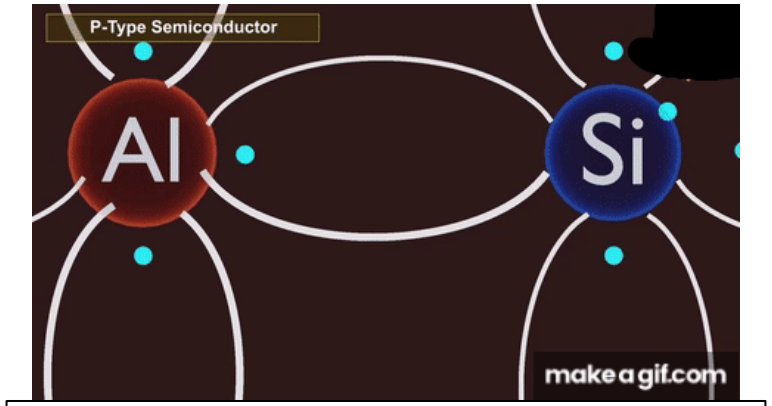
No doping

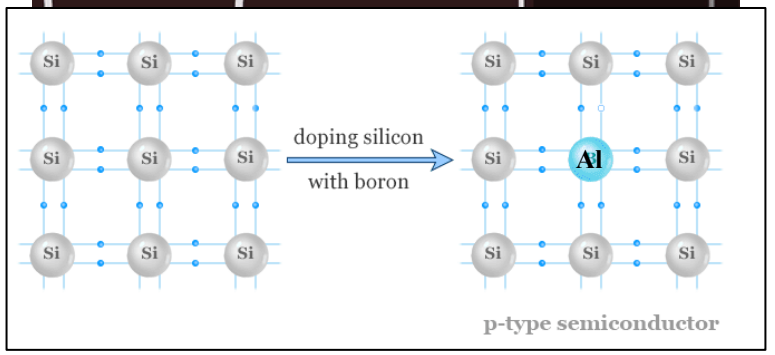




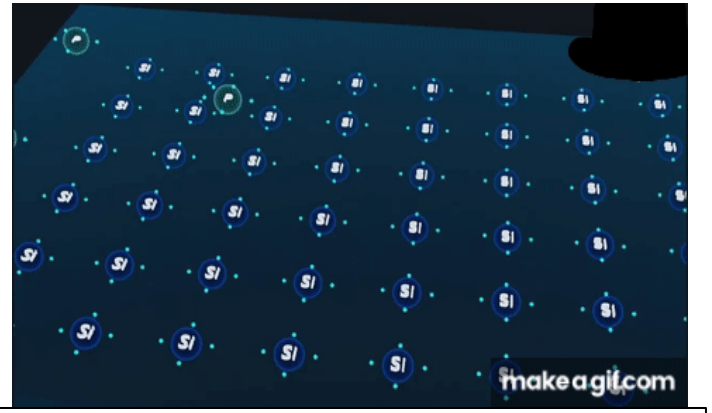
Extrinsic Semiconductor (doping)

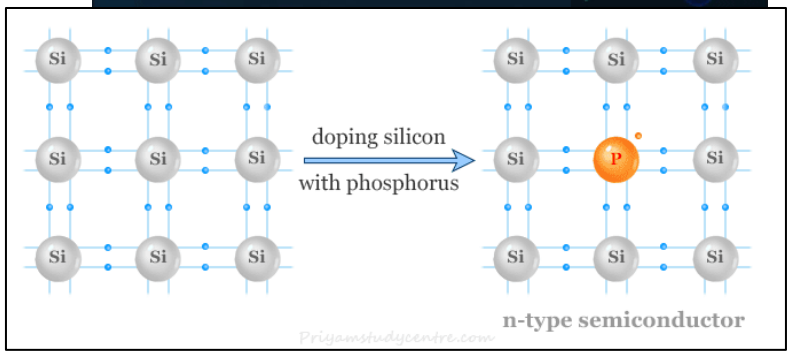
P-type doping (group III)





N-type doping (group V)

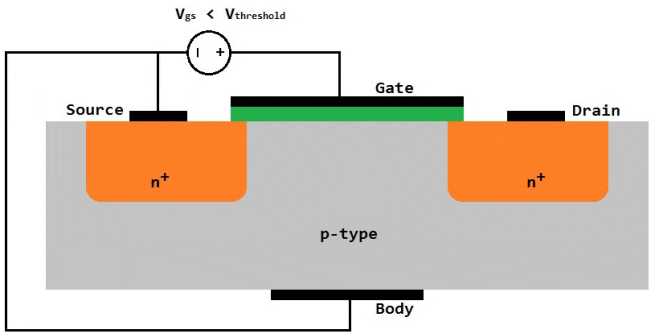


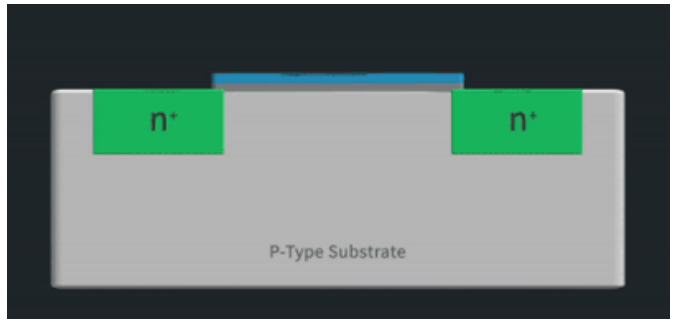


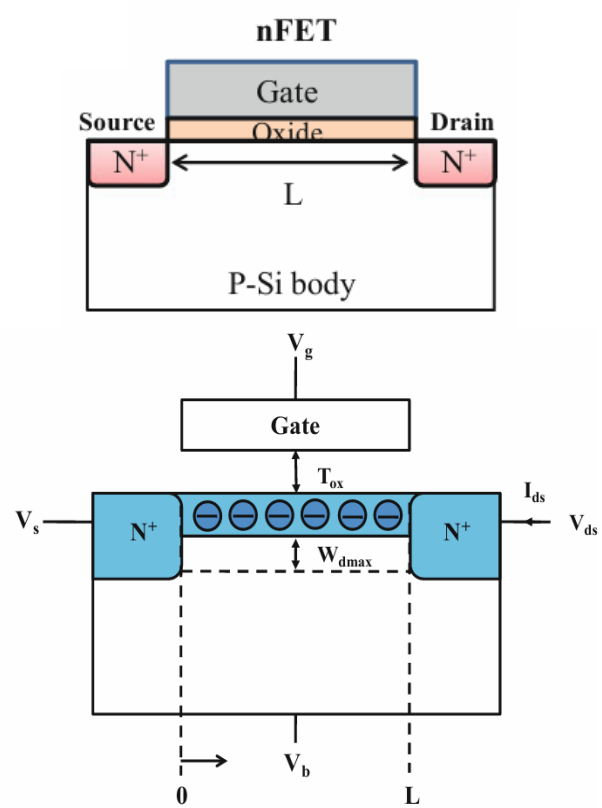
Symbol	Type	Typical Doping (cm^{-3})	Use Case
i	Intrinsic	~10^{10}	Pure Si/Ge
n	Light n	10^{14}–10^{16}	Channel, lightly doped drain
n^+	Heavy n	10^{17}–10^{18}	Source/drain regions
n^{++}	Degenerate n	≥10^{19}	Ohmic contacts

p	Light p	10^{14}–10^{16}	Channel, substrate
p^+	Heavy p	10^{17}–10^{18}	Wells, junction regions
p^{++}	Degenerate p	≥10^{19}	Ohmic contacts, tunnel junctions

SIMPLE 2D N-TYPE MOSFET DEVICE EQUATIONS







I_{ds} = drain to source current (A)
V_{ds} = drain to source voltage (V)
I_{dsat} = drain to source saturated current (A)
V_{dsat} = drain to sources saturated voltage (V)
V_{gs} = gate to sources voltage (V)
C_{oxe} = effective oxide capacitance (C)
μ_{ns} = electron surface mobility ($m^2/(V \cdot s)$)
V_t = gate threshold voltage (V)
W = width of the channel (m)
L = length of the channel (m)
g_m = transconductance (S = A/V)
g_{msat} = saturation transconductance (S = A/V)

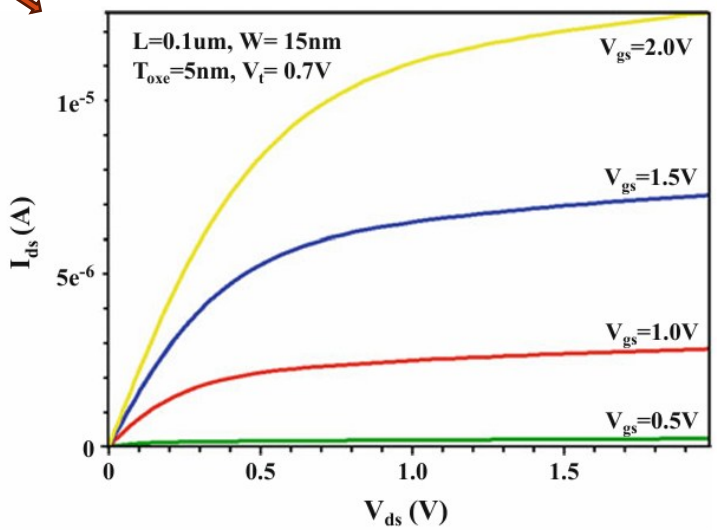
$$I_{ds} = \frac{W}{L} C_{oxe} \mu_{ns} \left(V_{gs} - V_t - \frac{1}{2} V_{ds} \right) V_{ds}$$

$$V_{dsat} = V_{gs} - V_t$$

$$I_{dsat} = \frac{W}{2L} C_{oxe} \mu_{ns} (V_{gs} - V_t)^2$$

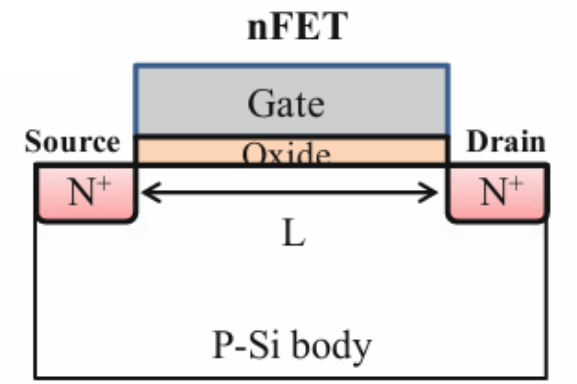
$$g_m \equiv dI_{ds} / dV_{gs} \big|_{V_{ds}}$$

$$g_{msat} = \frac{W}{L} C_{oxe} \mu_{ns} (V_{gs} - V_t)$$

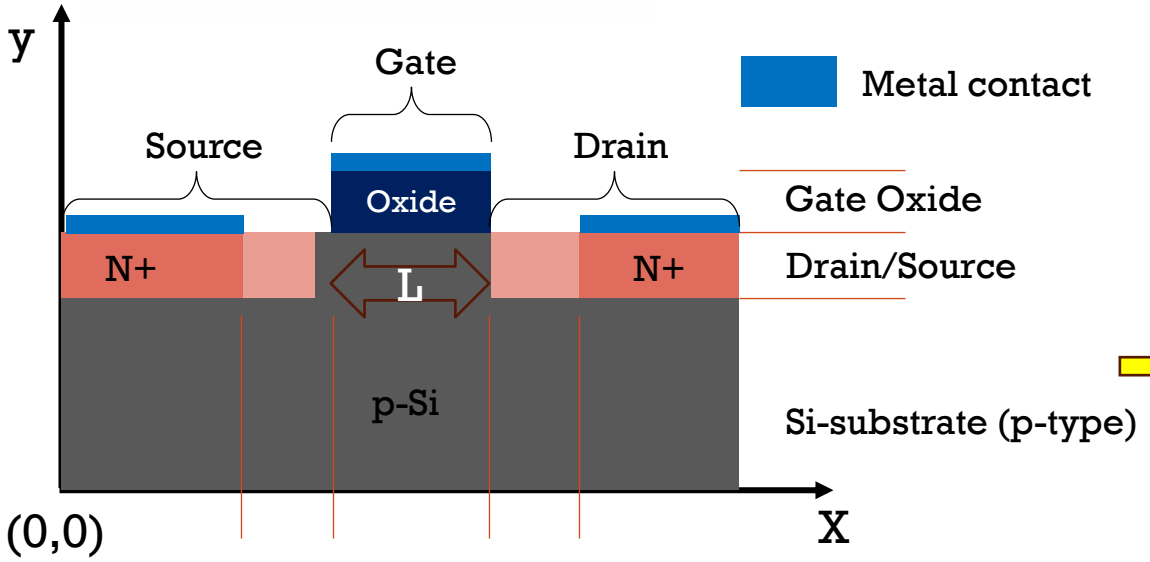


Credits: FETs (Field-Effect Transistors) by Alec_Schmidt (top-left), CircuitBread/Josh Bishop (top-right), S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, 3rd ed (Wiley, NY, 2007) (device equations); Wu et al. 3D TCAD Simulation for CMOS Nanoeletronic Devices (Springer, 2018)

SENTAURUS TCAD MODELING – PART 1 - STRUCTURE

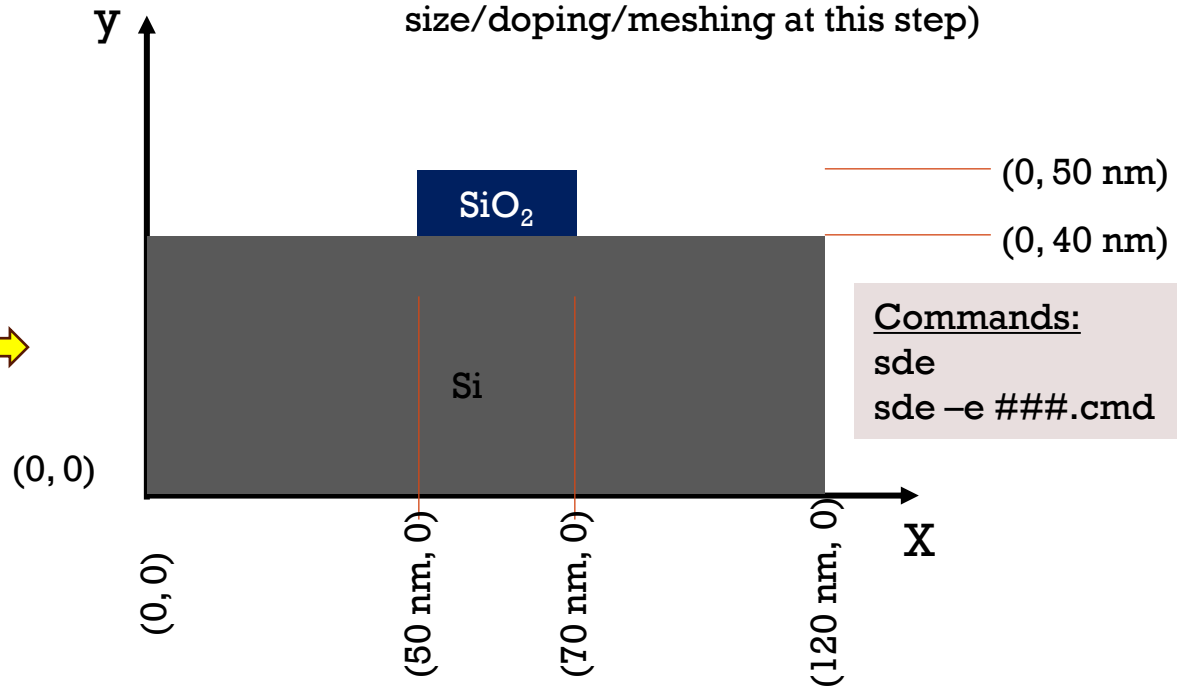


Four things to do in this step:
(1) Parameter (lengths, carrier concentration values, etc.)
(2) Structure (designing the structure)
(3) Contact (contact metal placing)
(4) Doping (doping profile)
(5) Mesh (solver mesh)



2D MOSFET structure (concept -> overall figure)

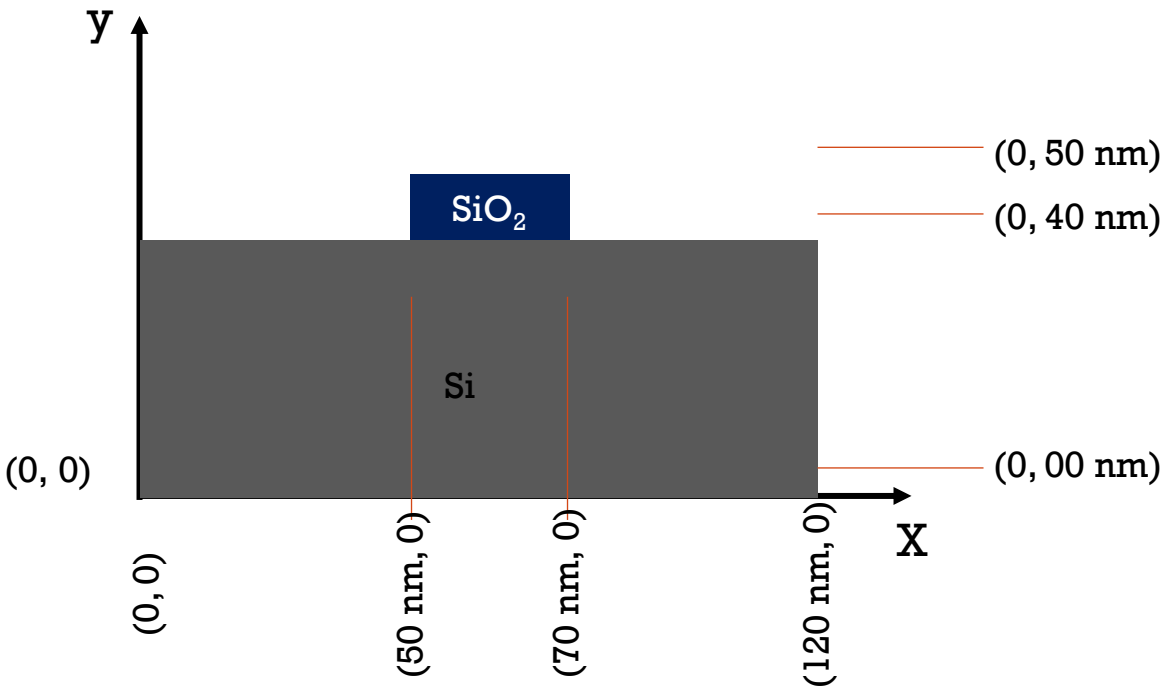
(no need to think about contact size/doping/meshing at this step)



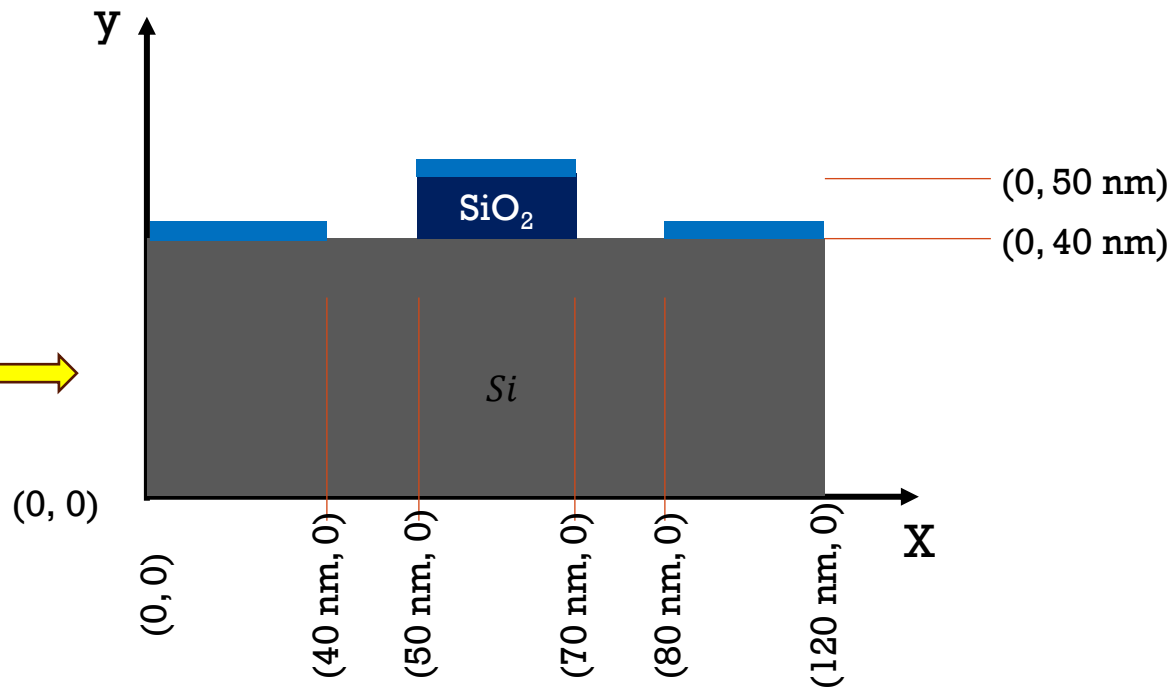
2D MOSFET structure (figure -> added parameters/co-ordinates) Cartoon plot

SENTAURUS TCAD MODELING – ADD CONTACT

(no need to think about doping/meshing at this step)



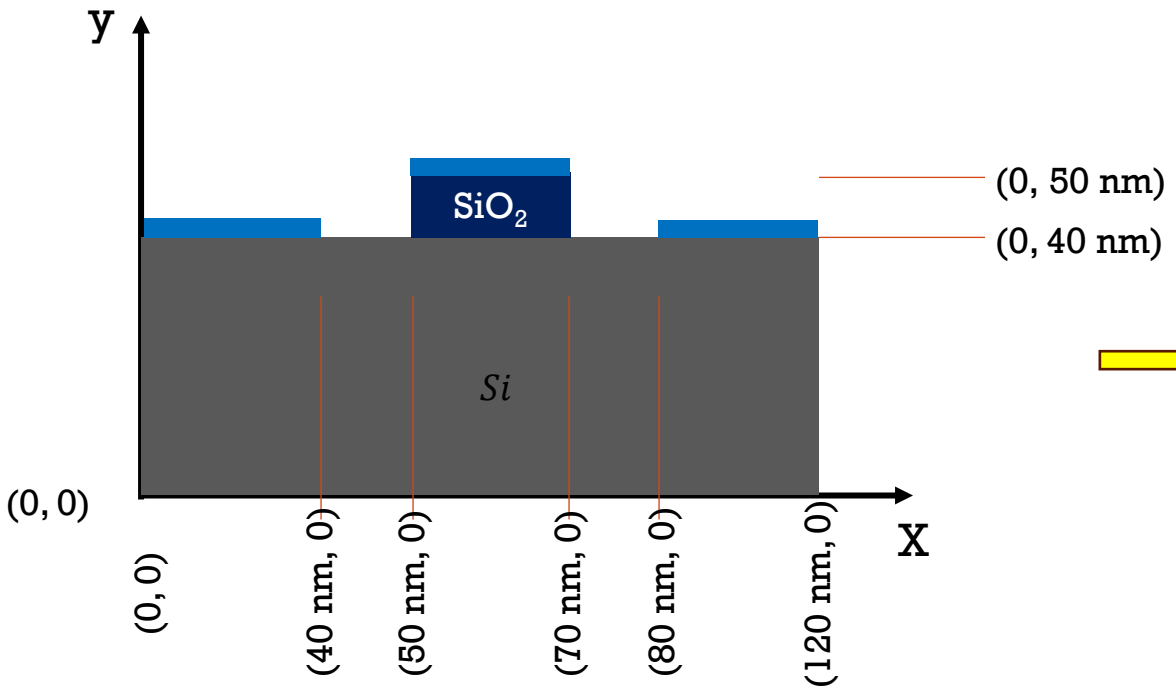
2D MOSFET structure (figure/added parameters/co-ordinates)



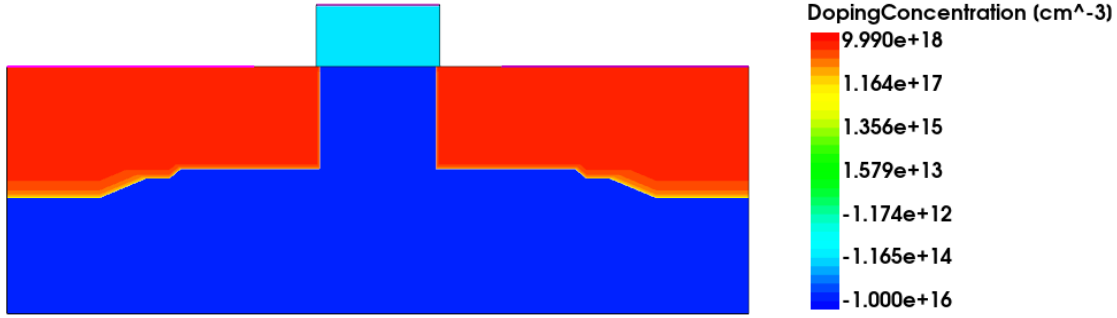
2D MOSFET structure (figure/parameters/co-ordinates/ -> added contact)

SENTAURUS TCAD MODELING – PART 2 – DOPING

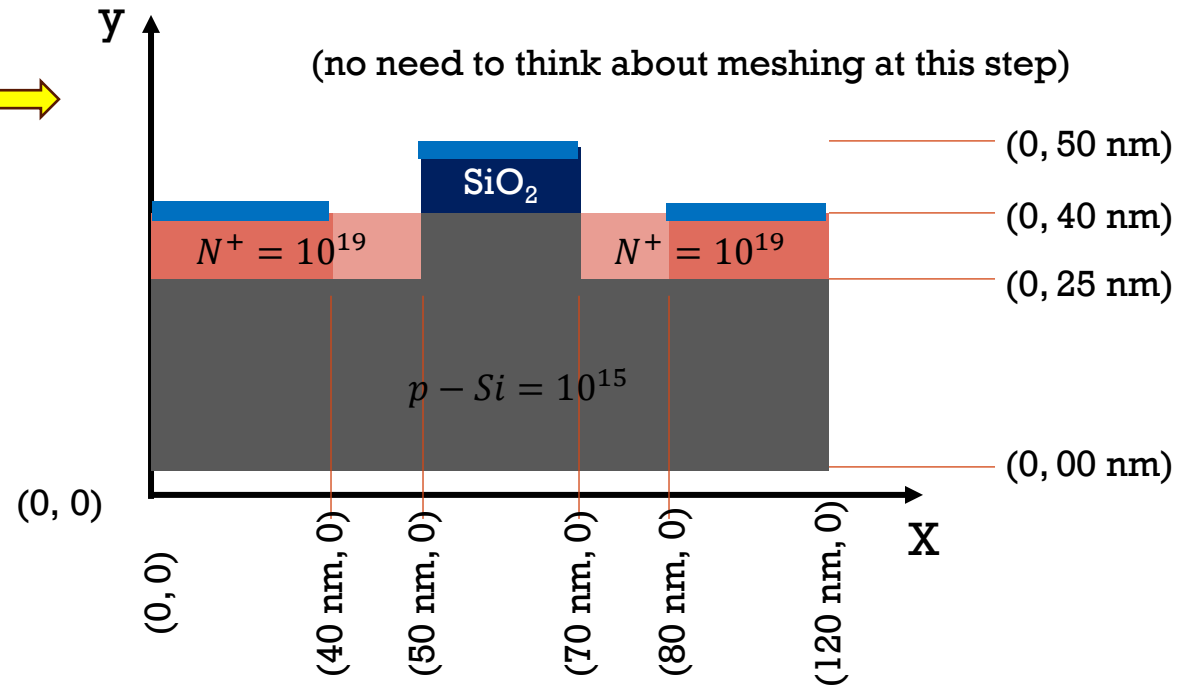
(no need to think about meshing at this step)



2D MOSFET structure (figure/parameters/co-ordinates/contact)

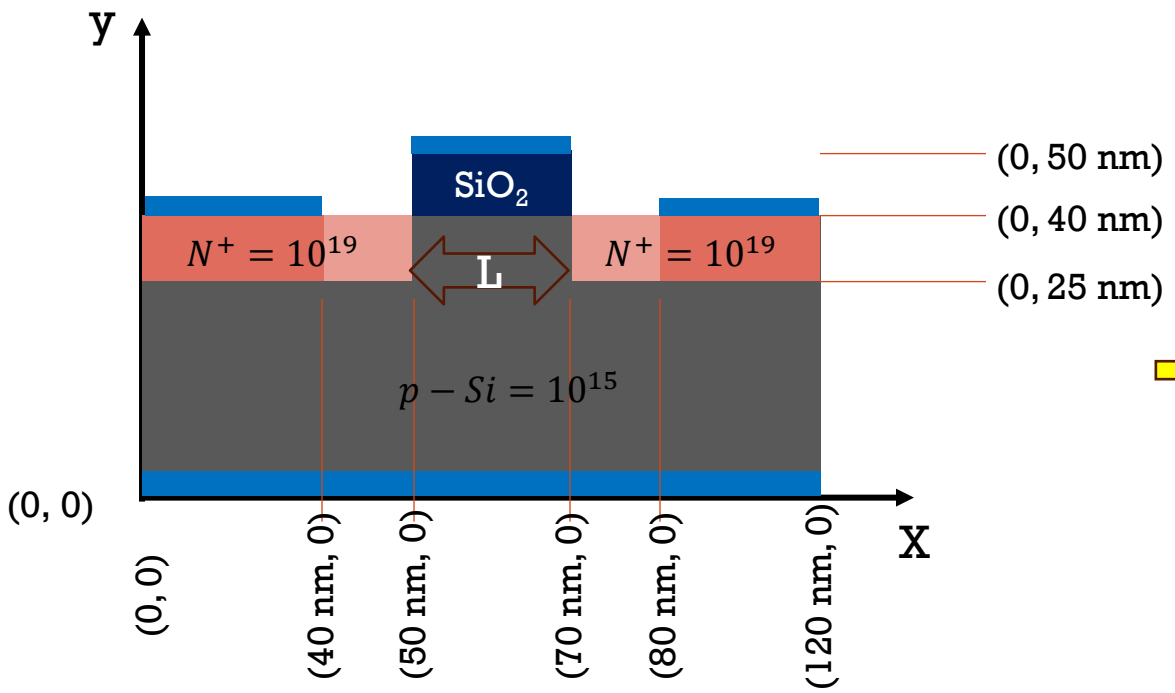


(no need to think about meshing at this step)



2D MOSFET structure (figure/ parameters/co-ordinates/contact-> added

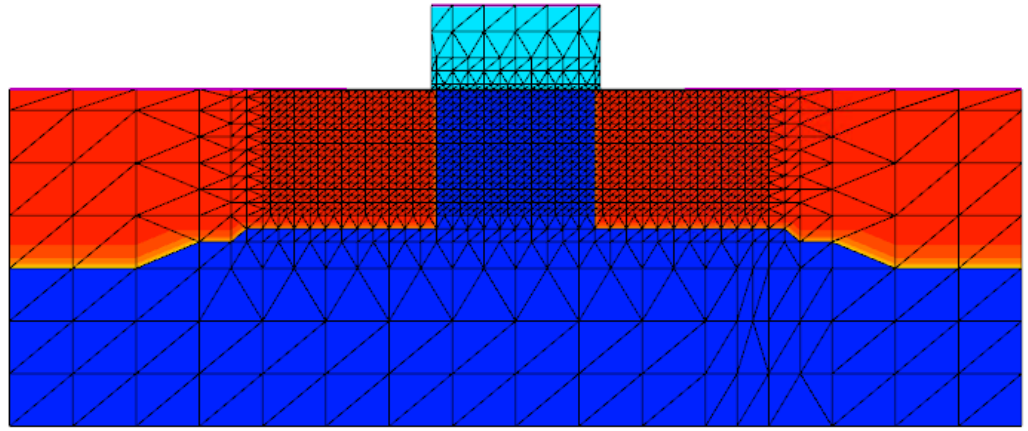
SENTAURUS TCAD MODELING – PART 3 - MESHING



2D MOSFET structure (structure + parameters/co-ordinates/contact/doping)

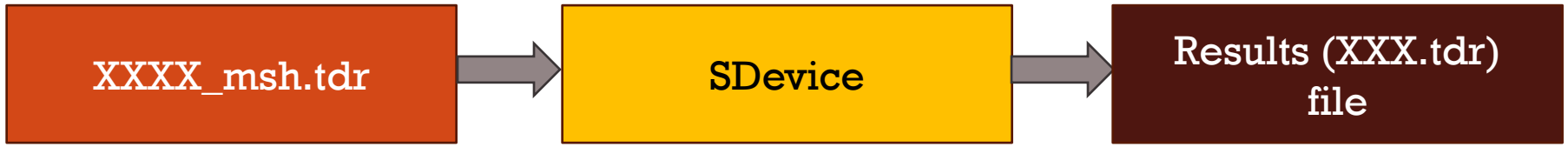
Commands:
svisual ###_msh.tdr

$N^+ = 10^{19}$



Mesh size: Si – region and gate region 10 nm, Channel region 1 nm

SENTAURUS TCAD MODELING – PART 4 - DEVICE



File generated after meshing

Provide device physics and sweep parameters (XXX.cmd) file
(create from scratch/edit from existing file – update electrodes name and sweep parameters)

Result could be viewed in SVisual tool

Commands:
sdevice ###.cmd

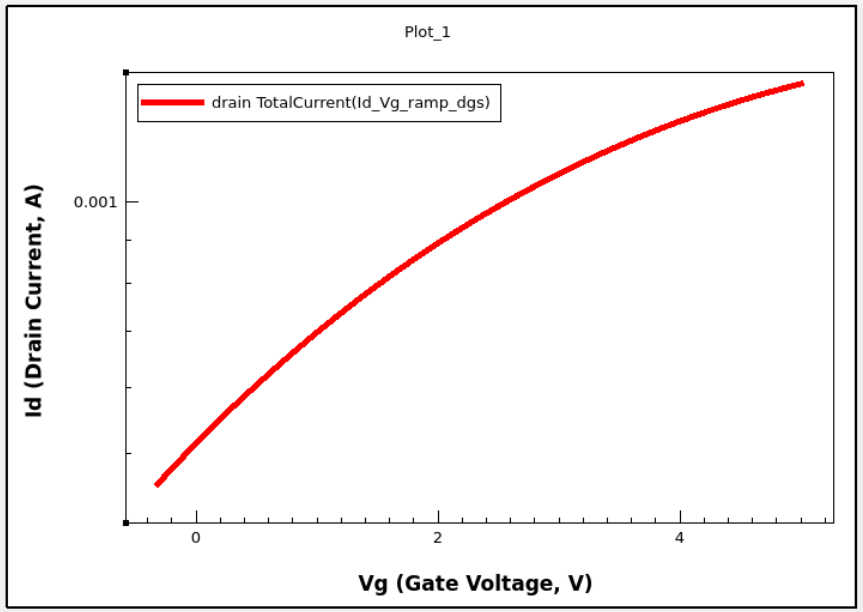
```
Solve {
    Coupled (Iterations=100000 LinesearchDamping=0.01) {Poisson}
    Coupled (Iterations=100) {Poisson Electron Hole }

    ******************************************************************
    * Zero bias plot
    ******************************************************************
    Plot(FilePrefix="Zero_Bias")

    ******************************************************************
    * Put -0.400 V on gate and 0.700 V on drain
    ******************************************************************
    NewCurrent="InitialCurrent_"
    Quasistationary (
        InitialStep=0.05 Minstep=1e-3 MaxStep=0.05 Increment=1.7
        Goal {Name="gate" Voltage=-0.400}
        Goal {Name="drain" Voltage=0.700}
    ) {
        Coupled { Poisson Electron Hole }
    }
```

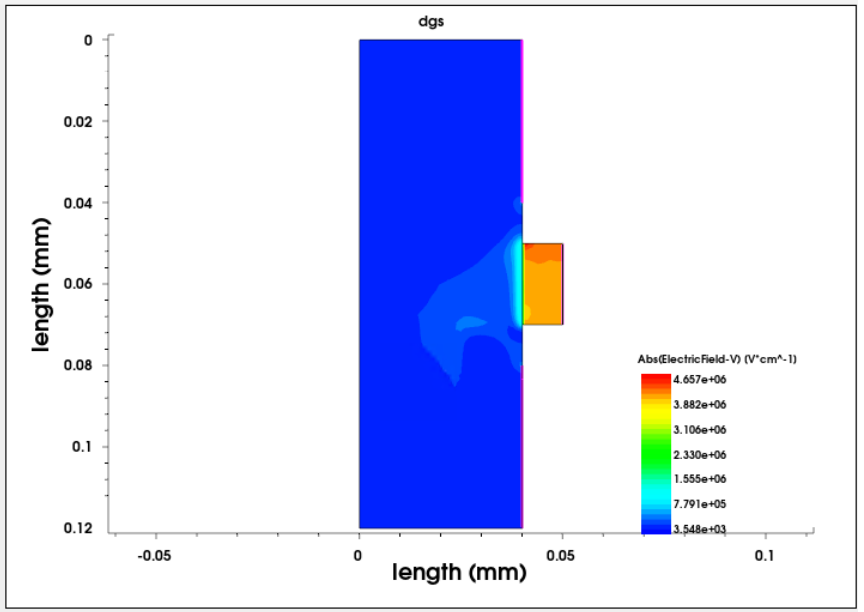
```
    ******************************************************************
    * Ramp gate to 1 V in 15 mV steps
    ******************************************************************
    NewCurrent="Id_Vg_ramp_"
    Quasistationary (
        InitialStep=0.03 Minstep=0.015 MaxStep=0.015 Increment=1
        Goal {Name="gate" Voltage=1}
    ) {
        Coupled {Poisson Electron Hole }
        Plot(FilePrefix="Gateramp_" NoOverWrite Time=(Range=(-0.250 1.0) Intervals=10))
    }
}
```

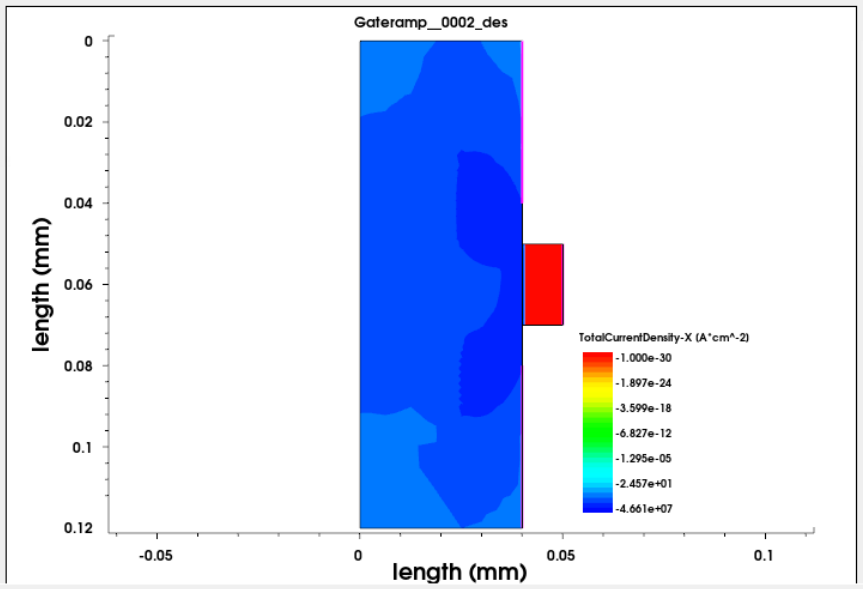
Sdevice generates a few .tdr files during each iteration
- Plotting these files helps to understand how the device is behaving

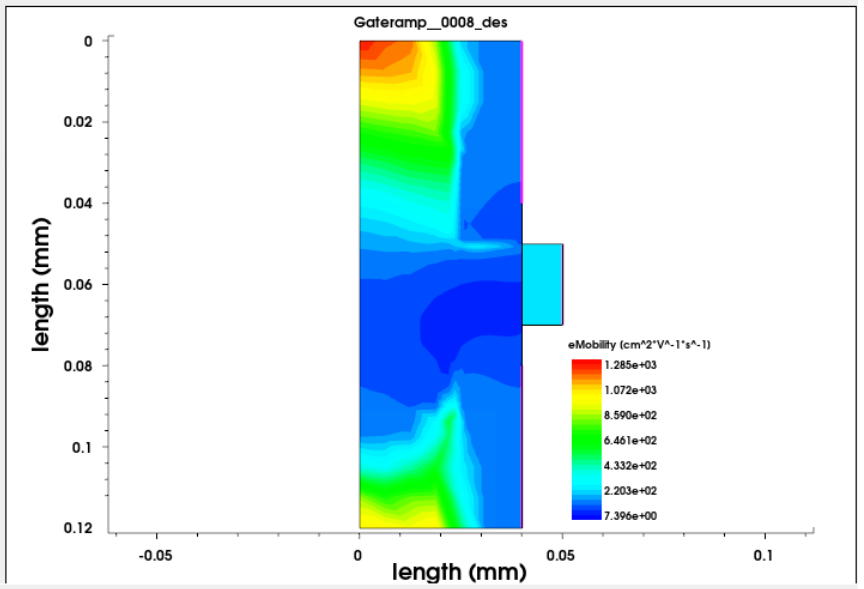
- xxx.cmd file will be provided for editing and running!

SENTAURUS TCAD MODELING – PART 5 - RESULTS







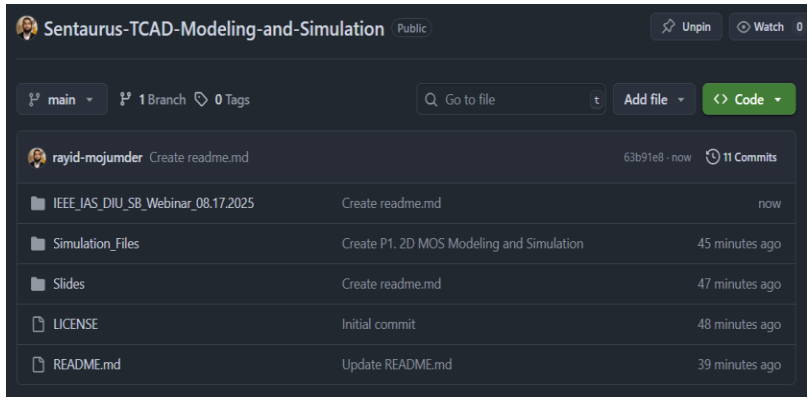


SENTAURUS TCAD MODELING – DEMONSTRATION

For full video – follow attached Youtube Channel link

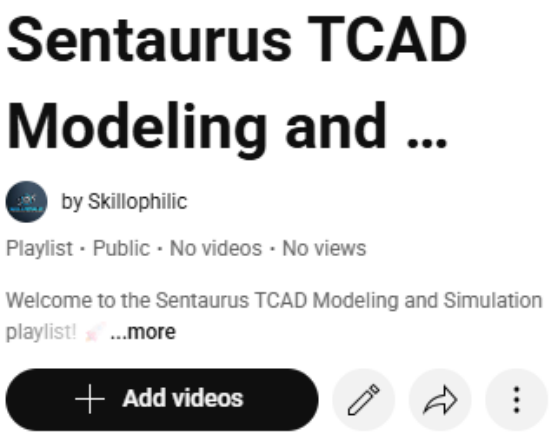
MATERIALS & RESOURCES

- Follow GitHub Repository for accessing the Slides and Simulation files shown here:



- https://github.com/rayid-mojumder/Sentaurus-TCAD-Modeling-and-Simulation

- Follow YouTube Playlist for full TCAD tutorial list (beginner to intermediate level) (in-progress):

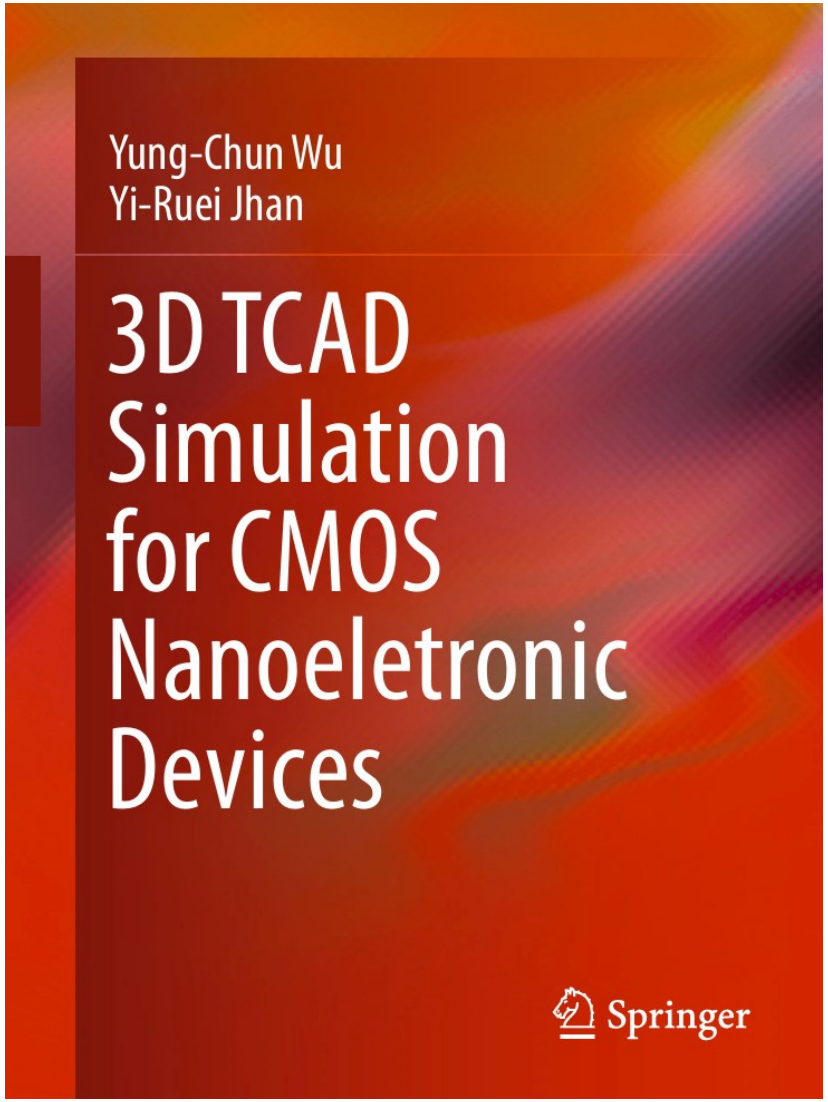


- https://youtube.com/playlist?list=PLSm7ZQMDqBcdGek5XmNanFV-JLpHOxE_o&feature=shared

NEXT STEPS

Go from absolute beginner to advanced level (Chapter-wise) [easy to follow book chapters]:

- Introduction of Synopsys Sentaurus TCAD Simulation
- 2D MOSFET Simulation (related to what we learnt here!)
- 3D FinFET with Lg = 15 nm and Lg = 10 nm Simulation
- Inverter and SRAM of FinFET with Lg = 15 nm Simulation
- Gate-All-Around (GAA) NWFET with Lg = 10 nm Simulation
- Junctionless FET with Lg = 10 nm Simulation
- Steep Slope Tunnel FET Simulation
- Extremely Scaled Si and Ge to Lg = 3-nm FinFETs and Lg = 1-nm Ultra-Thin Body Junctionless FET Simulation



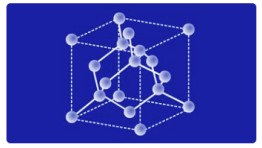
MORE LEARNING RESOURCES

- Semiconductor materials and device (foundation courses) – free (BEST COURSES out there!)

Semiconductor Fundamentals

From smartphones to satellites, semiconductors are everywhere. Tying together physics, chemistry, and electrical engineering, this course provides the essential foundations required to understand the operation of semiconductor devices such as transistors, diodes, solar cells, light-emitting devices, and more.

light emitting diodes (LED) · nanoelectronics · nanoHUB-U · NCN Group - Nanoelectronics · NCN Group - Semiconductor Device Physics · semiconductor physics · semiconductors · solar cells · transistors

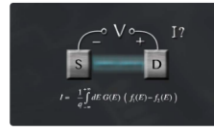


https://nanohub.org/courses/SFUN/

nanoHUB-U: Fundamentals of Nanoelectronics - Part A: Basic Concepts, 2nd Edition

Basic Concepts presents key concepts in nanoelectronics and mesoscopic physics and relates them to the traditional view of electron flow in solids.

Boltzmann Transport Equation (BTE) · bottom up approach · Capacitance · conductance · density of states · Drude formula · electrostatics · Landauer · nanoHUB-U · nanotransistors · NCN Group - Nanoelectronics · quantum capacitance · quasi-Fermi levels · Seebeck coefficient · Shannon entropy · thermoelectricity/thermoelectrics



https://nanohub.org/courses/FON1

- Learn Semiconductor Design ($20), and/or Get free Virtual Fabrication (cleanroom) experience (Free)

SYNOPSYS ACADEMIC & RESEARCH ALLIANCES · PURDUE UNIVERSITY

Introducing:

https://shorturl.at/Xkbt7

https://shorturl.at/4OfIt

ACKNOWLEDGEMENT

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- Prof. Muhammad Hussain, Purdue University – for developing courses like Semiconductor Design 101 and Semiconductor Fabrication 101
- NanoHub, Purude University – for providing free access to excellent semiconductor device courses

QUESTION / ANSWER(S)