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| **Project:** | | | | Project Name | | | | | | |
| **Customer:** | | | | Customer Name | | | | **Review date:** | yy-mm-dd | |
|  | | | | | | | | | | |
| **Object to be reviewed:** | | | | | | | | | | |
| Document name: | | | Project\_Software\_Module\_Unit\_Design | | | | | | | |
| Version: | | | 1.0 | | | | | | | |
|  | | | | | | | | | | |
| **Participants:** | | | | | **Name** | | | **Org. unit** | | **Review manager**  **(x)** |
| Person responsible (author): | | | | | Gil-Dong, Hong | | | R&D | | x |
| SW Project Manager: | | | | |  | | |  | |  |
| SW Architect: | | | | |  | | |  | |  |
| Reviewer: | | | | |  | | |  | |  |
| Reviewer: | | | | |  | | |  | |  |
| Other reviewer(s): | | | | |  | | |  | |  |
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| **Review type:** | | | | | | | | | **Project status:** | |
|  | |  | |  | |  |  |  | Phase: |  |
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| **Last review of the object to be reviewed:** | | | | | | | | | | |
| Performed on: |  | | | | | | | | | |
| Doc. name: |  | | | | | | | | | |
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| **Follow Up:** | | | | | | | | | | |
|  | |  | | | | | | | Date: |  |
|  | |  | | | | | | | Date: |  |

| **Checklist 'Review Meeting'** | **OK?** | | **Action/comments** |
| --- | --- | --- | --- |
| **yes** | **no** |
| Are cross-references implemented to the best knowledge? |  |  | If this checklist is not applicable, you should leave comment and 'NA'.  If you have comment then you should leave comment at this. |
| Was the respective analysis review completed successfully? |  |  |  |
| Is the design comprehensible? |  |  |  |
| Is the design unambiguous and complete for coding the module? |  |  |  |
| Is a list of abbreviations available? Does it contain all module specific abbreviations used? |  |  |  |
| Is the documentation of the changes up-to-date? |  |  |  |
| Is the call tree of the (C-) functions documented? |  |  |  |
| Have safety-critical functions been denoted with their ASIL level? |  |  |  |
| Have potential module specific risks been detected and rated accordingly? |  |  |  |
| Does the module design match the SW architecture? |  |  |  |
| Has the module class been defined? |  |  |  |
| Are all interfaces in line with the SW architecture design? |  |  |  |
| Are only functionalities used that are adequate for the module’s layer (meaning the level of hardware abstraction (driver, handler, application)).  Example: Are input / output ports neither read nor set outside the driver layer? |  |  |  |
| Do the names conform to the requested standards? |  |  |  |
| Are all names of functions, constants and variables comprehensible? Do they meet the requirements of the applied (coding-)styleguides? |  |  |  |
| Were any global variables applied unnecessarily? |  |  |  |
| Does the module under review contain global data that is not protected by access functions? |  |  |  |
| Were specifications regarding processing speed and timing taken into account, if applicable? |  |  |  |
| Is the problem of pre-set time limit excesses approached? Were appropriate corrective actions provided? |  |  |  |
| Are time outs or a specified cancellation in case of a fault designated to all event-dependent parts of the program? |  |  |  |
| Are the calculations precise enough? |  |  |  |
| Do the calculations necessarily have to be that precise? |  |  |  |
| Were reused modules or (C-) functions checked for their correct application prior to usage for the current project? Were necessary modifications examined and implemented, if applicable? |  |  |  |
| Is the initialisation carried out for all variables, constants and pointers? |  |  |  |
| Were value ranges, units, resolutions and default settings of variables specified? |  |  |  |
| Do all (C-) functions serve a clearly defined purpose? Are there no redundancies between the functionalities of the (C-) functions? |  |  |  |
| Have interfaces been designed with respect to minimal coupling? |  |  |  |
| Were the implemented algorithms chosen according to their efficiency (e.g. time and memory)? |  |  |  |
| Are modifications regarding origin and implementation easily retraceable? (→Are all specifications of change management strictly adhered to?) |  |  |  |
| Are only defined input values accepted for further processing? |  |  |  |
| Were modifications in comparison to the analysis documented and explained? |  |  |  |
| Does the design also comprise a defined reaction on known hardware and software errors, where applicable (e.g. wrong calculations, hardware faults, clock interrupts, I/O errors ...)? |  |  |  |
| Did you provide a specification text for => every module, operation and variable? |  |  |  |
| Did you use a project specific template for the specification text of every operation, module and variable? |  |  |  |

|  | **Complaint / fault** | | | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **No** | **Page / Line** | **Issue** | **Safety**  **relevant** | | **Action** | | | |
| **yes** | **no** | **Solution** | **Responsible person** | **Completion deadline** | **Done**  **(🗸)** |
| 1 | 15/20 | There is no diagram for explian of module. |  | x | Add diagram for module. | Gil-Dong, Hong | yy-mm-dd | **🗸** |
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