Memories

SAED_EDK32/28_RAM

DATABOOK

Document #: SAED_EDK32/28_RAM
Revision : b.1.0.0
Technology : SAED32/28nm
Process : SAED32/28nm 1P9M 1.05v/1.8v/2.5v

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1. Set of Memories SAED_EDK32/28_RAM

1.1. Introduction

This Databook describes possibilities, peculiarities of SAED_EDK32/28_RAM set of memories and technical parameters of separate cells included in it. It is one of the components of SAED_EDK32/28 Educational Design Kit (EDK).

The SAED_EDK32/28_RAM set of memories is designed using SAED32/28nm 1P9M 1.05V/1.8V/2.5V process. It represents a set of several static RAMs (SRAMs) with small number of words (word depth - m) and bits in word (data width - n). All SRAMs, included in SAED_EDK32/28_RAM, represent Synchronous Dual-Port or Single-port SRAM with Write Enable, Output Enable, Chip Select port(s). Each SRAM**p**RW**nxw**, included in the set, have the same architecture and differ from the rest with its number of words and word size (nxw) sizes and number of Read/Write access ports (p). As SAED_EDK32/28_RAM is anticipated for the use of educational purposes, only SRAMs of the sizes, shown in Table 1.1., are included in it.

Table 1.1. SRAMpRWnxw Cell List

No	Data width (n)	Word depth (m)	Address width ($k=\log_2 m$)	Read/Write access ports	Cell Name
1	4	16	4	2	SRAM2RW16x4
2	4	32	5	2	SRAM2RW32x4
3	4	64	6	2	SRAM2RW64x4
4	4	128	7	2	SRAM2RW128x4
5	8	16	4	2	SRAM2RW16x8
6	8	32	5	2	SRAM2RW32x8
7	8	64	6	2	SRAM2RW64x8
8	8	128	7	2	SRAM2RW128x8
9	16	16	4	2	SRAM2RW16x16
10	16	32	5	2	SRAM2RW32x16
11	16	64	6	2	SRAM2RW64x16
12	16	128	7	2	SRAM2RW128x16
13	32	16	4	2	SRAM2RW16x32
14	32	32	5	2	SRAM2RW32x32
15	32	64	6	2	SRAM2RW64x32
16	32	128	7	2	SRAM2RW128x32
17	8	128	7	1	SRAM1RW128x8
18	32	64	6	1	SRAM1RW64x32
19	22	32	5	2	SRAM2RW32x22
20	39	32	5	2	SRAM2RW32x39
21	32	256	8	1	SRAM1RW256x32
22	8	1024	10	1	SRAM1RW102x84
23	8	512	9	1	SRAM1RW512x8
24	48	128	7	1	SRAM1RW128x48
25	50	32	5	1	SRAM1RW32x50
26	34	64	6	1	SRAM1RW64x34
27	46	256	8	1	SRAM1RW256x46
28	46	128	7	1	SRAM1RW128x46
29	8	64	6	1	SRAM1RW64x8
30	128	64	6	1	SRAM1RW64x128
31	128	256	8	1	SRAM1RW256x128
32	8	256	8	1	SRAM1RW256x8
33	48	256	8	1	SRAM1RW256x48
34	128	512	9	1	SRAM1RW512x128
35	32	512	9	1	SRAM1RW512x32

1.2. General Information

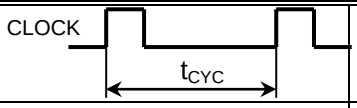
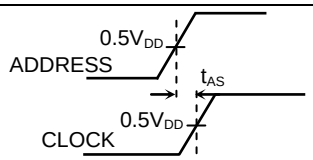
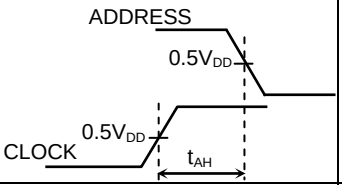
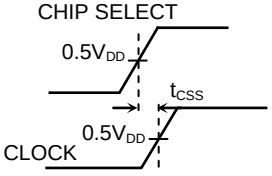
The Synchronous Dual-Port SRAMpRWnxw have two ports (Primary and Dual) for the same memory location. Both ports can be independently accessed for read or write operations. Single-port cells have only one port.
The used symbols of SRAMpRWnxw states are shown in Table 1.2.

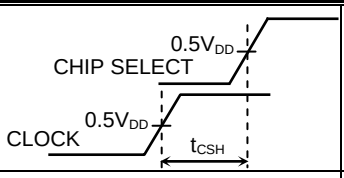
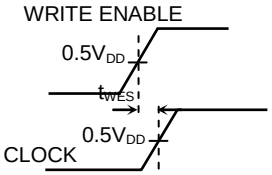
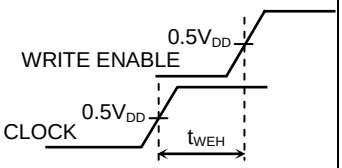
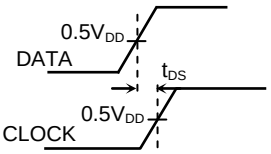
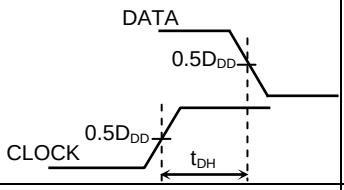
Table 1.2. Symbols of SRAMpRWnxw states

Symbol	State
L (“0”)	LOW Logic Level
H (“1”)	HIGH Logic Level
Z	High-impedance State
LH (“0”→”1”)	LOW to HIGH Transition
HL (“1”→”0”)	HIGH to LOW Transition
X	Either HIGH or LOW Logic Level

Parameters and measurement conditions of SRAMpRWnxw, included in SAED_EDK32/28_RAM set of memories, are shown in Table 1.3.

Table 1.3. Parameters and measurement conditions of SRAMpRWnxw

No	Parameter	Unit	Symbol	Figure	Definition
Timing parameters					
1	Cycle time	ns	t_{CYC}		The amount of time between two sequential active edges of clock signal
2	Access time	ns	t_A	None	The amount of time between applying Write/Read Enable signal and obtaining Access to Data in Memory
3	Address setup	ns	t_{AS}		The minimum amount of time in which the address to a SRAMpRWnxw must be stable before the active edge of the clock occurs
4	Address hold	ns	t_{AH}		The minimum amount of time in which the address to a SRAMpRWnxw must remain stable after the active edge of the clock has occurred
5	Chip select setup	ns	t_{CSS}		The minimum amount of time in which the Chip select signal to a SRAMpRWnxw must be stable before the active edge of the clock occurs

No	Parameter	Unit	Symbol	Figure	Definition
6	Chip select hold	ns	t_{CSH}		The minimum amount of time in which the Chip select signal to a SRAMpRWnxw must remain stable after the active edge of the clock has occurred
7	Write enable setup	ns	t_{WES}		The minimum amount of time in which the Write enable signal to a SRAMpRWnxw must be stable before the active edge of the clock occurs
8	Write enable hold	ns	t_{WEH}		The minimum amount of time in which the Write enable signal to a SRAMpRWnxw must remain stable after the active edge of the clock has occurred
9	Data setup	ns	t_{DS}		The minimum amount of time in which the input data to a SRAMpRWnxw must be stable before the active edge of the clock occurs
10	Data hold	ns	t_{DH}		The minimum amount of time in which the input data to a SRAMpRWnxw must remain stable after the active edge of the clock has occurred
11	Output Z state entry time	ns	t_{OZ}	None	The amount of time that takes the outputs to change to Z state after output enable signal is applied
12	Output Z state exit time	ns	t_{ZO}	None	The amount of time that takes the outputs to exit from Z state after output enable signal is applied
			Power parameters		
13	AC current	mA	i_{AC}	None	Average value of dynamic current for read/write operations
14	Read AC current	mA	i_{ACR}	None	Dynamic current for read operation
15	Write AC current	mA	i_{ACW}	None	Dynamic current for write operation
16	Peak current	mA	i_{ACP}	None	Maximum value of dynamic current for read/write operations
17	Deselected current	mA	i_{ACD}	None	The value of current when SRAMpRWnxw is disabled, all addresses switch and 50% of data input switch
18	Standby current	mA	i_{ACS}	None	The value of current in standby mode when all inputs and outputs are stable

1.3. Dual port SRAMs

1.3.1. Basic Pins

The Basic Pins of dual port SRAMpRWnxw are shown in Figure 6.1 and its descriptions are shown in Table 1.4.

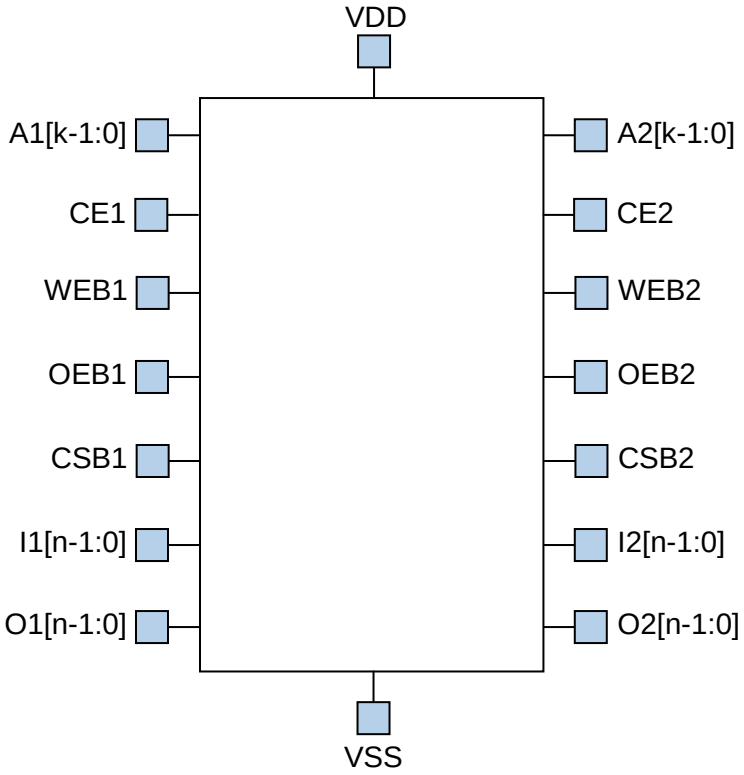


Figure 1.1. Dual port SRAMpRWnxw Basic Pins

Table 1.4. Dual port SRAMpRWnxw Pin Definition

Pin Symbol	Width (bits)	Type	Name and Function
A1	k	Input	Primary Read/Write Address
CE1	1	Input	Primary Positive-Edge Clock
WEB1	1	Input	Primary Write Enable, Active Low
OEB1	1	Input	Primary Output Enable, Active Low
CSB1	1	Input	Primary Chip Select, Active Low
I1	n	Input	Primary Input data bus
O1	n	Output	Primary Output data bus
A2	k	Input	Dual Read/Write Address
CE2	1	Input	Dual Positive-Edge Clock
WEB2	1	Input	Dual Write Enable, Active Low
OEB2	1	Input	Dual Output Enable, Active Low
CSB2	1	Input	Dual Chip Select, Active Low
I2	n	Input	Dual Input data bus
O2	n	Output	Dual Output data bus
VDD	Power supply		
VSS	Power ground		

1.3.2. Dual port SRAMpRWnxw Description

The general block-diagram of SRAMpRWnxw is shown in Figure 1.2.

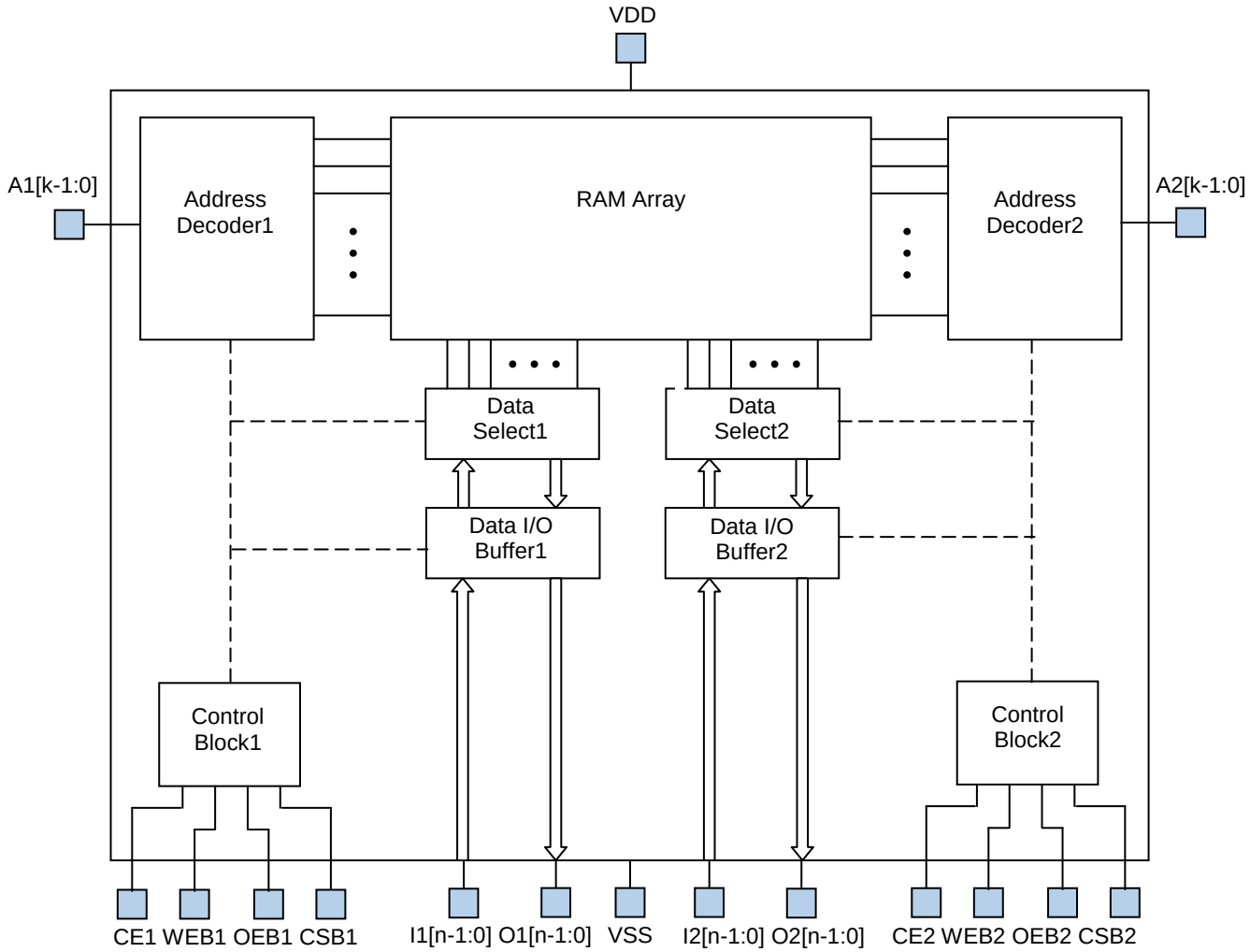


Figure 1.2. Dual port SRAMpRWnxw block diagram

Dual port SRAMpRWnxw Basic Operations is shown in Table 1.5.
Dual port SRAMpRWnxw access is synchronous and triggered by the rising edge of the clock signals (CE1, CE2). Read/Write addresses (A1, A2), Input data (I1, I2), Write enable signals (WEB1, WEB2), and Chip select signals (CSB1, CSB2) are latched by the rising edge of the clocks (CE1, CE2).
The value of Chip Select signal is low (CS1/CS2=0) for read/write operation. The SRAMpRWnxw enter read mode when CS1/CS2=0 and WEB1/WEB2=1. During read operations, data read from the memory location D(A1[k-1:0])/D(A2[k-1:0]) specified on the address bus I1[n-1:0]/I2[n-1:0] and appear on the data output bus O1[n-1:0]/O2[n-1:0].

Table 1.5. Dual port SRAMpRWnxw Basic Operations

Pins						Data in Memory	Access to Memory	Operation
A1[k-1:0]	WEB1	OEB1	CSB1	I1[n-1:0]	O1[n-1:0] (t+1)	D(A1[k-1:0]) (t+1)		
X	X	0	1	Disabled	O1[n-1:0] (t)	D(A1[k-1:0]) (t)	No	Standby
		1			Z			
X	0	0	0	Enabled	I1[n-1:0]	I1[n-1:0]	Yes	Write
		1			Z			
X	1	0	0	X	D(A1[k-1:0]) (t)	D(A1[k-1:0]) (t)	No	Read
		1			Z			
A2[k-1:0]	WEB2	OEB2	CSB2	I2[n-1:0]	O2[n-1:0] (t+1)	D(A2[k-1:0]) (t+1)		
X	X	0	1	Disabled	O2[n-1:0] (t)	D(A2[k-1:0]) (t)	No	Standby
		1			Z			
X	0	0	0	Enabled	I2[n-1:0]	I2[n-1:0]	Yes	Write
		1			Z			
X	1	0	0	X	D(A2[k-1:0]) (t)	D(A2[k-1:0]) (t)	No	Read
		1			Z			

Note: O1[n-1:0] (t) is the value of Primary Port Output bus in the previous moment of time, and O1[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A1[k-1:0]) (t) is the data in the RAM location specified on the address bus A1[k-1:0] in the previous moment of time, and D(A1[k-1:0]) (t+1) in the next moment of time.
O2[n-1:0] (t) is the value of Dual Port Output bus in the previous moment of time, and O2[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A2[k-1:0]) (t) is the data in the RAM location specified on the address bus A2[k-1:0] in the previous moment of time, and D(A2[k-1:0]) (t+1) in the next moment of time.

Dual port SRAMpRWnxw enter write mode when CSB1/CSB2=0 and WEB1/WEB2=0. During write mode, data on the data input bus I1[n-1:0]/I2[n-1:0] is writing into the memory location D(A1[k-1:0])/D(A2[k-1:0]) specified on the address bus I1[n-1:0]/I2[n-2:0].
If OEB1/OEB2=1, data on the output bus O1[n-1:0]/O2[n-1:0] placed in Z state. At that time read/write operation continue. When OEB1/OEB2=0, the data appear on the output bus O1[n-a:0]/O2[n-1:0].
Power dissipation is minimized using static circuit implementations. A standby mode is provided to further reduce power dissipation during periods of non-operation (CCB1/CSB2=1). While in standby mode, address and data inputs are disabled; data stored in the memory D(A1[k-1:0])/D(A2[k-1:0]) is retained, but the memory cannot be accessed for reads or writes.

Address contention occurs when both ports simultaneously access the same address. In this case, both ports read the same data.

1.3.3. Dual port SRAMpRWnxw Timing Waveforms

SRAMpRWnxw functions according to the block-diagrams shown in Figures 1.4 – 1.6.

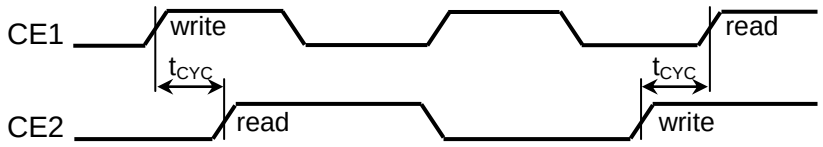


Figure 1.3. Dual port SRAMpRWnxw Write-Read Clock Timing Waveforms

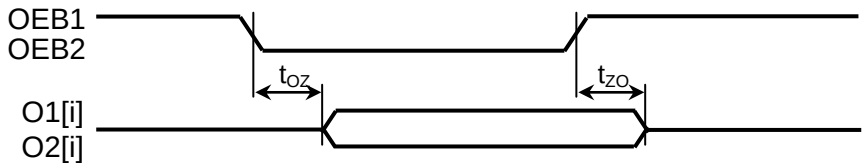


Figure 1.4. Dual port SRAMpRWnxw Output-Enable Timing Waveforms

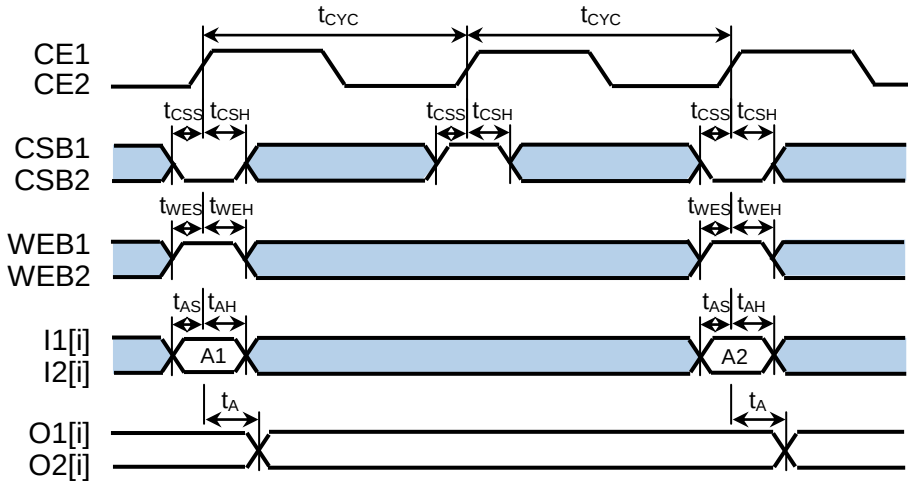


Figure 1.5. Dual port SRAMpRWnxw Read-Cycle Timing Waveforms

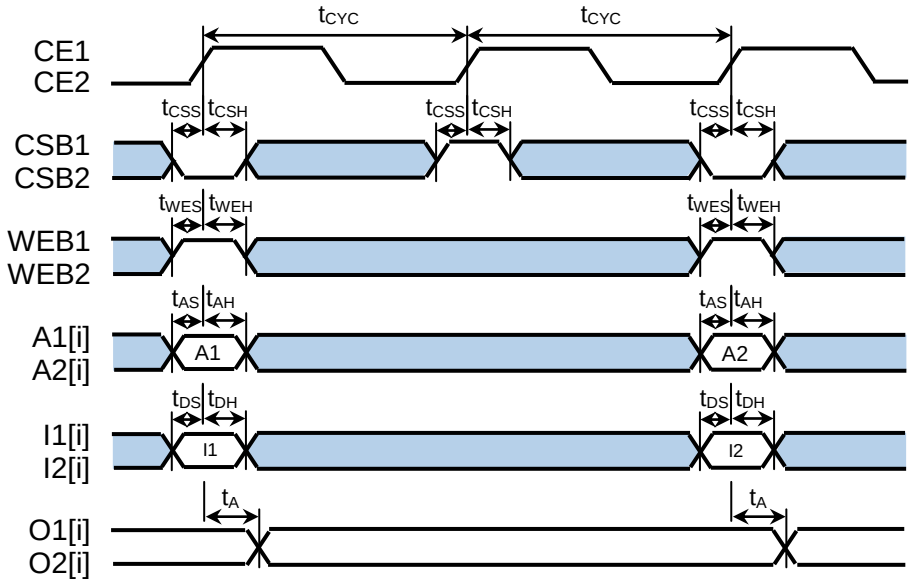


Figure 1.6. Dual port SRAMpRWnxw Write-Cycle Timing Waveforms

1.4. Single port SRAMs

1.4.1. Basic Pins

The Basic Pins of single port SRAMpRWnxw_1rw are shown in Figure 1.7 and its descriptions are shown in Table 1.6.

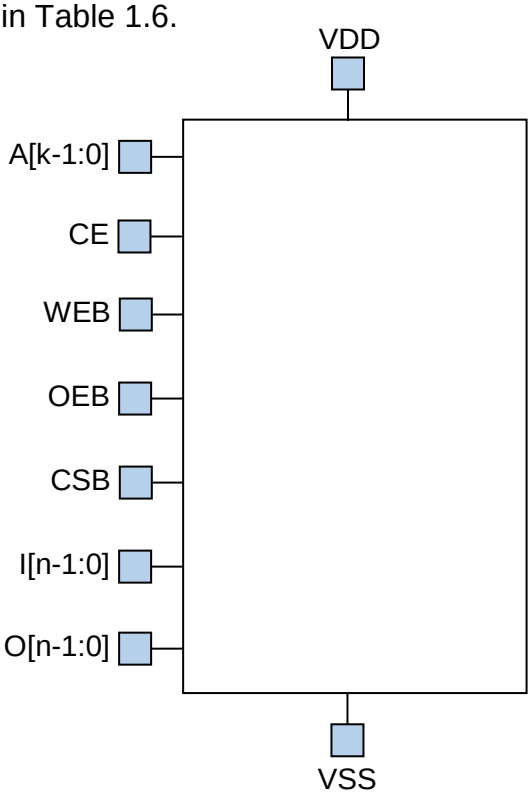


Figure 1.7. Single port SRAMpRWnxw_1rw Basic Pins

Table 1.6. Single port SRAMpRWnxw_1rw Pin Definition

Pin Symbol	Width (bits)	Type	Name and Function
A	k	Input	Primary Read/Write Address
CE	1	Input	Primary Positive-Edge Clock
WEB	1	Input	Primary Write Enable, Active Low
OEB	1	Input	Primary Output Enable, Active Low
CSB	1	Input	Primary Chip Select, Active Low
I	n	Input	Primary Input data bus
O	n	Output	Primary Output data bus
VDD	Power supply		
VSS	Power ground		

1.4.2. Single port SRAMpRWnxw_1rw Description

The general block-diagram of single port SRAMpRWnxw is shown in Figure 1.8.

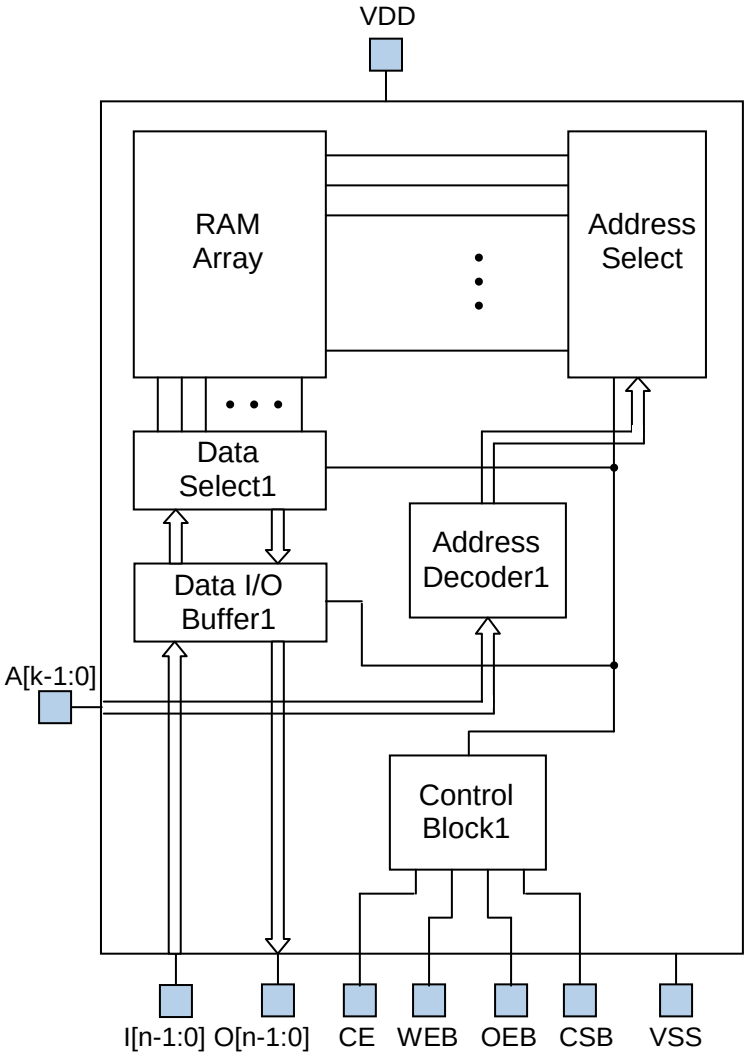


Figure 1.8. Single port SRAMpRWnxw_1rw block diagram

Single port SRAMpRWnxw_1rw Basic Operations is shown in Table 6.7.

Single port SRAMpRWnxw_1rw access is synchronous and triggered by the rising edge of the clock signals (CE). Read/Write addresses (A), Input data (I), Write enable signals (WEB), and Chip select signals (CSB) are latched by the rising edge of the clocks (CE).

The value of Chip Select signal is low (CS=0) for read/write operation. SRAM enter read mode when CS=0 and WEB=1. During read operations, data read from the memory location D(A[k-1:0]) specified on the address bus I[n-1:0] and appear on the data output bus O[n-1:0].

Table 1.7. Single port SRAMpRWnxw_1rw Basic Operations

Pins						Data in Memory	Access to Memory	Operation
A[k-1:0]	WEB	OEB	CSB	I[n-1:0]	O[n-1:0] (t+1)	D(A[k-1:0]) (t+1)		
X	X	0	1	Disabled	O[n-1:0] (t)	D(A[k-1:0]) (t)	No	Standby
		1			Z			
X	0	0	0	Enabled	I[n-1:0]	I[n-1:0]	Yes	Write
		1			Z			
X	1	0	0	X	D(A[k-1:0]) (t)	D(A[k-1:0]) (t)	No	Read
		1			Z			

Note: O[n-1:0] (t) is the value of Primary Port Output bus in the previous moment of time, and O[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A[k-1:0]) (t) is the data in the RAM location specified on the address bus A[k-1:0] in the previous moment of time, and D(A[k-1:0]) (t+1) in the next moment of time.
O[n-1:0] (t) is the value of Dual Port Output bus in the previous moment of time, and O[n-1:0] (t+1) is the value of the same bus in the next moment of time.
D(A[k-1:0]) (t) is the data in the RAM location specified on the address bus A[k-1:0] in the previous moment of time, and D(A[k-1:0]) (t+1) in the next moment of time.

Single port SRAMpRWnxw_1rw enter write mode when CSB=0 and WEB=0. During write mode, data on the data input bus I[n-1:0] is writing into the memory location D(A[k-1:0]) specified on the address bus I[n-1:0].
If OEB=1, data on the output bus O[n-1:0] placed in Z state. At that time read/write operation continue. When OEB=0, the data appear on the output bus O[n-a:0].
Power dissipation is minimized using static circuit implementations. A standby mode is provided to further reduce power dissipation during periods of non-operation (CCB=1). While in standby mode, address and data inputs are disabled; data stored in the memory D(A[k-1:0]) is retained, but the memory cannot be accessed for reads or writes.

1.4.3. Single port SRAMpRWnxw_1rw Timing Waveforms

Single port SRAMpRWnxw_1rw functions according to the block-diagrams shown in Figures 1.9 – 1.11.

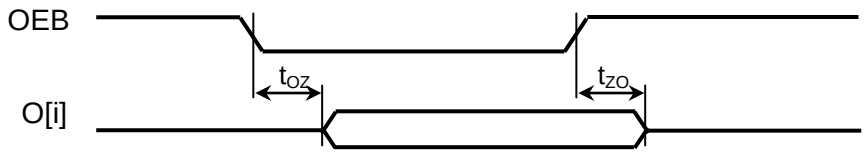


Figure 1.9. Single port SRAMpRWnxw_1rw Output-Enable Timing Waveforms

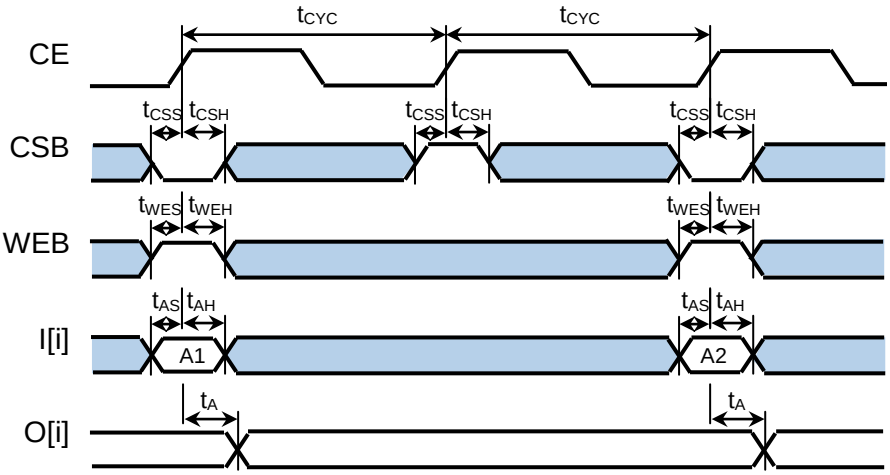


Figure 1.10. Single port SRAMpRWnxw_1rw Read-Cycle Timing Waveforms

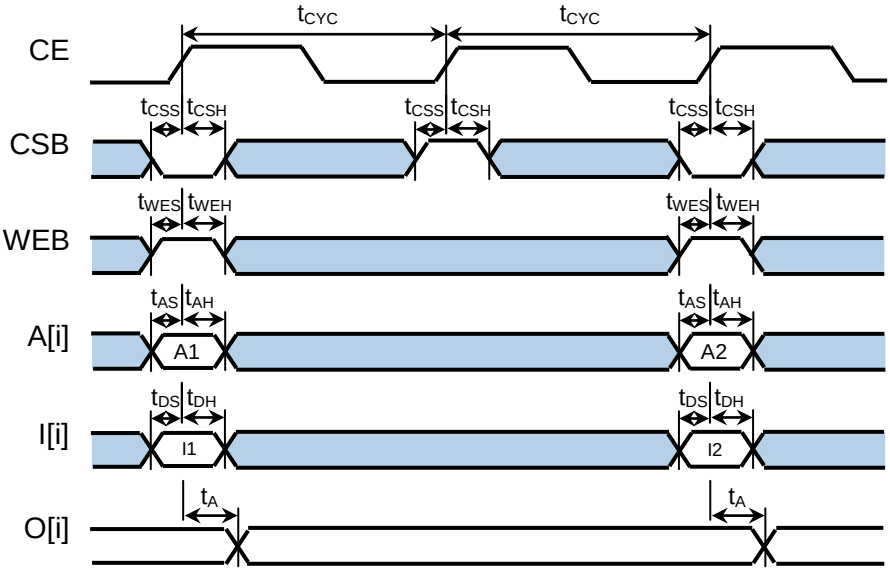


Figure 1.11. Single port SRAMpRWnxw_1rw Write-Cycle Timing Waveforms

1.5. Operating conditions

The operating conditions of SAED_EDK32/28_RAM set of memories are shown in Table 1.8.

Table 1.8. Operating conditions

Parameter	Min	Typ	Max	Units
Power supply (VDD) range	0.95	1.05	1.16	V
Operating Temperature	-40	+25	+125	°C
Operating Frequency (F)			500	MHz

1.6. Timing and Current Data

Table 1.9. SRAM Timing and Current Data

Parameter	Min	Max	Units
Cycle time (t_{CYC})	3.0		ns
Access time (t_A)		2.0	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	1.2		ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.5		ns
CSB1/CSB2 setup (t_{CSS})	1.2		ns
CSB1/CSB2 hold (t_{CSH})	0.5		ns
WEB1/WEB2 setup (t_{WES})	1.2		ns
WEB1/WEB2 hold (t_{WEH})	0.5		ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1.2		ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.5		ns
Output enable to hi-Z (t_{OZ})		2.0	ns
Output enable active (t_{ZO})		2.0	ns
AC current (i_{AC})		0.5	mA
Standby current (i_{ACS})		0.5	mA

1.7. Characterization corners

The characterization corners are shown in Table 1.10.

Table 1.10. Characterization Corners

Corner Name	Process (NMOS proc. – PMOS proc.)	Power Supply (VDD) (V)	Temperature (°C)	Library Name Suffix
FF	Fast - Fast	1.16	125	ff1p16v125c
FF	Fast - Fast	1.16	25	ff1p16v25c
FF	Fast - Fast	1.16	-40	ff1p16vn40c
SS	Slow - Slow	0.95	125	ss0p95v125c
SS	Slow - Slow	0.95	25	ss0p95v25c
SS	Slow - Slow	0.95	-40	ss0p95vn40c
TT	Typical - Typical	1.05	125	tt1p05v125c
TT	Typical - Typical	1.05	25	tt1p05v25c
TT	Typical - Typical	1.05	-40	tt1p05vn40c

Critical path, setup and hold analyses were performed for the mentioned corners.

2. Deliverables

Table 2.1. Memories deliverables

N	Type	Description
	.pdf	Databook / User guide, Layer usage file
	.db, .lib	Synthesis models
	.v	Verilog simulation models
	.tv	TetraMAX Verilog models
	.vhd	VHDL / Vital simulation models
	.cdl, .sp	LVS, HSPICE netlists
	.spf	Extracted C and RC netlists for different corners
	.gds	GDSII layout views
	.lef	LEF files
	.FRAM, .CEL	FRAM views, layout views
	.drc, .erc, .lvs	Report files

3. SRAM naming conventions

All memories in the set are named according to the following template (Fig. 3.1):

Figure 3.1. Memories naming template

The template contains symbols denoting specifics of the memory, the descriptions of the symbols are given in Table 3.1.

Table 3.1. Memories naming conventions

Symbol	Description	Values
p	Number of access ports	1,2
n	Number of words	Integer number, 2^n
w	Word size	Integer, various

4. Parameters

4.1. SRAM2RW16x4

This represents dual port static RAM which has 16 4-bit words, it has 4-bit address.

Table 4.1. SRAM2RW16x4 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.41	0.49	0.79	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.22	0.41	0.31	ns
CSB1/CSB2 setup (t_{CSS})	1.2	0.79	1.12	ns
CSB1/CSB2 hold (t_{CSH})	0.29	0.51	0.41	ns
WEB1/WEB2 setup (t_{WES})	0.31	0.41	0.21	ns
WEB1/WEB2 hold (t_{WEH})	0.1	0.39	0.19	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1.12	0.81	1.15	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.42	0.55	0.42	ns
Output enable to hi-Z (t_{OZ})	1.72	1.55	1.82	ns
Output enable active (t_{ZO})	1.9	1.19	2.1	ns
AC current (i_{AC})	0.32	0.41	0.15	mA
Standby current (i_{ACS})	0.041	0.049	0.031	mA
Area	2337			um^2

4.2. SRAM2RW32x4

This represents dual port static RAM which has 32 4-bit words, it has 5-bit address

Table 4.2. SRAM2RW32x4 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.39	0.51	0.82	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.21	0.39	0.32	ns
CSB1/CSB2 setup (t_{CSS})	1.15	0.81	1.15	ns
CSB1/CSB2 hold (t_{CSH})	0.35	0.55	0.39	ns
WEB1/WEB2 setup (t_{WES})	0.32	0.41	0.25	ns
WEB1/WEB2 hold (t_{WEH})	0.15	0.39	0.25	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1.15	0.79	1.15	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.43	0.52	0.42	ns
Output enable to hi-Z (t_{OZ})	1.71	1.52	1.82	ns
Output enable active (t_{ZO})	1.92	1.25	2.2	ns
AC current (i_{AC})	0.41	0.55	0.35	mA
Standby current (i_{ACS})	0.045	0.05	0.38	mA
Area	2337			um^2

4.3. SRAM2RW64x4

This represents dual port static RAM which has 64 4-bit words, it has 6-bit address

Table 4.3. SRAM2RW64x4 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.39	0.55	0.85	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.25	0.42	0.33	ns
CSB1/CSB2 setup (t_{CSS})	1.15	0.83	1.13	ns
CSB1/CSB2 hold (t_{CSH})	0.32	0.55	0.42	ns
WEB1/WEB2 setup (t_{WES})	0.34	0.42	0.25	ns
WEB1/WEB2 hold (t_{WEH})	0.15	0.39	0.24	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1.1	0.79	1.15	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.43	0.52	0.43	ns
Output enable to hi-Z (t_{OZ})	1.69	1.52	1.79	ns
Output enable active (t_{ZO})	1.88	1.19	2.1	ns
AC current (i_{AC})	0.65	0.65	0.52	mA
Standby current (i_{ACS})	0.055	0.06	0.04	mA
Area	4371			um^2

4.4. SRAM2RW128x4

This represents dual port static RAM which has 128 4-bit words, it has 7-bit address

Table 4.4. SRAM2RW128x4 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.41	0.55	0.82	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.23	0.42	0.35	ns
CSB1/CSB2 setup (t_{CSS})	1.15	0.82	1.13	ns
CSB1/CSB2 hold (t_{CSH})	0.31	0.5	0.4	ns
WEB1/WEB2 setup (t_{WES})	0.32	0.41	0.25	ns
WEB1/WEB2 hold (t_{WEH})	0.15	0.42	0.22	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1.15	0.82	1.15	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.42	0.53	0.45	ns
Output enable to hi-Z (t_{OZ})	1.69	1.49	1.81	ns
Output enable active (t_{ZO})	1.92	1.22	2.1	ns
AC current (i_{AC})	0.82	0.85	0.54	mA
Standby current (i_{ACS})	0.05	0.05	0.041	mA
Area	7064			um^2

4.5. SRAM2RW16x8

This represents dual port static RAM which has 16 8-bit words, it has 4-bit address

Table 4.5. SRAM2RW16x8 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.39	0.54	0.81	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.25	0.42	0.31	ns
CSB1/CSB2 setup (t_{CSS})	1.1	0.79	1.11	ns
CSB1/CSB2 hold (t_{CSH})	0.31	0.52	0.41	ns
WEB1/WEB2 setup (t_{WES})	0.32	0.41	0.25	ns
WEB1/WEB2 hold (t_{WEH})	0.12	0.42	0.22	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1.1	0.79	1.15	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.43	0.52	0.41	ns
Output enable to hi-Z (t_{OZ})	1.71	1.52	1.83	ns
Output enable active (t_{ZO})	1.89	1.25	2.1	ns
AC current (i_{AC})	0.9	1.5	0.65	mA
Standby current (i_{ACS})	0.04	0.05	0.03	mA
Area	2337			um^2

4.6. SRAM2RW32x8

This represents dual port static RAM which has 32 8-bit words, it has 5-bit address

Table 4.6. SRAM2RW32x8 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.42	0.51	0.83	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.19	0.39	0.29	ns
CSB1/CSB2 setup (t_{CSS})	0.9	0.82	1.15	ns
CSB1/CSB2 hold (t_{CSH})	0.33	0.54	0.46	ns
WEB1/WEB2 setup (t_{WES})	0.32	0.41	0.22	ns
WEB1/WEB2 hold (t_{WEH})	0.11	0.42	0.21	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1	0.79	1.12	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.43	0.55	0.44	ns
Output enable to hi-Z (t_{OZ})	1.71	1.51	1.81	ns
Output enable active (t_{ZO})	1.89	1.22	1.51	ns
AC current (i_{AC})	1	1.32	1.83	mA
Standby current (i_{ACS})	0.7	0.75	0.54	mA
Area	3724			um^2

4.7. SRAM2RW64x8

This represents dual port static RAM which has 64 8-bit words, it has 6-bit address

Table 4.7. SRAM2RW64x8 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.44	0.51	0.81	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.21	0.43	0.32	ns
CSB1/CSB2 setup (t_{CSS})	1.05	0.82	1.12	ns
CSB1/CSB2 hold (t_{CSH})	0.33	0.52	0.43	ns
WEB1/WEB2 setup (t_{WES})	0.32	0.41	0.23	ns
WEB1/WEB2 hold (t_{WEH})	0.1	0.42	0.24	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	0.9	0.81	1.12	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.42	0.55	0.44	ns
Output enable to hi-Z (t_{OZ})	1.72	1.51	1.84	ns
Output enable active (t_{ZO})	2	1.3	1.54	ns
AC current (i_{AC})	1.1	1.56	1.83	mA
Standby current (i_{ACS})	0.72	0.78	0.65	mA
Area	5394			um^2

4.8. SRAM2RW128x8

This represents dual port static RAM which has 128 8-bit words, it has 7-bit address

Table 4.8. SRAM2RW128x8 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.39	0.51	0.82	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.19	0.44	0.31	ns
CSB1/CSB2 setup (t_{CSS})	1.1	0.82	1.15	ns
CSB1/CSB2 hold (t_{CSH})	0.31	0.52	0.43	ns
WEB1/WEB2 setup (t_{WES})	0.32	0.44	0.21	ns
WEB1/WEB2 hold (t_{WEH})	0.16	0.42	0.22	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1.1	0.79	1.12	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.43	0.52	0.44	ns
Output enable to hi-Z (t_{OZ})	1.75	1.54	1.84	ns
Output enable active (t_{ZO})	1.91	1.22	1.53	ns
AC current (i_{AC})	1.25	1.82	1.1	mA
Standby current (i_{ACS})	0.9	1.3	0.5	mA
Area	8679			um^2

4.9. SRAM2RW16x16

This represents dual port static RAM which has 16 16-bit words, it has 4-bit address

Table 4.9. SRAM2RW16x16 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.42	0.52	0.82	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.22	0.41	0.31	ns
CSB1/CSB2 setup (t_{CSS})	1.05	0.82	1.15	ns
CSB1/CSB2 hold (t_{CSH})	0.32	0.54	0.44	ns
WEB1/WEB2 setup (t_{WES})	0.33	0.45	0.25	ns
WEB1/WEB2 hold (t_{WEH})	0.15	0.42	0.23	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1.1	0.82	1.14	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.44	0.55	0.43	ns
Output enable to hi-Z (t_{OZ})	1.72	1.53	1.81	ns
Output enable active (t_{ZO})	2	1.25	1.59	ns
AC current (i_{AC})	2.05	2.49	1.69	mA
Standby current (i_{ACS})	1.2	1.5	1	mA
Area	4284			um^2

4.10. SRAM2RW32x16

This represents dual port static RAM which has 32 16-bit words, it has 5-bit address

Table 4.10. SRAM2RW32x16 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.42	0.53	0.81	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.25	0.42	0.32	ns
CSB1/CSB2 setup (t_{CSS})	1.1	0.82	1.14	ns
CSB1/CSB2 hold (t_{CSH})	0.32	0.53	0.44	ns
WEB1/WEB2 setup (t_{WES})	0.33	0.42	0.22	ns
WEB1/WEB2 hold (t_{WEH})	0.15	0.44	0.25	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1	0.85	1.14	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.44	0.55	0.44	ns
Output enable to hi-Z (t_{OZ})	1.74	1.52	1.84	ns
Output enable active (t_{ZO})	2	1.25	1.9	ns
AC current (i_{AC})	2.1	2.55	1.72	mA
Standby current (i_{ACS})	0.4	0.5	0.28	mA
Area	5377			um^2

4.11. SRAM2RW64x16

This represents dual port static RAM which has 64 16-bit words, it has 6-bit address

Table 4.11. SRAM2RW64x16 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.41	0.51	0.82	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.23	0.42	0.33	ns
CSB1/CSB2 setup (t_{CSS})	1.1	0.82	1.15	ns
CSB1/CSB2 hold (t_{CSH})	0.32	0.55	0.44	ns
WEB1/WEB2 setup (t_{WES})	0.31	0.41	0.19	ns
WEB1/WEB2 hold (t_{WEH})	0.15	0.39	0.2	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1	0.85	1.12	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.43	0.52	0.44	ns
Output enable to hi-Z (t_{OZ})	1.71	1.51	1.82	ns
Output enable active (t_{ZO})	1.9	1.25	2	ns
AC current (i_{AC})	2.84	3.52	2.05	mA
Standby current (i_{ACS})	0.8	1.5	0.48	mA
Area	7545			um^2

4.12. SRAM2RW128x16

This represents dual port static RAM which has 128 16-bit words, it has 7-bit address

Table 4.12. SRAM2RW128x16 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.39	0.49	0.79	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.25	0.41	0.29	ns
CSB1/CSB2 setup (t_{CSS})	1.1	0.84	1.12	ns
CSB1/CSB2 hold (t_{CSH})	0.33	0.52	0.41	ns
WEB1/WEB2 setup (t_{WES})	0.32	0.41	0.22	ns
WEB1/WEB2 hold (t_{WEH})	0.15	0.43	0.22	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1	0.82	1.15	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.44	0.52	0.41	ns
Output enable to hi-Z (t_{OZ})	1.71	1.52	1.83	ns
Output enable active (t_{ZO})	2	1.25	1.9	ns
AC current (i_{AC})	2.5	3.58	1.69	mA
Standby current (i_{ACS})	0.8	1.55	0.54	mA
Area	11889			um^2

4.13. SRAM2RW16x32

This represents dual port static RAM which has 16 32-bit words, it has 4-bit address

Table 4.13. SRAM2RW16x32 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.41	0.52	0.82	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.22	0.41	0.31	ns
CSB1/CSB2 setup (t_{CSS})	0.9	0.79	1.15	ns
CSB1/CSB2 hold (t_{CSH})	0.32	0.53	0.42	ns
WEB1/WEB2 setup (t_{WES})	0.31	0.42	0.25	ns
WEB1/WEB2 hold (t_{WEH})	0.15	0.43	0.24	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1	0.82	1.14	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.42	0.55	0.42	ns
Output enable to hi-Z (t_{OZ})	1.72	1.51	1.82	ns
Output enable active (t_{ZO})	2	1.19	1.59	ns
AC current (i_{AC})	3.22	3.9	2.82	mA
Standby current (i_{ACS})	1.4	1.8	1	mA
Area	7595			um^2

4.14. SRAM2RW32x32

This represents dual port static RAM which has 32 32-bit words, it has 5-bit address

Table 4.14. SRAM2RW32x32 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.44	0.52	0.81	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.21	0.44	0.32	ns
CSB1/CSB2 setup (t_{CSS})	0.9	0.79	1.12	ns
CSB1/CSB2 hold (t_{CSH})	0.33	0.52	0.41	ns
WEB1/WEB2 setup (t_{WES})	0.32	0.41	0.24	ns
WEB1/WEB2 hold (t_{WEH})	0.15	0.43	0.22	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1	0.84	1.12	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.42	0.51	0.41	ns
Output enable to hi-Z (t_{OZ})	1.71	1.51	1.82	ns
Output enable active (t_{ZO})	2	1.25	1.9	ns
AC current (i_{AC})	3.48	4.1	2.7	mA
Standby current (i_{ACS})	1.5	1.9	1.28	mA
Area	9308			um^2

4.15. SRAM2RW64x32

This represents dual port static RAM which has 64 32-bit words, it has 6-bit address

Table 4.15. SRAM2RW64x32 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.7	0.9	0.8	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.22	0.41	0.31	ns
CSB1/CSB2 setup (t_{CSS})	0.9	0.82	1.12	ns
CSB1/CSB2 hold (t_{CSH})	0.32	0.51	0.42	ns
WEB1/WEB2 setup (t_{WES})	0.33	0.42	0.25	ns
WEB1/WEB2 hold (t_{WEH})	0.12	0.44	0.24	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1	0.82	1.13	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.41	0.52	0.41	ns
Output enable to hi-Z (t_{OZ})	1.72	1.51	1.82	ns
Output enable active (t_{ZO})	2	1.25	1.9	ns
AC current (i_{AC})	3.62	4.22	2.82	mA
Standby current (i_{ACS})	1.49	2	1.3	mA
Area	12471			um^2

4.16. SRAM2RW128x32

This represents dual port static RAM which has 128 32-bit words, it has 7-bit address

Table 4.16. SRAM2RW128x32 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.8	1	0.6	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.23	0.41	0.32	ns
CSB1/CSB2 setup (t_{CSS})	1	0.84	1.12	ns
CSB1/CSB2 hold (t_{CSH})	0.32	0.52	0.42	ns
WEB1/WEB2 setup (t_{WES})	0.33	0.41	0.23	ns
WEB1/WEB2 hold (t_{WEH})	0.15	0.42	0.22	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	0.9	0.82	1.15	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.44	0.53	0.41	ns
Output enable to hi-Z (t_{OZ})	1.72	1.52	1.82	ns
Output enable active (t_{ZO})	1.95	1.25	1.9	ns
AC current (i_{AC})	5.15	5.81	4.32	mA
Standby current (i_{ACS})	2.5	3	1.7	mA
Area	18993			um^2

4.17. SRAM1RW128x8

This represents single port static RAM which has 128 8-bit words, it has 7-bit address

Table 4.17. SRAM1RW128x8 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.45	0.55	0.82	ns
A[k-1:0] hold (t_{AH})	0.25	0.42	0.33	ns
CSB setup (t_{CSS})	1.1	0.82	1.15	ns
CSB hold (t_{CSH})	0.31	0.5	0.42	ns
WEB setup (t_{WES})	0.33	0.42	0.24	ns
WEB hold (t_{WEH})	0.15	0.41	0.25	ns
I[n-1:0] setup (t_{DS})	0.9	0.84	1.12	ns
I[n-1:0] hold (t_{DH})	0.45	0.52	0.44	ns
Output enable to hi-Z (t_{OZ})	1.72	1.51	1.82	ns
Output enable active (t_{ZO})	1.92	1.25	1.49	ns
AC current (i_{AC})	3.22	3.82	2.79	mA
Standby current (i_{ACS})	2.23	2.51	1.65	mA
Area	7680			um^2

4.18. SRAM2RW32x22

This represents dual port static RAM which has 32 22-bit words, it has 5-bit address

Table 4.18. SRAM2RW32x22 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.42	0.53	0.81	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.22	0.43	0.32	ns
CSB1/CSB2 setup (t_{CSS})	1.1	0.82	1.13	ns
CSB1/CSB2 hold (t_{CSH})	0.31	0.55	0.42	ns
WEB1/WEB2 setup (t_{WES})	0.32	0.43	0.24	ns
WEB1/WEB2 hold (t_{WEH})	0.13	0.44	0.25	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	1.1	0.82	1.13	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.45	0.52	0.44	ns
Output enable to hi-Z (t_{OZ})	1.72	1.51	1.83	ns
Output enable active (t_{ZO})	2	1.25	2.1	ns
AC current (i_{AC})	2.52	2.9	2.1	mA
Standby current (i_{ACS})	2	2.9	1.58	mA
Area	6843			um^2

4.19. SRAM2RW32x39

This represents dual port static RAM which has 32 39-bit words, it has 5-bit address

Table 4.19. SRAM2RW32x39 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A1[k-1:0]/A2[k-1:0] setup (t_{AS})	0.82	1	0.63	ns
A1[k-1:0]/A2[k-1:0] hold (t_{AH})	0.23	0.42	0.32	ns
CSB1/CSB2 setup (t_{CSS})	1	0.82	1.15	ns
CSB1/CSB2 hold (t_{CSH})	0.32	0.54	0.42	ns
WEB1/WEB2 setup (t_{WES})	0.33	0.42	0.22	ns
WEB1/WEB2 hold (t_{WEH})	0.15	0.42	0.25	ns
I1[n-1:0]/I2[n-1:0] setup (t_{DS})	0.9	0.83	1.12	ns
I1[n-1:0]/I2[n-1:0] hold (t_{DH})	0.45	0.52	0.44	ns
Output enable to hi-Z (t_{OZ})	1.72	1.51	1.82	ns
Output enable active (t_{ZO})	1.92	1.25	2.1	ns
AC current (i_{AC})	5.2	6.1	4.62	mA
Standby current (i_{ACS})	3.5	4.7	3	mA
Area	11098			um^2

4.20. SRAM1RW256x32

This represents single port static RAM which has 256 32-bit words, it has 5-bit address

Table 4.20. SRAM1RW256x32 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.42	0.53	0.82	ns
A[k-1:0] hold (t_{AH})	0.25	0.43	0.32	ns
CSB setup (t_{CSS})	0.9	0.82	1.15	ns
CSB hold (t_{CSH})	0.33	0.55	0.42	ns
WEB setup (t_{WES})	0.32	0.45	0.25	ns
WEB hold (t_{WEH})	0.15	0.42	0.22	ns
I[n-1:0] setup (t_{DS})	0.9	0.82	1.15	ns
I[n-1:0] hold (t_{DH})	0.45	0.52	0.42	ns
Output enable to hi-Z (t_{OZ})	1.72	1.53	1.82	ns
Output enable active (t_{ZO})	1.92	1.25	1.55	ns
AC current (i_{AC})	3	3.9	2.5	mA
Standby current (i_{ACS})	2.2	2.8	1.6	mA
Area	27352			um^2

4.21. SRAM1RW102x84

This represents single port static RAM which has 1024 8-bit words, it has 10-bit address

Table 4.21. SRAM1RW102x84 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.39	0.49	0.79	ns
A[k-1:0] hold (t_{AH})	0.25	0.42	0.29	ns
CSB setup (t_{CSS})	1.1	0.82	1.15	ns
CSB hold (t_{CSH})	0.35	0.52	0.42	ns
WEB setup (t_{WES})	0.32	0.45	0.25	ns
WEB hold (t_{WEH})	0.15	0.44	0.24	ns
I[n-1:0] setup (t_{DS})	0.9	0.84	1.15	ns
I[n-1:0] hold (t_{DH})	0.42	0.55	0.44	ns
Output enable to hi-Z (t_{OZ})	1.75	1.55	1.82	ns
Output enable active (t_{ZO})	2	1.24	1.52	ns
AC current (i_{AC})	1.9	2.45	1.55	mA
Standby current (i_{ACS})	2.6	3	2.25	mA
Area	25783			um^2

4.22. SRAM1RW512x8

This represents single port static RAM which has 512 8-bit words, it has 9-bit address

Table 4.22. SRAM1RW512x8 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.44	0.52	0.82	ns
A[k-1:0] hold (t_{AH})	0.19	0.39	0.33	ns
CSB setup (t_{CSS})	0.9	0.85	1.15	ns
CSB hold (t_{CSH})	0.33	0.54	0.42	ns
WEB setup (t_{WES})	0.32	0.42	0.21	ns
WEB hold (t_{WEH})	0.1	0.44	0.25	ns
I[n-1:0] setup (t_{DS})	0.9	0.82	1.15	ns
I[n-1:0] hold (t_{DH})	0.45	0.52	0.44	ns
Output enable to hi-Z (t_{OZ})	1.72	1.55	1.82	ns
Output enable active (t_{ZO})	2	1.22	1.52	ns
AC current (i_{AC})	1.58	2.48	1.21	mA
Standby current (i_{ACS})	2.4	2.8	1.75	mA
Area	15477			um^2

4.23. SRAM1RW128x48

This represents single port static RAM which has 128 48-bit words, it has 7-bit address

Table 4.23. SRAM1RW128x48 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.8	1	0.7	ns
A[k-1:0] hold (t_{AH})	0.22	0.53	0.32	ns
CSB setup (t_{CSS})	1.1	0.81	1.12	ns
CSB hold (t_{CSH})	0.32	0.55	0.42	ns
WEB setup (t_{WES})	0.32	0.44	0.22	ns
WEB hold (t_{WEH})	0.15	0.41	0.23	ns
I[n-1:0] setup (t_{DS})	0.9	0.85	1.12	ns
I[n-1:0] hold (t_{DH})	0.44	0.52	0.45	ns
Output enable to hi-Z (t_{OZ})	1.69	1.48	1.78	ns
Output enable active (t_{ZO})	2	1.22	1.54	ns
AC current (i_{AC})	5.25	5.72	4.62	mA
Standby current (i_{ACS})	2	2.5	1.65	mA
Area	20438			um^2

4.24. SRAM1RW32x50

This represents single port static RAM which has 32 50-bit words, it has 5-bit address

Table 4.24. SRAM1RW32x50 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.42	0.51	0.83	ns
A[k-1:0] hold (t_{AH})	0.22	0.41	0.32	ns
CSB setup (t_{CSS})	1.11	0.82	1.12	ns
CSB hold (t_{CSH})	0.33	0.52	0.43	ns
WEB setup (t_{WES})	0.32	0.42	0.24	ns
WEB hold (t_{WEH})	0.15	0.45	0.22	ns
I[n-1:0] setup (t_{DS})	1	0.82	1.14	ns
I[n-1:0] hold (t_{DH})	0.45	0.55	0.42	ns
Output enable to hi-Z (t_{OZ})	1.68	1.48	1.84	ns
Output enable active (t_{ZO})	1.9	1.25	1.52	ns
AC current (i_{AC})	4.22	4.81	3.41	mA
Standby current (i_{ACS})	1.9	2.8	1.6	mA
Area	7725			um^2

4.25. SRAM1RW64x32

This represents single port static RAM which has 64 32-bit words, it has 6-bit address

Table 4.25. SRAM1RW64x32 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.42	0.52	0.81	ns
A[k-1:0] hold (t_{AH})	0.25	0.44	0.32	ns
CSB setup (t_{CSS})	0.95	0.81	1.12	ns
CSB hold (t_{CSH})	0.33	0.51	0.44	ns
WEB setup (t_{WES})	0.32	0.45	0.22	ns
WEB hold (t_{WEH})	0.15	0.44	0.22	ns
I[n-1:0] setup (t_{DS})	1	0.82	1.12	ns
I[n-1:0] hold (t_{DH})	0.45	0.53	0.43	ns
Output enable to hi-Z (t_{OZ})	1.72	1.55	1.82	ns
Output enable active (t_{ZO})	1.9	1.25	1.51	ns
AC current (i_{AC})	3.1	3.78	2.65	mA
Standby current (i_{ACS})	2	2.6	1.5	mA
Area	8714			um^2

4.26. SRAM1RW64x34

This represents single port static RAM which has 128 8-bit words, it has 7-bit address

Table 4.26. SRAM1RW64x34 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.39	0.54	0.82	ns
A[k-1:0] hold (t_{AH})	0.25	0.44	0.33	ns
CSB setup (t_{CSS})	0.9	0.85	1.15	ns
CSB hold (t_{CSH})	0.32	0.55	0.44	ns
WEB setup (t_{WES})	0.29	0.44	0.22	ns
WEB hold (t_{WEH})	0.15	0.42	0.25	ns
I[n-1:0] setup (t_{DS})	1.1	0.82	1.15	ns
I[n-1:0] hold (t_{DH})	0.45	0.52	0.45	ns
Output enable to hi-Z (t_{OZ})	1.7	1.54	1.82	ns
Output enable active (t_{ZO})	1.95	1.21	1.52	ns
AC current (i_{AC})	3.25	4.1	2.78	mA
Standby current (i_{ACS})	2.2	2.8	1.6	mA
Area	8884			um^2

4.27. SRAM1RW256x46

This represents single port static RAM which has 256 46-bit words, it has 8-bit address

Table 4.27. SRAM1RW256x32 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.7	1	0.6	ns
A[k-1:0] hold (t_{AH})	0.25	0.51	0.32	ns
CSB setup (t_{CSS})	1	0.81	1.15	ns
CSB hold (t_{CSH})	0.29	0.52	0.44	ns
WEB setup (t_{WES})	0.32	0.41	0.22	ns
WEB hold (t_{WEH})	0.1	0.39	0.19	ns
I[n-1:0] setup (t_{DS})	0.95	0.81	1.15	ns
I[n-1:0] hold (t_{DH})	0.39	0.55	0.42	ns
Output enable to hi-Z (t_{OZ})	1.68	1.52	1.84	ns
Output enable active (t_{ZO})	1.94	1.25	1.52	ns
AC current (i_{AC})	4.9	5.62	4.58	mA
Standby current (i_{ACS})	2.55	2.8	1.85	mA
Area	38124			um^2

4.28. SRAM1RW128x46

This represents single port static RAM which has 128 46-bit words, it has 7-bit address

Table 4.28. SRAM1RW128x46 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.8	1	0.7	ns
A[k-1:0] hold (t_{AH})	0.9	0.54	0.32	ns
CSB setup (t_{CSS})	0.95	0.82	1.15	ns
CSB hold (t_{CSH})	0.32	0.51	0.4	ns
WEB setup (t_{WES})	0.29	0.39	0.23	ns
WEB hold (t_{WEH})	0.15	0.42	0.25	ns
I[n-1:0] setup (t_{DS})	1.1	0.81	1.15	ns
I[n-1:0] hold (t_{DH})	0.41	0.55	0.41	ns
Output enable to hi-Z (t_{OZ})	1.71	1.52	1.82	ns
Output enable active (t_{ZO})	1.9	1.25	1.52	ns
AC current (i_{AC})	5.22	5.72	4.59	mA
Standby current (i_{ACS})	2	2.5	1.65	mA
Area	20438			um^2

4.29. SRAM1RW64x8

This represents single port static RAM which has 64 8-bit words, it has 6-bit address

Table 4.29. SRAM1RW64x8 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.42	0.51	0.82	ns
A[k-1:0] hold (t_{AH})	0.25	0.39	0.33	ns
CSB setup (t_{CSS})	0.9	0.82	1.15	ns
CSB hold (t_{CSH})	0.32	0.52	0.41	ns
WEB setup (t_{WES})	0.29	0.42	0.21	ns
WEB hold (t_{WEH})	0.15	0.43	0.25	ns
I[n-1:0] setup (t_{DS})	1.1	0.82	1.15	ns
I[n-1:0] hold (t_{DH})	0.42	0.55	0.42	ns
Output enable to hi-Z (t_{OZ})	1.71	1.52	1.81	ns
Output enable active (t_{ZO})	2	1.21	1.55	ns
AC current (i_{AC})	3.1	3.62	2.81	mA
Standby current (i_{ACS})	2.2	2.55	1.68	mA
Area	4501			um^2

4.30. SRAM1RW64x128

This represents single port static RAM which has 64 128-bit words, it has 6-bit address

Table 4.30. SRAM1RW64x128 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.82	1.1	0.69	ns
A[k-1:0] hold (t_{AH})	0.25	0.52	0.33	ns
CSB setup (t_{CSS})	1.1	0.81	1.12	ns
CSB hold (t_{CSH})	0.35	0.52	0.41	ns
WEB setup (t_{WES})	0.32	0.44	0.22	ns
WEB hold (t_{WEH})	0.15	0.42	0.25	ns
I[n-1:0] setup (t_{DS})	0.9	0.82	1.15	ns
I[n-1:0] hold (t_{DH})	0.45	0.52	0.42	ns
Output enable to hi-Z (t_{OZ})	1.72	1.52	1.82	ns
Output enable active (t_{ZO})	1.95	1.25	1.51	ns
AC current (i_{AC})	11	11.5	10.3	mA
Standby current (i_{ACS})	3.6	4	3	mA
Area	25693			um^2

4.31. SRAM1RW256x128

This represents single port static RAM which has 256 128-bit words, it has 8-bit address

Table 4.31. SRAM1RW256x128 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.82	1.1	0.72	ns
A[k-1:0] hold (t_{AH})	0.25	0.52	0.33	ns
CSB setup (t_{CSS})	0.9	0.82	1.12	ns
CSB hold (t_{CSH})	0.33	0.52	0.41	ns
WEB setup (t_{WES})	0.32	0.44	0.25	ns
WEB hold (t_{WEH})	0.15	0.42	0.22	ns
I[n-1:0] setup (t_{DS})	0.9	0.85	1.1	ns
I[n-1:0] hold (t_{DH})	0.41	0.52	0.45	ns
Output enable to hi-Z (t_{OZ})	1.75	1.52	1.82	ns
Output enable active (t_{ZO})	1.9	1.24	1.52	ns
AC current (i_{AC})	12	13	10.4	mA
Standby current (i_{ACS})	4	4.7	3.3	mA
Area	112189			um^2

4.32. SRAM1RW256x8

This represents single port static RAM which has 256 8-bit words, it has 8-bit address

Table 4.32. SRAM1RW256x8 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.45	0.52	0.81	ns
A[k-1:0] hold (t_{AH})	0.21	0.41	0.32	ns
CSB setup (t_{CSS})	0.9	0.82	1.13	ns
CSB hold (t_{CSH})	0.33	0.52	0.45	ns
WEB setup (t_{WES})	0.32	0.44	0.25	ns
WEB hold (t_{WEH})	0.15	0.42	0.22	ns
I[n-1:0] setup (t_{DS})	1.1	0.82	1.11	ns
I[n-1:0] hold (t_{DH})	0.45	0.51	0.45	ns
Output enable to hi-Z (t_{OZ})	1.7	1.51	1.81	ns
Output enable active (t_{ZO})	1.95	1.25	1.52	ns
AC current (i_{AC})	1.25	2.1	0.92	mA
Standby current (i_{ACS})	2	2.5	1.7	mA
Area	8632			um^2

4.33. SRAM1RW256x48

This represents single port static RAM which has 256 48-bit words, it has 8-bit address

Table 4.33. SRAM1RW256x48 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.82	1.1	0.72	ns
A[k-1:0] hold (t_{AH})	0.25	0.52	0.31	ns
CSB setup (t_{CSS})	0.9	0.8	1.1	ns
CSB hold (t_{CSH})	0.32	0.55	0.41	ns
WEB setup (t_{WES})	0.33	0.42	0.22	ns
WEB hold (t_{WEH})	0.15	0.43	0.24	ns
I[n-1:0] setup (t_{DS})	0.9	0.82	1.15	ns
I[n-1:0] hold (t_{DH})	0.42	0.55	0.41	ns
Output enable to hi-Z (t_{OZ})	1.72	1.52	1.81	ns
Output enable active (t_{ZO})	2	1.25	1.5	ns
AC current (i_{AC})	5.51	6	5.1	mA
Standby current (i_{ACS})	2.3	2.8	1.75	mA
Area	39492			um^2

4.34. SRAM1RW512x128

This represents single port static RAM which has 512 128-bit words, it has 9-bit address

Table 4.34. SRAM1RW512x128 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.82	1.1	0.72	ns
A[k-1:0] hold (t_{AH})	0.25	0.51	0.32	ns
CSB setup (t_{CSS})	1	0.82	1.15	ns
CSB hold (t_{CSH})	0.32	0.51	0.42	ns
WEB setup (t_{WES})	0.33	0.39	0.22	ns
WEB hold (t_{WEH})	0.11	0.42	0.24	ns
I[n-1:0] setup (t_{DS})	1	0.82	1.15	ns
I[n-1:0] hold (t_{DH})	0.44	0.52	0.42	ns
Output enable to hi-Z (t_{OZ})	1.71	1.52	1.81	ns
Output enable active (t_{ZO})	1.9	1.25	1.52	ns
AC current (i_{AC})	14	15	11.5	mA
Standby current (i_{ACS})	5	6	4.1	mA
Area	218850			um^2

4.35. SRAM1RW512x32

This represents single port static RAM which has 512 32-bit words, it has 9-bit address

Table 4.35. SRAM1RW512x32 Parameters

Parameter	SS	TT	FF	Units
Cycle time (t_{CYC})	6	6	6	ns
Access time (t_A)	3	3	3	ns
A[k-1:0] setup (t_{AS})	0.44	0.52	0.81	ns
A[k-1:0] hold (t_{AH})	0.25	0.41	0.32	ns
CSB setup (t_{CSS})	0.9	0.82	1.15	ns
CSB hold (t_{CSH})	0.32	0.53	0.42	ns
WEB setup (t_{WES})	0.3	0.45	0.25	ns
WEB hold (t_{WEH})	0.13	0.42	0.22	ns
I[n-1:0] setup (t_{DS})	1.12	0.82	1.15	ns
I[n-1:0] hold (t_{DH})	0.41	0.53	0.41	ns
Output enable to hi-Z (t_{OZ})	1.72	1.52	1.83	ns
Output enable active (t_{ZO})	2	1.21	1.52	ns
AC current (i_{AC})	4.1	5.9	3.5	mA
Standby current (i_{ACS})	2.6	3	2	mA
Area	50936			um^2

6. Revision history

Table 6.1. Revision history

Revision	Date	EDK Version	Change
1.0.0	31/01/2012	b1.0.0	Initial release