



PIC24FJ256GA705 FAMILY

PIC24FJ256GA705 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ256GA705 family devices that you have received conform functionally to the current Device Data Sheet (DS30010118C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in [Table 1](#). The silicon issues are summarized in [Table 2](#).


The errata described in this document will be addressed in future revisions of the PIC24FJ256GA705 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of [Table 2](#) apply to the current silicon revision (A4).

Data Sheet clarifications and corrections start on [Page 9](#), following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
 - a) For MPLAB IDE 8, select *Programmer > Reconnect*.
 - b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ256GA705 family silicon revisions are shown in [Table 1](#).

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾		Part Number	Device ID ⁽¹⁾	Revision ID for Silicon Revision ⁽²⁾	
		A3	A4			A3	A4
PIC24FJ64GA705	0x7507	0x03	0x04	PIC24FJ256GA704	0x750D	0x03	0x04
PIC24FJ128GA705	0x750B			PIC24FJ64GA702	0x7506		
PIC24FJ256GA705	0x750F			PIC24FJ128GA702	0x750A		
PIC24FJ64GA704	0x7505			PIC24FJ256GA702	0x750E		
PIC24FJ128GA704	0x7509			—			

- Note 1:** The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format “DEVID DEVREV”.
- 2:** Refer to the “PIC24FJ256GA705 Family Flash Programming Specification” (DS30010102) for detailed information on Device and Revision IDs for your specific device.

PIC24FJ256GA705 FAMILY

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions ⁽¹⁾	
				A3	A4
I ² C	Address Hold	1.	In Slave mode when AHEN = 1 (Address Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.	X	X
Reset	Trap Conflict	2.	The TRAPR bit is not getting set when a hard trap conflict occurs.	X	X
I ² C	Data Hold	3.	In Slave mode when DHEN = 1 (Data Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of data reception, then a slave interrupt will not occur after the 8th clock.	X	X
Primary XT and HS Oscillator (POSC)	Primary Oscillator Start-up Timer (OST)	4.	OST may indicate oscillator is ready for use too early.	X	X
Power	Retention Sleep	5.	When the device wakes up from Retention Sleep mode (RETEN bit (RCON<12>) = 1, LPCFG bit (FPOR<2>) = 0), a device Reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.	X	
Power	Power BOR	6.	The main BOR may not function on some devices.	X	
I ² C	Slave Mode	7.	Bus data can get corrupted when it matches with one of the slave addresses connected to the bus.	X	X
I ² C	Slave Mode	8.	In 10-Bit Addressing Slave mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence.	X	X
I ² C	Slave Receive Mode	9.	The Acknowledge Time Status bit (ACKTIM) is asserted only if the Address Hold Enable (AHEN) or Data Hold Enable (DHEN) bit is enabled.	X	X
I ² C	Bus Collisions	10.	In Slave mode, false bus collision triggers are generated when bus collision is enabled (SBCDE = 1).	X	X
I ² C	Hold Time	11.	Minimum hold time of 300 ns is not achieved when the SDAx Hold Time Selection bit (SDAHT) is set.	X	X
I ² C	Slave Mode	12.	In Slave mode, the Bus Collision Detect bit (BCL) cannot be cleared when bus collision detection is enabled (SBCDE = 1).	X	X
I ² C	Slave Mode	13.	In Slave mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).	X	X
UART	Break Character Transmission	14.	The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.	X	X
ADC	Differential Nonlinearity	15.	Increase DNL specification on the positive side.		X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

PIC24FJ256GA705 FAMILY

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: I²C

In Slave mode when AHEN = 1 (Address Hold Enable), if the ACKDT bit (Acknowledge Data) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.

Work around

In Slave mode, user software should clear ACKDT on receiving the Start bit.

Affected Silicon Revisions

A3	A4						
X	X						

2. Module: Reset

If a lower priority address error trap occurs while a higher priority oscillator failure trap is being processed, the TRAPR bit (RCON<15>) is not set. A Trap Conflict Reset does not occur as expected and the device may stop executing code.

Work around

None. However, a $\overline{\text{MCLR}}$ /POR Reset will recover the device.

Affected Silicon Revisions

A3	A4						
X	X						

3. Module: I²C

In Slave mode when DHEN = 1 (Data Hold Enable), if the ACKDT bit (Acknowledge Data) is set at the beginning of data reception, then the slave interrupt will not occur after the 8th clock.

Work around

In Slave mode, user software should clear ACKDT on receiving the Start bit.

Affected Silicon Revisions

A3	A4						
X	X						

PIC24FJ256GA705 FAMILY

4. Module: Primary XT and HS Oscillator (POSC)

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize the POSC.
3. Switch to the POSC source.

[Example 1](#) shows a work around for the device power-on and [Example 2](#) explains the work around when the device wakes from Sleep.

EXAMPLE 1: USING POSC AT POWER-ON

```
#pragma config FNOSC = FRC           // Oscillator Selection bits (Fast RC oscillator (FRC))
// Clock Switching Enabled (Fail-safe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
-----
int main()
{
    // configure REFO to request POSC
    REFOCONLbits.ROSEL = 2;           // POSC
    REFOCONLbits.ROOUT = 0;           // disable output
    REFOCONLbits.ROEN = 1;            // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    { // delay for 9 ms
        unsigned int delaysms = 9;
        while(delaysms--) asm volatile("repeat #(8000000/1000/2) \n nop");
    }

    // switch to POSC = 2
    __builtin_write_OSCCONH(2);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch
```

PIC24FJ256GA705 FAMILY

EXAMPLE 2: USING POSC WHEN WAKING FROM SLEEP

```
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
-----
// switch to FRC = 0 before entering sleep
__builtin_write_OSCCONH(0);
__builtin_write_OSCCONL(1);
while(OSCCONbits.OSWEN == 1);    // wait for switch

// enter sleep mode
Sleep();

// configure REFO to request POSC
REFOCONLbits.ROSEL = 2;          // POSC
REFOCONLbits.ROOUT = 0;          // disable output
REFOCONLbits.ROEN = 1;           // enable module

// wait for POSC stable clock
// this delay may vary depending on different application conditions
// such as voltage, temperature, layout, XT or HS mode and components
{
    // delay for 9 ms
    unsigned int delaysms = 9;
    while(delaysms--) asm volatile("repeat #(8000000/1000/2) \n nop");
}

// switch to POSC = 2
__builtin_write_OSCCONH(2);
__builtin_write_OSCCONL(1);
while(OSCCONbits.OSWEN == 1);    // wait for switch
```

Affected Silicon Revisions

A3	A4						
X	X						

5. Module: Power

When the device wakes up from Retention Sleep mode (RETEN bit (RCON<12>) = 1, LPCFG bit (FPOR<2>) = 0), occasionally a device reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.

Work around

To provide a consistent behavior when the device wakes up from Retention Sleep mode, a software RESET instruction (RESET) should be inserted following the SLEEP instruction. In this case, a Reset will be always be generated when the device wakes up from Retention Sleep. [Example 3](#) shows the software RESET instruction implementation:

EXAMPLE 3: SOFTWARE RESET AFTER SLEEP INSTRUCTION

```
// ENTER SLEEP MODE.
asm volatile ("pwrsav #0");
// SOFTWARE RESET RIGHT AFTER SLEEP.
asm volatile("reset");
```

Affected Silicon Revisions

A3	A4						
X							

PIC24FJ256GA705 FAMILY

6. Module: Power

The main BOR may not occur when the operating voltage drops below the BOR trip voltage.

Work around

Ensure the device operating voltage does not violate the specified values. Use an external supervisor circuit to reset the device if the operating voltage can be outside the specified values.

Affected Silicon Revisions

A3	A4						
X							

7. Module: I²C

In applications with multiple I²C slaves, bus data can become corrupted when the data payload sent to an addressed slave device matches the bus address of another (unaddressed) slave device.

Work around

Keep track of the bus address and data phases in software. When Address Hold Enable is used (the AHEN bit is set), the application can assert a NACK for any of the received bytes (invalid addresses and data bytes for other slave devices) until a Stop bit is received.

Affected Silicon Revisions

A3	A4						
X	X						

8. Module: I²C

In I²C 10-Bit Slave Addressing mode, on receiving the upper address byte (A9 and A8 bits), the Acknowledge Time Status bit (ACKTIM) is not asserted during the Acknowledgment sequence. This issue is not seen during the reception of the lower address byte (A7 to A0) and data bytes. The hardware asserts the ACKTIM bit on the falling edge of the eighth clock and deasserts on the rising edge of the ninth clock. In this case, ACKTIM is not asserted on upper address byte reception. When AHEN = 1, the clock is stretched after the 8th falling edge and the ACKTIM bit is asserted until the clock is released. If AHEN = 0, the clock is not stretched and ACKTIM is asserted during the Acknowledgment sequence, which is of a short duration. Therefore, the user application can see this issue of the ACKTIM bit not getting asserted when AHEN = 1.

Work around

Instead of polling for ACKTIM to be asserted, poll for the RBF flag.

Affected Silicon Revisions

A3	A4						
X	X						

9. Module: I²C

In I²C Slave Receive mode, the Acknowledge Time Status bit (ACKTIM) has no effect if the Address Hold Enable (AHEN) and Data Hold Enable (DHEN) bits are disabled (AHEN = 0 and DHEN = 0). The Acknowledge Time Status bit (ACKTIM) is asserted only if the Address Hold Enable (AHEN) or Data Hold Enable (DHEN) bit is enabled.

Work around

Instead of polling for the ACKTIM bit to be asserted, poll for the RBF flag.

Affected Silicon Revisions

A3	A4						
X	X						

PIC24FJ256GA705 FAMILY

10. Module: I²C

In Slave mode, false bus collision triggers are generated when the bus collision is enabled (SBCDE = 1).

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

11. Module: I²C

A minimum hold time of 300 ns on SDAx, after the falling edge of SCLx, is not achieved when the SDAx Data Hold Time Selection bit (SDAHT) is set.

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

12. Module: I²C

In Slave mode, the Bus Collision Detect bit (BCL) cannot be cleared when bus collision detection is enabled (SBCDE = 1).

Work around

Disable the I²C module and then re-enable the module.

Affected Silicon Revisions

A3	A4						
X	X						

13. Module: I²C

In Slave mode, an address cannot be received when the device is in Idle and the module is set for discontinue in Idle (I2CSIDL = 1).

Work around

None.

Affected Silicon Revisions

A3	A4						
X	X						

14. Module: UART

The Transmit Shift Register Empty (TRMT) bit is unreliable when there are back-to-back Break character transmissions.

For back-to-back Break characters, the TRMT bit may not reflect the actual status. If user software is polling for this bit to be set, it may result in dummy bytes getting transmitted instead of Break characters.

Work around

Poll the UARTx Transmit Break bit, UTXBRK (UxSTA<11>), to be cleared instead of the TRMT bit (U1STA<8>) to be set. The UTXBRK status bit will be cleared after a Break character transmission.

Affected Silicon Revisions

A3	A4						
X	X						

PIC24FJ256GA705 FAMILY

15. Module: ADC

As shown in the following table, the ADC Differential Nonlinearity (DNL) specification on the positive side changes (changes shown in **bold**).

TABLE 32-24: A/D MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
A/D Accuracy							
AD22B	DNL	Differential Nonlinearity	—	—	< +2	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V
					< -1		

Work around

None.

Affected Silicon Revisions

A3	A4						
	X						

PIC24FJ256GA705 FAMILY

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30010118C):

Note:	Corrections are shown in bold . Where possible, the original bold text formatting has been removed for clarity.
--------------	--

None.

PIC24FJ256GA705 FAMILY

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2016)

Initial release of this document; issued for Revision A3.

Rev B Document (12/2016)

Added silicon errata issue 5 ([Power](#)).

Rev C Document (6/2017)

Added silicon errata issue 6 ([Power](#)).

Added data sheet clarifications 1 (Referenced Sources), 2 (Device Overview), 3 (Power-Saving Features), 4 (Capture/Compare/PWM/Timer Modules (MCCP)), 5 (Serial Peripheral Interface), 6 (Serial Peripheral Interface), 7 (Comparator Voltage Reference), 8 (High/Low-Voltage Detect (HLVD)), 9 (High/Low-Voltage Detect (HLVD)), 10 (Electrical Characteristics) and 11 (Packaging Information).

Rev D Document (3/2018)

Rev D is updated for the silicon revision A4.

Added silicon errata issues 7 ([I²C](#)), 8 ([I²C](#)), 9 ([I²C](#)), 10 ([I²C](#)), 11 ([I²C](#)), 12 ([I²C](#)), 13 ([I²C](#)), 14 ([UART](#)) and 15 ([ADC](#)).

Incorporated all data sheet clarifications into the "*PIC24FJ256GA705 Family Data Sheet*" (DS30010118C).

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Information contained in this publication regarding device applications and the like is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION, INCLUDING BUT NOT LIMITED TO ITS CONDITION, QUALITY, PERFORMANCE, MERCHANTABILITY OR FITNESS FOR PURPOSE. Microchip disclaims all liability arising from this information and its use. Use of Microchip devices in life support and/or safety applications is entirely at the buyer's risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELoQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
== ISO/TS 16949 ==

Trademarks

The Microchip name and logo, the Microchip logo, AnyRate, AVR, AVR logo, AVR Freaks, BeaconThings, BitCloud, CryptoMemory, CryptoRF, dsPIC, FlashFlex, flexPWR, Helder, JukeBlox, KEELoQ, KEELoQ logo, Klear, LANCheck, LINK MD, maxStylus, maxTouch, MediaLB, megaAVR, MOST, MOST logo, MPLAB, OptoLyzer, PIC, picoPower, PICSTART, PIC32 logo, Prochip Designer, QTouch, RightTouch, SAM-BA, SpyNIC, SST, SST Logo, SuperFlash, tinyAVR, UNI/O, and XMEGA are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

ClockWorks, The Embedded Control Solutions Company, EtherSynch, Hyper Speed Control, HyperLight Load, IntelliMOS, mTouch, Precision Edge, and Quiet-Wire are registered trademarks of Microchip Technology Incorporated in the U.S.A.

Adjacent Key Suppression, AKS, Analog-for-the-Digital Age, Any Capacitor, AnyIn, AnyOut, BodyCom, chipKIT, chipKIT logo, CodeGuard, CryptoAuthentication, CryptoCompanion, CryptoController, dsPICDEM, dsPICDEM.net, Dynamic Average Matching, DAM, ECAN, EtherGREEN, In-Circuit Serial Programming, ICSP, Inter-Chip Connectivity, JitterBlocker, KlearNet, KlearNet logo, Mindi, MiWi, motorBench, MPASM, MPF, MPLAB Certified logo, MPLIB, MPLINK, MultiTRAK, NetDetach, Omniscient Code Generation, PICDEM, PICDEM.net, PICKit, PICtail, PureSilicon, QMatrix, RightTouch logo, REAL ICE, Ripple Blocker, SAM-ICE, Serial Quad I/O, SMART-I.S., SQI, SuperSwitcher, SuperSwitcher II, Total Endurance, TSHARC, USBCheck, VariSense, ViewSpan, WiperLock, Wireless DNA, and ZENA are trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

SQTP is a service mark of Microchip Technology Incorporated in the U.S.A.

Silicon Storage Technology is a registered trademark of Microchip Technology Inc. in other countries.

GestIC is a registered trademark of Microchip Technology Germany II GmbH & Co. KG, a subsidiary of Microchip Technology Inc., in other countries.

All other trademarks mentioned herein are property of their respective companies.

© 2016-2018, Microchip Technology Incorporated, All Rights Reserved.

ISBN: 978-1-5224-2826-8

Worldwide Sales and Service

AMERICAS

Corporate Office
 2355 West Chandler Blvd.
 Chandler, AZ 85224-6199
 Tel: 480-792-7200
 Fax: 480-792-7277
 Technical Support:
<http://www.microchip.com/support>
 Web Address:
www.microchip.com

Atlanta
 Duluth, GA
 Tel: 678-957-9614
 Fax: 678-957-1455

Austin, TX
 Tel: 512-257-3370

Boston
 Westborough, MA
 Tel: 774-760-0087
 Fax: 774-760-0088

Chicago
 Itasca, IL
 Tel: 630-285-0071
 Fax: 630-285-0075

Dallas
 Addison, TX
 Tel: 972-818-7423
 Fax: 972-818-2924

Detroit
 Novi, MI
 Tel: 248-848-4000

Houston, TX
 Tel: 281-894-5983

Indianapolis
 Noblesville, IN
 Tel: 317-773-8323
 Fax: 317-773-5453
 Tel: 317-536-2380

Los Angeles
 Mission Viejo, CA
 Tel: 949-462-9523
 Fax: 949-462-9608
 Tel: 951-273-7800

Raleigh, NC
 Tel: 919-844-7510

New York, NY
 Tel: 631-435-6000

San Jose, CA
 Tel: 408-735-9110
 Tel: 408-436-4270

Canada - Toronto
 Tel: 905-695-1980
 Fax: 905-695-2078

ASIA/PACIFIC

Australia - Sydney
 Tel: 61-2-9868-6733

China - Beijing
 Tel: 86-10-8569-7000

China - Chengdu
 Tel: 86-28-8665-5511

China - Chongqing
 Tel: 86-23-8980-9588

China - Dongguan
 Tel: 86-769-8702-9880

China - Guangzhou
 Tel: 86-20-8755-8029

China - Hangzhou
 Tel: 86-571-8792-8115

China - Hong Kong SAR
 Tel: 852-2943-5100

China - Nanjing
 Tel: 86-25-8473-2460

China - Qingdao
 Tel: 86-532-8502-7355

China - Shanghai
 Tel: 86-21-3326-8000

China - Shenyang
 Tel: 86-24-2334-2829

China - Shenzhen
 Tel: 86-755-8864-2200

China - Suzhou
 Tel: 86-186-6233-1526

China - Wuhan
 Tel: 86-27-5980-5300

China - Xian
 Tel: 86-29-8833-7252

China - Xiamen
 Tel: 86-592-2388138

China - Zhuhai
 Tel: 86-756-3210040

ASIA/PACIFIC

India - Bangalore
 Tel: 91-80-3090-4444

India - New Delhi
 Tel: 91-11-4160-8631

India - Pune
 Tel: 91-20-4121-0141

Japan - Osaka
 Tel: 81-6-6152-7160

Japan - Tokyo
 Tel: 81-3-6880-3770

Korea - Daegu
 Tel: 82-53-744-4301

Korea - Seoul
 Tel: 82-2-554-7200

Malaysia - Kuala Lumpur
 Tel: 60-3-7651-7906

Malaysia - Penang
 Tel: 60-4-227-8870

Philippines - Manila
 Tel: 63-2-634-9065

Singapore
 Tel: 65-6334-8870

Taiwan - Hsin Chu
 Tel: 886-3-577-8366

Taiwan - Kaohsiung
 Tel: 886-7-213-7830

Taiwan - Taipei
 Tel: 886-2-2508-8600

Thailand - Bangkok
 Tel: 66-2-694-1351

Vietnam - Ho Chi Minh
 Tel: 84-28-5448-2100

EUROPE

Austria - Wels
 Tel: 43-7242-2244-39
 Fax: 43-7242-2244-393

Denmark - Copenhagen
 Tel: 45-4450-2828
 Fax: 45-4485-2829

Finland - Espoo
 Tel: 358-9-4520-820

France - Paris
 Tel: 33-1-69-53-63-20
 Fax: 33-1-69-30-90-79

Germany - Garching
 Tel: 49-8931-9700

Germany - Haan
 Tel: 49-2129-3766400

Germany - Heilbronn
 Tel: 49-7131-67-3636

Germany - Karlsruhe
 Tel: 49-721-625370

Germany - Munich
 Tel: 49-89-627-144-0
 Fax: 49-89-627-144-44

Germany - Rosenheim
 Tel: 49-8031-354-560

Israel - Ra'anana
 Tel: 972-9-744-7705

Italy - Milan
 Tel: 39-0331-742611
 Fax: 39-0331-466781

Italy - Padova
 Tel: 39-049-7625286

Netherlands - Drunen
 Tel: 31-416-690399
 Fax: 31-416-690340

Norway - Trondheim
 Tel: 47-7289-7561

Poland - Warsaw
 Tel: 48-22-3325737

Romania - Bucharest
 Tel: 40-21-407-87-50

Spain - Madrid
 Tel: 34-91-708-08-90
 Fax: 34-91-708-08-91

Sweden - Gothenberg
 Tel: 46-31-704-60-40

Sweden - Stockholm
 Tel: 46-8-5090-4654

UK - Wokingham
 Tel: 44-118-921-5800
 Fax: 44-118-921-5820