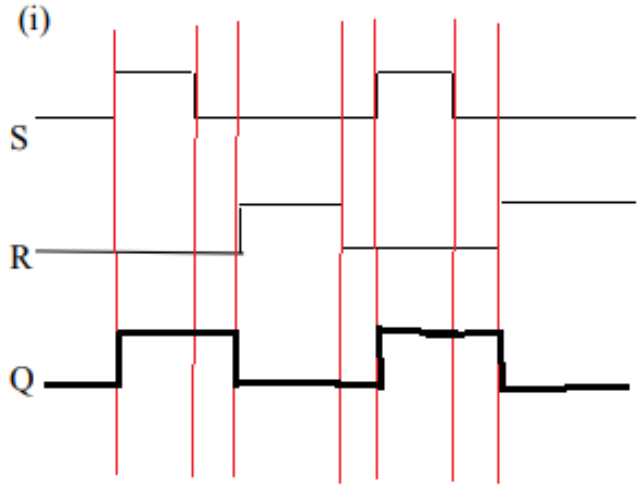
Raymond You

EECE 2160 Kimani

HW 5

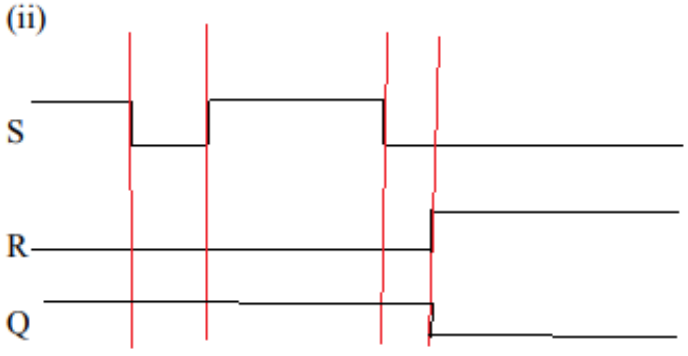
1.

(i)



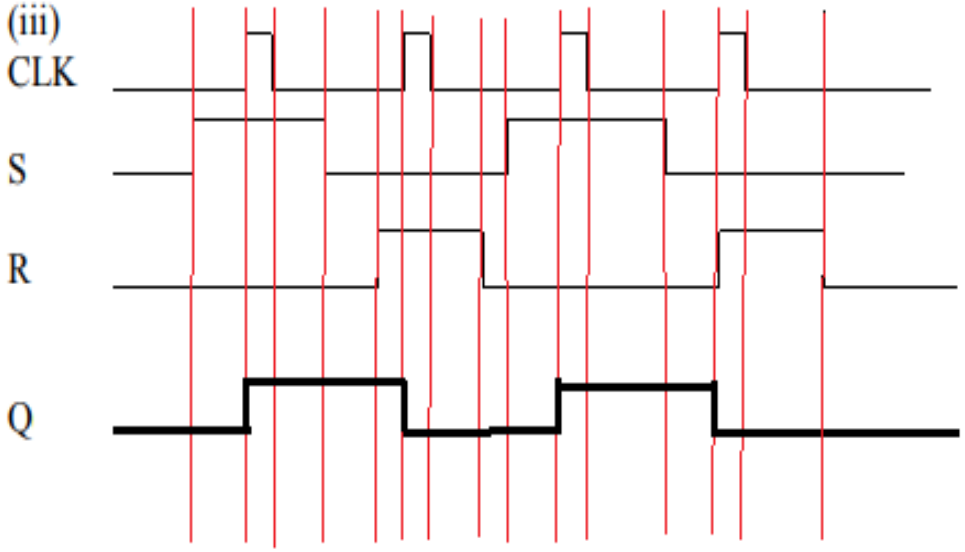
S	R	Q
0	0	no change
0	1	0
1	0	1
1	1	not allowed

(ii)



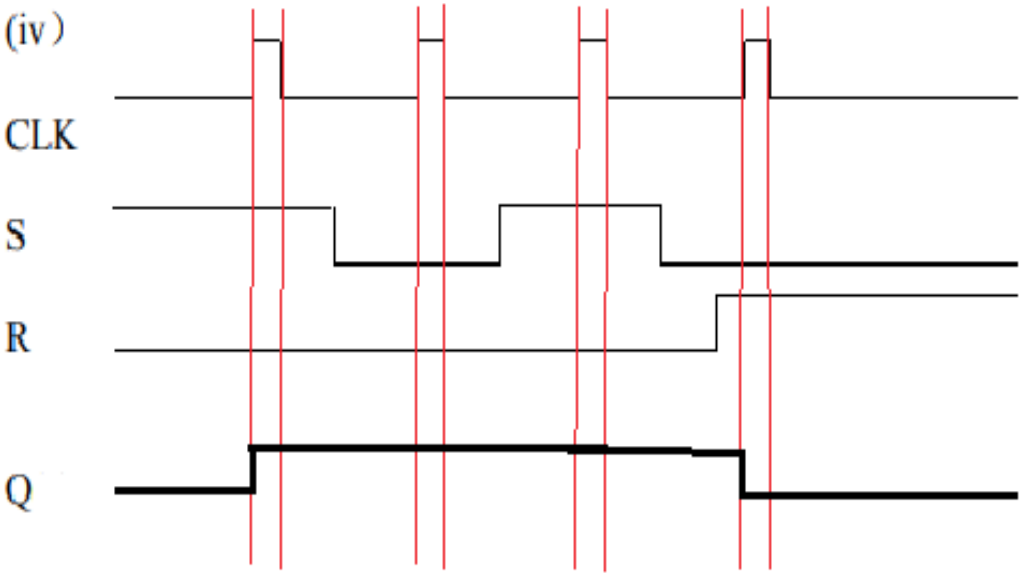
S	R	Q
0	0	no change
0	1	0
1	0	1
1	1	not allowed

(iii)



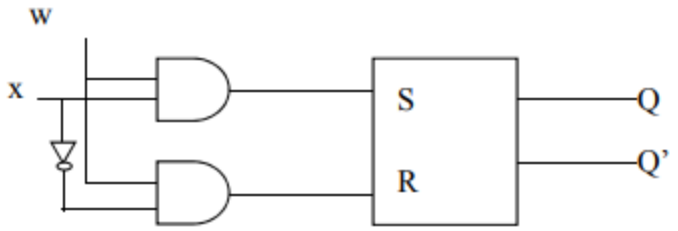
S	R	Q
0	0	no change
0	1	0
1	0	1
1	1	not allowed

(iv)

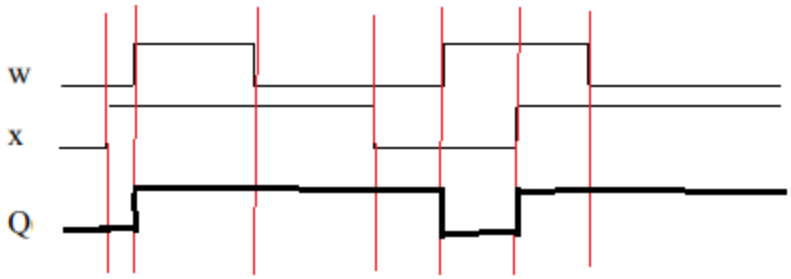


S	R	Q
0	0	no change
0	1	0
1	0	1
1	1	not allowed

2. (10 points) Draw the timing diagram for the signal Q in the following circuit. Assume Q=0 initially, the S-R Flip Flop is unclocked, and it behaves as shown in problem 1 above.



W	X	S	R
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	0




```
S  R   Q
----------
0  0   no change
0  1   0
1  0   1
1  1   not allowed
----------
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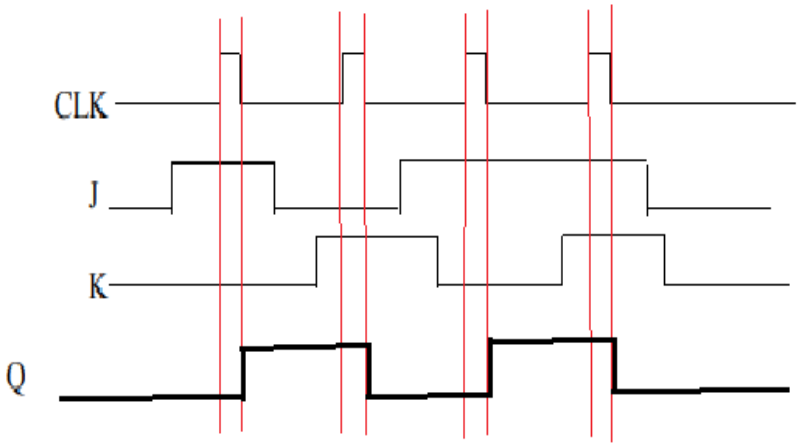
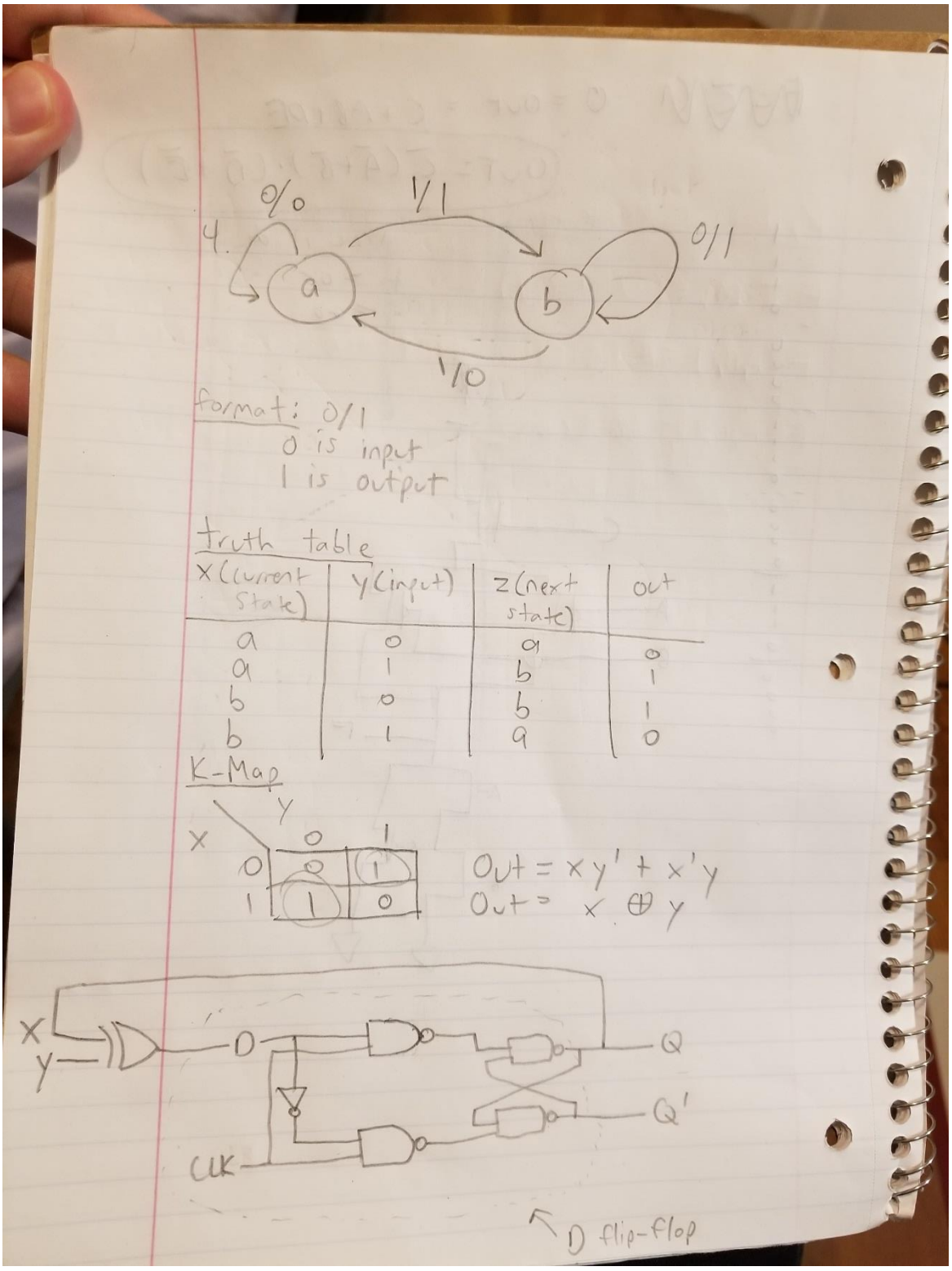
3. (5 points) Complete the timing diagram for a trailing (falling) edge triggered J-K Flip-Flop.
Assume Q=0 initially.



Truth Table

J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	$\overline{Q}_0$ (toggles)

4.


0/0
1/1
0/1
4.
a
b
1/0
format: 0/1
0 is input
1 is output
truth table
x (current state) | y (input) | z (next state) | out
a | 0 | a | 0
a | 1 | b | 1
b | 0 | b | 1
b | 1 | a | 0
K-Map
y
x
0
1
0
1
1
1
0
Out = xy' + x'y
Out = x ⊕ y
x
y
D
Q
Q'
CLK
D flip-flop

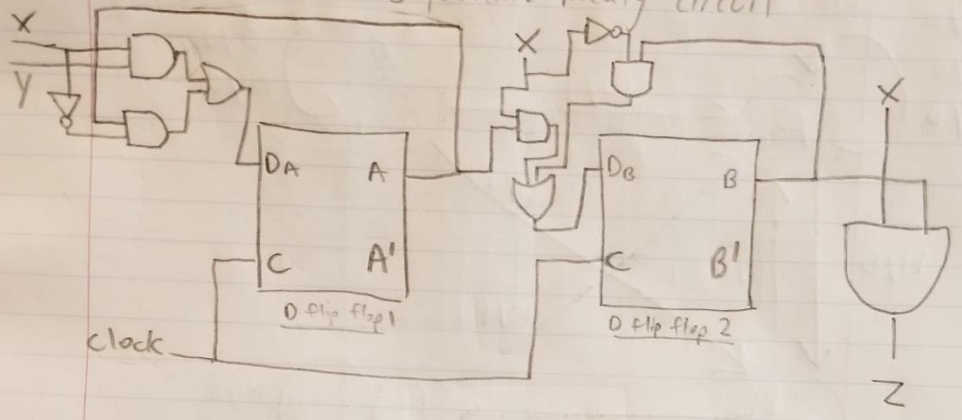
5.

$D_A = X'A + XY$

$D_B = X'A + XY$

$Z = XB$

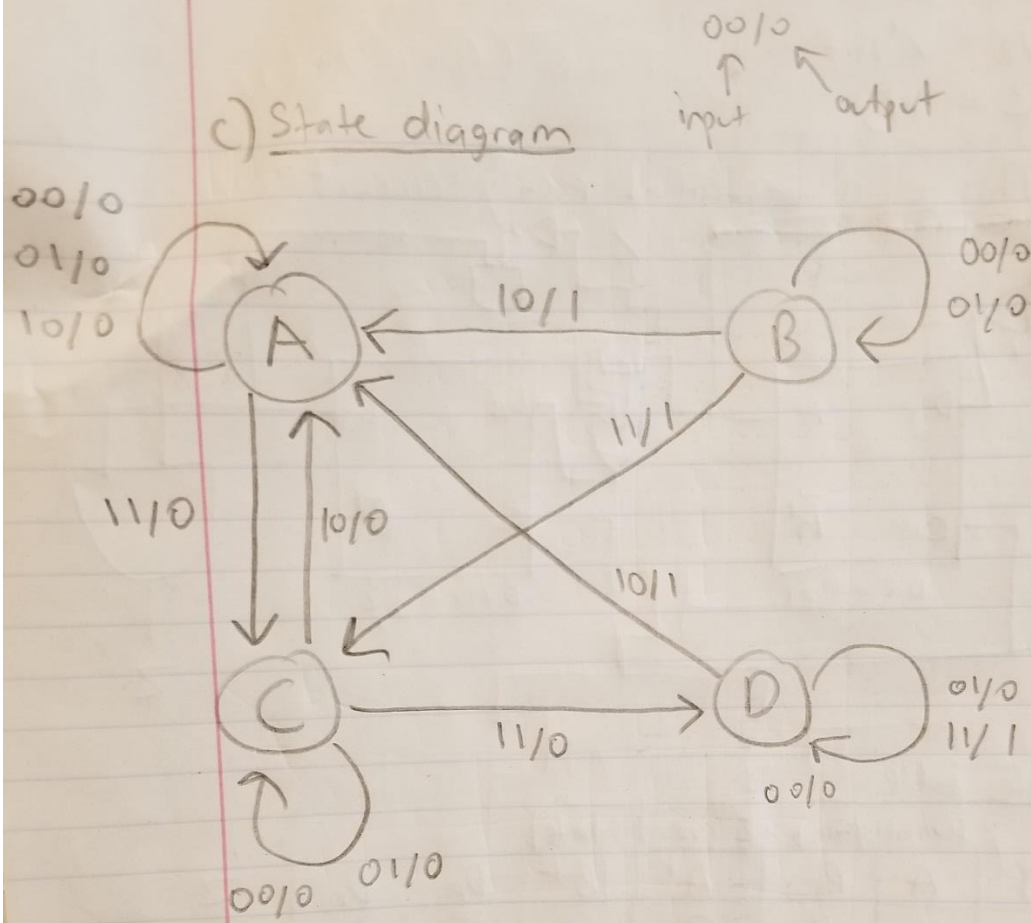
5. a) This is a sequential mealy circuit



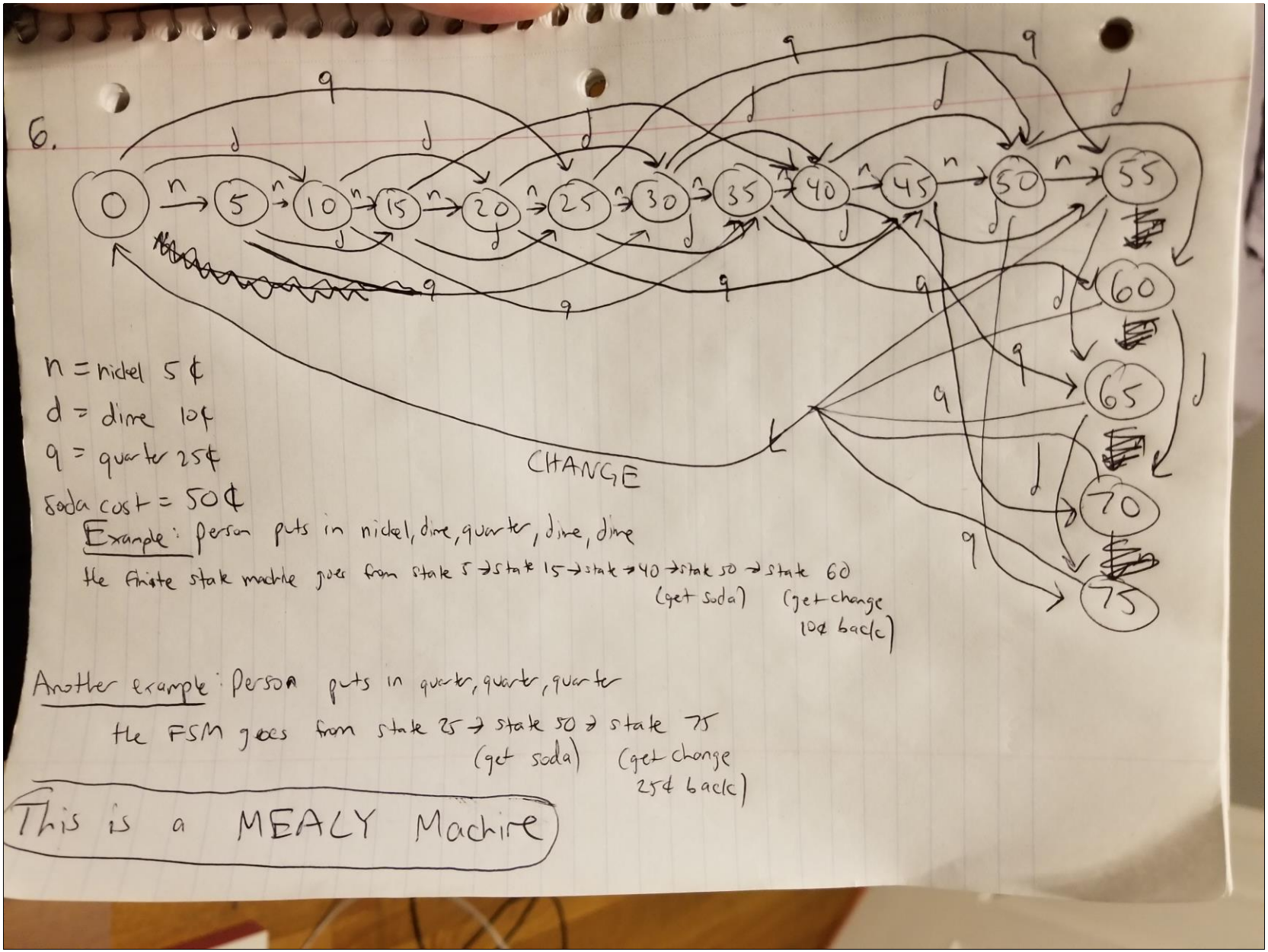
b) State table

		(current state)		(next state)				
X	Y	A	B	A^+	B^+	D_A	D_B	Z
0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	1	0
0	0	1	0	1	0	1	0	0
0	0	1	1	1	1	1	1	0
0	1	0	0	0	0	0	0	0
0	1	0	1	0	1	0	1	0
0	1	1	0	1	0	1	0	0
0	1	1	1	1	1	1	1	0
1	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	1
1	0	1	0	0	0	0	0	0
1	0	1	1	0	0	0	0	1
1	1	0	0	1	0	1	0	0
1	1	0	1	1	0	1	0	1
1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	1	1

c) State diagram



A = 00
B = 01
C = 10
D = 11



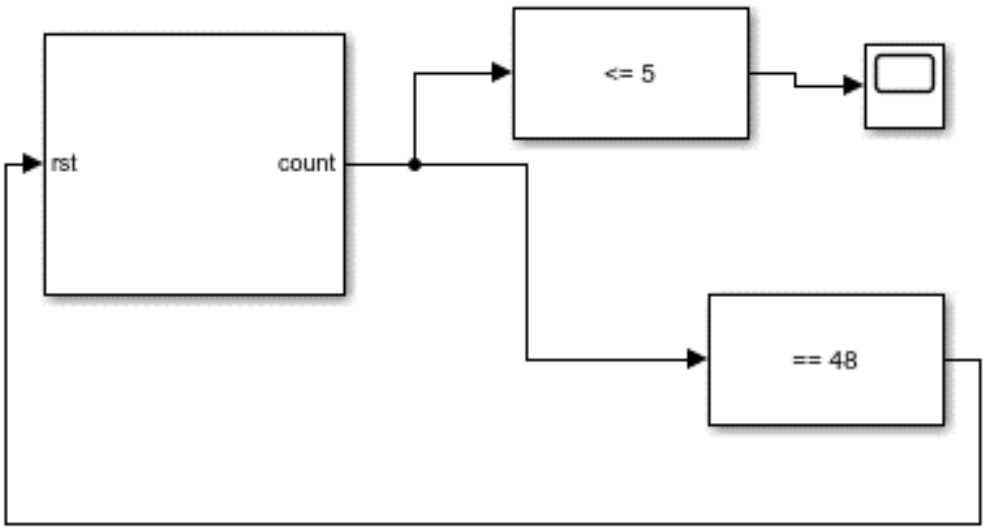
n = nickel 5¢
d = dime 10¢
q = quarter 25¢
Soda cost = 50¢

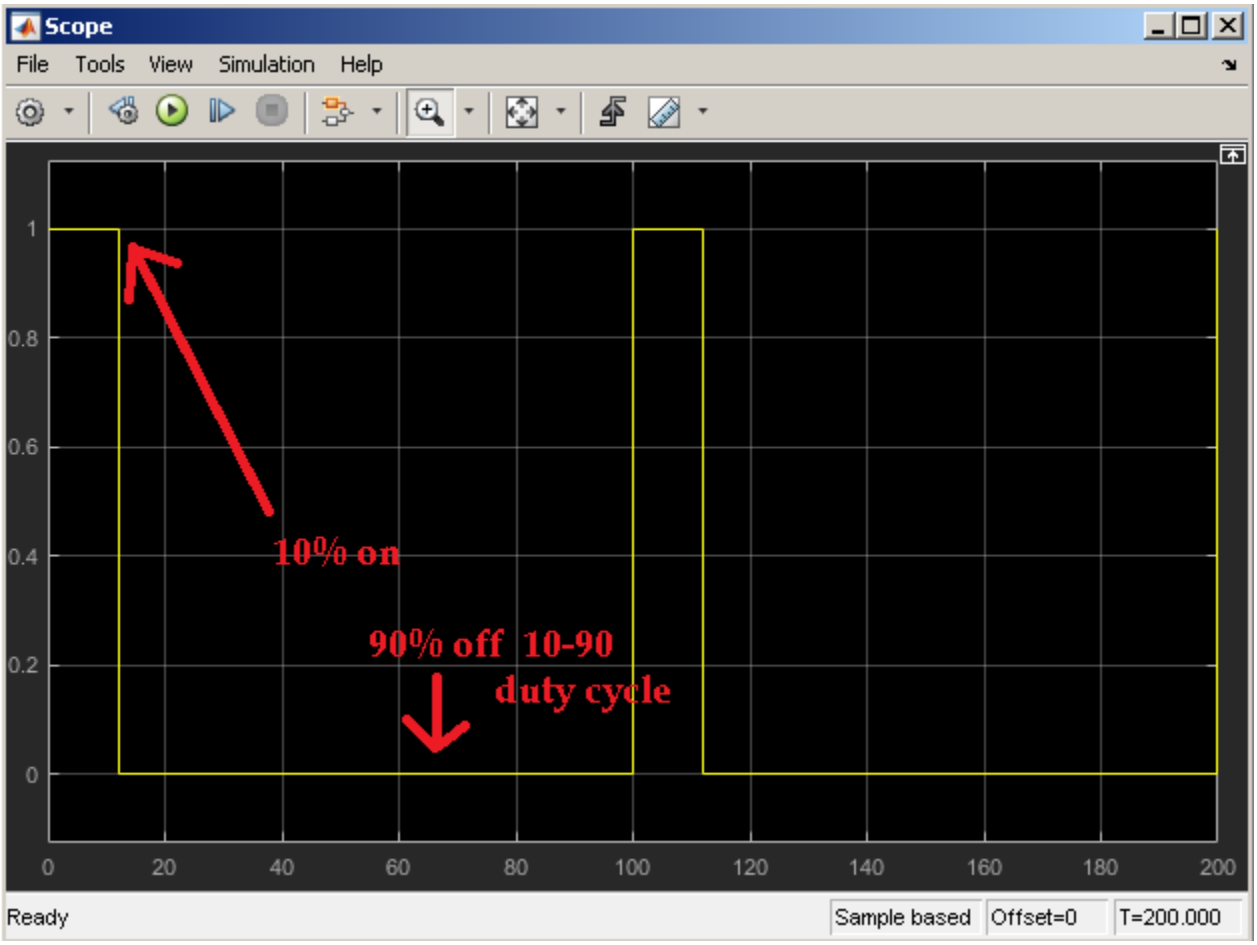
Example: Person puts in nickel, dime, quarter, dime, dime
the finite state machine goes from state 5 → state 15 → state 40 → state 50 → state 60
(get soda) (get change 10¢ back)

Another example: Person puts in quarter, quarter, quarter
the FSM goes from state 25 → state 50 → state 75
(get soda) (get change 25¢ back)

This is a MEALY Machine

7.


rst
count
<= 5
== 48


Scope
File Tools View Simulation Help
1
0.8
0.6
0.4
0.2
0
0 20 40 60 80 100 120 140 160 180 200
10% on
90% off 10-90
duty cycle
Ready
Sample based
Offset=0
T=200.000

In the scope, it is generated for 2 cycles. Each cycle having 100 periods. Everything got scaled down to smaller number for simpler scoping purposes. The original values for the 2 gigahertz clock were: 1 ms was 2,000,000,000 cycles. This was based off of the zedboard which is 50 MHZ and each ms in the zedboard is 50,000,000 cycles. The initial value of the counter is 0 and it goes up by step values of 2. Because the step values are 2, both the compare to constants are also halved. So the original compare to constants were 10 and 96. Now they are 5 and 48.