Homework 8 - ECE 1238

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8.6

S	R	Q	$\bar{Q}$
0	1	1	0
1	0	0	1
1	1	Q	$\bar{Q}$

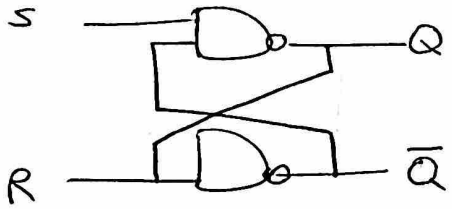
here, the '0' is the input that matters

⇒ if S = 0 ⇒ Set

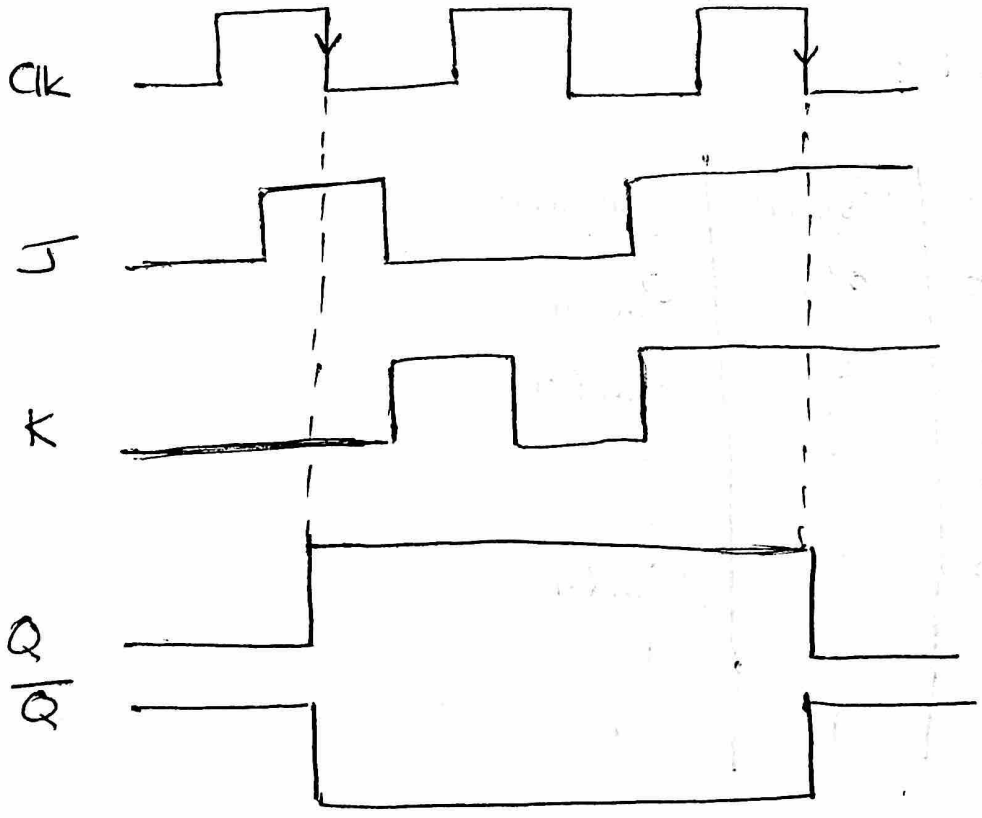
if R = 0 ⇒ Reset

⇒ This is a NAND based SR latch

Gate level design

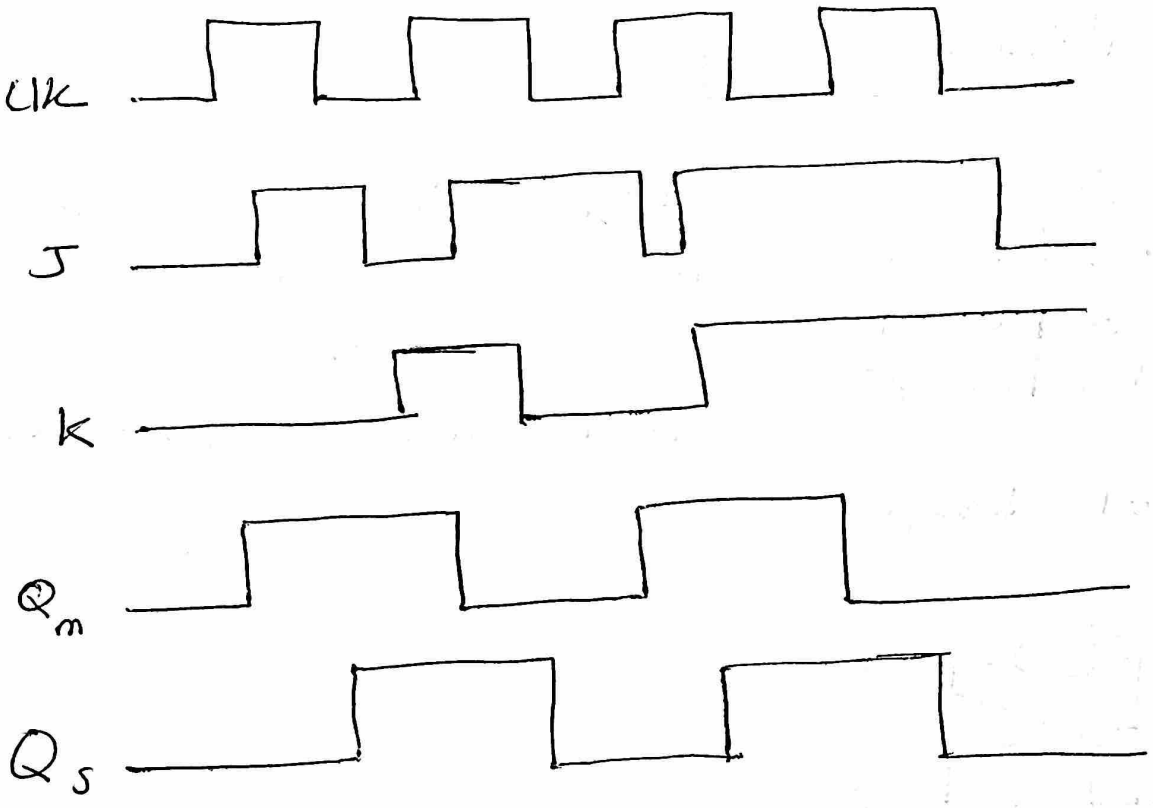


8.7



(negative-edge-triggered)

8.8



Explanation

When $Clk = 0 \Rightarrow Q_m$ unchanged

When $Clk = 1$:

J	K	$Q_{s(n+1)}$	$Q_{m(n+1)}$
0	0	0/1	$Q_m(n)$
0	1	0	$Q_m(n)$
0	1	1	0
1	0	0	1
1	0	1	$Q_m(n)$
1	1	0	1
1	1	1	0