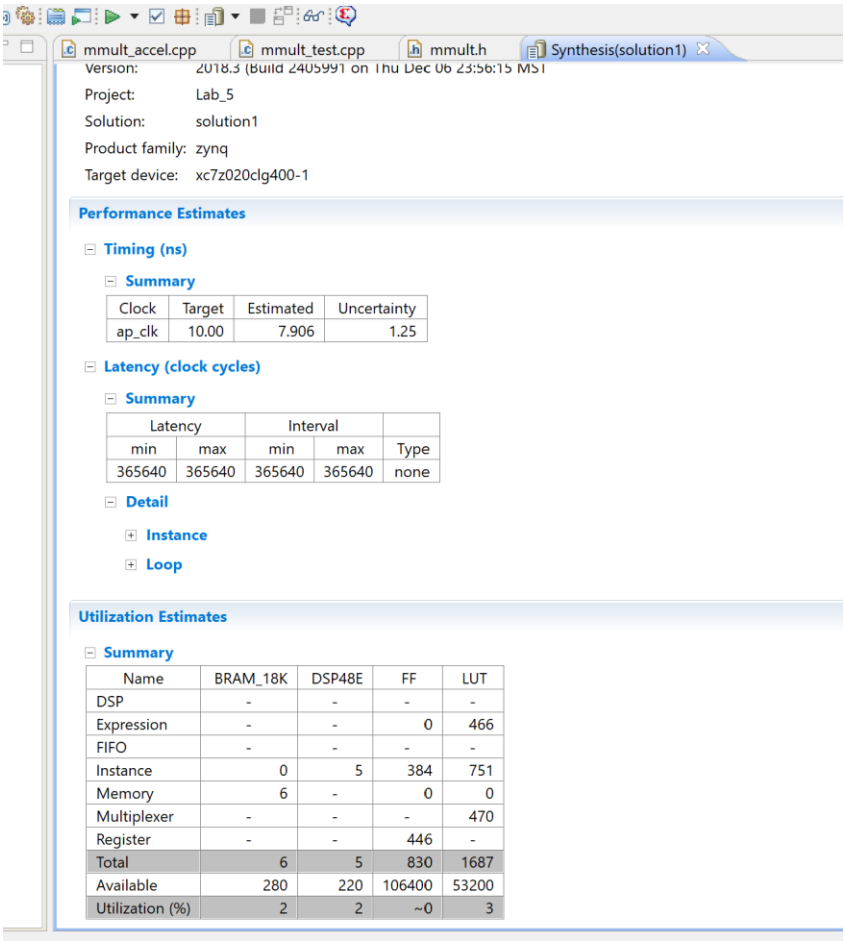
Lab5 report – Rayan Hassan

Trial 1, no optimization



mmult_accel.cpp | mmult_test.cpp | mmult.h | Synthesis(solution1)

Version: 2018.3 (Build 2405991 on Thu Dec 06 23:56:15 MST

Project: Lab_5

Solution: solution1

Product family: zynq

Target device: xc7z020clg400-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	7.906	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
365640	365640	365640	365640	none

Detail

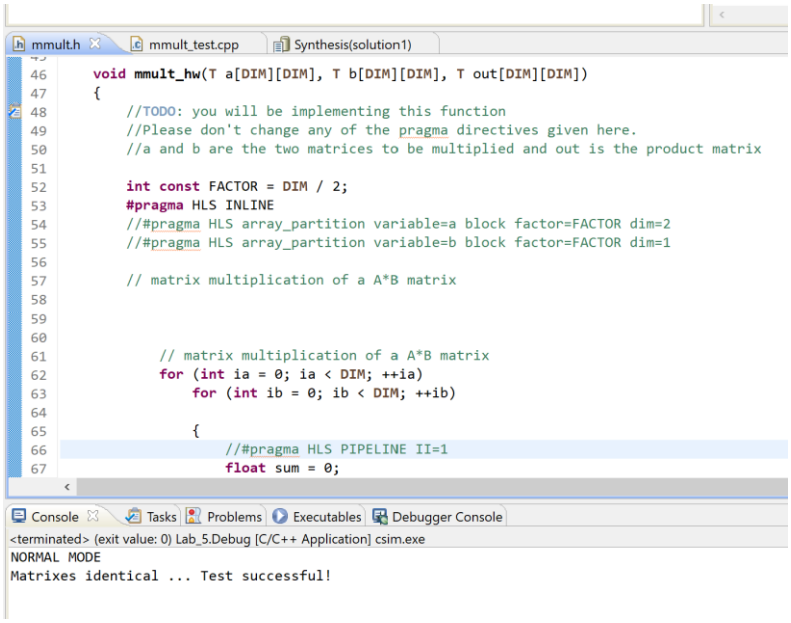
Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	466
FIFO	-	-	-	-
Instance	0	5	384	751
Memory	6	-	0	0
Multiplexer	-	-	-	470
Register	-	-	446	-
Total	6	5	830	1687
Available	280	220	106400	53200
Utilization (%)	2	2	~0	3



mmult.h | mmult_test.cpp | Synthesis(solution1)

```
46  void mmult_hw(T a[DIM][DIM], T b[DIM][DIM], T out[DIM][DIM])
47  {
48      //TODO: you will be implementing this function
49      //Please don't change any of the pragma directives given here.
50      //a and b are the two matrices to be multiplied and out is the product matrix
51
52      int const FACTOR = DIM / 2;
53      #pragma HLS INLINE
54      //#pragma HLS array_partition variable=a block factor=FACTOR dim=2
55      //#pragma HLS array_partition variable=b block factor=FACTOR dim=1
56
57      // matrix multiplication of a A*B matrix
58
59
60
61          // matrix multiplication of a A*B matrix
62          for (int ia = 0; ia < DIM; ++ia)
63              for (int ib = 0; ib < DIM; ++ib)
64
65              {
66                  //#pragma HLS PIPELINE II=1
67                  float sum = 0;
```

Console | Tasks | Problems | Executables | Debugger Console

<terminated> (exit value: 0) Lab_5.Debug [C/C++ Application] csim.exe

```
NORMAL MODE
Matrixes identical ... Test successful!
```

Trial 2, fully pipelined

In the synthesis report, we can see that the latency dropped drastically from trial 1.

Target device: xc7z020clg400-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.317	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
19615	19615	19615	19615	none

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	3295
FIFO	-	-	-	-
Instance	0	10	732	1462
Memory	6	-	0	0
Multiplexer	-	-	-	1221
Register	0	-	4328	896
Total	6	10	5060	6874
Available	280	220	106400	53200
Utilization (%)	2	4	4	12

Detail

Instance

<terminated>Lab_5.Debug [C/C++ Application]

Name

mmult.h | Synthesis(solution1) | mmult_test.cpp

```
46  void mmult_hw(T a[DIM][DIM], T b[DIM][DIM], T out[DIM][DIM])
47  {
48      //TODO: you will be implementing this function
49      //Please don't change any of the pragma directives given here.
50      //a and b are the two matrices to be multiplied and out is the product matrix
51
52      int const FACTOR = DIM / 2;
53      #pragma HLS INLINE
54      //#pragma HLS array_partition variable=a block factor=FACTOR dim=2
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57      // matrix multiplication of a A*B matrix
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59
60
61          // matrix multiplication of a A*B matrix
62          for (int ia = 0; ia < DIM; ++ia)
63              for (int ib = 0; ib < DIM; ++ib)
64
65              {
66                  #pragma HLS PIPELINE II=1
67                  float sum = 0;
68
69                  for (int id = 0; id < DIM; ++id)
70
```

Console | Tasks | Problems | Executables | Debugger Console

```
<terminated> (exit value: 0) Lab_5.Debug [C/C++ Application] csim.exe
NORMAL MODE
Matrixes identical ... Test successful!
```

Trial 3 – fully pipelined with partitioning

The latency dropped even more, as expected.

Solution: solution1
Product family: zynq
Target device: xc7z020clg400-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.092	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
4270	4270	4270	4270	none

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	538
FIFO	-	-	-	-
Instance	0	160	11172	22792
Memory	66	-	0	0
Multiplexer	-	-	-	884
Register	0	-	5021	896
Total	66	160	16193	25110
Available	280	220	106400	53200
Utilization (%)	23	72	15	47

Detail

mmult.h | Synthesis(solution1) | mmult_test.cpp

```
46  void mmult_hw(T a[DIM][DIM], T b[DIM][DIM], T out[DIM][DIM])
47  {
48      //TODO: you will be implementing this function
49      //Please don't change any of the pragma directives given here.
50      //a and b are the two matrices to be multiplied and out is the product matrix
51
52      int const FACTOR = DIM / 2;
53      #pragma HLS INLINE
54      #pragma HLS array_partition variable=a block factor=FACTOR dim=2
55      #pragma HLS array_partition variable=b block factor=FACTOR dim=1
56
57      // matrix multiplication of a A*B matrix
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61          // matrix multiplication of a A*B matrix
62          for (int ia = 0; ia < DIM; ++ia)
63              for (int ib = 0; ib < DIM; ++ib)
64
65              {
66                  #pragma HLS PIPELINE II=1
67                  float sum = 0;
```

Console | Tasks | Problems | Executables | Debugger Console

```
<terminated> (exit value: 0) Lab_5.Debug [C/C++ Application] csim.exe
NORMAL MODE
Matrixes identical ... Test successful!
```