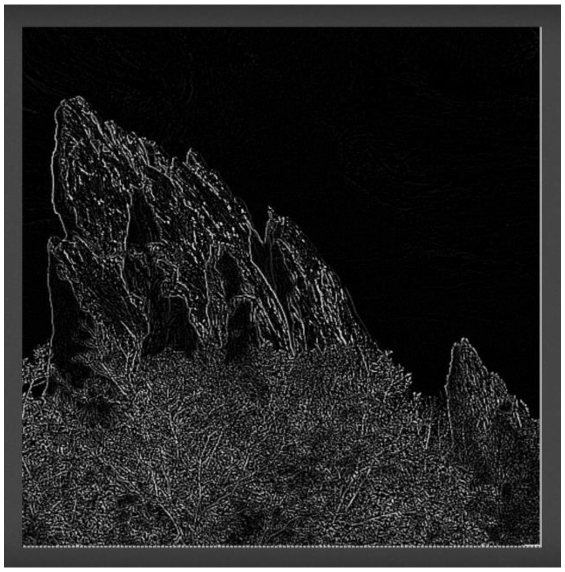
Lab 6 report – Rayan Hassan

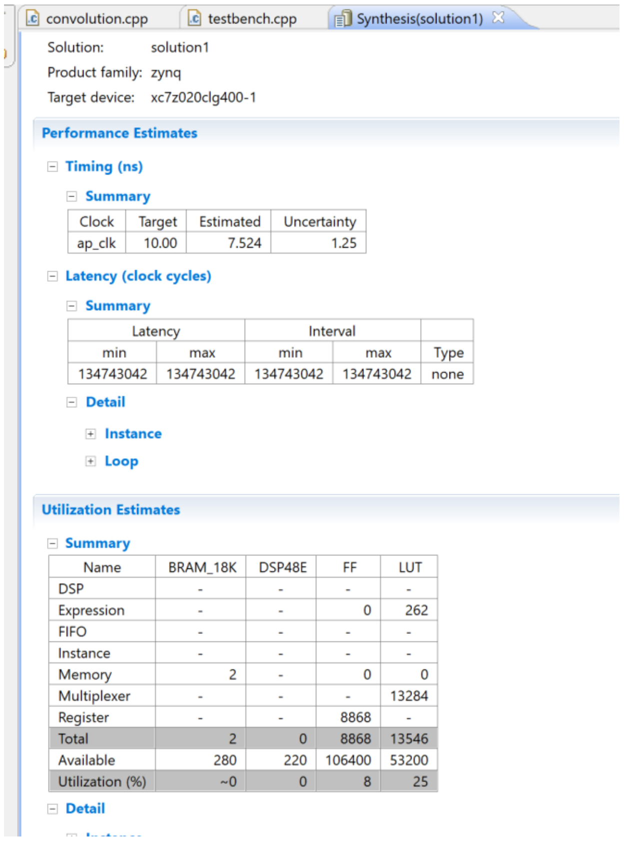
<u>sw_conv</u>

The following picture corresponds to the software convolution implemented.



<u>Hw_conv: line buffers implemented as shift registers</u>

This is the utilization summary.



Solution: solution1
Product family: zynq
Target device: xc7z020clg400-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	7.524	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
134743042	134743042	134743042	134743042	none

Detail

Instance

Loop

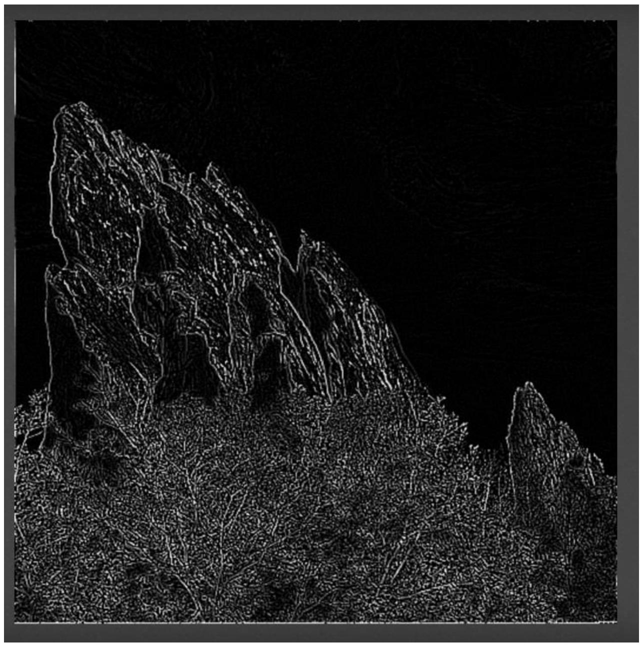
Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	262
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	2	-	0	0
Multiplexer	-	-	-	13284
Register	-	-	8868	-
Total	2	0	8868	13546
Available	280	220	106400	53200
Utilization (%)	~0	0	8	25

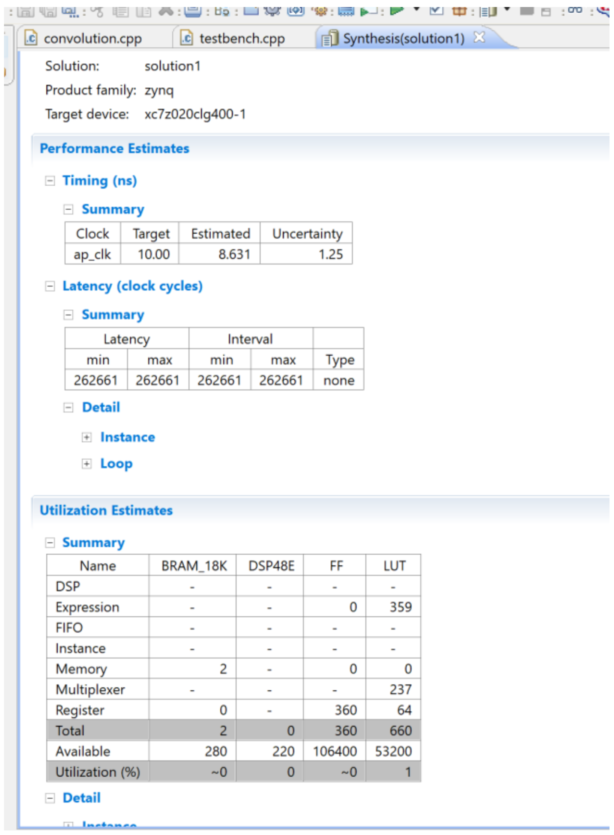
Detail

This is the generated image, which is similar to the sw_conv one as expected.



<u>Hw_conv: line buffers implemented as ring buffers</u>

I wrote comments that explain my thought process in the convolution.cpp file. I used modulo to implement the line buffers as ring buffers. Here is the utilization report.



Solution: solution1
Product family: zynq
Target device: xc7z020clg400-1

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	8.631	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
262661	262661	262661	262661	none

Detail

Instance

Loop

Utilization Estimates

Summary

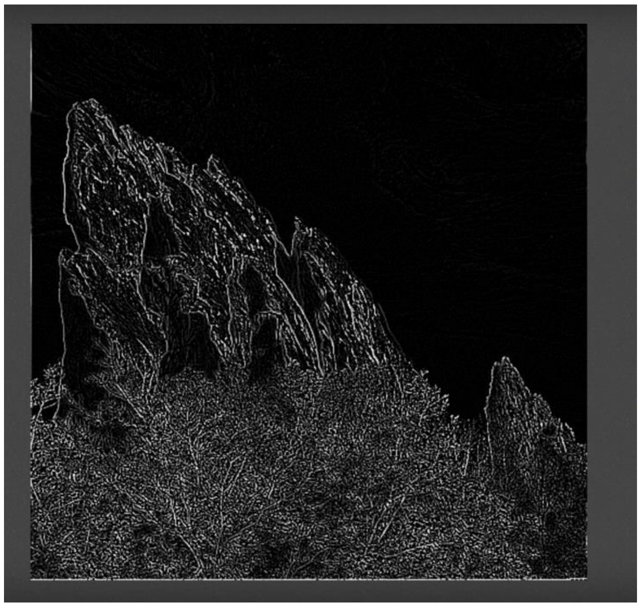
Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	359
FIFO	-	-	-	-
Instance	-	-	-	-
Memory	2	-	0	0
Multiplexer	-	-	-	237
Register	0	-	360	64
Total	2	0	360	660
Available	280	220	106400	53200
Utilization (%)	~0	0	~0	1

Detail

Instance

As expected, the ring buffer implementation takes less time, which is why latency is much lower.

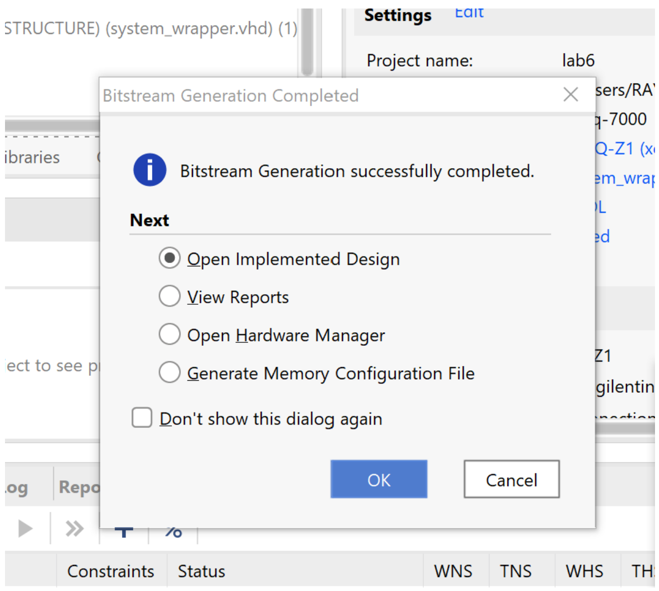
Here is the generated hw_conv picture:



As expected, it is similar to the previous pictures.

Generating bit stream

The following picture shows that I was able to generate bitstream successfully.



Bitstream Generation Completed

Bitstream Generation successfully completed.

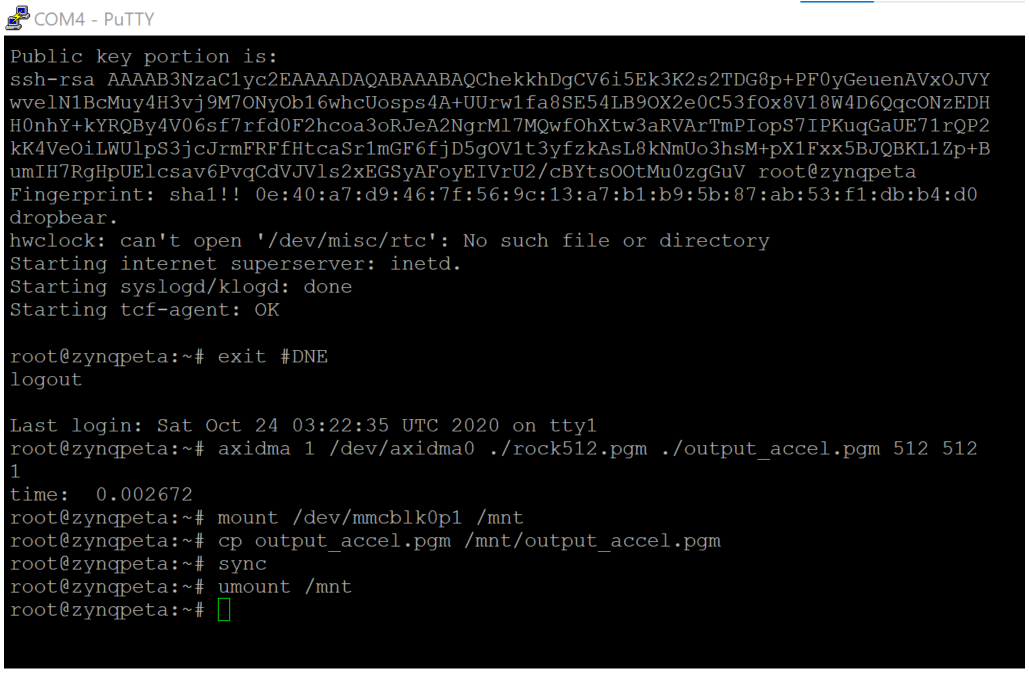
Next

- [✓ Open Implemented Design]
- View Reports
- Open Hardware Manager
- Generate Memory Configuration File

Don't show this dialog again

Running the accelerator

This is a screenshot of the putty window and all the commands I ran.


COM4 - PuTTY

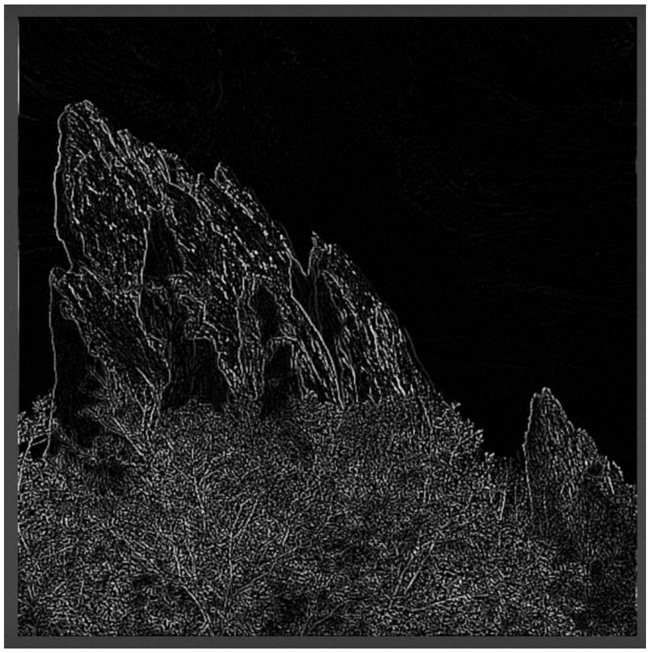
```
Public key portion is:
ssh-rsa AAAAB3NzaC1yc2EAAAADAQABAAABAQChekkhDgCV6i5Ek3K2s2TDG8p+PF0yGeuenAVxOJVY
wvelN1BcMuy4H3vj9M7ONyOb16whcUosps4A+UUrw1fa8SE54LB9OX2e0C53fOx8V18W4D6QqcONzEDH
H0nhY+kYRQBy4V06sf7rfd0F2hcoa3oRJeA2NgrMl7MQwfOhXtw3aRVArTmPIopS7IPKuqGaUE71rQP2
kK4VeOiLWUlpS3jcJrmFRFfHtcaSr1mGF6fjD5gOV1t3yfzkAsL8kNmUo3hsM+pX1Fxx5BJQBKL1Zp+B
umIH7RgHpUElcsav6PvqCdVJVls2xEGSyAFoyEIVrU2/cBYtsOOtMu0zgGuV root@zynqpeta
Fingerprint: sha1!! 0e:40:a7:d9:46:7f:56:9c:13:a7:b1:b9:5b:87:ab:53:f1:db:b4:d0
dropbear.
hwclock: can't open '/dev/misc/rtc': No such file or directory
Starting internet superserver: inetd.
Starting syslogd/klogd: done
Starting tcf-agent: OK

root@zynqpeta:~# exit #DNE
logout

Last login: Sat Oct 24 03:22:35 UTC 2020 on tty1
root@zynqpeta:~# axidma 1 /dev/axidma0 ./rock512.pgm ./output_accel.pgm 512 512
1
time:  0.002672
root@zynqpeta:~# mount /dev/mmcblk0p1 /mnt
root@zynqpeta:~# cp output_accel.pgm /mnt/output_accel.pgm
root@zynqpeta:~# sync
root@zynqpeta:~# umount /mnt
root@zynqpeta:~#
```

The execution time is 0.002672 s.

The generate convoluted picture from the accelerator is shown below



It worked successfully and the picture is identical to the other ones (hw_conv and sw_conv).