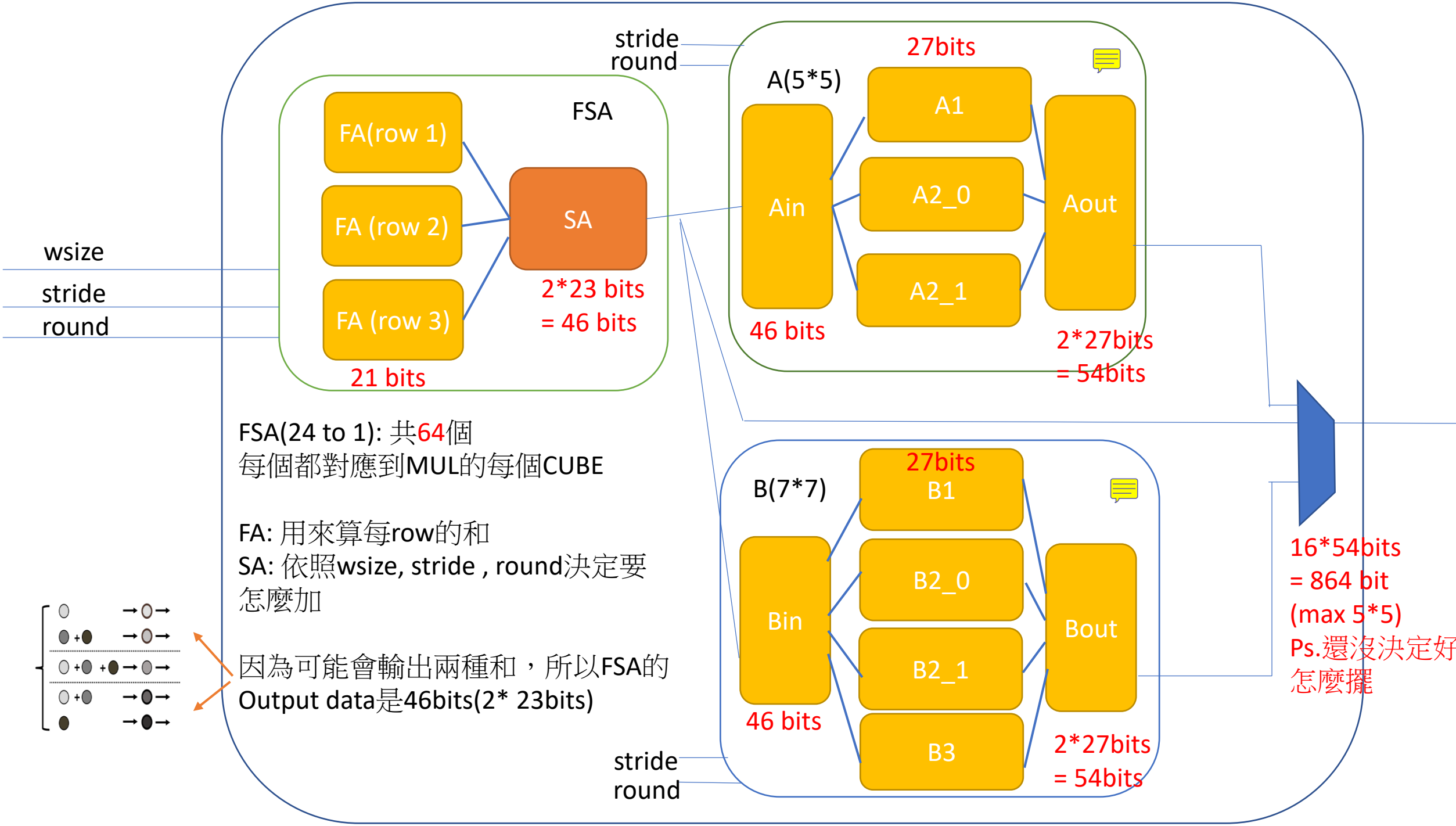

stride
round
FSA
FA(row 1)
FA (row 2)
FA (row 3)
SA
21 bits
2*23 bits
= 46 bits
wsize
stride
round
A(5*5)
27bits
A1
Ain
A2_0
A2_1
Aout
46 bits
2*27bits
= 54bits
FSA(24 to 1): 共64個
每個都對應到MUL的每個CUBE
FA: 用來算每row的和
SA: 依照wsize, stride , round決定要怎麼加
因為可能會輸出兩種和，所以FSA的Output data是46bits(2* 23bits)
B(7*7)
27bits
B1
Bin
B2_0
B2_1
B3
Bout
46 bits
2*27bits
= 54bits
stride
round
16*54bits
= 864 bit
(max 5*5)
Ps.還沒決定好怎麼擺

3*3

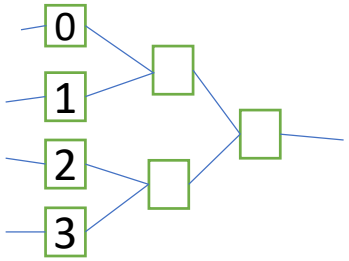
NO3_0 ~NO3_ 5 : 1 + 2 + 3
NO3_6 : 3 , 1 + 2
NO3_7 : 1 , 2 + 3

1: FA(row1)'s output
2: FA(row2)'s output
3: FA(row3)'s output

5*5

Stride1,round1
(NO5_0 ~ NO5_3)

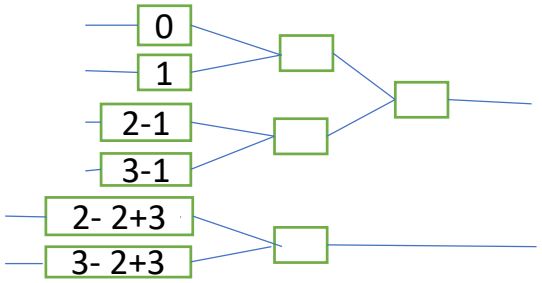
0 1 2	ID0,1 1 + 2 + 3
3 4	ID2,3 1 + 2 + 3



Stride1,round2

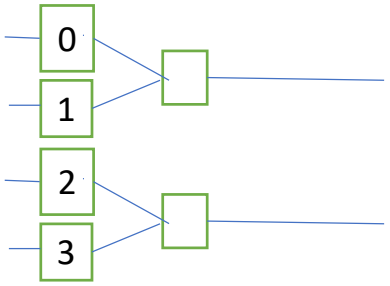
NO5_0

4 5 6	ID0,1 1 + 2 + 3
7 1	ID2,3 1 2 + 3



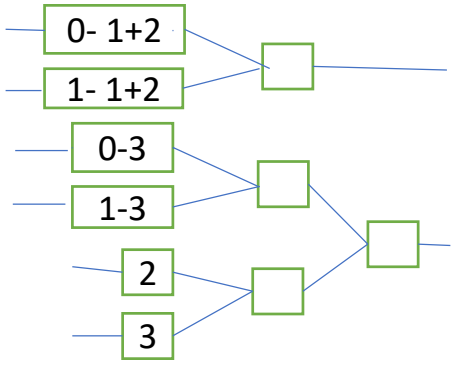
NO5_1

5 6 7	ID0,1 1 + 2 + 3
0 1	ID2,3 1 + 2 + 3



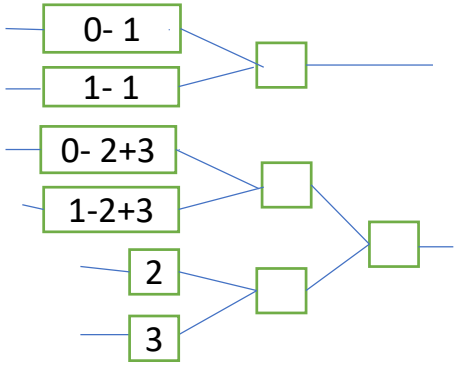
NO5_2

6 7 0	ID0,1 1 + 2 3
1 2	ID2,3 1 + 2 + 3



NO5_3

7 0 1	ID0,1 1 2 + 3
2 3	ID2,3 1 + 2 + 3



Stride2

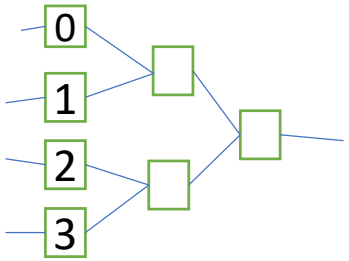
NO5_0

0
1
2

ID0,1
1 + 2 + 3

3
4

ID2,3
1 + 2 + 3



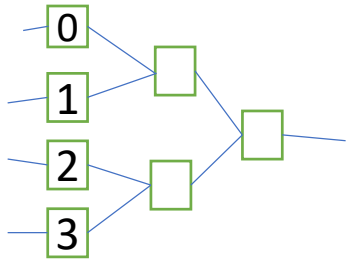
NO5_1

2
3
4

ID0,1
1 + 2 + 3

5
6

ID2,3
1 + 2 + 3



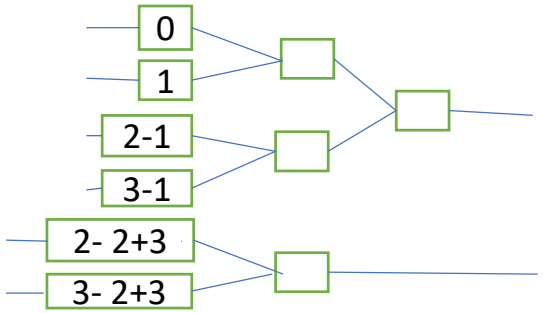
NO5_2

4
5
6

ID0,1
1 + 2 + 3

7
1

ID2,3
1
2 + 3



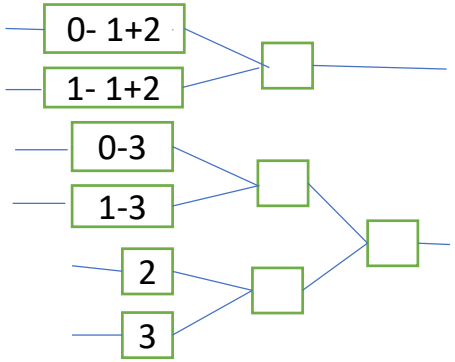
NO5_3

6
7
0

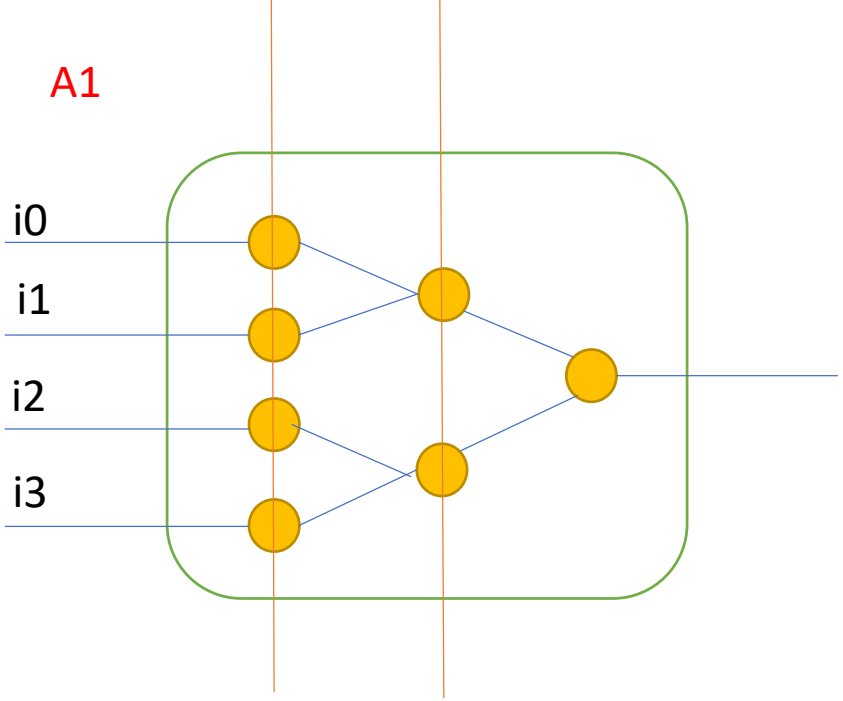
ID0,1
1 + 2
3

1
2

ID2,3
1 + 2 + 3

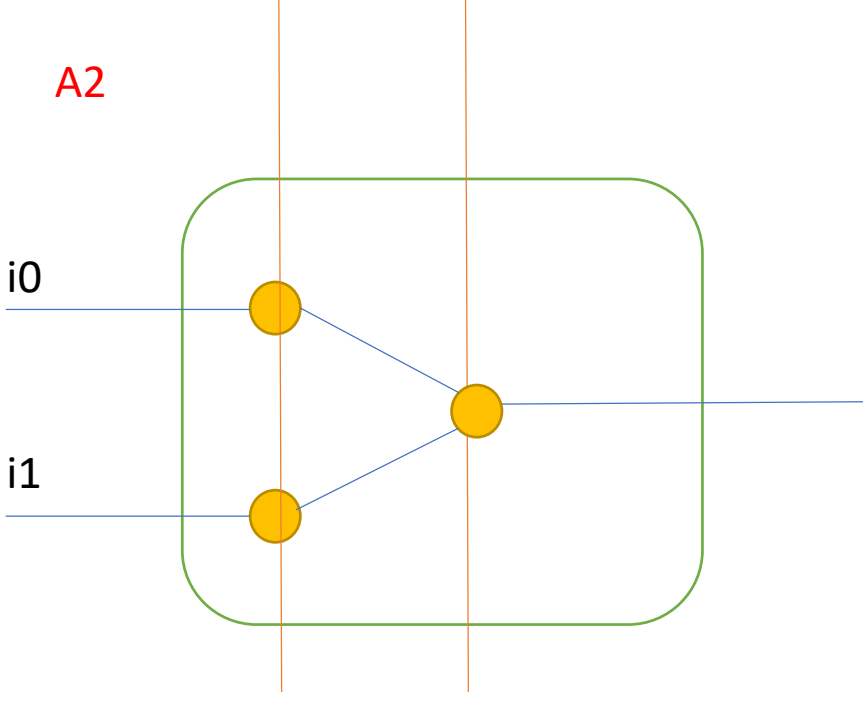


A1

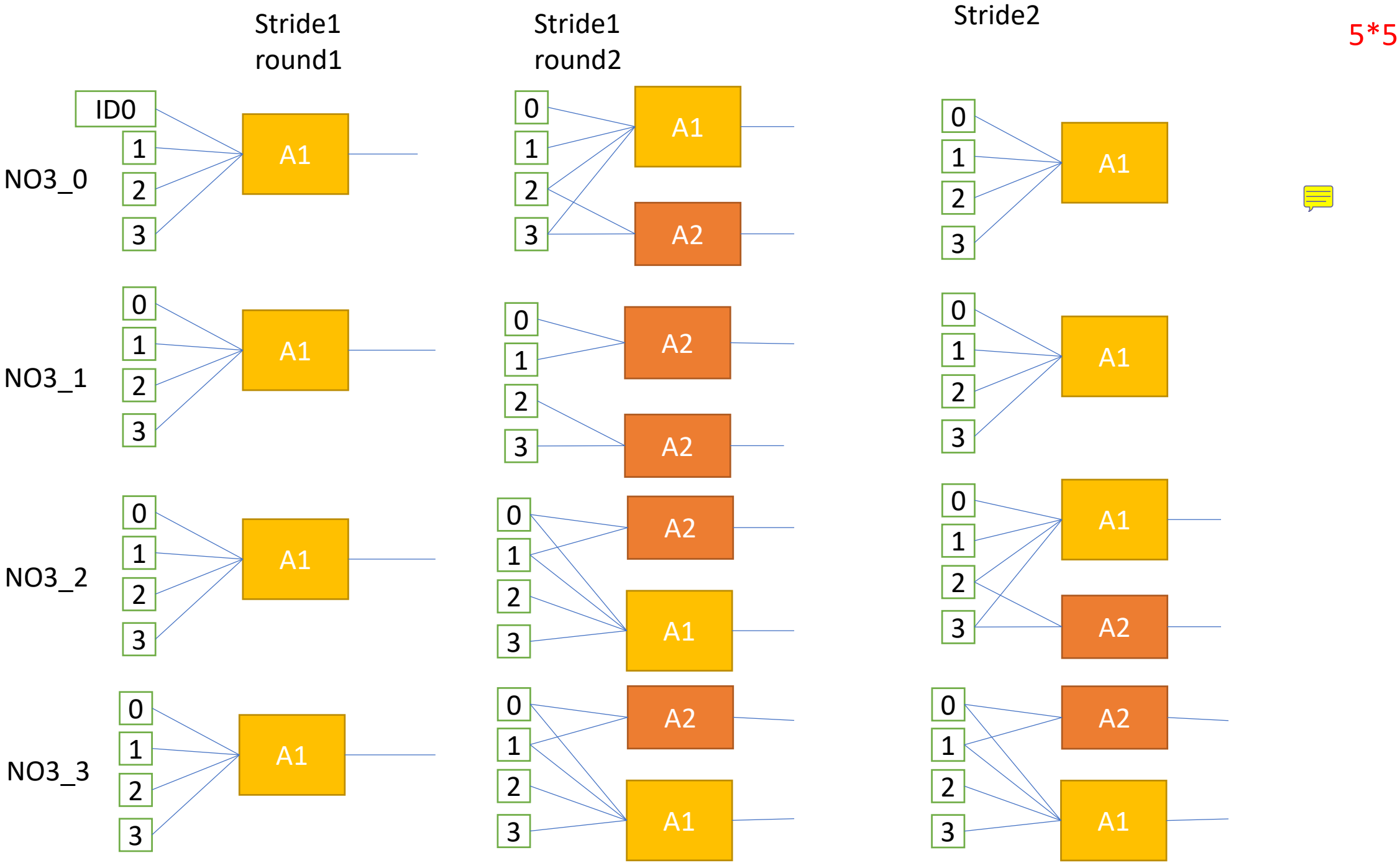


23 bits 24 bits 27 bits

A2



23 bits 24 bits 27 bits


Stride1
round1
Stride1
round2
Stride2
5*5
NO3_0
NO3_1
NO3_2
NO3_3
ID0
0
1
2
3
A1
A2

7*7

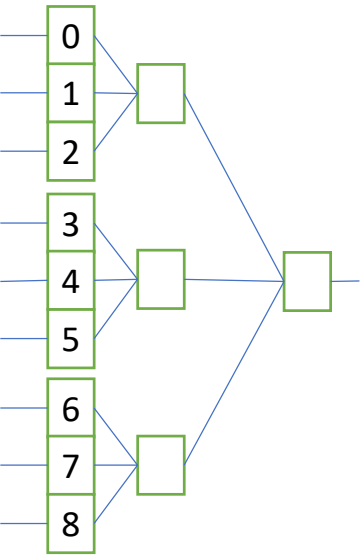
1: FA(row1)'s output
2: FA(row2)'s output
3: FA(row3)'s output

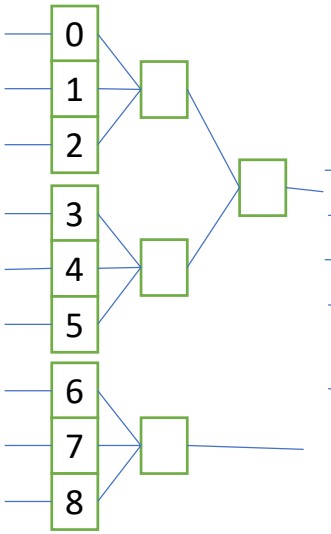
Stride1,round1 (NO7_0 , NO7_1)	
0 1 2	ID0,1,2 1 + 2 + 3
3 4 5	ID3,4,5 1 + 2 + 3
6	ID6,7,8 1 + 2 + 3

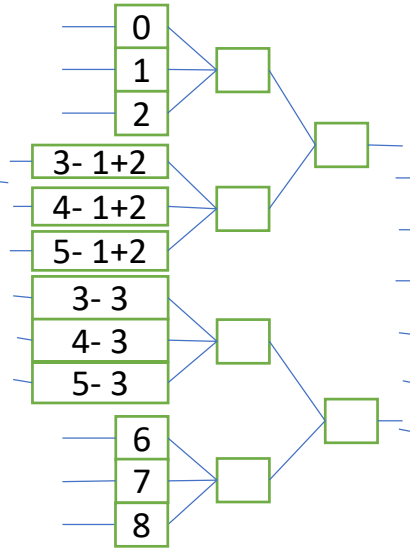
Stride1,round2 NO7_0		N07_1	
2 3 4	ID0,1,2 1 + 2 + 3	3 4 5	ID0,1,2 1 + 2 + 3
5 6 7	ID3,4,5 1 + 2 + 3	6 7 0	ID3,4,5 1 + 2 3
0	ID6,7,8 1 + 2 + 3	1	ID6,7,8 1 + 2 + 3

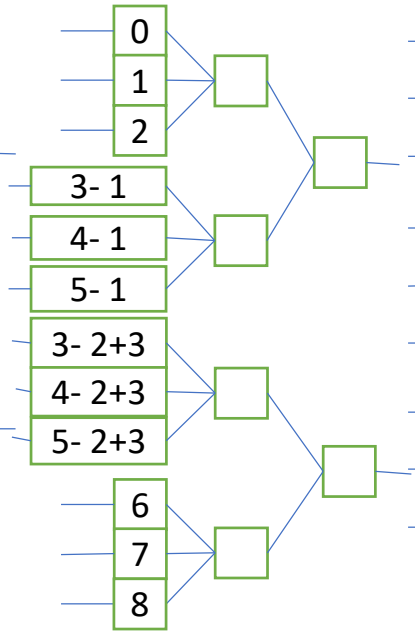
Stride1,round3 NO7_0		N07_1	
4 5 6	ID0,1,2 1 + 2 + 3	5 6 7	ID0,1,2 1 + 2 + 3
7 0 1	ID3,4,5 1 2 + 3	0 1 2	ID3,4,5 1 + 2 + 3
2	ID6,7,8 1 + 2 + 3	3	ID6,7,8 1 + 2 + 3

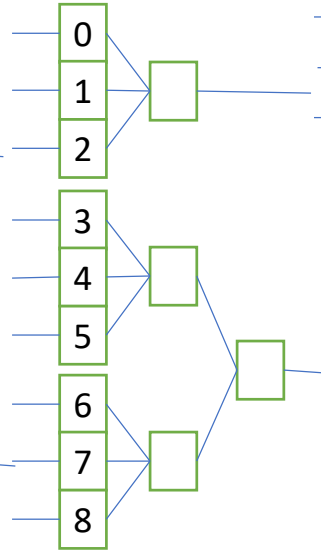
Stride1,round4 NO7_0		N07_1	
6 7 0	ID0,1,2 1 + 2 3	7 0 1	ID0,1,2 1 2 + 3
1 2 3	ID3,4,5 1 + 2 + 3	2 3 4	ID3,4,5 1 + 2 + 3
4	ID6,7,8 1 + 2 + 3	5	ID6,7,8 1 + 2 + 3

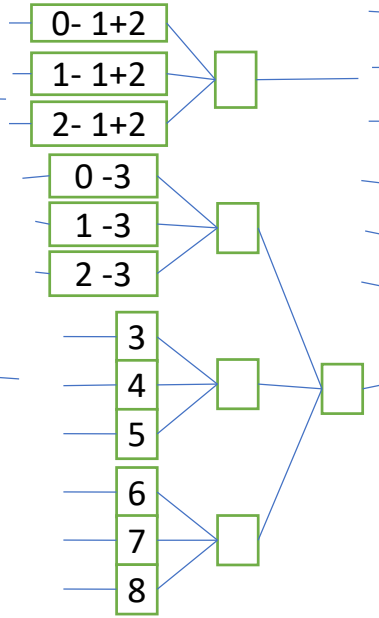


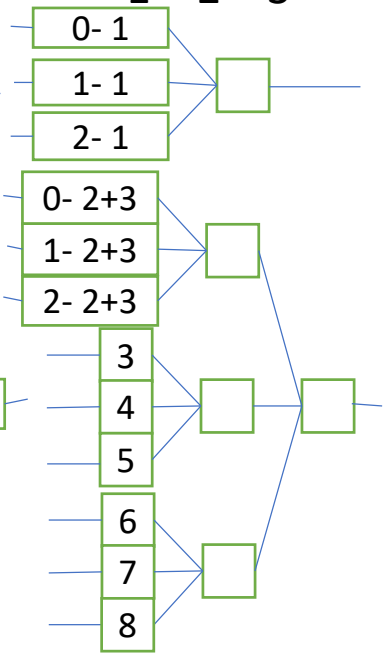










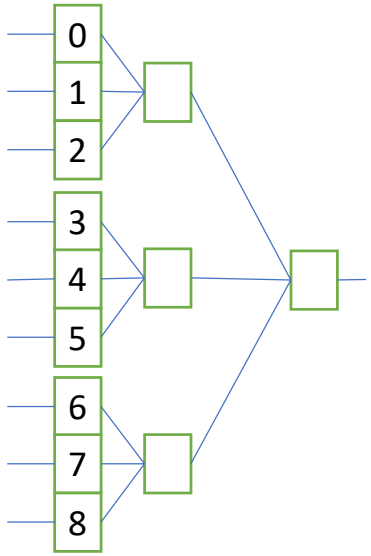


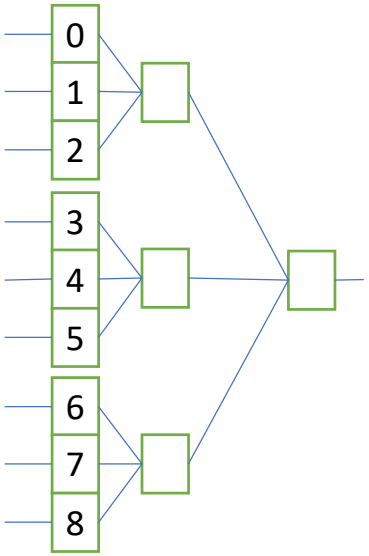
Stride2,round1

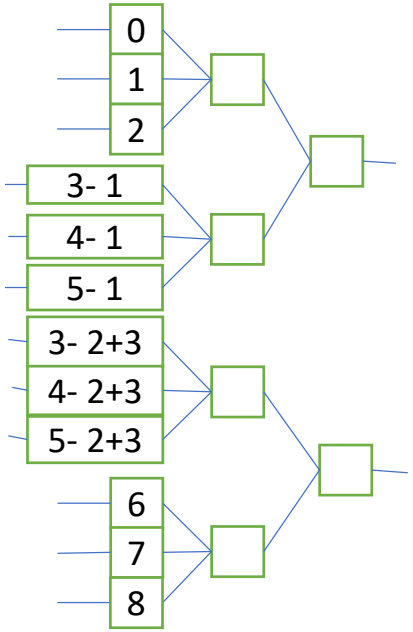
NO7_0		N07_1	
0 1 2	ID0,1,2 1 + 2 + 3	2 3 4	ID0,1,2 1 + 2 + 3
3 4 5	ID3,4,5 1 + 2 + 3	5 6 7	ID3,4,5 1 + 2 + 3
6	ID6,7,8 1 + 2 + 3	0	ID6,7,8 1 + 2 + 3

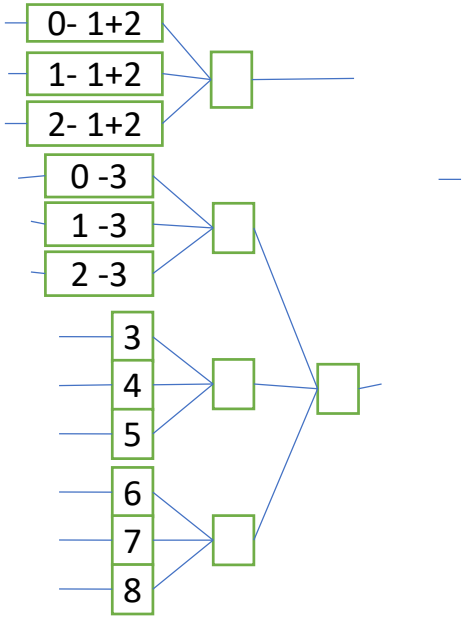
Stride2,round2

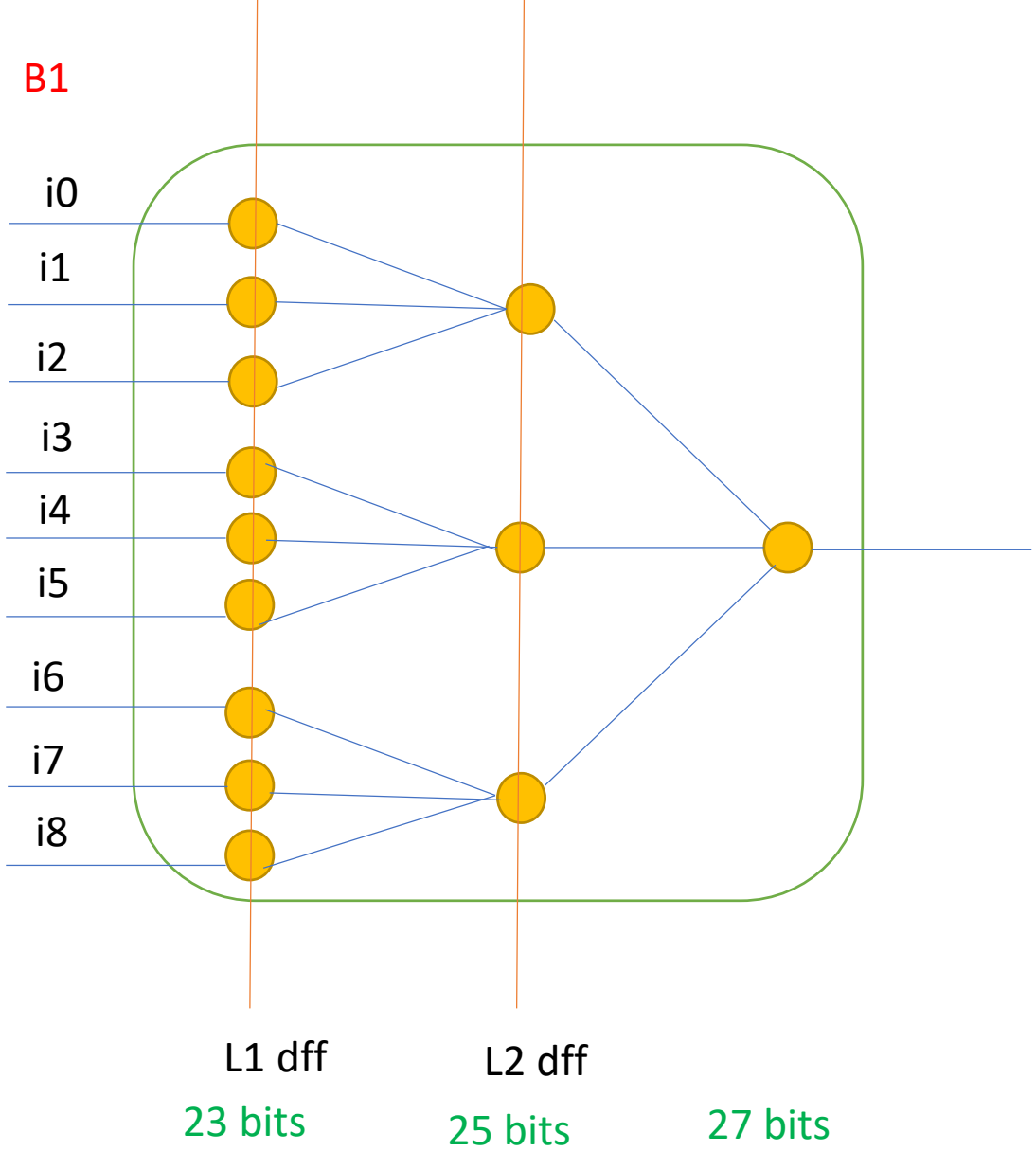
NO7_0		N07_1	
4 5 6	ID0,1,2 1 + 2 + 3	6 7 0	ID0,1,2 1 + 2 3
7 0 1	ID3,4,5 1 2 + 3	1 2 3	ID3,4,5 1 + 2 + 3
2	ID6,7,8 1 + 2 + 3	4	ID6,7,8 1 + 2 + 3

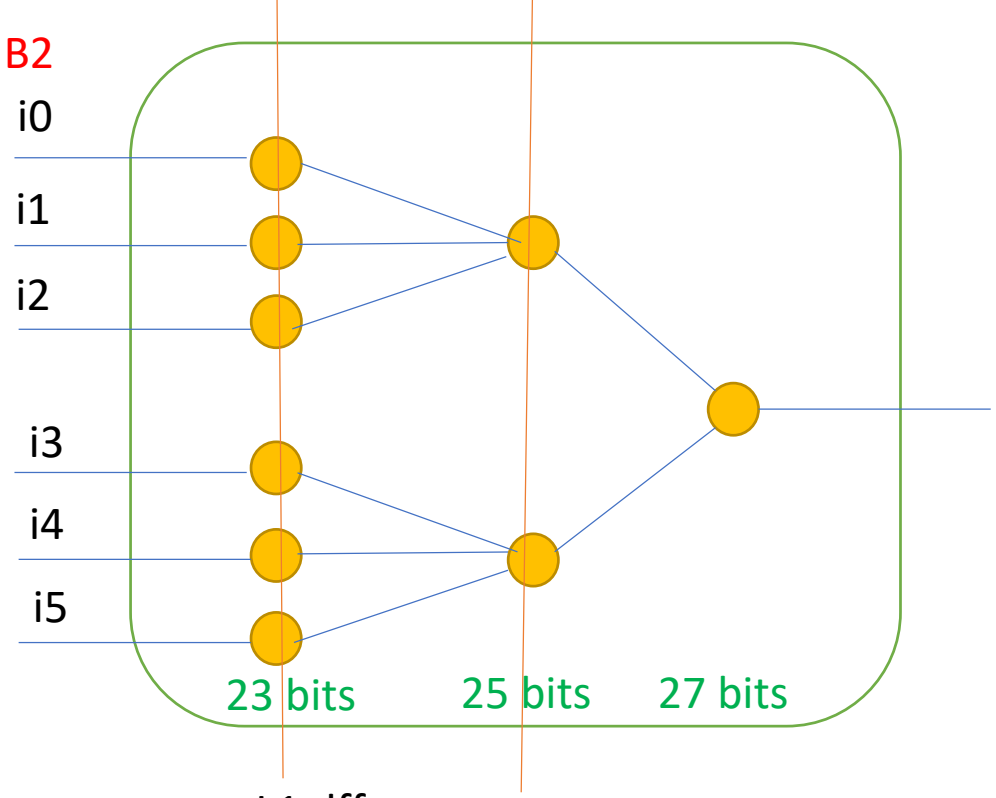


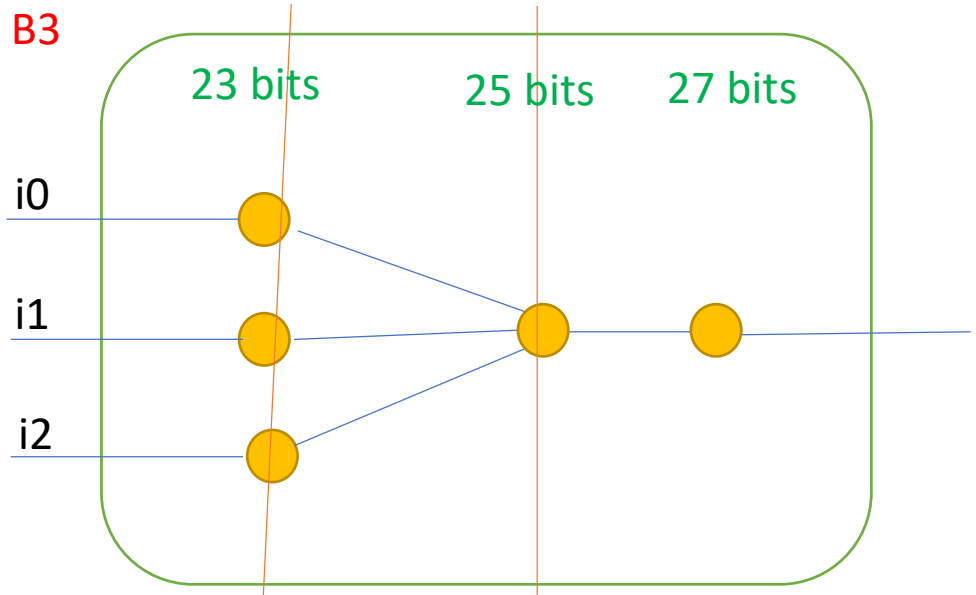


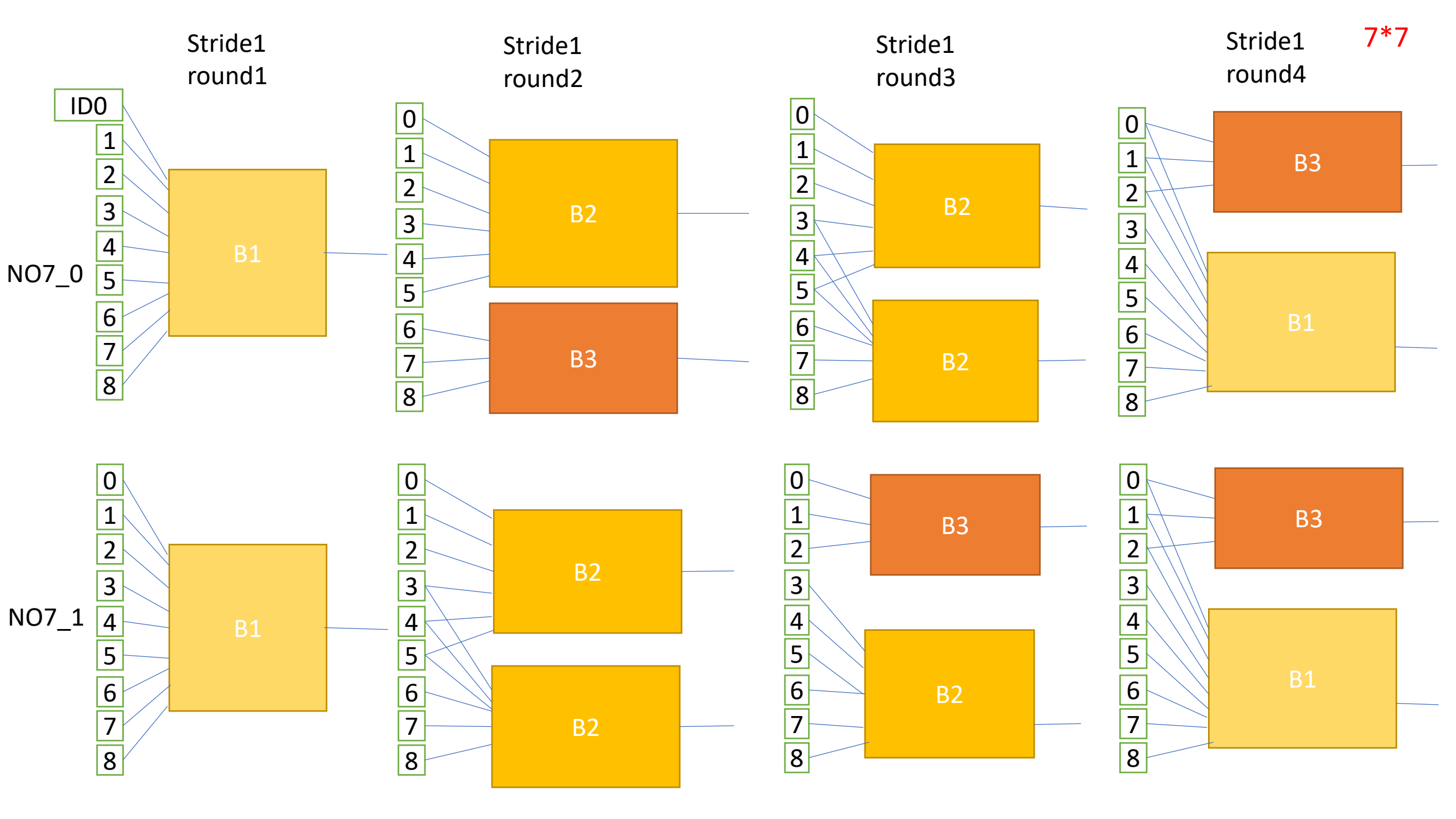





B1
i0
i1
i2
i3
i4
i5
i6
i7
i8
L1 dff
L2 dff
23 bits
25 bits
27 bits


B2
i0
i1
i2
i3
i4
i5
23 bits
25 bits
27 bits
L1 dff
L2 dff


B3
23 bits
25 bits
27 bits
i0
i1
i2

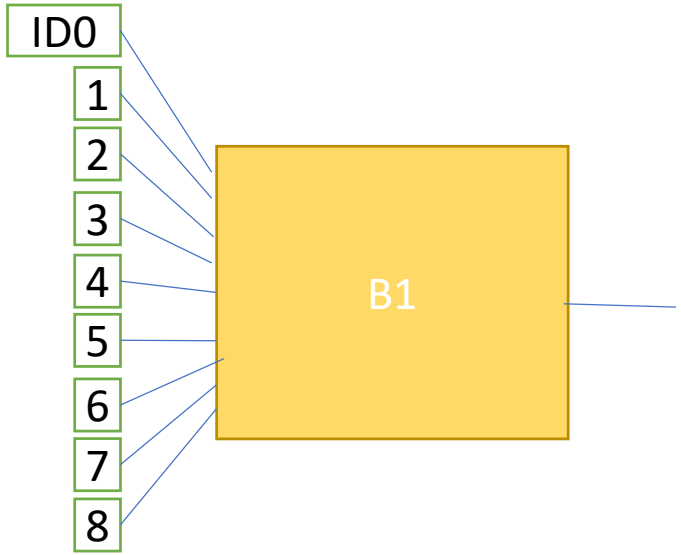

Stride1
round1
Stride1
round2
Stride1
round3
Stride1
round4
7*7
ID0
NO7_0
NO7_1
0
1
2
3
4
5
6
7
8
B1
B2
B3

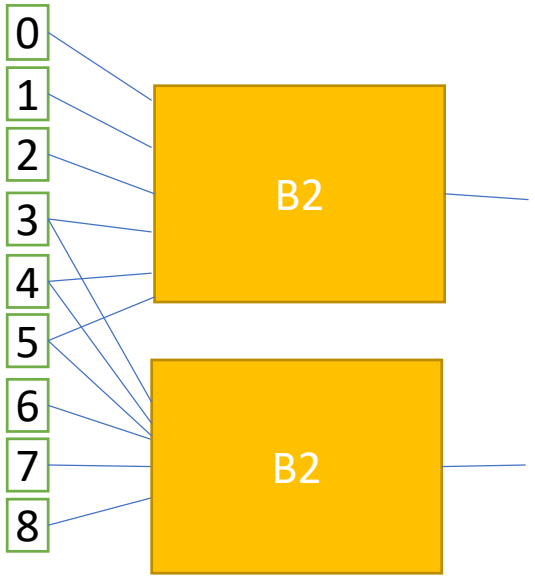
7*7

Stride2
round1

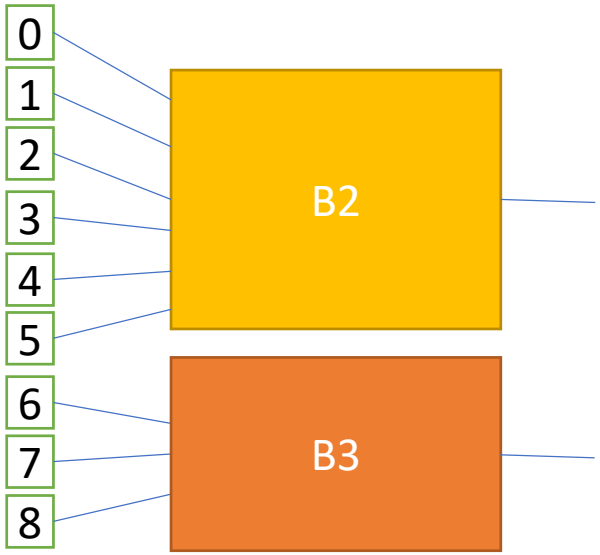
Stride2
round2

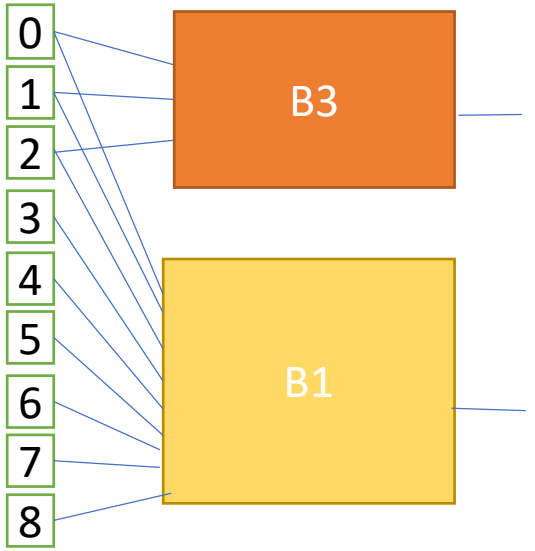
NO7_0

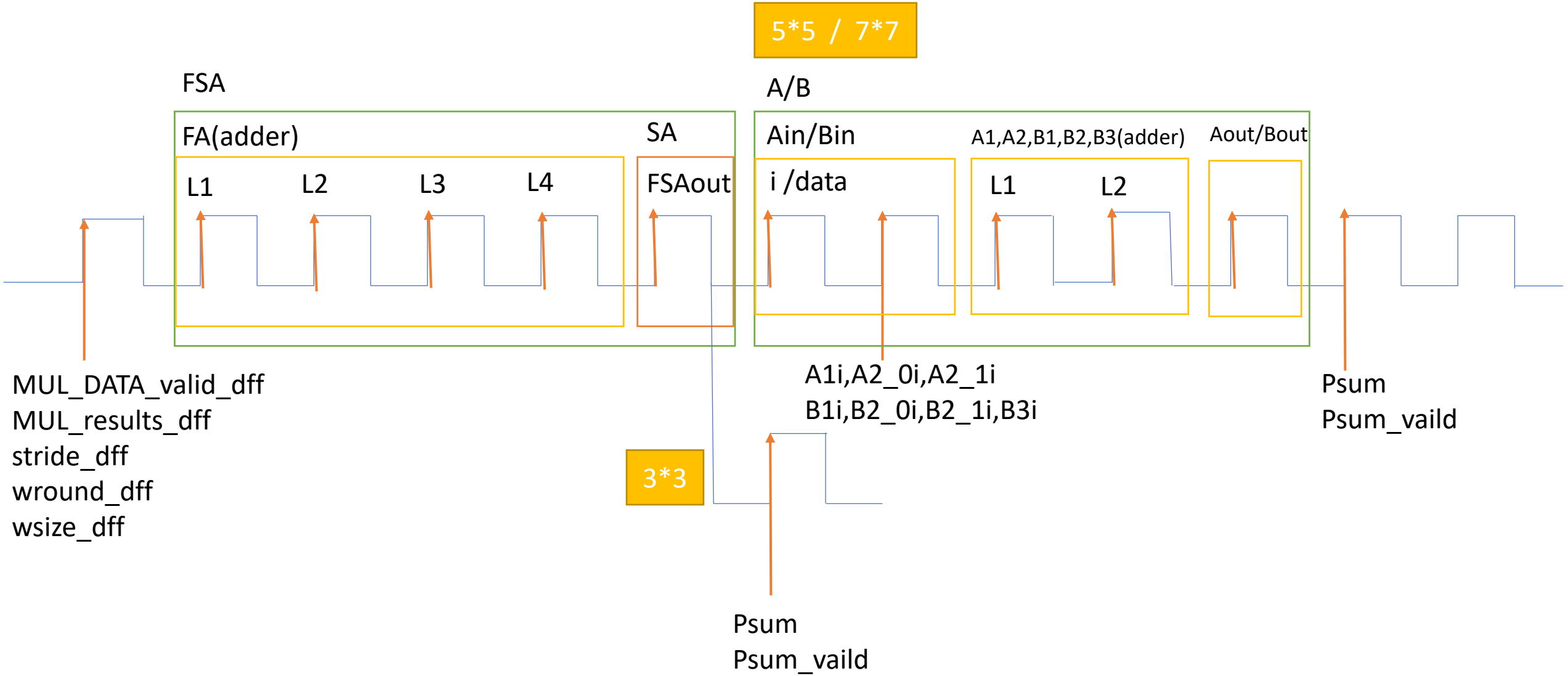




NO7_1






5*5 / 7*7
FSA
A/B
FA(adder)
SA
Ain/Bin
A1,A2,B1,B2,B3(adder)
Aout/Bout
L1
L2
L3
L4
FSAout
i /data
L1
L2
MUL_DATA_valid_dff
MUL_results_dff
stride_dff
wround_dff
wsize_dff
A1i,A2_0i,A2_1i
B1i,B2_0i,B2_1i,B3i
Psum
Psum_vaild
3*3
Psum
Psum_vaild