COMP 531: Assignment 3

Winter 2016

Due Monday March 7th

Each question is worth 12.5 points. Don't hesitate to use the office hours. You can submit the assignment in class on the due date, or, if you TeX it, by e-mail to harrison.humphrey@mail.mcgill.ca before midnight. A word of caution: Q1 is tricky, and you should follow the hint. If you google the question, you'll find a very confusing sketch of a proof on stackexchange. Don't copy this.

Question 1

Show that the sum of $log(n)$ n-bit integers can be computed in AC^0. Consider the following hint. Let $r = sqrt(logn)$.

Imagine the numbers being added as $log(n)$ rows of n-bits. Divide these rows into groups of size r. Further divide each grouping, by splitting the columns into groups of size r. How many bits are in each subdivision? Take the sum of the numbers in each subdivision, and combine them into a sum for the group of rows. Finally, repeat for each row. It will help to draw things out.

Question 2

Show that the multiplication of two n-bit integers cannot be computed in AC^0.

Question 3

A counting argument shows that almost all n-input boolean functions have minimal circuit size $\Omega(2^n/n)$. Show that this bound can be matched. In other words, show that any boolean function can be computed by a bounded fan-in circuit of size $O(2^n/n)$.

Hint: You should treat the last $log(n - logn)$ bits seperately from the remainder. Start by computing all possible functions on these last few bits. How many gates does this require? How can you use this to design a circuit for the original function? Remember that if you have a function $f(x_1, x_2, \ldots, x_n)$ then you can represent it as follows:

$$f(x_1, x_2, \ldots, x_n) = [x_1 \wedge f(1, x_2, \ldots, x_n)] \vee [(\neg x_1) \wedge f(0, x_2, \ldots, x_n)]$$

Question 4

Show that for any circuit consisting of a layer of $PARITY$ gates feeding into an AND gate, there exists a circuit of linear size computing the same function.