CSE511- Mid Project Evaluation

Group 9

ISA to implement

synaptic weight loading instructions					
imm[11:0]	**rs1[4:0]**	**funct3[2:0]**	**rd[4:0]**		**opcode[6:0]**
offset	base	lw.wv	WVR_dst		CUSTOM
imm[11:0]	**rs1[4:0]**	**funct3[2:0]**	**hint[0]**	**rd[3:0]**	**opcode[6:0]**
offset	base	lh.wv	hint	WVR_dst	CUSTOM
offset	base	la.wv	hint	WVR_dst	CUSTOM
spike vector loading instructions					
imm[11:0]	**rs1[4:0]**	**funct3[2:0]**	**hint[0]**	**rd[3:0]**	**opcode[6:0]**
offset	base	lw.sv	SVR_dst		CUSTOM
imm[11:0]	**rs1[4:0]**	**funct3[2:0]**	**hint[0]**	**rd[3:0]**	**opcode[6:0]**
offset	base	lh.sv	hint	SVR_dst	CUSTOM
offset	base	la.sv	hint	SVR_dst	CUSTOM

Assumptions

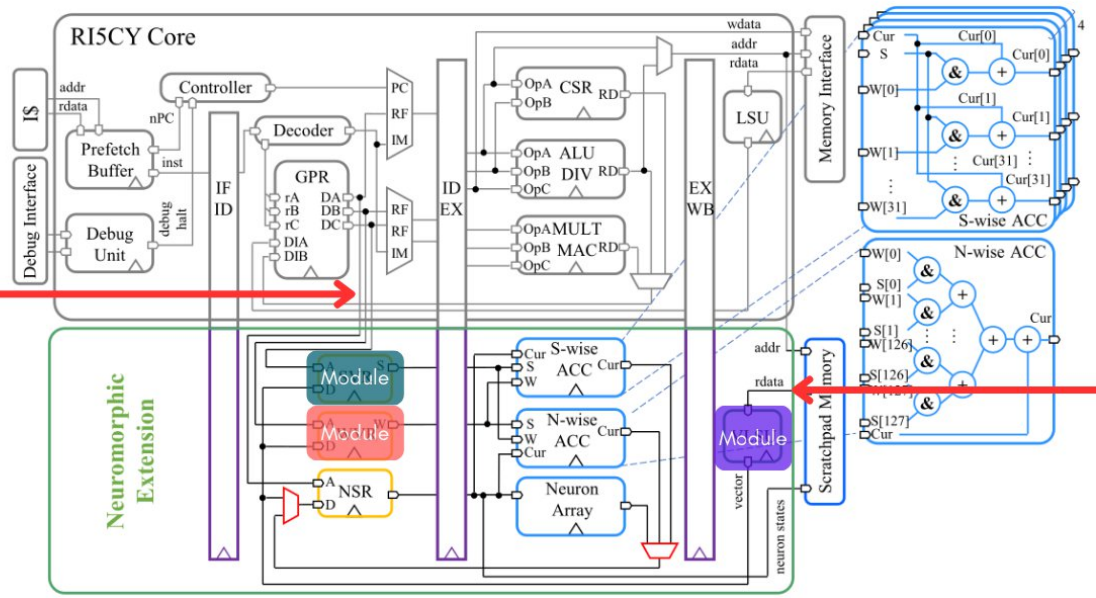
- Vector signal / D signal has a width of 512 bits
- ‘A’ signal: 8 bits - 5 bits for rd and 3 bits for funct3

funct3	rd
7:5	4:0

- 1 WVR register holds 8 weights => 1 weight = 4 bits
- 1 SVR register holds 32 spikes => 1 spike = 1 bit (future)
- lw = 1, lh = 4, la = 16 (rd sets the starting register)

Approach

Decode signals simulated in the testbench for various instructions



rdata signal set in the testbench

Demo