**Main control Truth Table:**

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Opcode | RegDes | RegWr | RegWr2 | | ExtOp | | ALUSrc | | Mem\_Rd | | Mem\_Wr | | WB\_data | | PushSig | PopSig |  |
| R-type | 1 🡪 Rd | 1 | 0 | | X | | 0 | | 0 | | 0 | | 0 = ALU | | X | X | X |
| ANDI | 0 🡪 Rs2 | 1 | 0 | | 0 🡪 zero | | 1 🡪 imm | | 0 | | 0 | | 0 = ALU | | X | X | X |
| ADDI | 0 🡪 Rs2 | 1 | 0 | | 1 🡪 sign | | 1 🡪 imm | | 0 | | 0 | | 0 = ALU | | X | X | X |
| LW | 0 🡪 Rs2 | 1 | 0 | | 1 🡪 sign | | 1 🡪 imm | | 1 | | 0 | | 1 = Mem | | X | X | X |
| LW.POI | 0 🡪 Rs2 | 1 | 1 | | 1 🡪 sign | | 1 🡪 imm | | 1 | | 0 | | 1 = Mem | | X | X | X |
| SW | X | 0 | 0 | | 1 🡪 sign | | 1 🡪 imm | | 0 | | 1 | | X | | X | X | X |
| BGT | X | 0 | 0 | | 1 🡪 sign | | 0 🡪 BusB | | 0 | | 0 | | X | | X | X | X |
| BLT | X | 0 | 0 | | 1 🡪 sign | | 0 🡪 BusB | | 0 | | 0 | | X | | X | X | X |
| BEQ | X | 1 | | 0 | | 1 🡪 sign | | 0 🡪 BusB | | 0 | | 0 | X | | x | X | X |
| BNQ | X | 1 | | 0 | | 1 🡪 sign | | 0 🡪 BusB | | 0 | | 0 | | X | X | X | X |
| JMP | X | X | | 0 | | X | | X | | 0 | | 0 | | X | x | x | X |
| CALL | X | X | | 0 | | X | | X | | 0 | | 0 | | X | 1 | 0 | 1 |
| RET | X | X | | 0 | | X | | X | | 0 | | 0 | | X | 0 | 1 | 1 |
| PUSH | X | 1 | | 0 | | X | | X | | 0 | | 0 | | X | 1 | 0 | 0 |
| POP | 1 | X | | 0 | | X | | X | | 0 | | 0 | | X | 0 | 1 | 0 |

RegDes = R-type + POP

\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

RegWr = SW + BGT + BLT

RegWr2 = LW.POI

\_\_\_\_\_\_

ExtOp = ANDI

ALUSrc = ANDI + ADDI+ LW + LW.POI + SW

Mem\_Rd = LW + LW.POI

Mem\_Wr = SW

WB\_data = LW + LW.POI

PushSig = CALL + PUSH

PopSig = RET + POP

**PC Truth Table :**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Opcode | Zero flag | Over flow flag | Negative flag | PCSrc |
| R type | X | x | X | 0 |
| JMP | X | X | x | 1 |
| CALL | X | x | X | 1 |
| RET | X | x | X | 3 |
| BGT | 1 | x | X | 0 |
| BGT | 0 | 1 | x | 2 |
| BGT | 0 | 0 | 1 | 0 |
| BLT | 1 | x | X | 0 |
| BLT | 0 | 1 | x | 0 |
| BLT | 0 | 0 | 1 | 2 |
| BNE | 0 | x | X | 2 |
| BNE | 1 | x | x | 0 |
| BEQ | 0 | x | X | 0 |
| BEQ | 1 | x | x | 2 |
| Other that J or B | X | x | x | 0 |

if (Op == RET) PCSrc = 3;

else if( (Op == JMP) ||(Op == CALL)) PCSrc = 1;

else if (Op == BGT && Over flow flag == 1 && Zero flag ==0)

|| (Op == BLT && Over flow flag == 0 && Zero flag ==0 && Negative flag ==1)

|| (Op == BNE &&Zero flag ==0)

||(Op == BEQ &&Zero flag ==1)

PCSrc = 2;

else PCSrc = 0;

**ALU Truth Table:**

|  |  |  |  |
| --- | --- | --- | --- |
| **OPcode** | **function** | **ALUOp** | **2 bit coding** |
| R-type | AND | AND | 00 |
| R-type | ADD | ADD | 01 |
| R-type | SUB | SUB | 10 |
| ANDI | X | AND | 00 |
| ADDI | X | ADD | 01 |
| LW | X | ADD | 01 |
| LW.POI | x | ADD | 01 |
| SW | X | ADD | 01 |
| BGT | X | SUB | 10 |
| BLT | X | SUB | 10 |
| BEQ | X | SUB | 10 |
| BNE | X | SUB | 10 |
| JMP | X | X | X |
| CALL | X | X | X |
| RET | X | X | X |
| PUSH | X | x | X |
| POP | X | x | X |

**Main Control Signals:**

|  |  |  |
| --- | --- | --- |
| **Signal** | **Effect when 0** | **Effect when 1** |
| **RegDs** |  |  |
| **RagWr** |  |  |
| **RagWr2** |  |  |
| **ExtOp** |  |  |
| **ALUSrc** |  |  |
| **Mem\_Wr** |  |  |
| **Mem\_Rd** |  |  |
| **WBdata** |  |  |
| **PushSig** |  |  |
| **PopSig** |  |  |
| **StackOp** |  |  |

|  |  |  |
| --- | --- | --- |
| **Signal** | **value** | **Effect** |
| **PcSrc** | **0** |  |
| **1** |  |
| **2** |  |
| **3** |  |