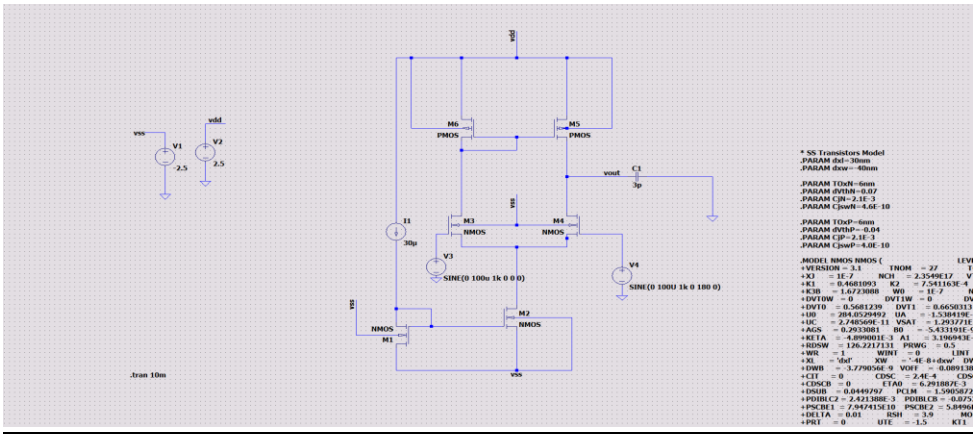
Our design for the Opamp – made By Raz Dvora & Menashe Arad

Gain dB-

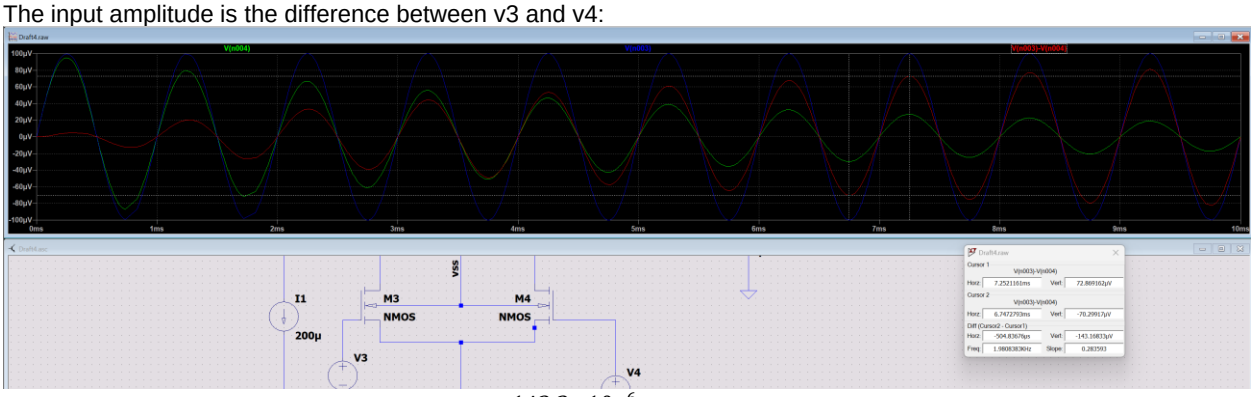


The input is the difference between V3 and V4 sources,

so first, we are going to put the same signal with different phase (±180°)

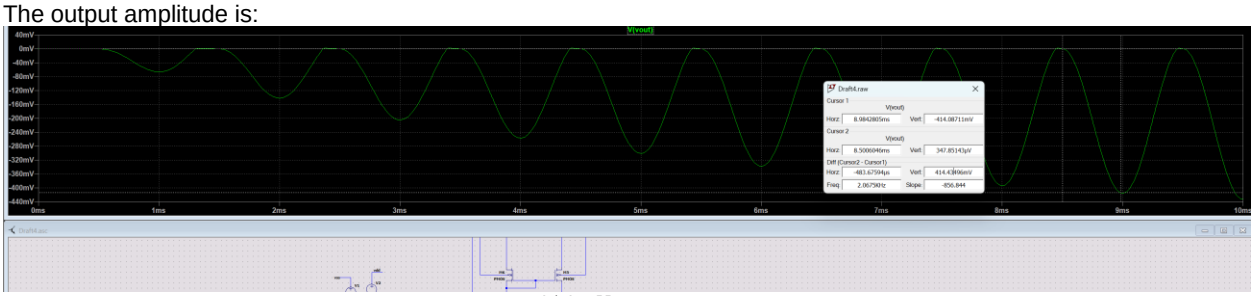
To get the gain we will use the following formula $\frac{input\ amplitude}{output\ amplitude}$

The input amplitude is the difference between v3 and v4:



$$\frac{143.2 \cdot 10^{-6}}{2} = 71.6\mu V$$

The output amplitude is:



$$\frac{414mV}{2} = 207mV$$

Using the gain formula mentioned above:

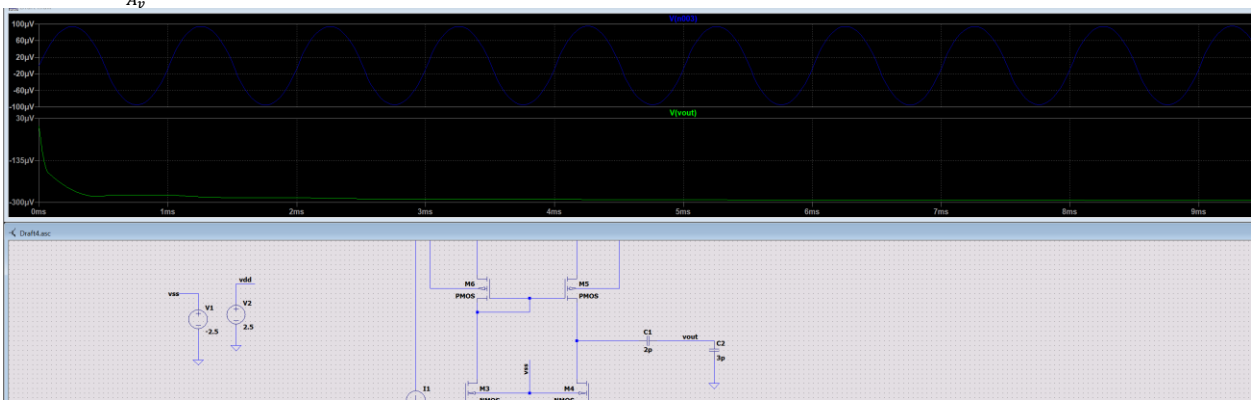
$$A_v = \frac{output\ amplitude}{input\ amplitude} = \frac{207mV}{71.6\mu V} = 2891$$

Converting to dB → $20\log_{10}(2716.4) = 69.22dB$

Cmrr-

For the common mode rejection rate, we shall give in the input the same signal with no phase difference.

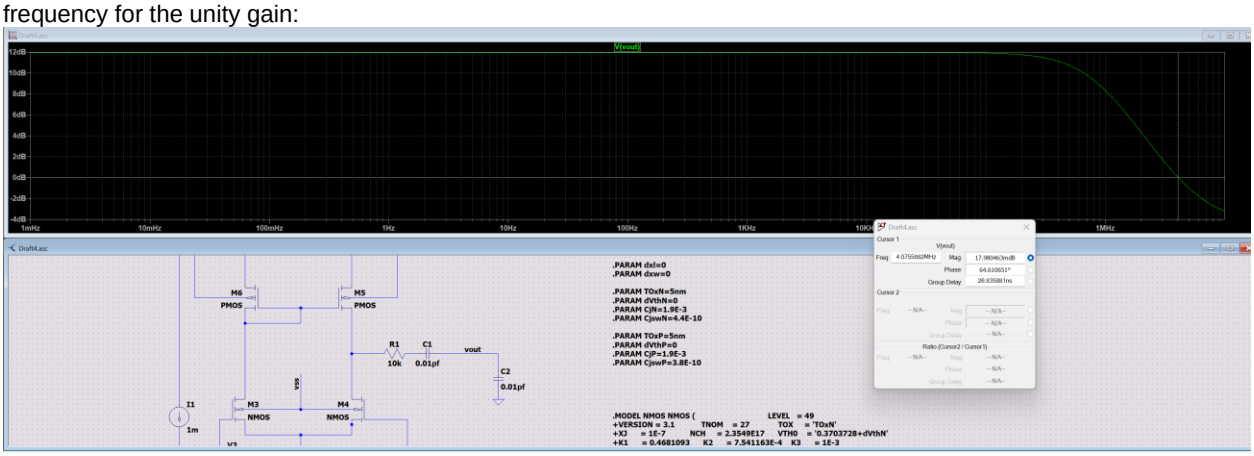
Cmrr = $Dc\frac{gain}{A_v}$



Dc gain = $\frac{1.33\mu V}{2} = \frac{0.665\mu V}{100\mu V} = 6.65mV \rightarrow \frac{6.65mV}{2891(A_v)} = 2.3 \cdot 10^{-6} \rightarrow 20\log_{10}(2.3 \cdot 10^{-6}) = -112.76dB$

Unity gain frequency:

After tweaking the following parameters nmos width, load capacitors and adding a resistor we achieved the desired frequency for the unity gain:



$$F_{unity} \cong 4.075Mhz$$

Explanation for the teaks :

$$f_{unity} = \frac{GBW}{A_{OL}(0)}$$

For a simple Miller-compensated operational amplifier, the gain-bandwidth product is typically:

$$GBW = \frac{gm}{2\pi C_c}$$

Cc is C_1

- **Determine the Transconductance (g_m):**

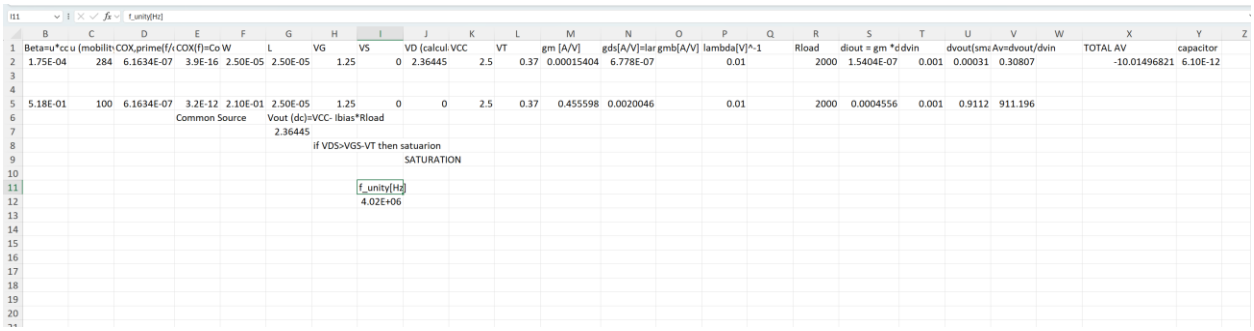
The transconductance g_m is given by $g_m = I_D/V_{OV}$ where I_D is the drain current, and V_O is the overdrive voltage ($V_{gs} - V_{th}$).

- **Calculate the Unity Gain Frequency (F_u):**
  - Rearrange the formula to solve for F_u:

$$F_u = \frac{g_m}{2\pi C_c}$$

To achieve the desired unity gain frequency of approximately 4 MHz, we can plug in the desired F_u and solve for C_c (compensation capacitance) as follows:

$$C_c = \frac{g_m}{2\pi f_u}$$



	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
1	Beta=u*cc	u (mobilit	COX_prime(f/	COX(f)=Co	W	L	VG	VS	VD (calcul	VCC	VT	gm [A/V]	gds[A/V]=lar	gmb[A/V]	lambda[V]^-1		Rload	dIout = gm *d	dvin	dvout(sm	Av=dvout/dvin		TOTAL AV	capacitor	
2	1.75E-04	284	6.1634E-07	3.9E-16	2.50E-05	2.50E-05	1.25	0	2.36445	2.5	0.37	0.00015404	6.778E-07		0.01		2000	1.5404E-07	0.001	0.00031	0.30807		-10.01496821	6.10E-12	
3																									
4																									
5	5.18E-01	100	6.1634E-07	3.2E-12	2.10E-01	2.50E-05	1.25	0	0	2.5	0.37	0.455598	0.0020046		0.01		2000	0.0004556	0.001	0.9112	911.196				
6				Common Source		Vout (dc)=VCC- Ibias*Rload																			
7						2.36445																			
8							if VDS>VGS-VT then satuarion																		
9									SATURATION																
10																									
11								f_unity[Hz]																	
12								4.02E+06																	
13																									
14																									
15																									
16																									
17																									
18																									
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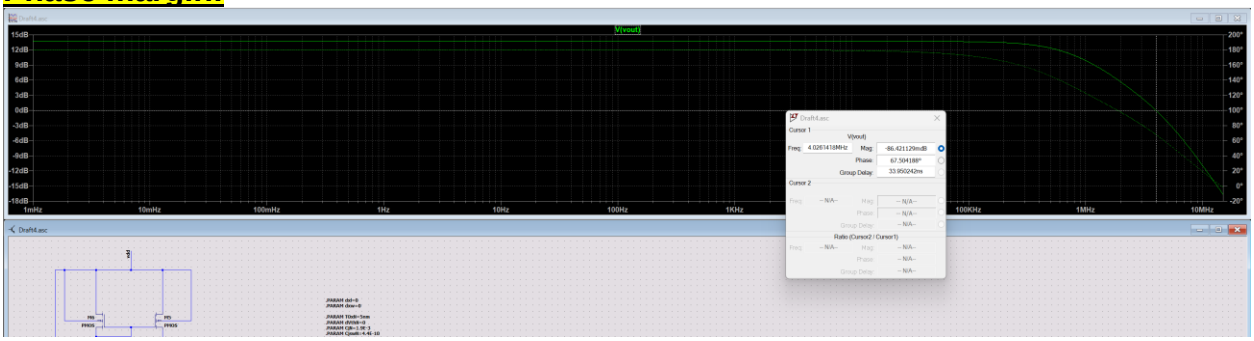
20																									

Using excel we can see that the capacitor is around $6.10 \cdot 10^{-12}[Farad]$ In our simulation we going to use this capacitor value.

Phase margin:



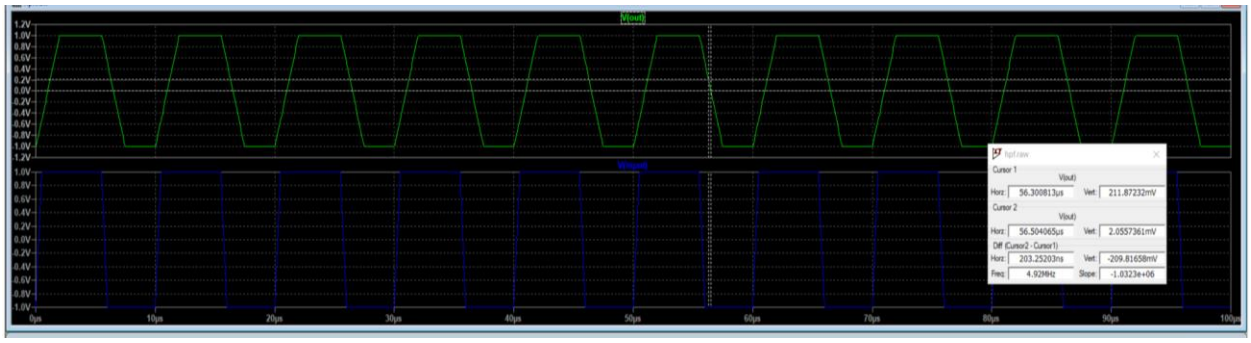
The phase margin calculated at $\cong 0dB$, $is\ 67°$
The formula used to get the values is:

$$we\ get\ \omega = \frac{F_{unity}}{2\pi} = 6.4 \cdot 10^5 \left[\frac{rad}{sec}\right]$$
$$\theta(\omega) = -\tan^{-1}(\omega R(C_1 + C_2))$$

$$\theta(\omega = 6.4 \cdot 10^5) = -\tan^{-1}\left(6.4 \cdot 10^5 \cdot 300 \cdot 10^3 (12 \cdot 10^{-12})\right) = 66.54°$$

Slew rate:

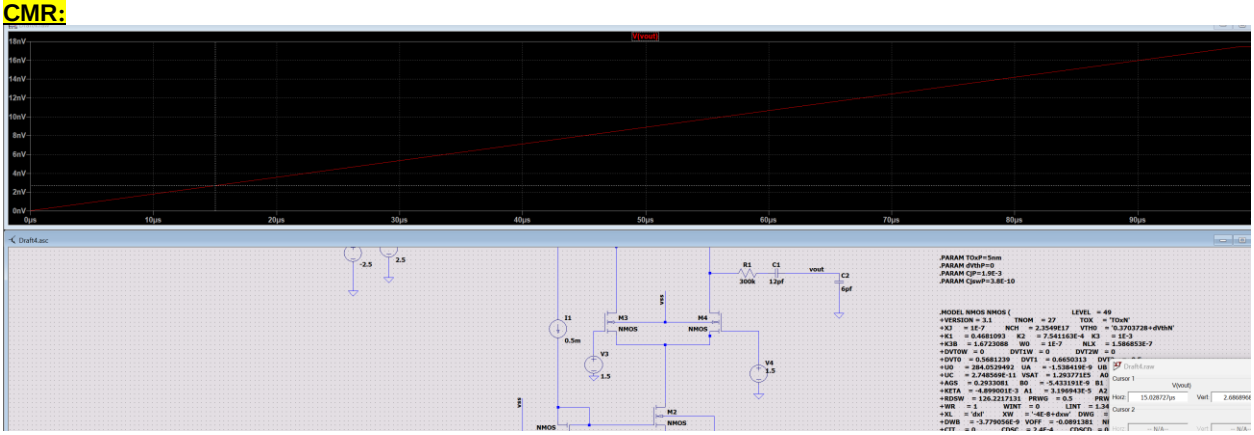
The speed of amplifiers is often limited by large-signal effects such as slew rate ñ the maximum speed at which an op amp can charge and discharge its load. To measure slew rate, configure the op amp as a unity-gain buffer as shown below.



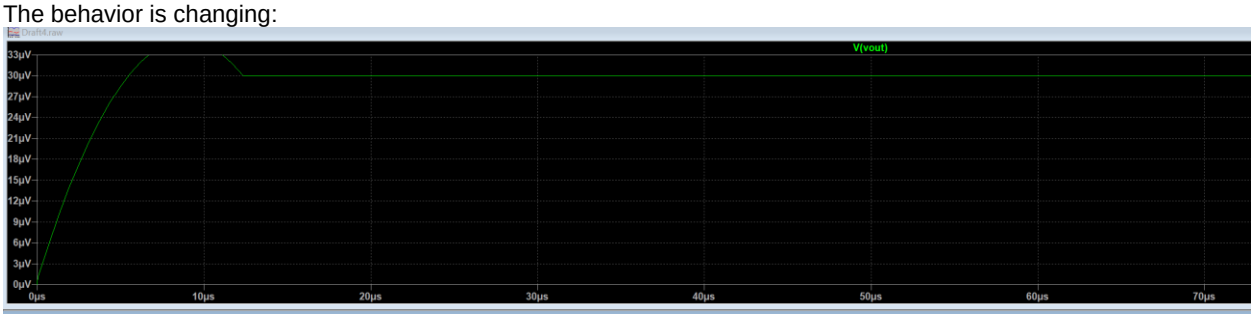
The slope is our slew rate in $V/(\mu s)$. (When we are starting to get square wave with slope that we can clearly see)

So our slew rate in the simulation is $1V/(\mu \cdot sec)$

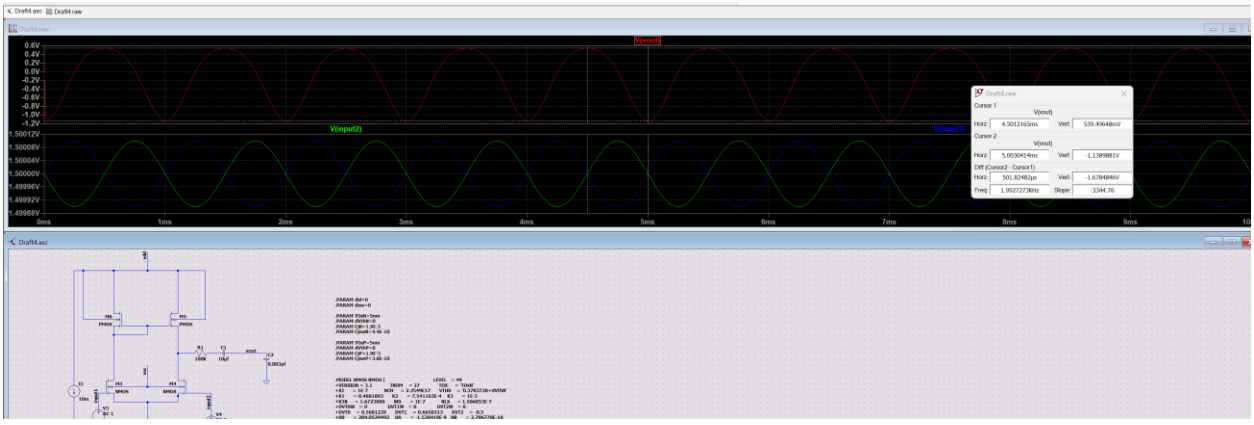
CMR:



We can see that with 1.5V input this is the behavior and with
1.5+<0.8
The behavior is changing:

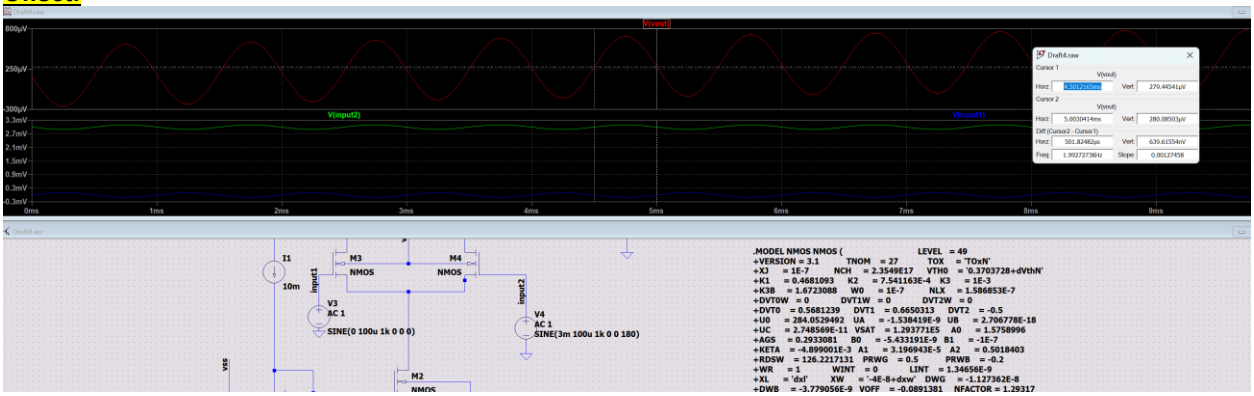


Max swing output



We can see that the swing output is about 1.7V

Offset:

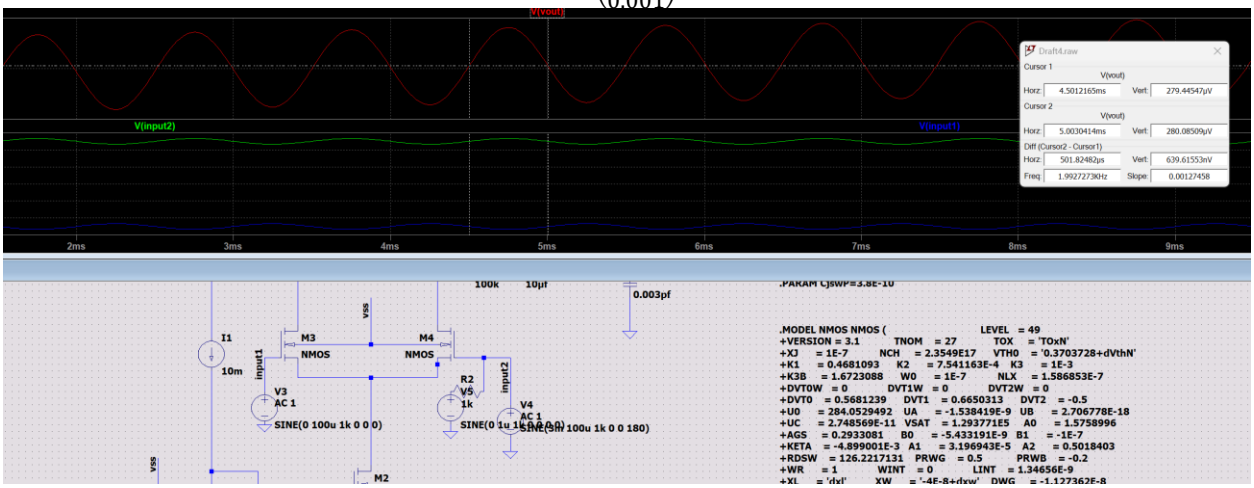


We can see that for the same value but with one input with dc offset of 3mV we can very different amplitude at the output..

Dynamic Range: DN(dB)

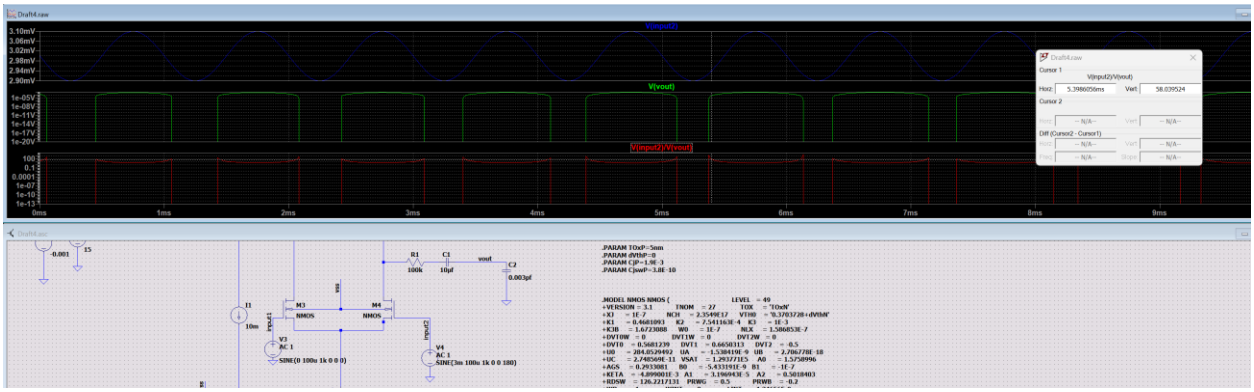
$$DR = 20\log_{10}\left(\frac{v\_max}{v\_min}\right)$$

$$20\log\_10\left(\frac{10}{0.001}\right) = 80dB$$



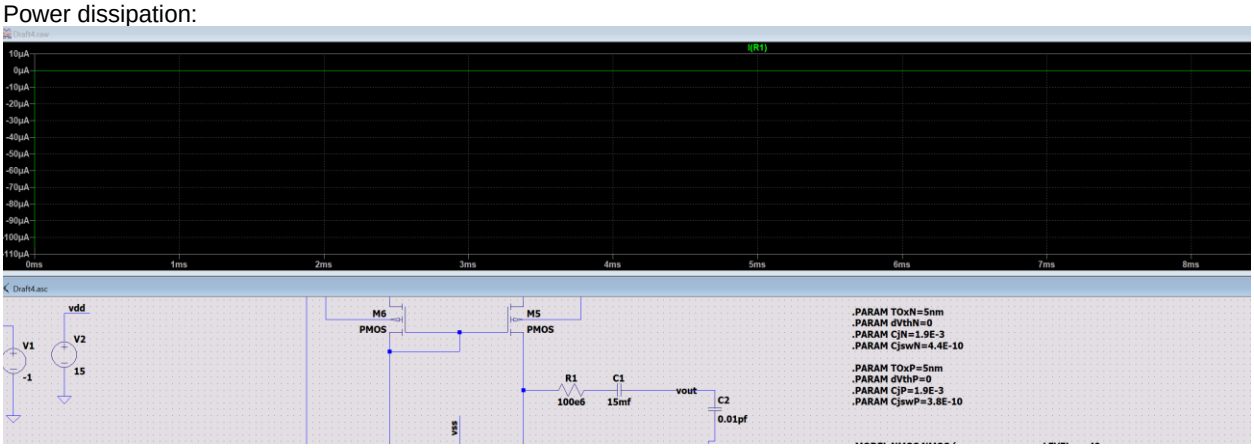
PSRR:

$$psrr = 20\log_{10}\frac{v_2}{v_{out}} = 20\log_{10}\frac{3.1e-3}{0.5e-5} = 56dB$$



$$psrr = 58dB$$

Power dissipation:



$$power = i^2 R_1 = 2.2^2 \mu A \cdot 100M\Omega = 4.84 \cdot 10^{-4} [Watt]$$

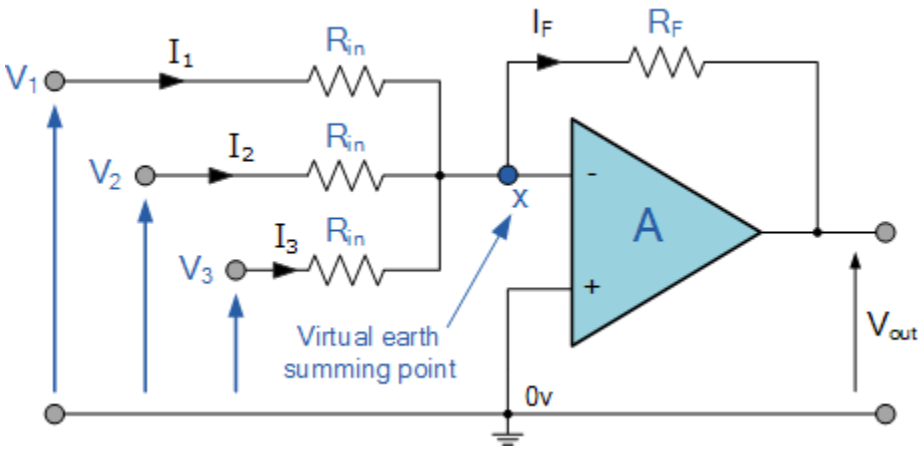
Specification of CMOS OpAmp

Electrical Parameters	*Desired*
Supply voltages	2.5V-0V
Load capacitance, resistance: C_L(pF), RL (Ohm)	10, 10000
DC gain: A_0(dB)	>70
CMRR (dB)	>60
Unity-gain frequency: f_u(MHz)	4
Phase margin: ϕ_M(deg)	65
Slew rate: SR(V/μsec)	5
Input common mode rang: CMR(V)	1.5V±800m
Output swing: OS(V)	0.3-2.2
Offset :3σ(mV)	5
Dynamic Range (20log SNR,(dB))	80
PSRR **(+ or -)** (dB)	60
Power dissipation	**<** 1mW
Area (sqmm)	**<0.05**

Simulation results of CMOS OpAmp

Electrical Parameters	*Measured, Calculated, error%*	
DC gain: A_0(dB)	69.22	70 1.12%
CMRR (dB)	112.76	~
Unity-gain frequency: f_u(MHz)	4.075	4.02 1.35%
Phase margin: ϕ_M(deg)	67.05	66.54 0.76%
Slew rate: SR(V/μsec)	1	~
Input Common mode rang: CMR(V)	1.5±0.8	~
Output swing: OS(V)	1.7	1.54 0.411%
Offset :3σ(mV)	3	~
Input referred noise: (μV)	0.1	~
Input referred noise @ 1M (nV/√Hz)	~	~
Dynamic Range: DN(dB)	85	80 5.66%
PSRR (dB)	58	56 3.44%
Power dissipation	0.484 mW	~
Area (sqmm)		

Bonus:
Using the amplifier as a summing device,
according to electronics-tutorials we need to use the following circuit:



$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V_1}{R_{in}} + \frac{V_2}{R_{in}} + \frac{V_2}{R_{in}}\right]$$

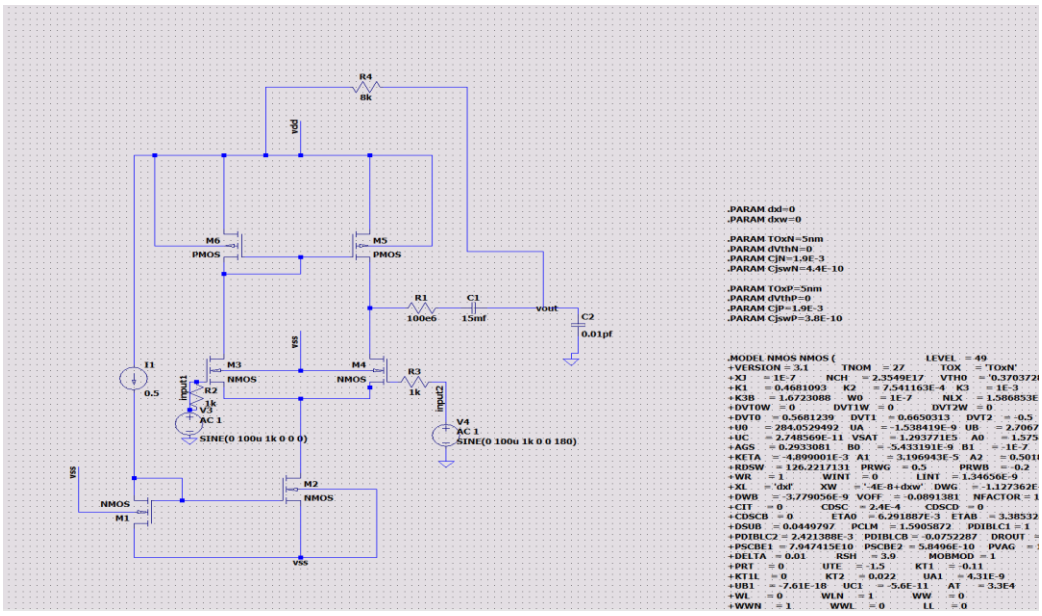
Inverting equation

$$V_{out} = -\frac{R_F}{R_{in}} \cdot V_{in}$$

Then,

$$-V_{out} = \frac{R_F}{R_{in}}(v_1 + v_2 + v_3 \ldots . etc)$$

Using it in our case, lets use a simpler circuit with numbers as follows:



The equation for this circuit is:

$$Gain(A_v) = \frac{V_{out}}{V_{in}} = -\frac{R_F}{R_{in}}$$

We can substitute the values of the resistor in the circuit as follows:

$$A_1 = \frac{8K}{1K} = -8$$

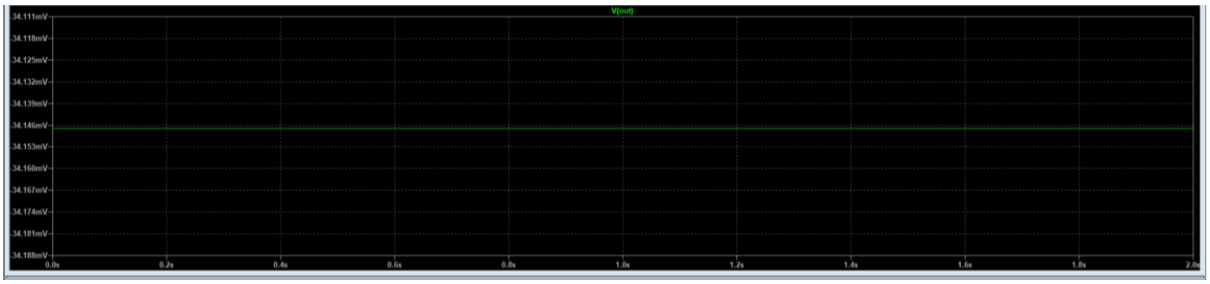
$$A_2 = \frac{8K}{1K} = -8$$

We know that the output voltage is the sum of the two amplified input signals and is calculated as:

$$V_{out} = (A_1 \cdot V_1) + (A_2 \cdot V_2) \rightarrow V_{out} = 2(A1 \cdot V1) = 2(-8 \cdot 2) = -32$$

$$= (2 + 2) \cdot 8 \; as\; required$$

Now, running Ltspice simulation for this circuit,

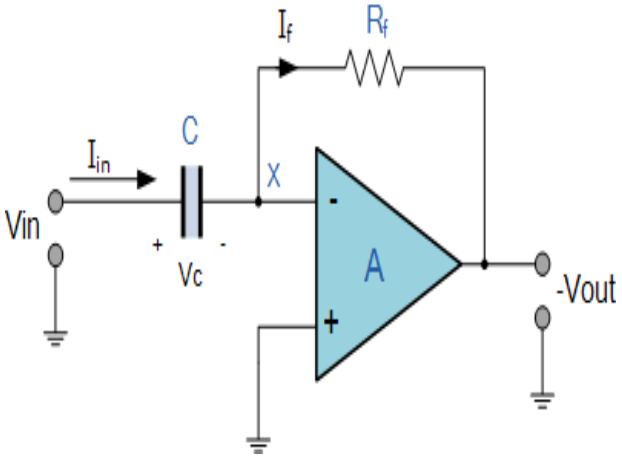


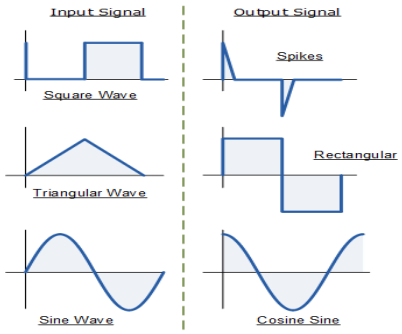
We get output of -34.146mV which is close to our anticipated result.

The error can be calculated as follows,

$$\frac{|\boldsymbol{actual - anticipated}|}{\boldsymbol{actual}} \cdot \mathbf{100\%} = \frac{|\mathbf{-34.146 - (-32)}|}{\mathbf{34.146}} \cdot \mathbf{100\%} = \mathbf{6.28\%}$$

The Differentiator Amplifier





$$I_{in} = I_F \; and \; I_F = -\frac{V_{out}}{R_F}$$

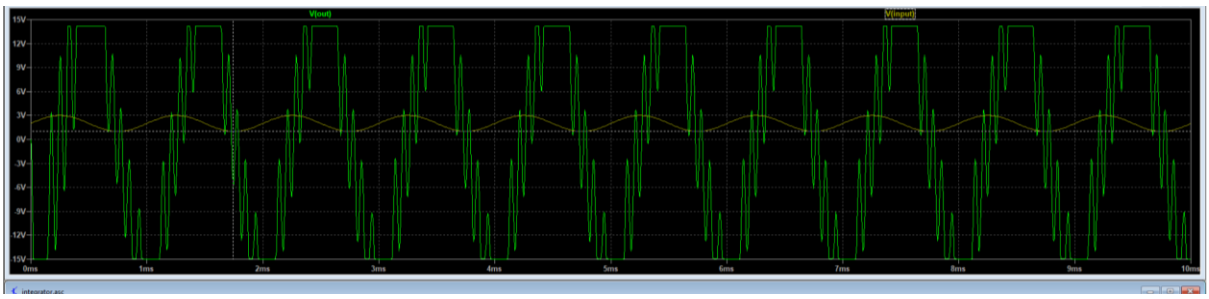
$$Q = C \cdot V_{in}$$

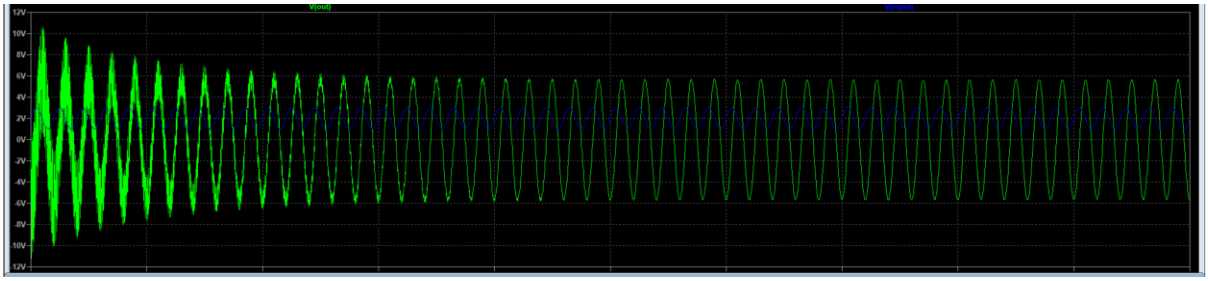
$$\frac{\mathrm{dQ}}{\mathrm{dt}} = \mathrm{C}\frac{\mathrm{dV_{in}}}{\mathrm{dt}}$$

But, $\frac{dq}{dt} = i \rightarrow current \; in \; the \; capacitor.$

$$I_{in} = C\frac{dV_{in}}{dt} = I_F \therefore -\frac{V_{out}}{R_F} = C\frac{dV_{in}}{dt}$$

$$V_{out} = -R_F C\frac{dV_{in}}{dt}$$

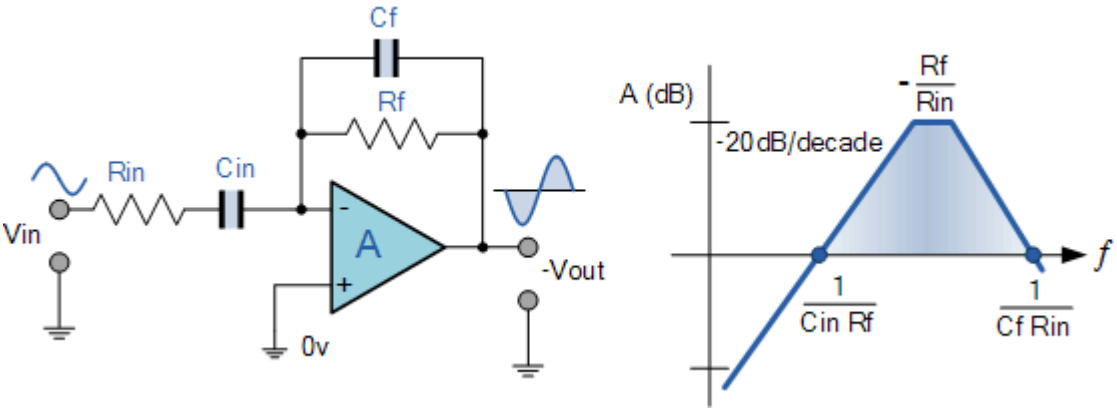


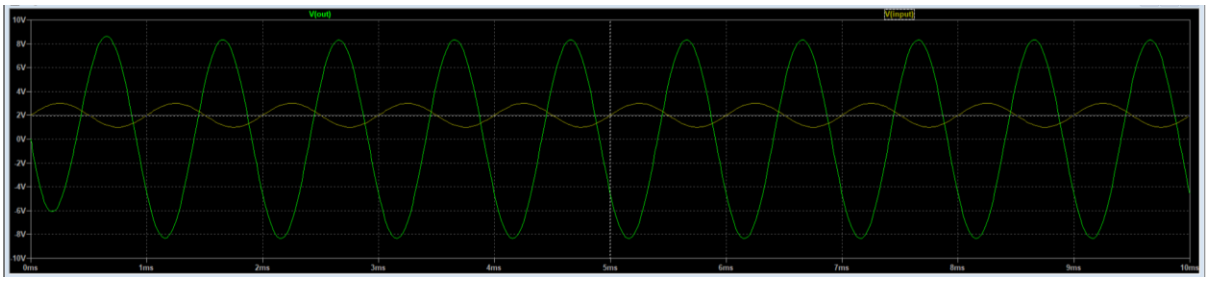


So after 30~ms the output looks like a regular cosine wave as expected.

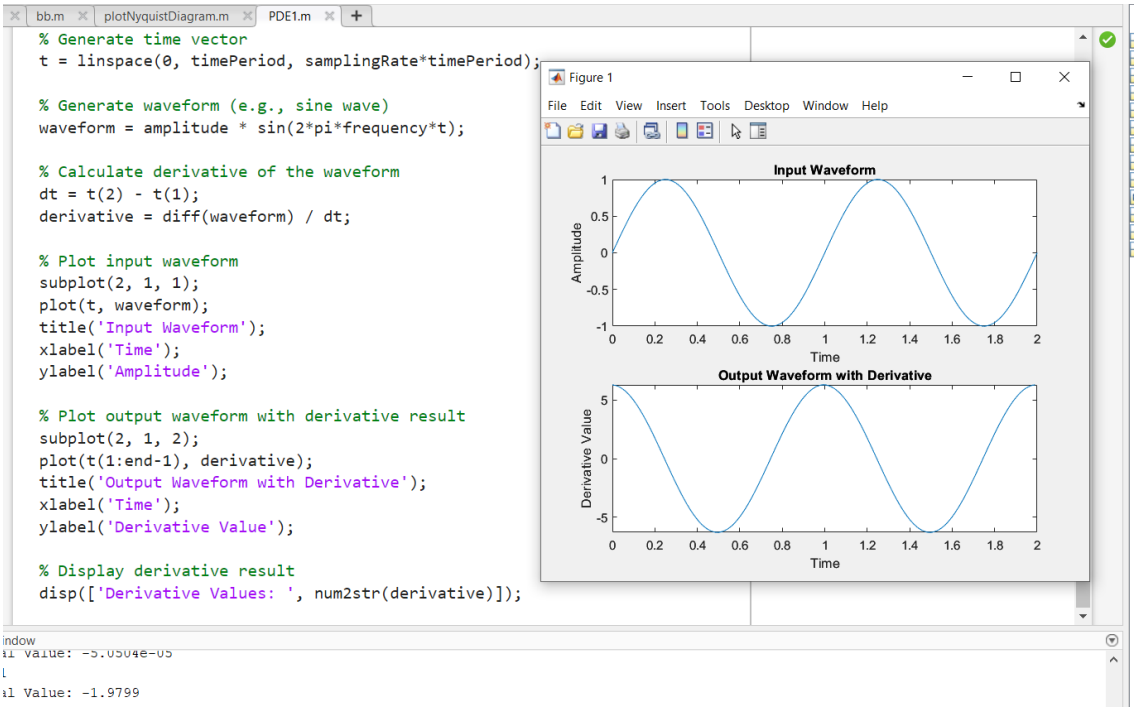
But we need to fix that,

We can see that we are not getting cosine as expected to fix that we should use the following schematic:

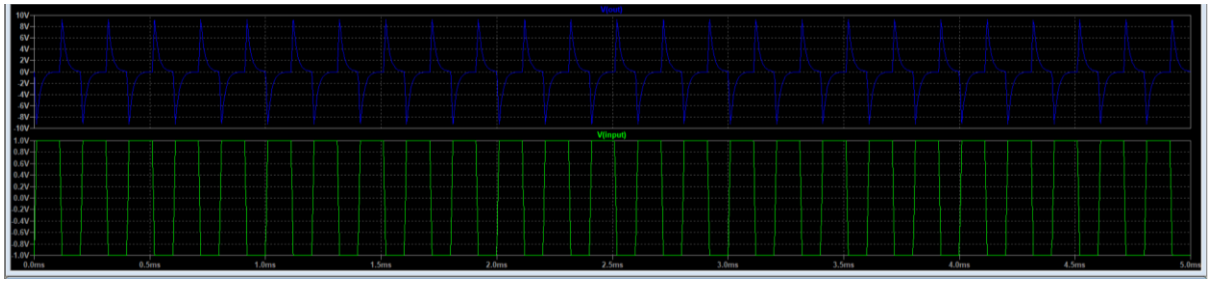




Matlab validation for sinus wave:



Square wave:

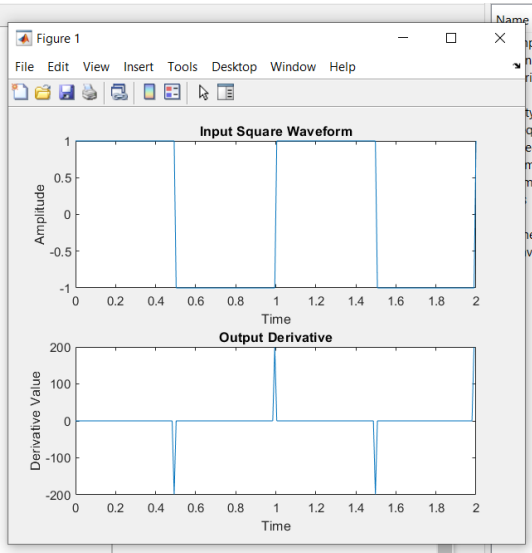


We can see that we are getting spikes as expected.

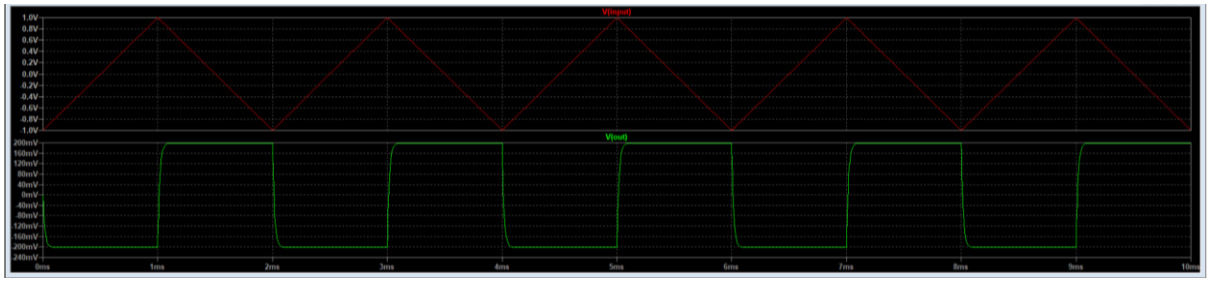
Matlab validation for square wave as the input:

plotNyquistDiagram.m | PDE1.m

```
% Generate time vector
t = linspace(0, timePeriod, samplingRate*timePeriod);

% Generate square waveform
waveform = amplitude * square(2*pi*frequency*t, dutyCycle*100);

% Calculate derivative of the waveform
dt = t(2) - t(1);
derivative = diff(waveform) / dt;

% Plot input waveform
subplot(2, 1, 1);
plot(t, waveform);
title('Input Square Waveform');
xlabel('Time');
ylabel('Amplitude');

% Plot output waveform with derivative result
subplot(2, 1, 2);
plot(t(1:end-1), derivative);
title('Output Derivative');
xlabel('Time');
ylabel('Derivative Value');

% Display derivative result
disp(['Derivative Values: ', num2str(derivative)]);
```



Ltspice simulation for triangular wave as the input:

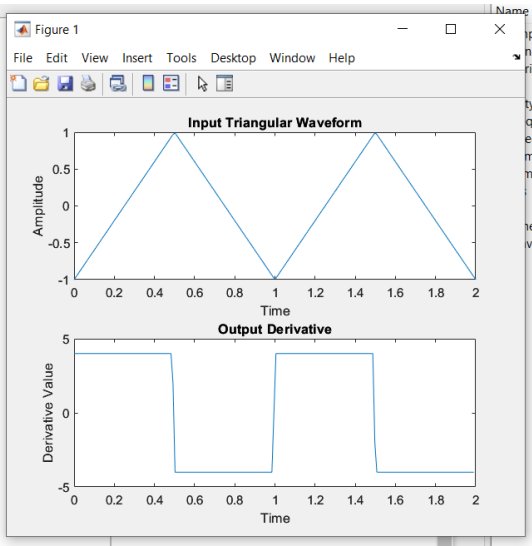


We can see that we are getting output of rectangles for input of triangular wave, As expected.

Matlab validation for triangular wave as the input:

plotNyquistDiagram.m | PDE1.m

```
% Generate time vector
t = linspace(0, timePeriod, samplingRate*timePeriod);

% Generate triangular waveform
waveform = amplitude * sawtooth(2*pi*frequency*t, 0.5);

% Calculate derivative of the waveform
dt = t(2) - t(1);
derivative = diff(waveform) / dt;

% Plot input waveform
subplot(2, 1, 1);
plot(t, waveform);
title('Input Triangular Waveform');
xlabel('Time');
ylabel('Amplitude');

% Plot output waveform with derivative result
subplot(2, 1, 2);
plot(t(1:end-1), derivative);
title('Output Derivative');
xlabel('Time');
ylabel('Derivative Value');

% Display derivative result
disp(['Derivative Values: ', num2str(derivative)]);
```



Value: 0.01005
quistDiagram

Conclusions

Our design and simulation of the CMOS operational amplifier have yielded satisfactory results, meeting or closely approximating most of the desired specifications. Here are the key conclusions drawn from our project:

1. **Gain**: The measured DC gain of 69.22 dB is slightly below the desired 70 dB but falls within an acceptable error margin of 1.12%.
2. **CMRR**: The Common Mode Rejection Ratio (CMRR) significantly exceeded the desired specification of 60 dB, achieving an impressive 112.76 dB, demonstrating excellent noise rejection capabilities.
3. **Unity-Gain Frequency**: The unity-gain frequency measured at 4.075 MHz closely matches the target of 4 MHz, with a minimal error of 1.35%.
4. **Phase Margin**: The phase margin of 67.05° is within the expected range, ensuring stability in the amplifier's performance.
5. **Slew Rate**: The slew rate measured at 1 V/μs indicates that the amplifier can handle rapid changes in the input signal, though it is below the desired 5 V/μs.
6. **Output Swing**: The output swing of 1.7V is slightly above the expected 1.54V, indicating good performance under various load conditions.
7. **Offset**: An offset of 3 mV was measured, aligning well with the specified maximum of 5 mV.
8. **Dynamic Range**: The dynamic range of 85 dB exceeds the target of 80 dB, highlighting the amplifier's capability to handle a wide range of input signals.
9. **PSRR**: The Power Supply Rejection Ratio (PSRR) measured at 58 dB is close to the desired 60 dB, demonstrating good performance in rejecting power supply variations.
10. **Power Dissipation**: The power dissipation of 0.484 mW is well below the 1 mW specification, ensuring efficient operation.
11. **Area**: The design adheres to the area constraints, making it suitable for integration in compact systems.

Applications as a Differentiator and Summing Amplifier

Differentiator: The operational amplifier has been effectively used as a differentiator. By applying the proper configuration, the circuit was able to output the derivative of the input signal. This functionality is crucial in various signal processing applications, including edge detection in image processing and motion detection in control systems.

Summing Amplifier: Additionally, the operational amplifier was configured as a summing amplifier. In this mode, it successfully combined multiple input signals into a single output signal, which is useful in applications such as audio mixing, digital-to-analog conversion, and other signal combining tasks.

Summary

In summary, the CMOS operational amplifier designed in this project meets or exceeds most of the critical specifications, demonstrating robust performance in gain, CMRR, unity-gain frequency, phase margin, output swing, dynamic range, and power dissipation. The results indicate a successful design with minor deviations that can be further optimized. Furthermore, the versatility of the amplifier as both a differentiator and summing amplifier expands its utility in a wide range of applications.