SACRAMENTO STATE

EEE 234
Digital IC Design

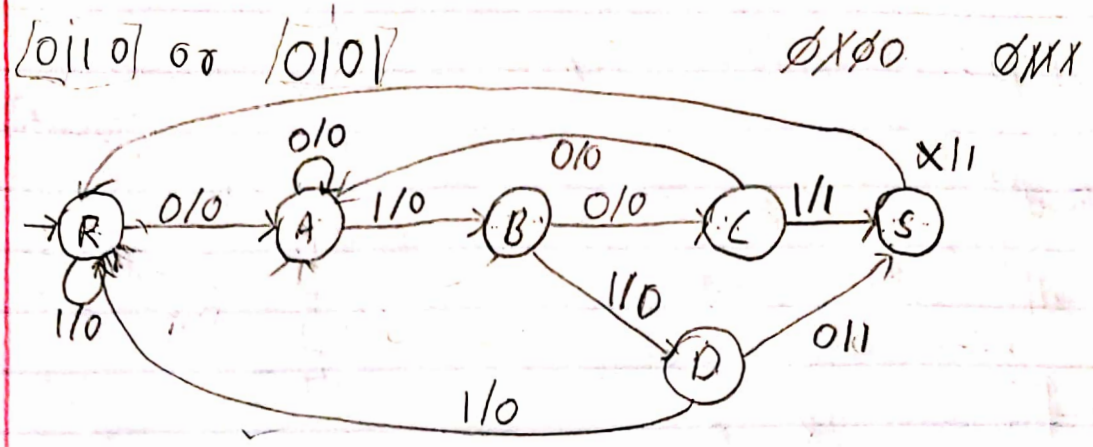
Project 2 – Assignment 1

Student Name: Raj Patel & Hemiha Vasanthakumaran
Email ID: rajkirtibhaipatel@csus.edu & hvasanthakumaran@csus.edu
Date of Submission: April 20, 2019

Contents

1. Sequence Detector

1.1 State Diagram



State Table

Current State	Next State		Output	
	X=0	X=1	X=0	X=1
R 000	A	R	0	0
A 001	A	B	0	0
B 011	C	D	0	0
C 010	A	S	0	1
D 110	S	R	1	0
S 100	R	R	1	1

1.2 Optimal State Assignment Map

	00	01	11	10
0	R	A	B	C
1	S			D

I. (R, A, C) (R, D, S)
II. (C, D) (A, S) (S, R)
III. (R, A, B, C) , , (D, S)

1.3 K-Maps

Q_0^+ K-Map Q0

XQ_0 \ Q_1Q_2	00	01	11	10
00	0	0	0	0
01	0	X	X	1
11	0	X	X	0
10	0	0	1	1

A B C D
X Q_0 Q_1 Q_2

$J_0 = XQ_1$

XQ_0 \ Q_1Q_2	00	01	11	10
00	0	0	0	0
01	X	X	X	X
11	X	X	X	X
10	0	0	1	1

$K_0 = X + \overline{Q_1}$

XQ_0 \ Q_1Q_2	00	01	11	10
00	X	X	X	X
01	1	X	X	0
11	1	X	X	1
10	X	X	X	X

Q_1^+ K-Map Q1

XQ_0 \ Q_1Q_2	00	01	11	10
00	0	0	1	0
01	0	X	X	0
11	0	X	X	0
10	0	1	1	0

$J_1 = XQ_2$

XQ_0 \ Q_1Q_2	00	01	11	10
00	0	0	X	X
01	0	X	X	X
11	0	X	X	X
10	0	1	X	X

$K_1 = \overline{Q_2}$

XQ_0 \ Q_1Q_2	00	01	11	10
00	X	X	0	1
01	X	X	X	1
11	X	X	X	1
10	X	X	0	1

K Map Q2

Q_2^+

$X Q_0$ \ $Q_1 Q_2$	00	01	11	10
00	1	1	0	1
01	0	X	X	0
11	0	X	X	0
10	0	1	0	0

A B C D
$X Q_0 Q_1 Q_2$

$J_2 = \bar{X}\bar{Q}_0$

$X Q_0$ \ $Q_1 Q_2$	00	01	11	10
00	1	X	X	1
01	0	X	X	0
11	0	X	X	0
10	0	X	X	0

$K_2 = Q_1$

$X Q_0$ \ $Q_1 Q_2$	00	01	11	10
00	X	0	1	X
01	X	X	X	X
11	X	X	X	X
10	X	0	1	X

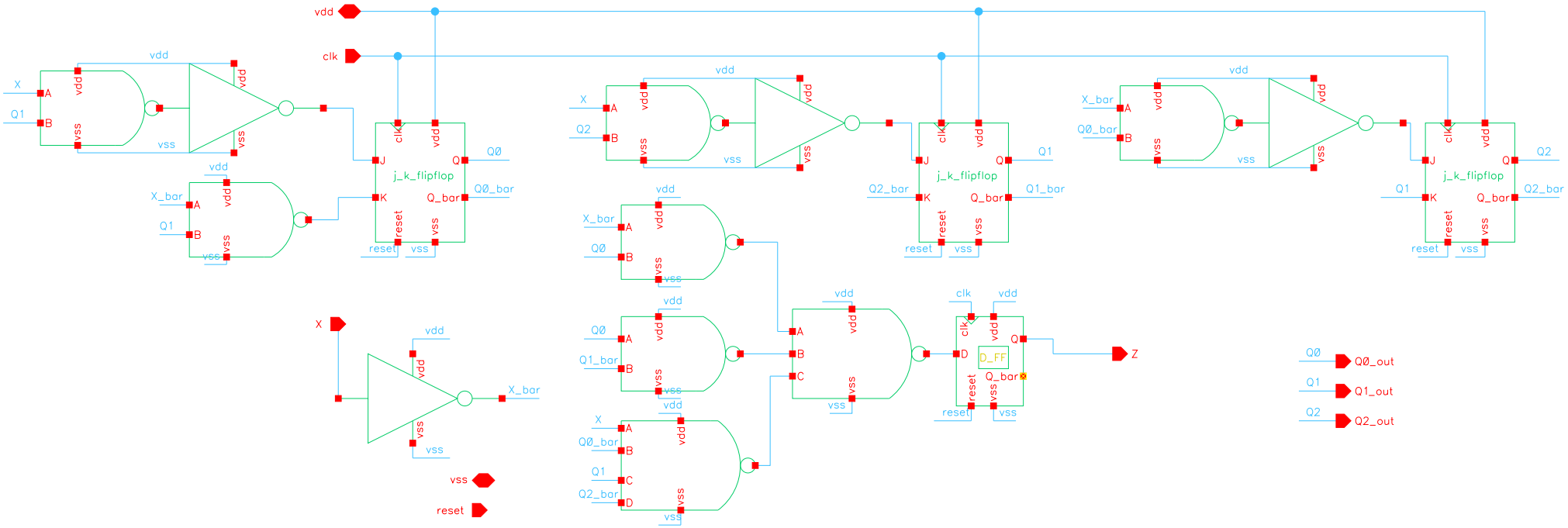
K Map Z

Z^+

$X Q_0$ \ $Q_1 Q_2$	00	01	11	10
00	0	0	0	0
01	1	X	X	1
11	1	X	X	0
10	0	0	0	1

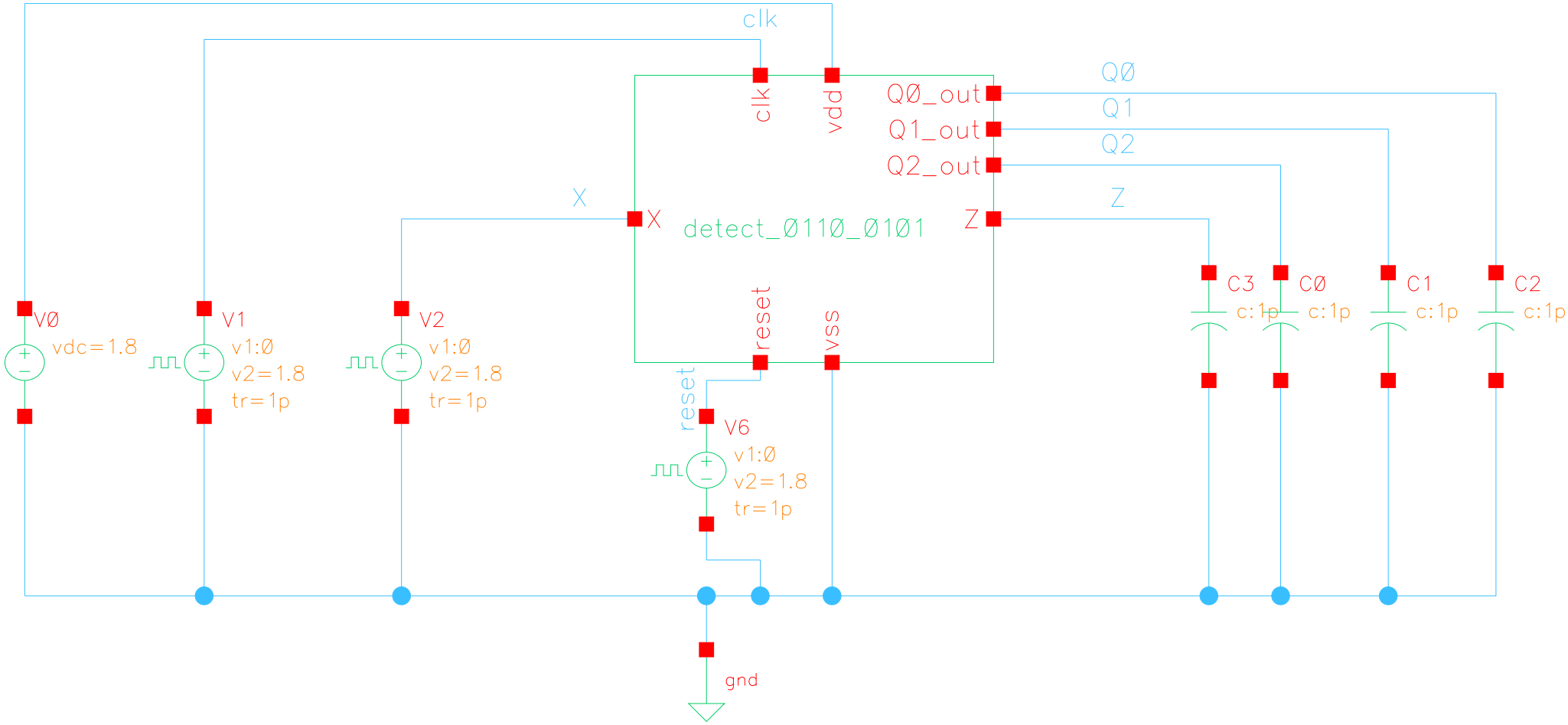
$Z = \bar{X}Q_0 + Q_0\bar{Q}_1 + X\bar{Q}_0Q_1\bar{Q}_2$

1.4 Sequence Detector Schematic:



Pin Q0_out, Q1_out, Q2_out, are added for testing purpose only

1.5 Sequence Detector Test Bench:

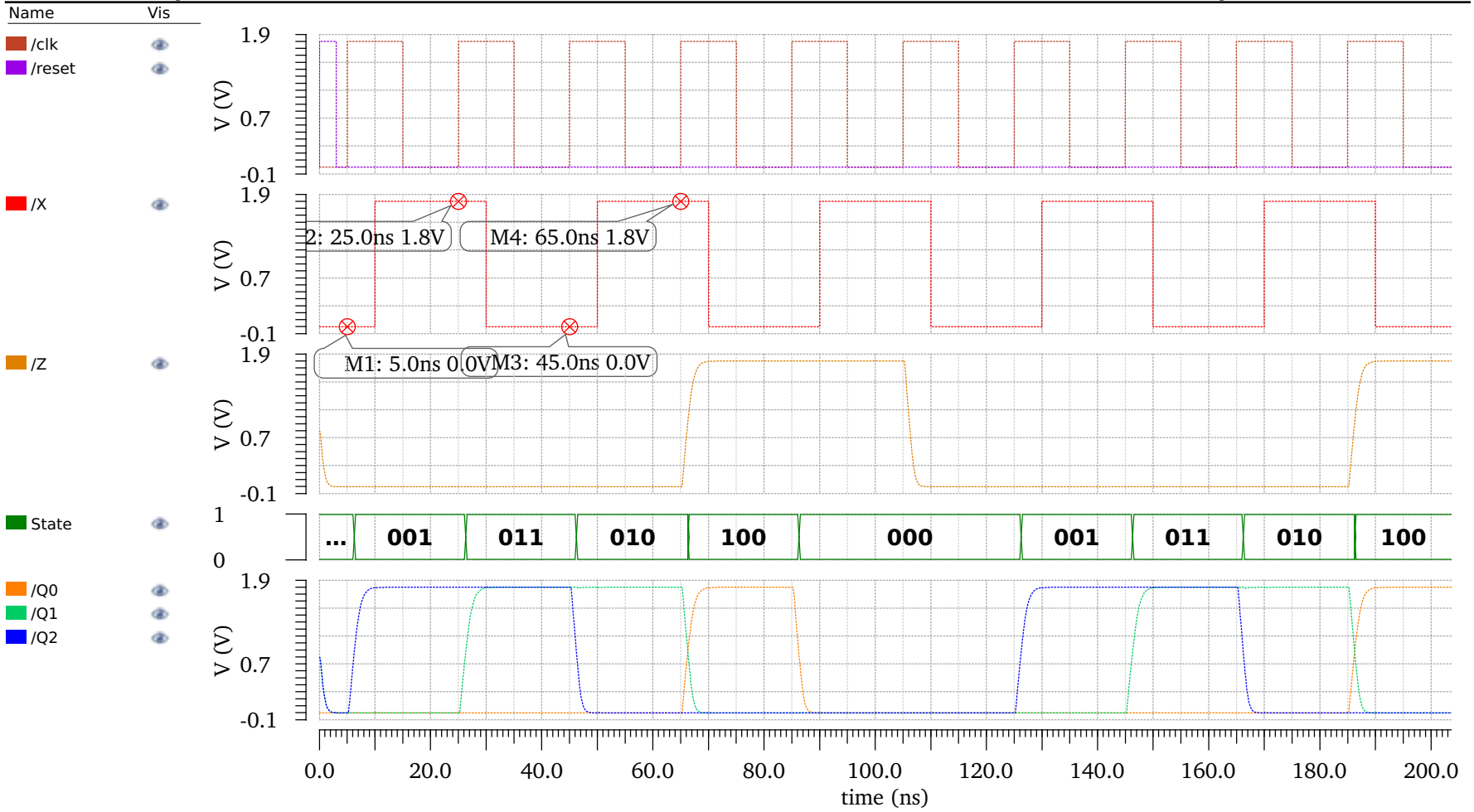


1.6 State Table

Current State		Next State		Output	
		X = 0	**X = 1**	**X = 0**	**X = 1**
R	000	A	R	0	0
A	001	A	B	0	0
B	011	C	D	0	0
C	010	A	S	0	1
D	110	S	R	1	0
S	100	R	R	1	1

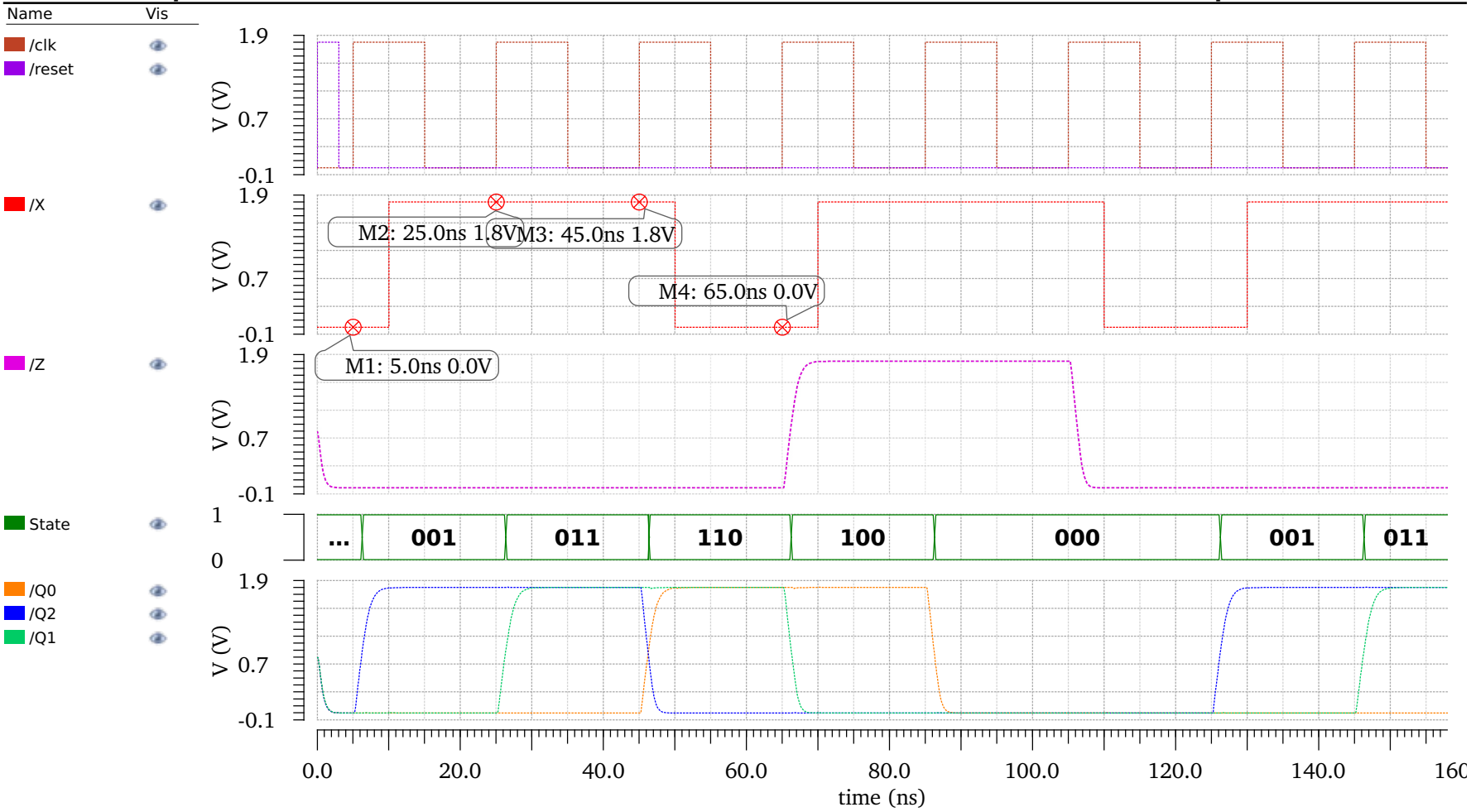
1.7 Sequence Detector Simulation (Input 0101):

Transient Response **Fri Apr 19 17:19:08 2019**



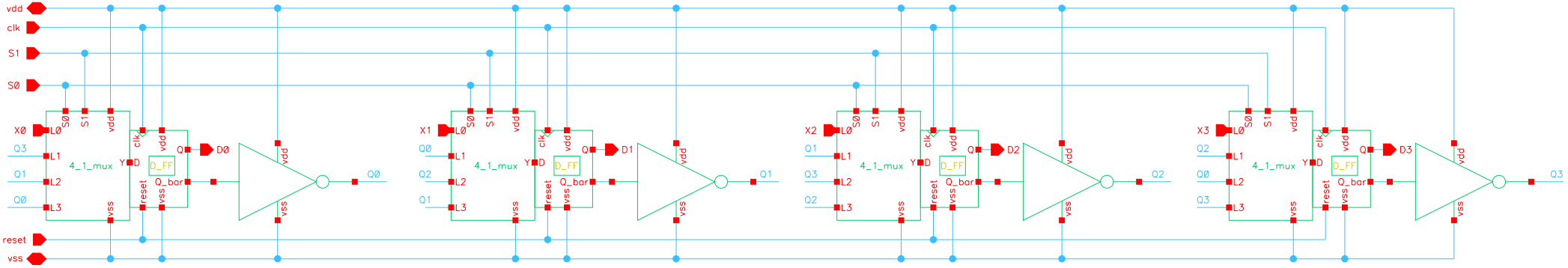
1.8 Sequence Detector Simulation (Input 0110):

Transient Response **Thu Apr 18 19:32:11 2019**

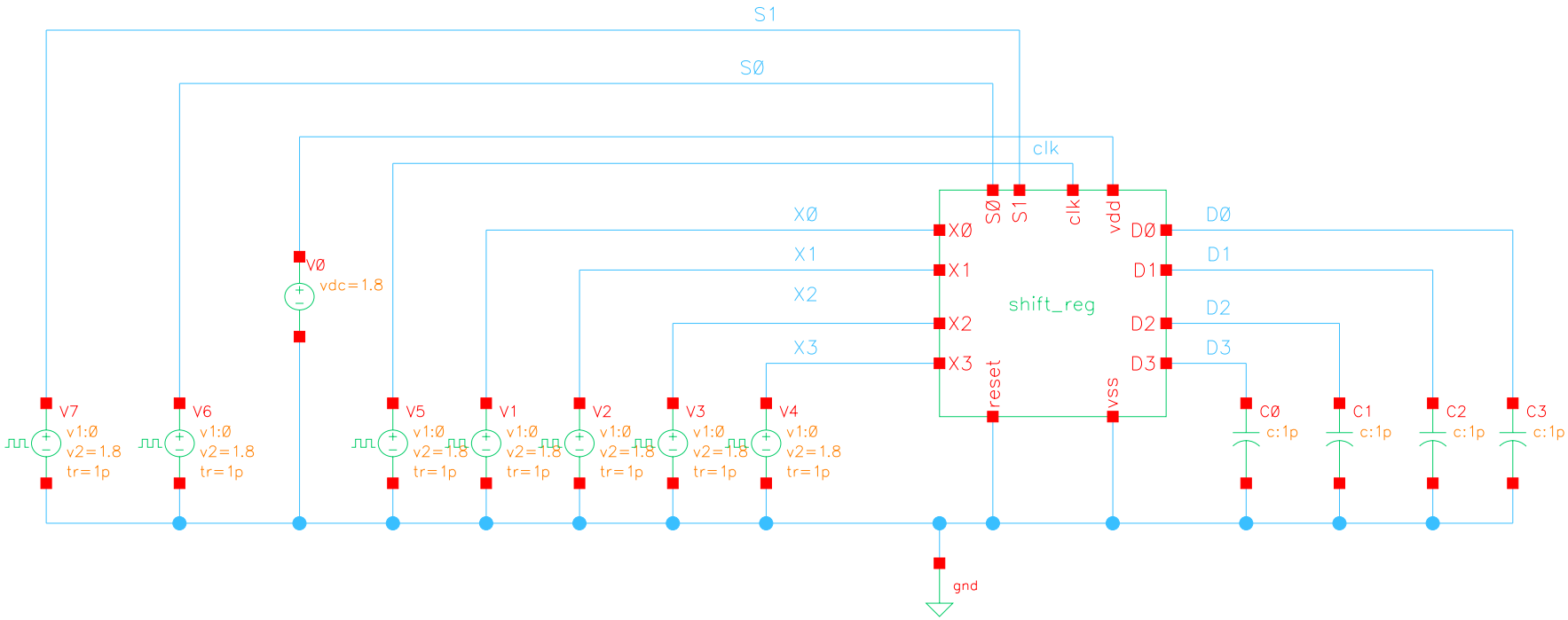


2. Shift Register

2.1 Schematic:

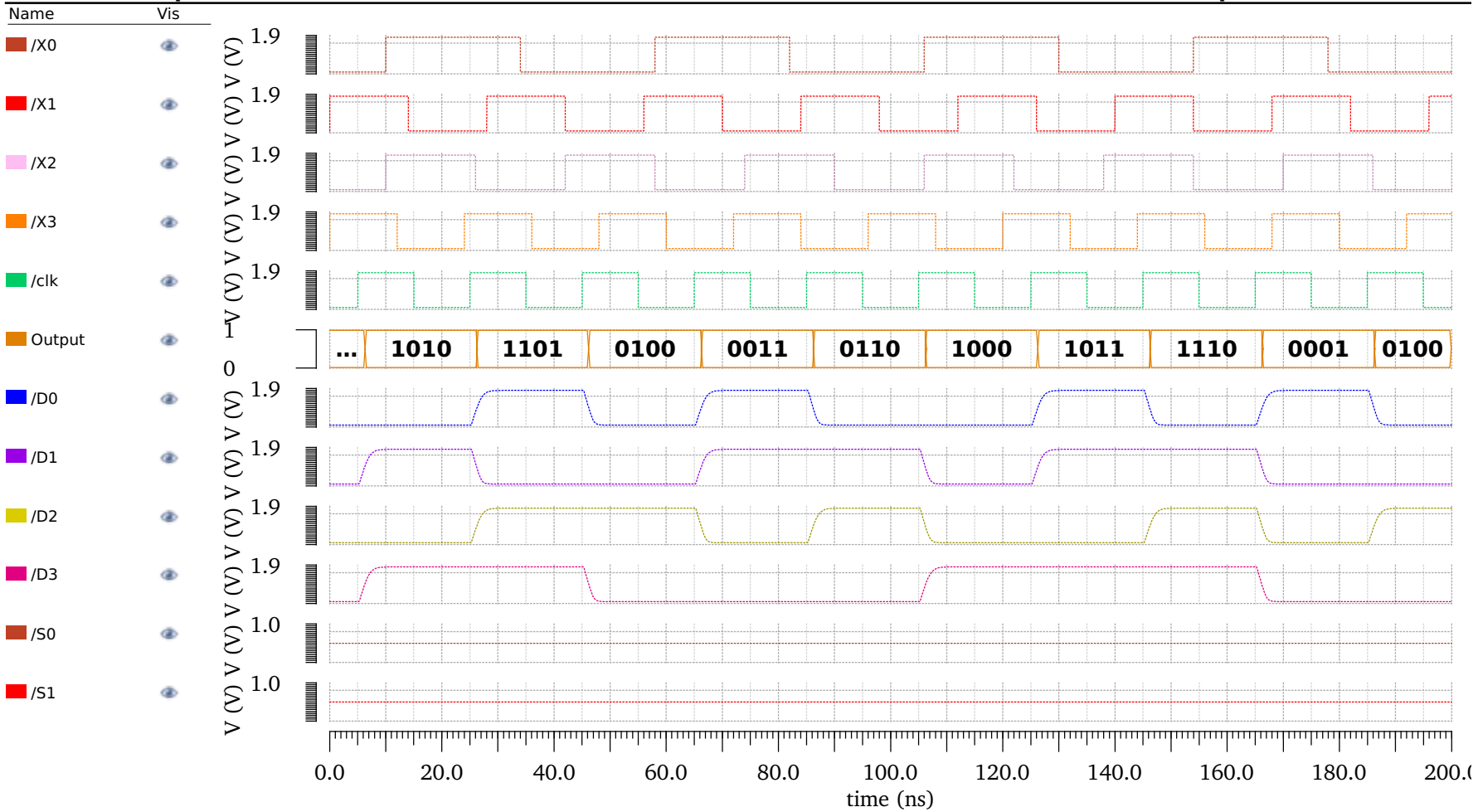


2.2 Shift Register Test Bench:



2.3 Shift Register (sel = 00 Output = Input) Simulation:

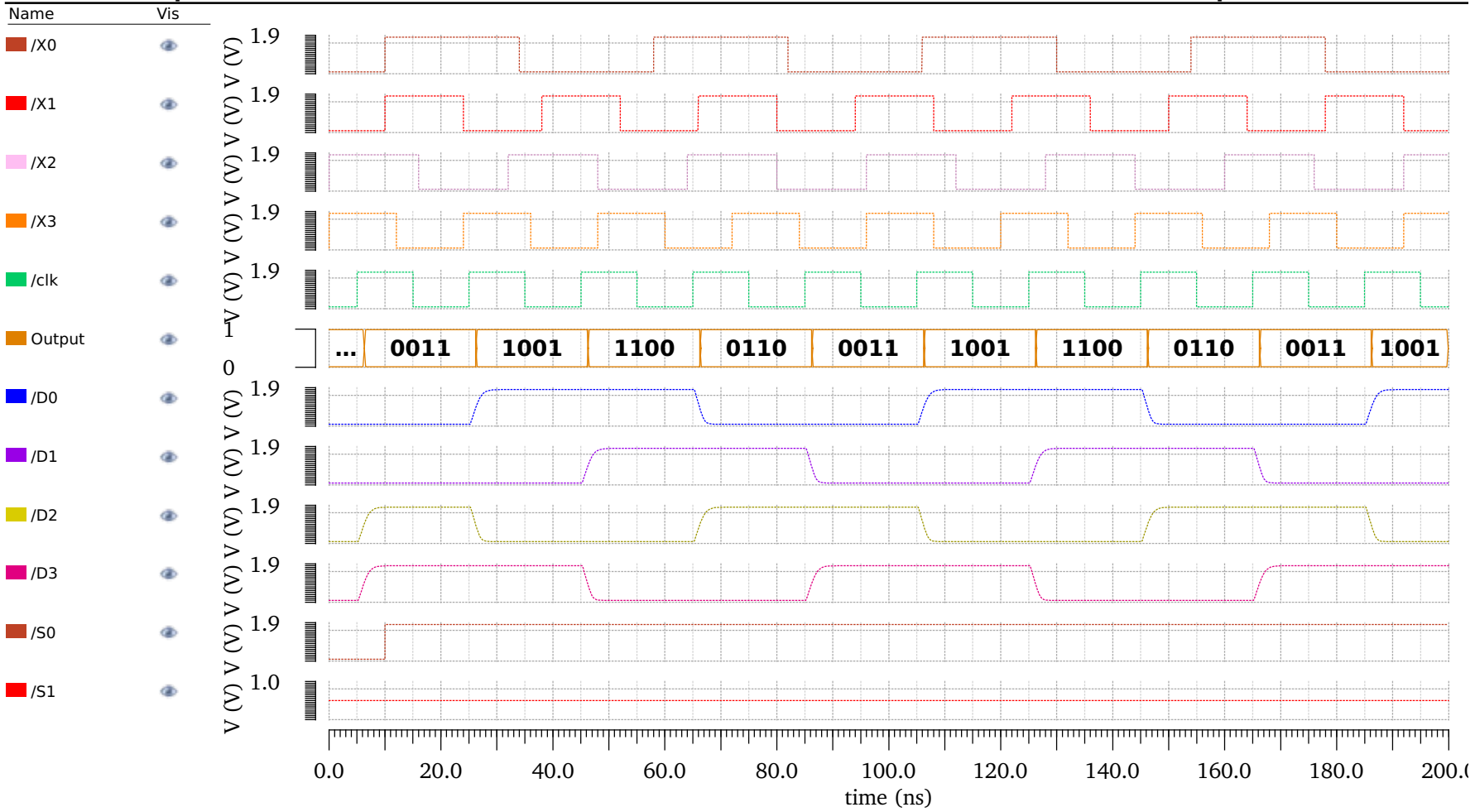
Transient Response **Fri Apr 19 18:16:47 2019**



MSB: D0, LSB:D3

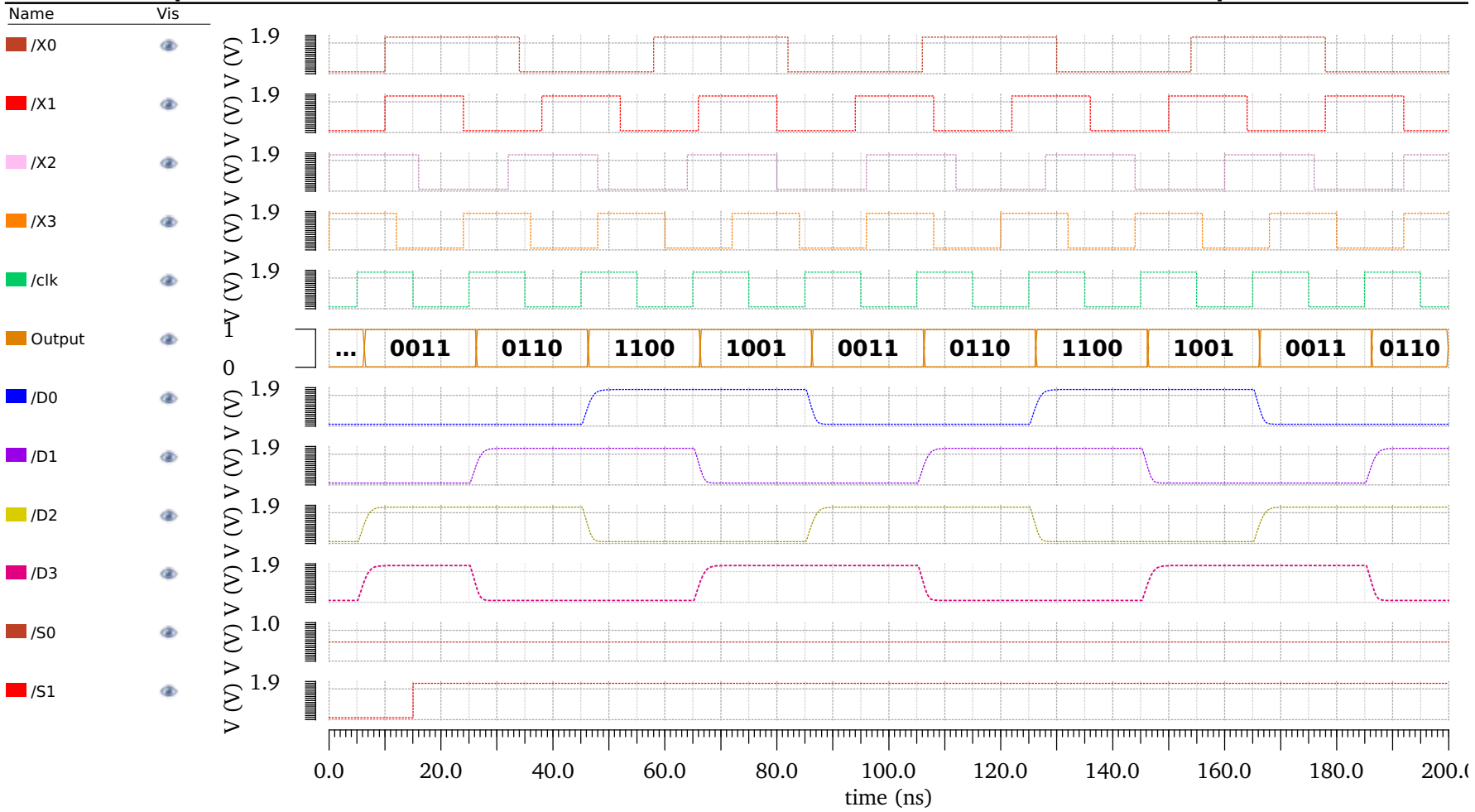
2.4 Shift Register (sel = 01 Right Shift) Simulation

Transient Response **Sat Apr 20 11:58:45 2019**



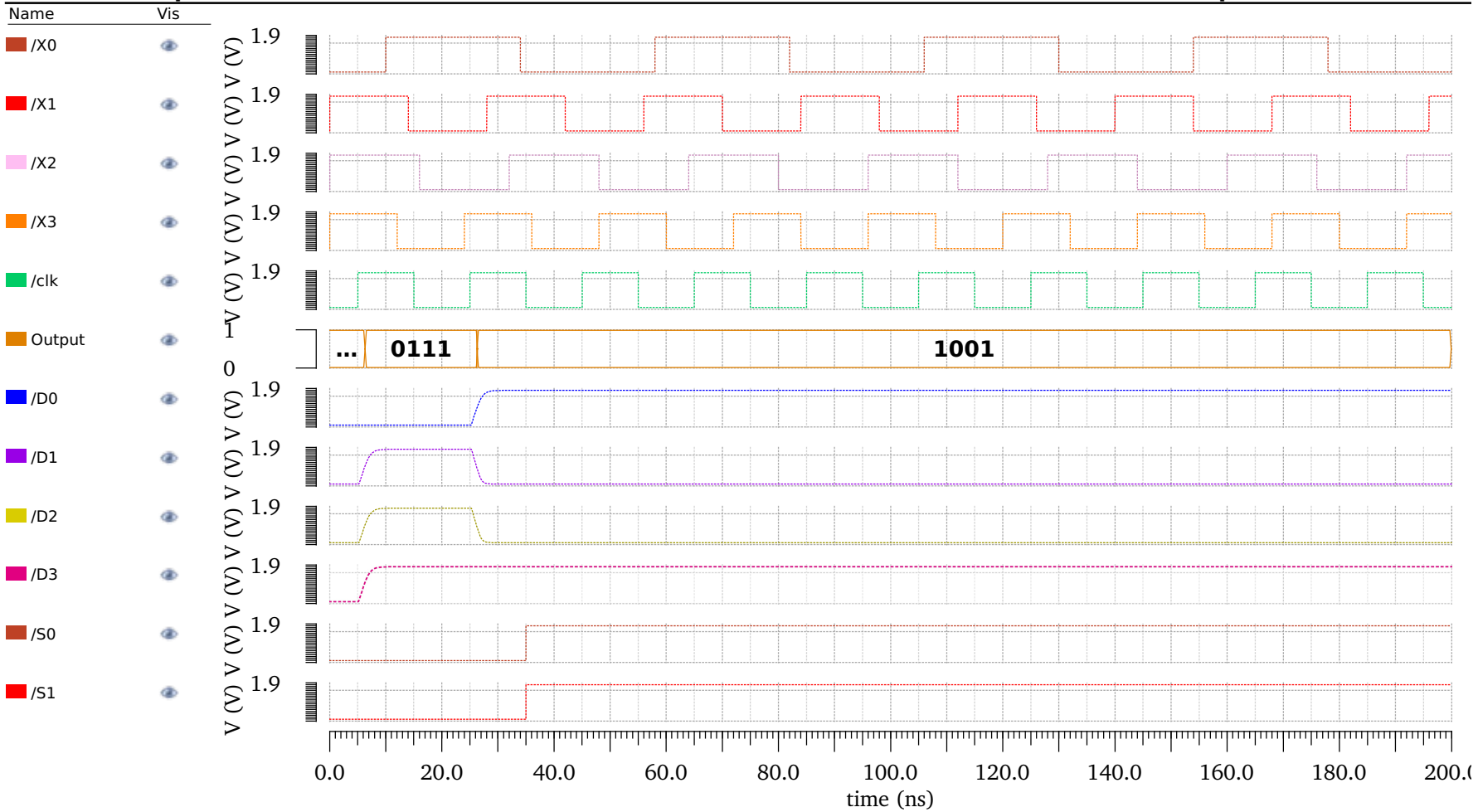
2.5 Shift Register (sel = 10 Left Shift)Simulation

Transient Response **Sat Apr 20 12:20:32 2019**



2.6 Shift Register (sel = 11 Output Holds Previous Value) Simulation

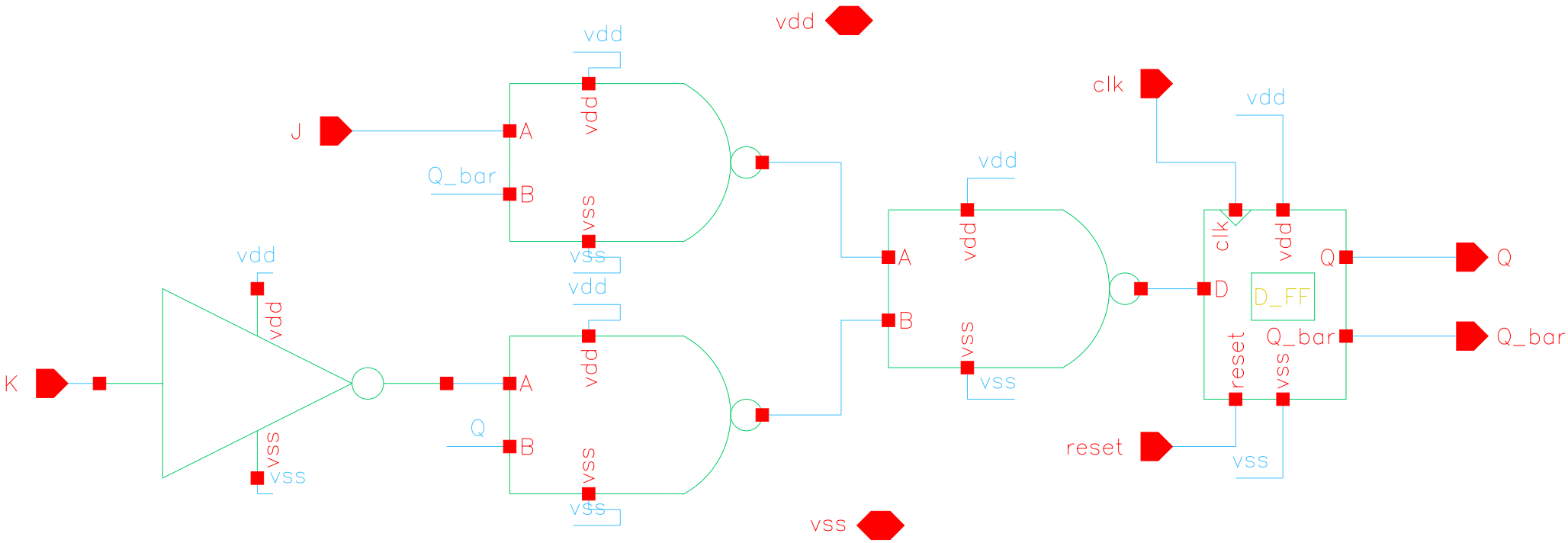
Transient Response **Sat Apr 20 12:29:51 2019**



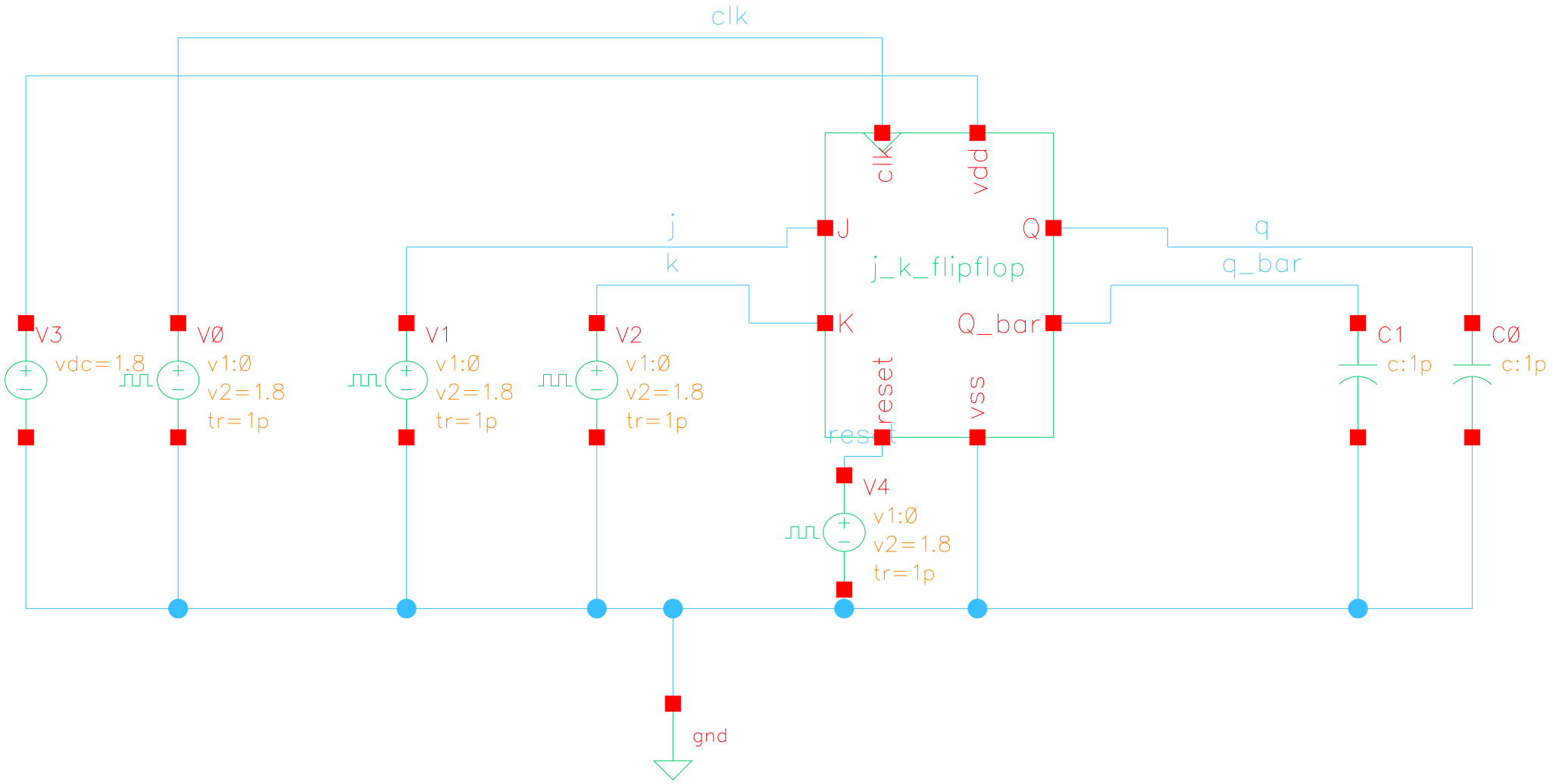
MSB: D0, LSB:D3

3. JK Flip-Flop

3.1 Schematic:

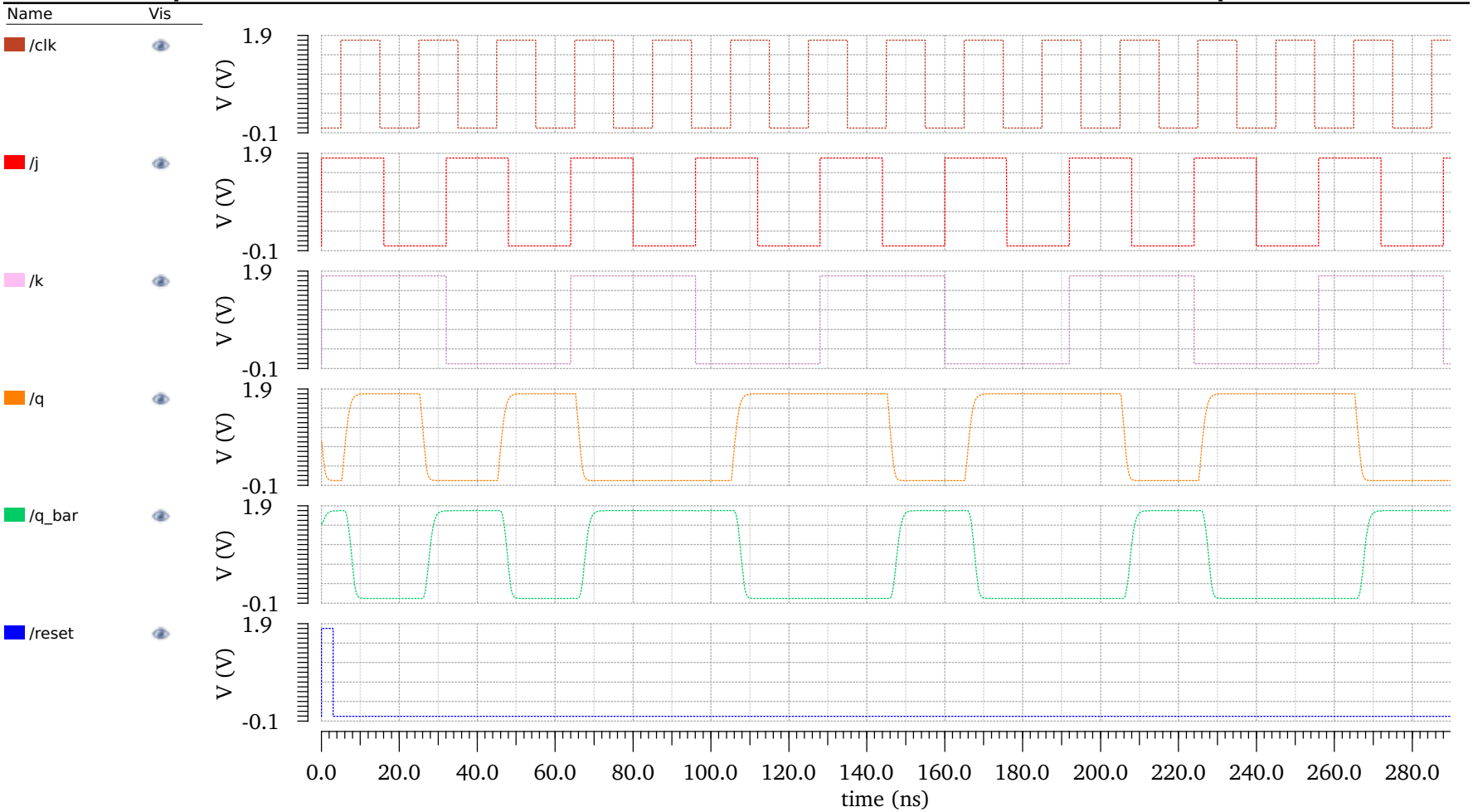


3.2 JK Flip-Flop Test Bench:



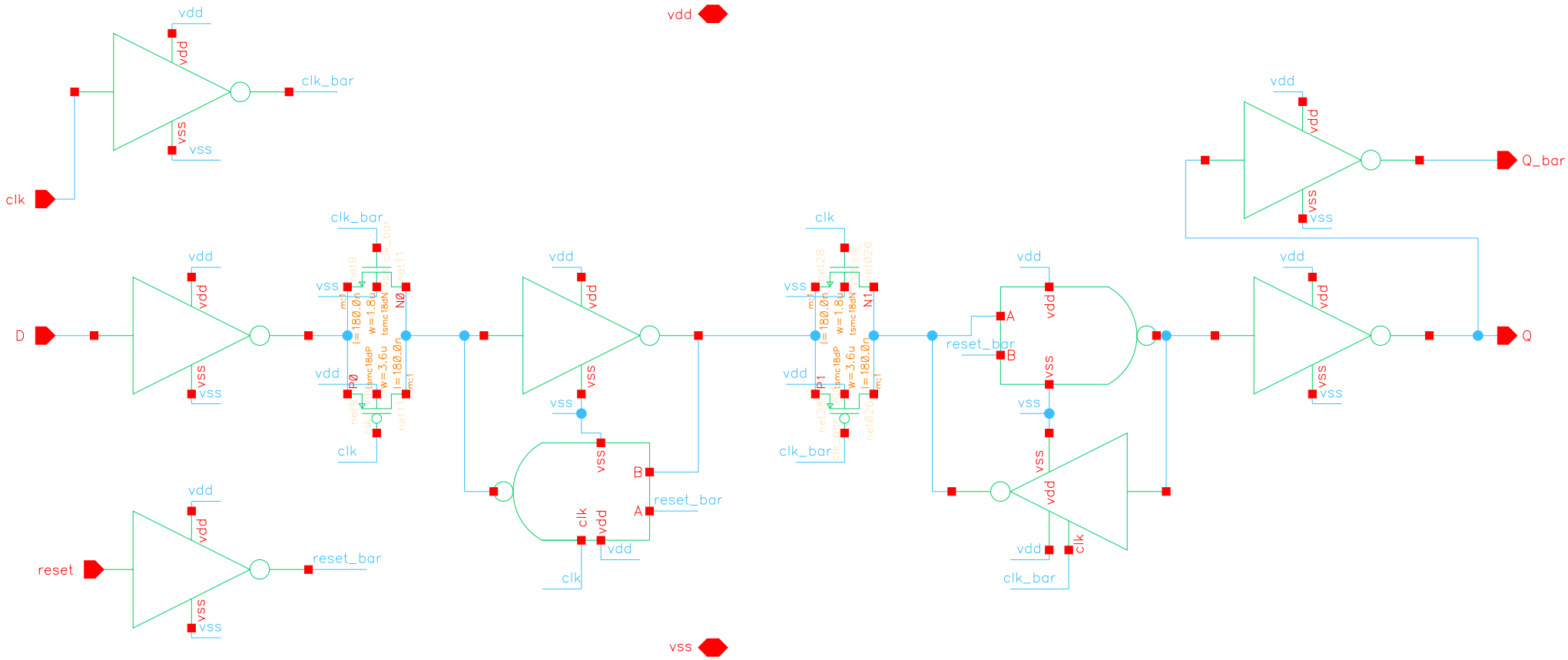
3.3 JK Flip-Flop Simulation:

Transient Response **Thu Apr 18 20:36:59 2019**

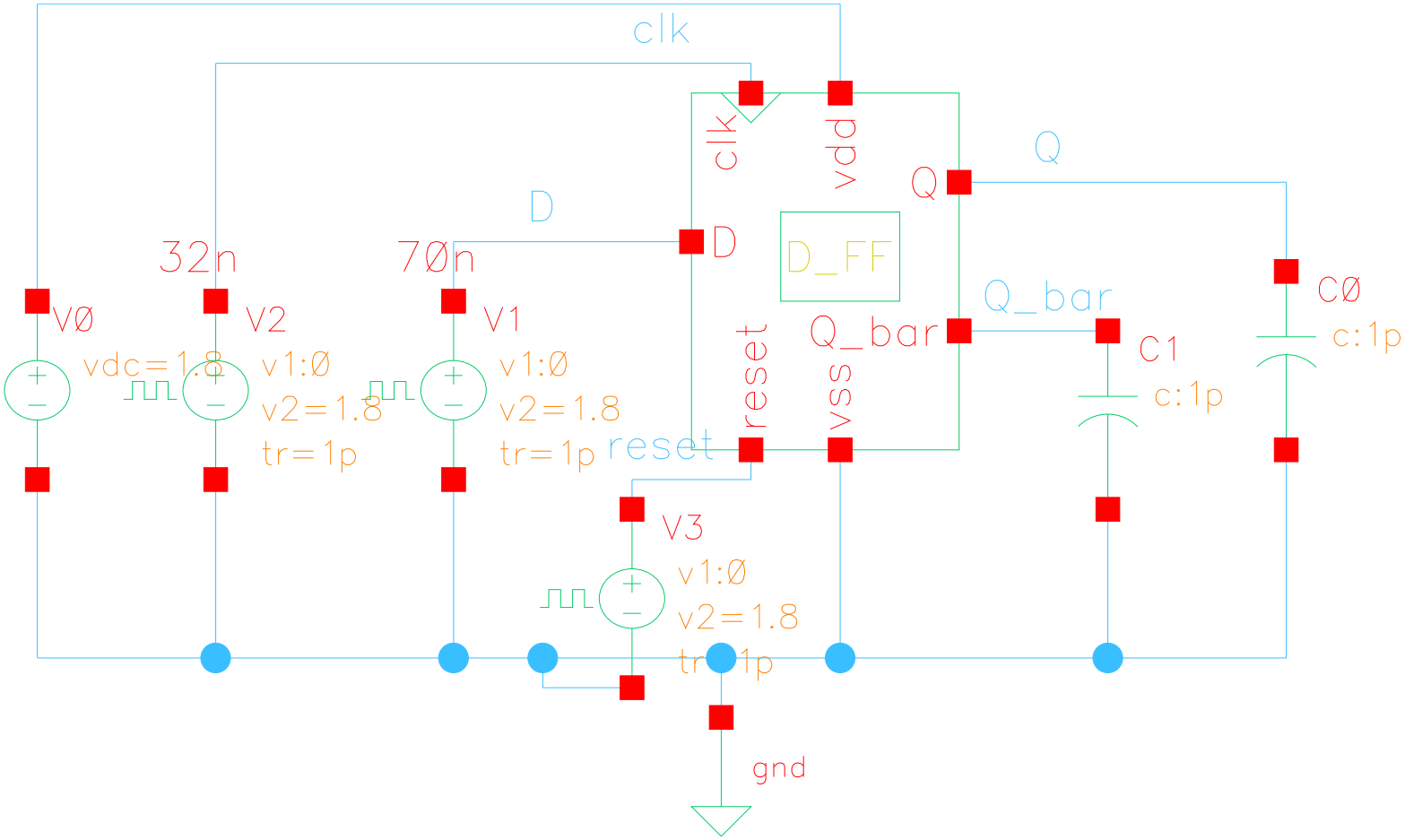


4. D Flip-Flop

4.1 Schematic:



4.2 D Flip-Flop Test Bench:



4.3 D Flip-Flop Simulation:

Transient Response **Thu Apr 18 20:13:19 2019**