



SACRAMENTO STATE

EEE 234
Digital IC Design

Project 2 – Assignment 1

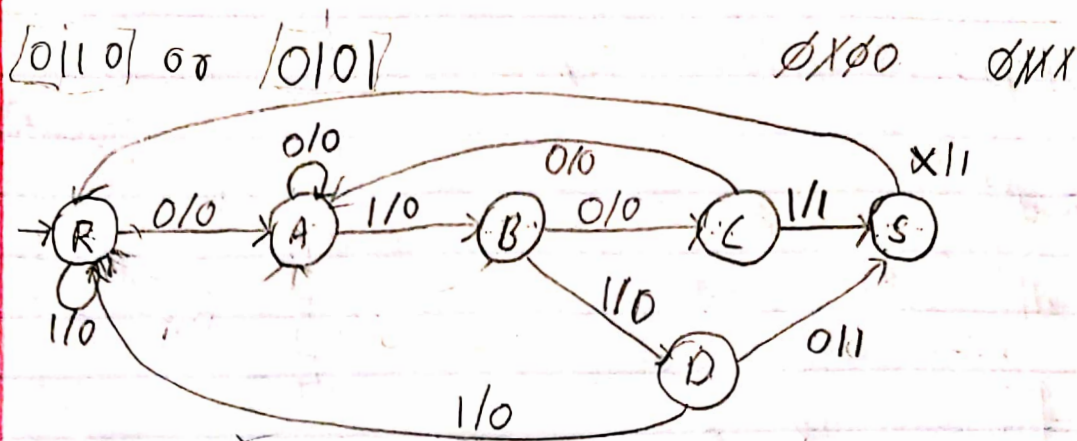
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Date of Submission: April 20, 2019

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1. Sequence Detector

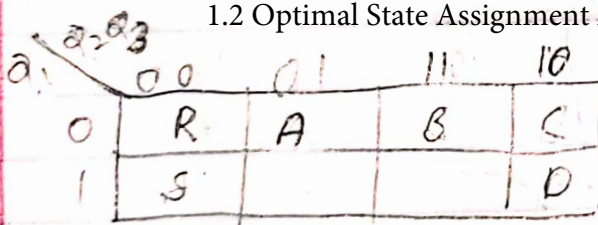
1.1 State Diagram



State Table

Current State	Next State		Output	
	X=0	X=1	X=0	X=1
R-000	A	R	0	0
A 001	A	B	0	0
B 011	C	D	0	0
C 010	A	S	0	1
D 110	S	R	1	0
S 100	R	R	1	1

1.2 Optimal State Assignment Map



- I. (R, A, C) (R, D, S)
 - II. (C, D) (A, S) (S, R)
 - III. (R, A, B, C) (D, S)
- ~~(C, S) (R, D)~~

1.3 K-Maps

Q_0

K-Map Q_0

Q_0 \ $Q_1 Q_2$	00	01	11	10
00	0	0	0	0
01	0	X	X	1
11	0	X	X	0
10	0	0	1	1

A B C D

X Q_0 Q_1 Q_2

$$J_0 = X Q_1$$

$$K_0 = X + \bar{Q}_1$$

Q_0 \ $Q_1 Q_2$	00	01	11	10
00	0	0	0	0
01	X	X	X	X
11	X	X	X	X
10	0	0	1	1

Q_0 \ $Q_1 Q_2$	00	01	11	10
00	X	X	X	X
01	1	X	X	0
11	1	X	X	1
10	X	X	X	X

Q_1

Q_1 \ $Q_0 Q_2$	00	01	11	10
00	0	0	1	0
01	0	X	X	0
11	0	X	X	0
10	0	1	1	0

K-Map Q_1

$$J_1 = X Q_2$$

$$K_1 = \bar{Q}_2$$

Q_1 \ $Q_0 Q_2$	00	01	11	10
00	0	0	X	X
01	0	X	X	X
11	0	X	X	X
10	0	1	X	X

Q_1 \ $Q_0 Q_2$	00	01	11	10
00	X	X	0	1
01	X	X	X	1
11	X	X	X	1
10	X	X	0	1

K Map Q2

Q_2^+	$x Q_0$	Q_1, Q_2			
		00	01	11	10
00		1	1	0	1
01		0	X	X	0
11		0	X	X	0
10		0	1	0	0

A B C D
X Q_0 Q_1, Q_2

$$J_2 = \bar{X} \bar{Q}_0$$

		Q ₁ Q ₂			
Q ₀		00	01	11	10
00		1	X	X	1
01		0	X	X	0
11		0	X	X	0
10		0	X	X	0

$$K_2 = Q_1$$

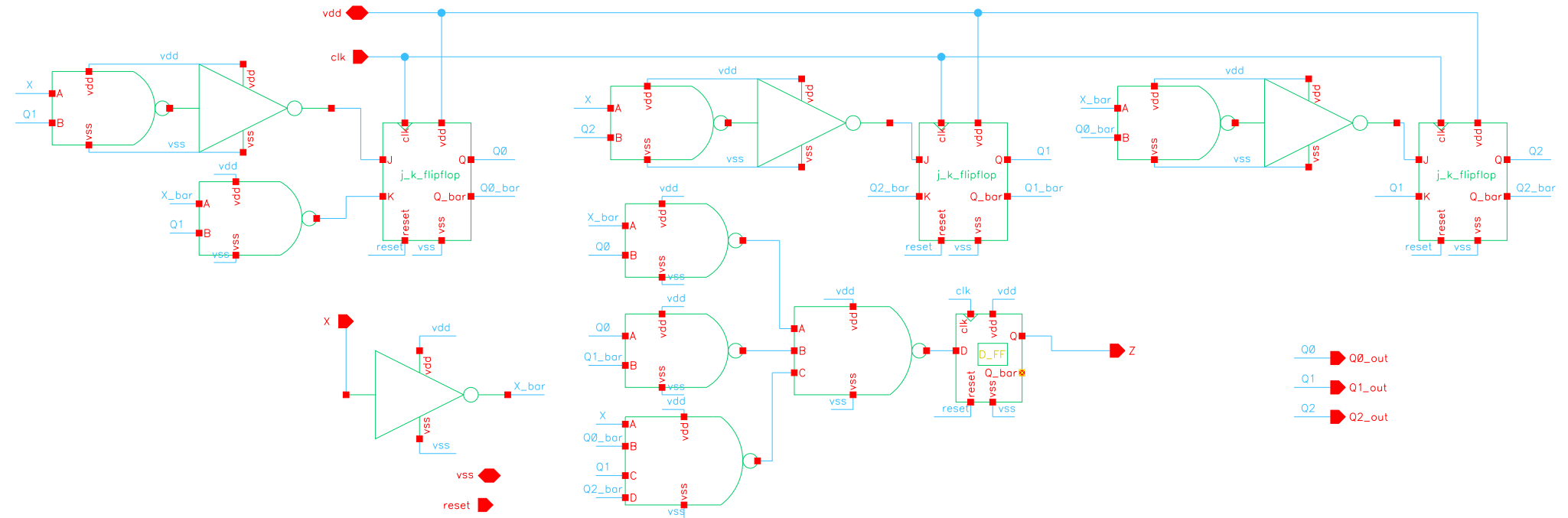
xq_0	q_1, q_2			
	X	0	1	X
	X	X	X	X
	x	X	X	x
	X	0	1	X

K Map Z

Z^+	x, Q_2	Q_1, Q_2			
		00	01	11	10
00	00	0	0	0	0
01	01	1	X	X	1
11	11	1	X	X	0
10	10	0	0	0	1

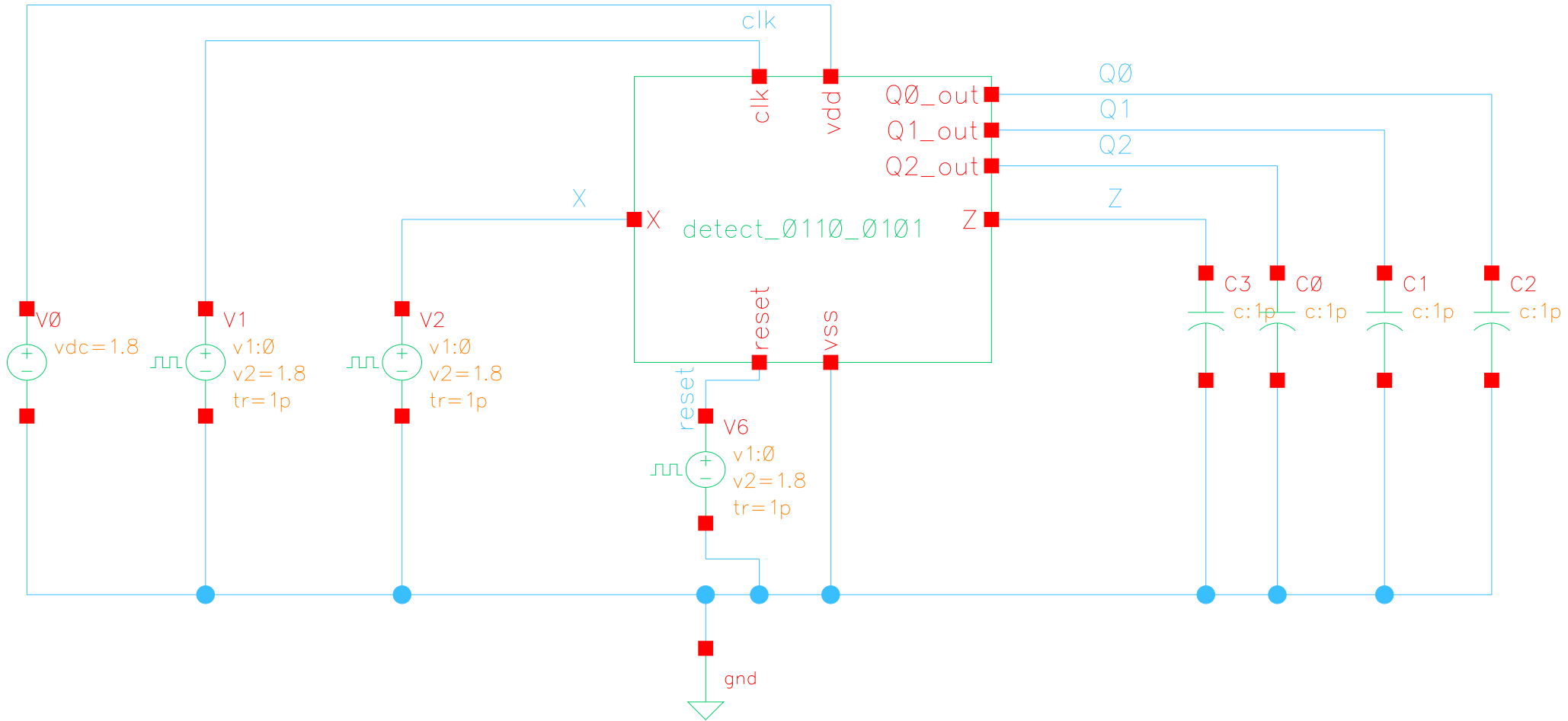
$$Z = \bar{X} Q_0 + Q_0 \bar{Q}_1 + X \bar{Q}_0 Q_1 \bar{Q}_2$$

1.4 Sequence Detector Schematic:



Pin `Q0_out`, `Q1_out`, `Q2_out`, are added for testing purpose only

1.5 Sequence Detector Test Bench:



1.6 State Table

Current State		Next State		Output	
		X = 0	X = 1	X = 0	X = 1
R	000	A	R	0	0
A	001	A	B	0	0
B	011	C	D	0	0
C	010	A	S	0	1
D	110	S	R	1	0
S	100	R	R	1	1

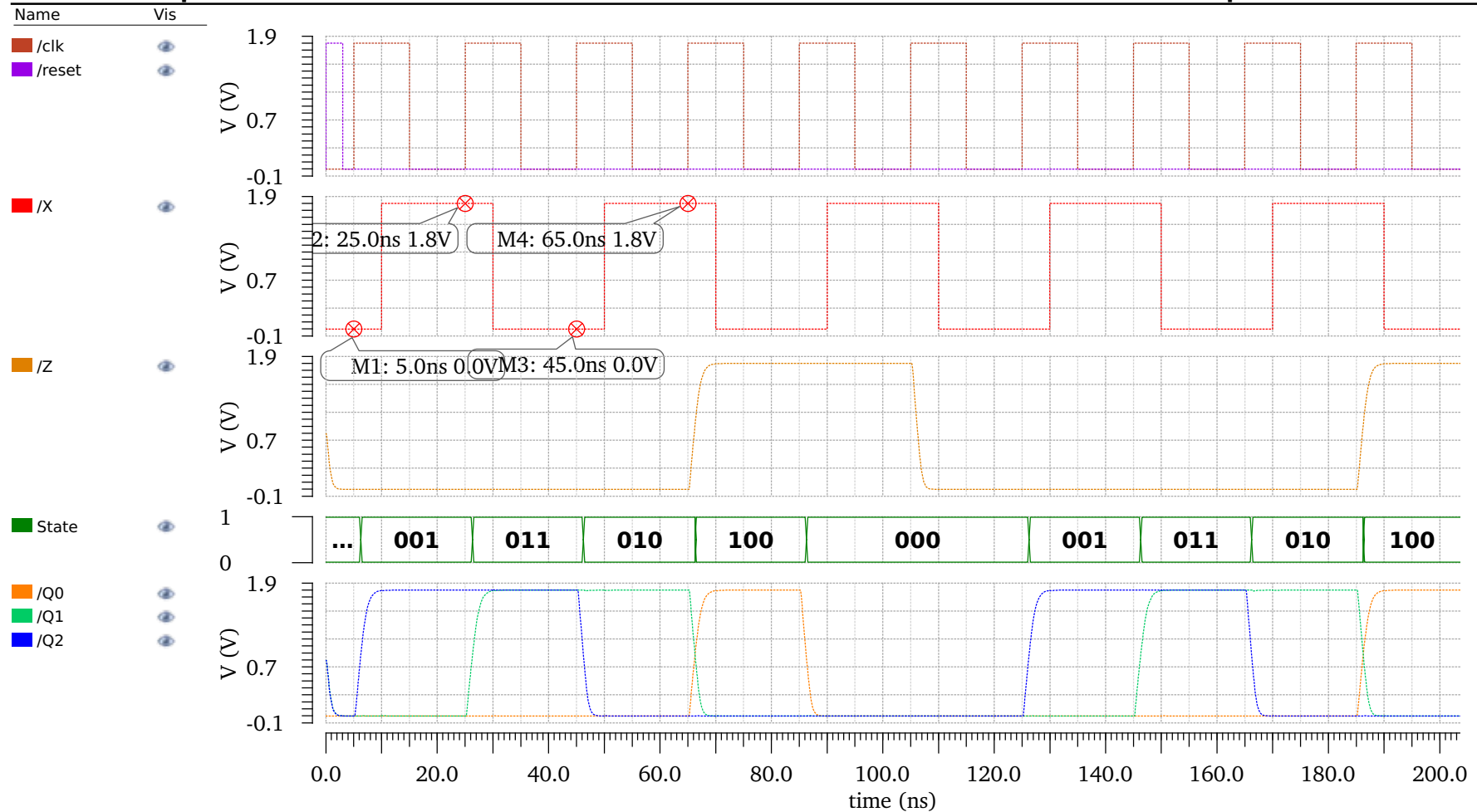
1.7 Sequence Detector Simulation (Input 0101):

project2:detect_0110_0101_test:1 : project2 detect_0110_0101_test schematic

17:31:54 Fri Apr 19 2019

Transient Response

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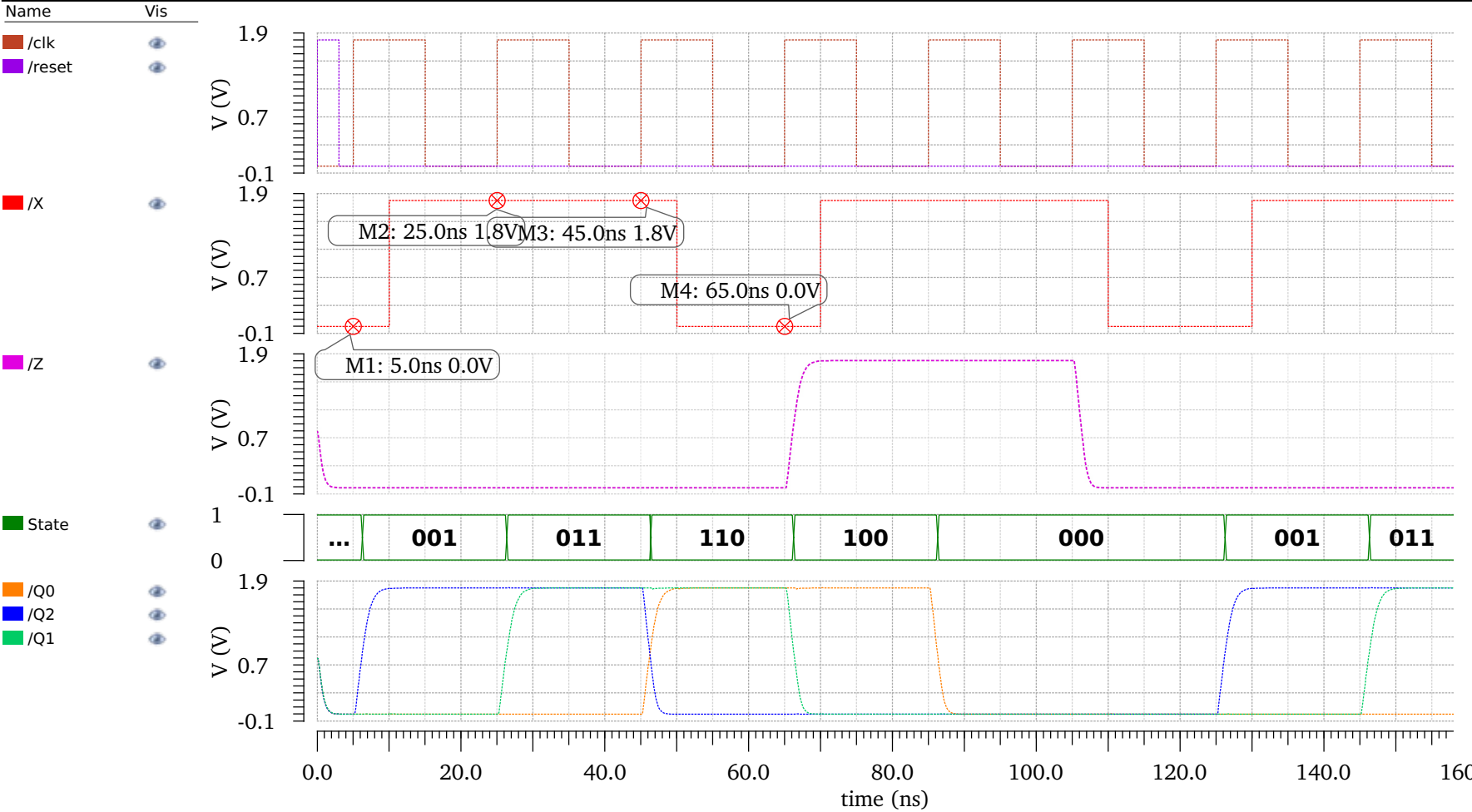
1.8 Sequence Detector Simulation (Input 0110):

project2:detect_0110_0101_test:1 : project2 detect_0110_0101_test schematic

19:56:19 Thu Apr 18 2019

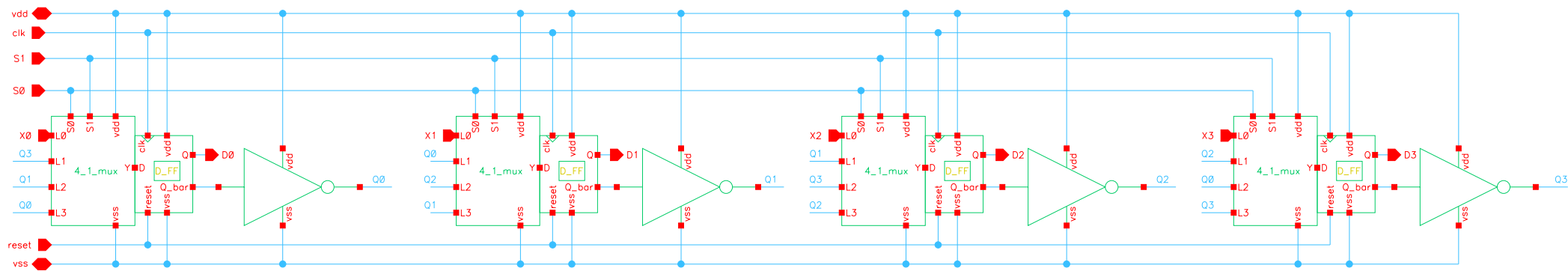
Transient Response

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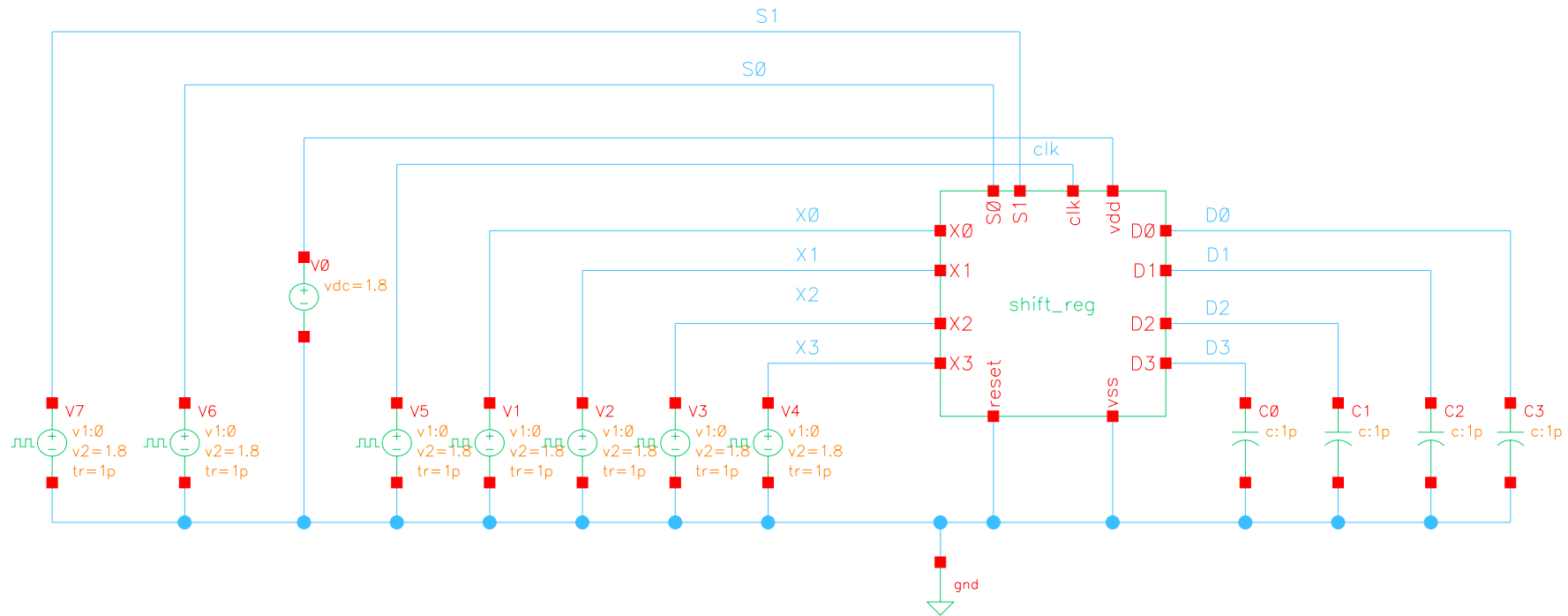


2. Shift Register

2.1 Schematic:



2.2 Shift Register Test Bench:



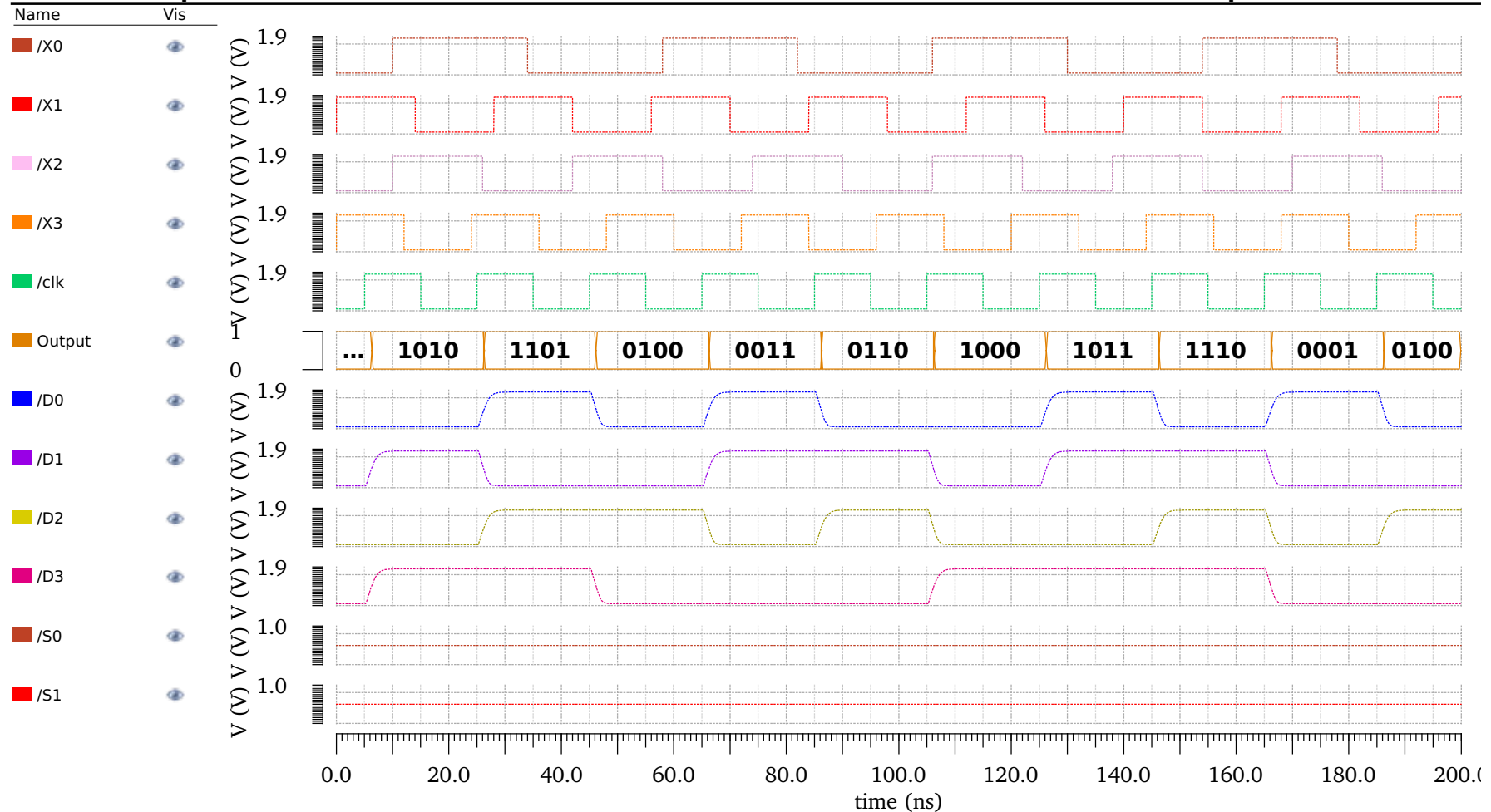
2.3 Shift Register (sel = 00 Output = Input) Simulation:

project2:shift_register_4bit_test:1 : project2 shift_register_4bit_test schematic

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MSB: D0, LSB:D3

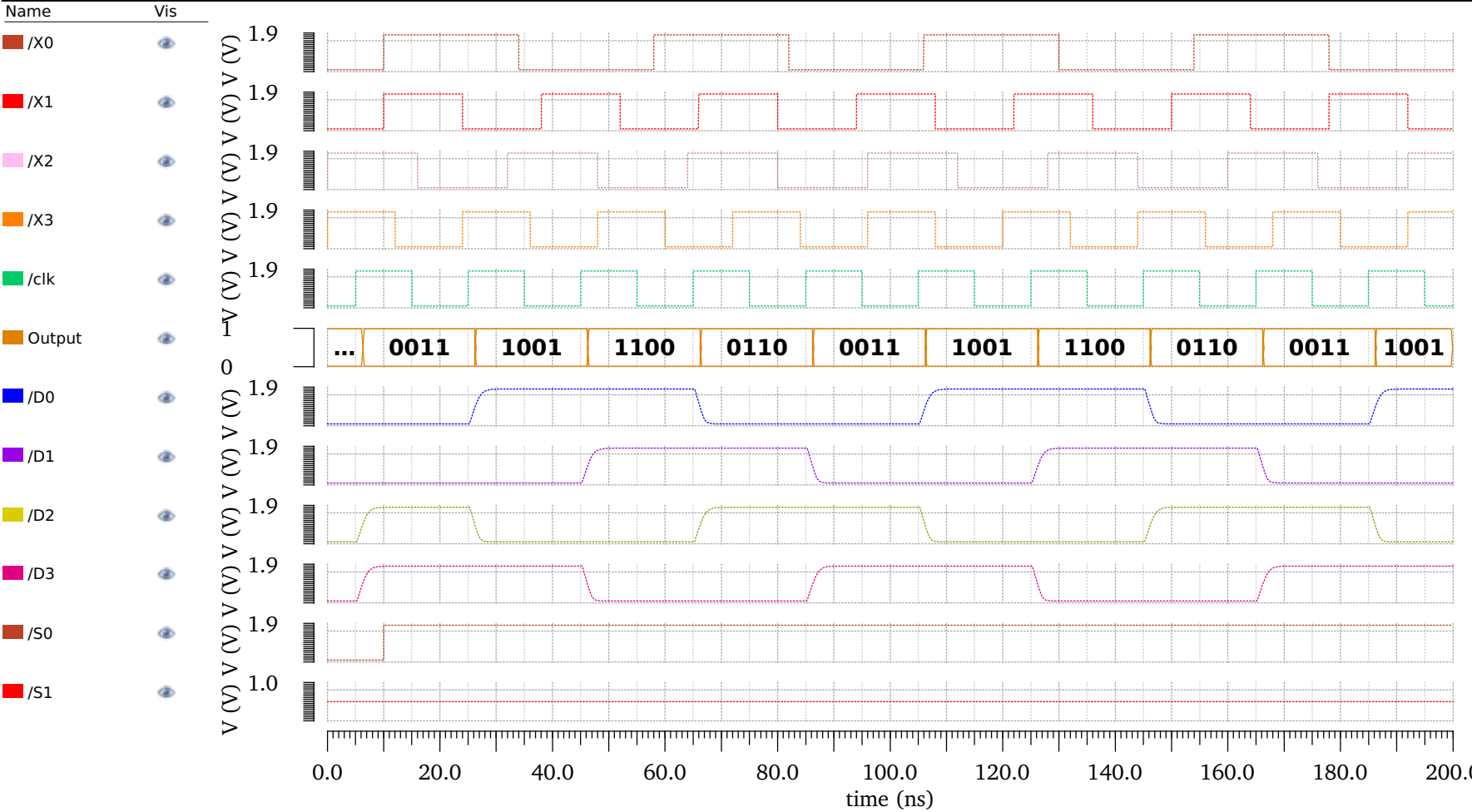
2.4 Shift Register (sel = 01 Right Shift) Simulation

project2:shift_register_4bit_test:1 : project2 shift_register_4bit_test schematic

12:12:37 Sat Apr 20 2019

Transient Response

Sat Apr 20 11:58:45 2019



2.5 Shift Register (sel = 10 Left Shift)Simulation

project2:shift_register_4bit_test:1 : project2 shift_register_4bit_test schematic

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Sat Apr 20 12:20:32 2019



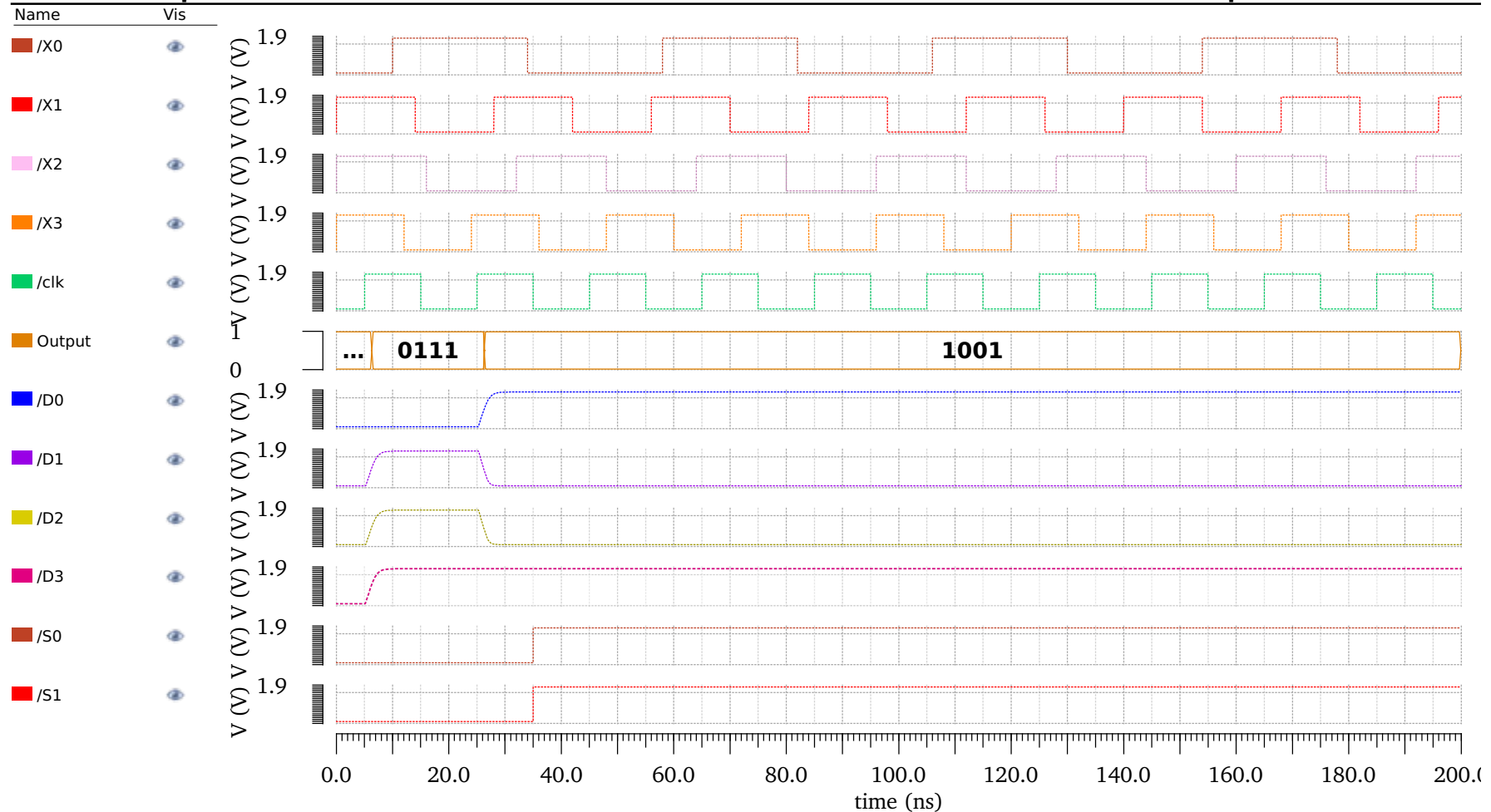
2.6 Shift Register (sel = 11 Output Holds Previous Value) Simulation

project2:shift_register_4bit_test:1 : project2 shift_register_4bit_test schematic

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Transient Response

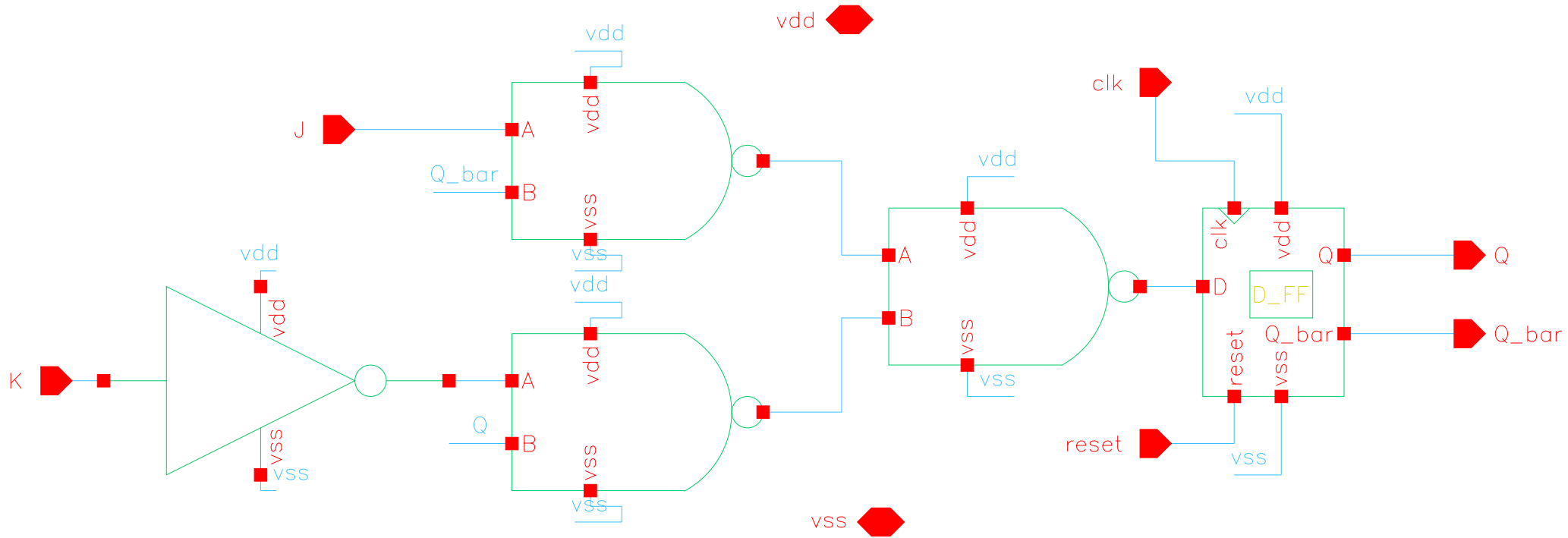
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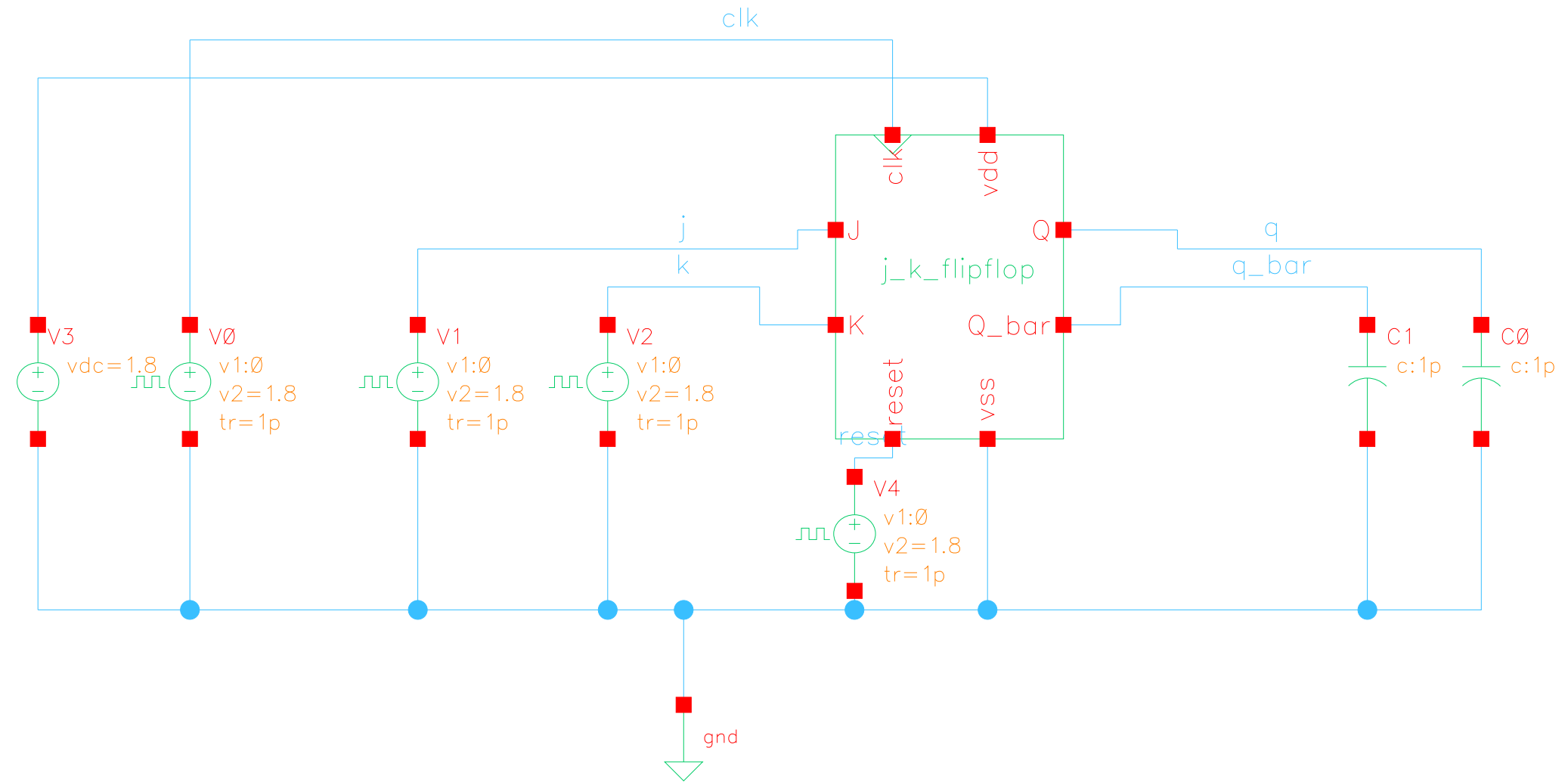
MSB: D0, LSB:D3

3. JK Flip-Flop

3.1 Schematic:



3.2 JK Flip-Flop Test Bench:



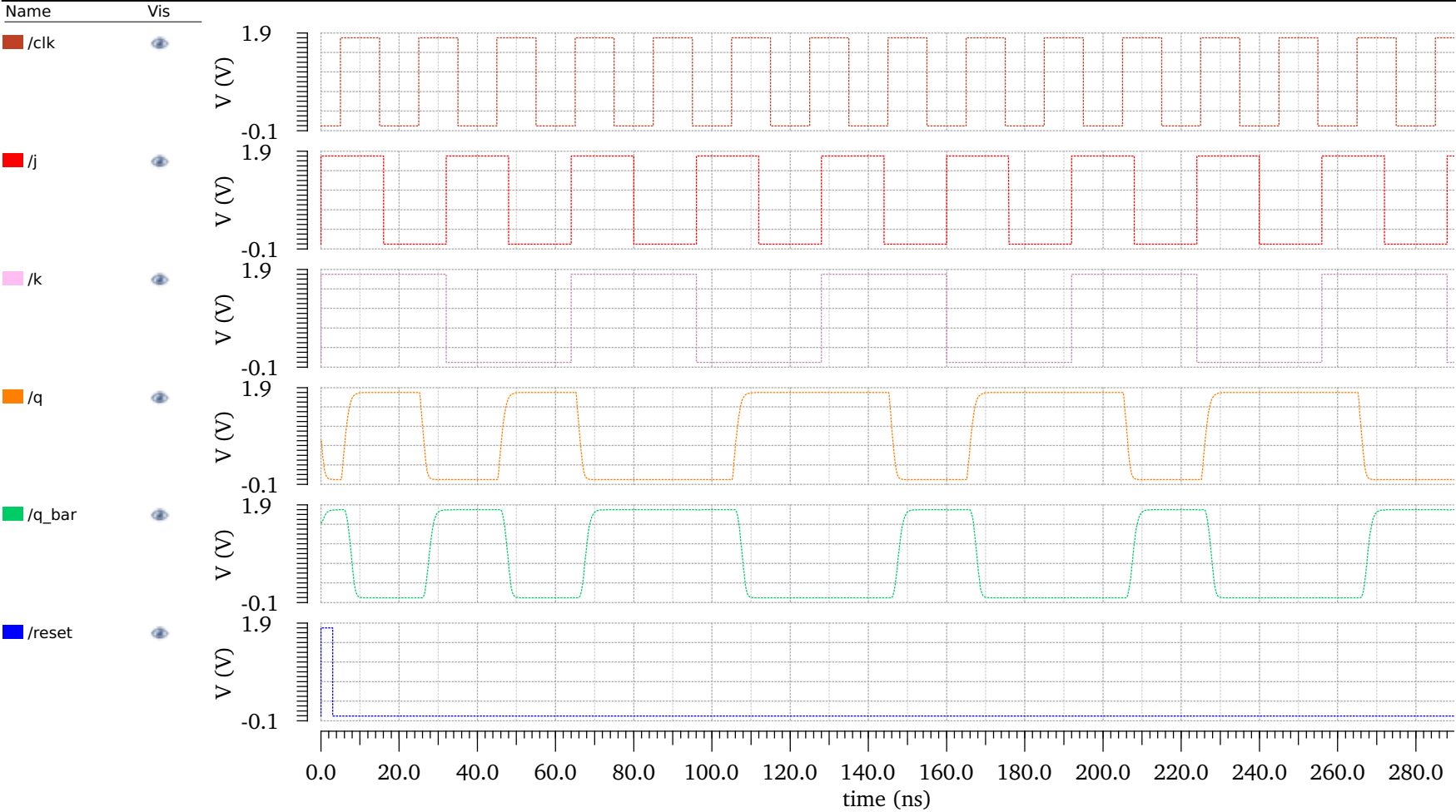
3.3 JK Flip-Flop Simulation:

project2:jk_flipflop_test:1 : project2 jk_flipflop_test schematic

20:41:08 Thu Apr 18 2019

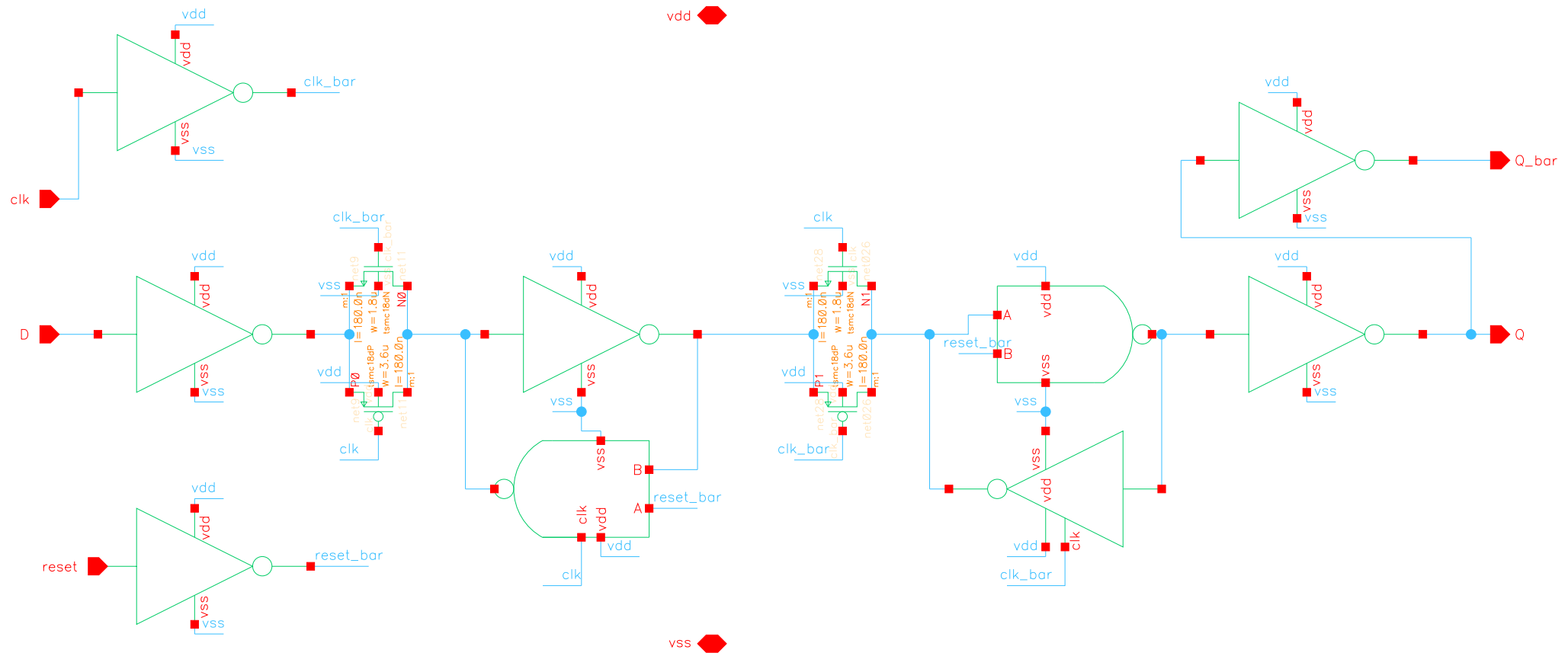
Transient Response

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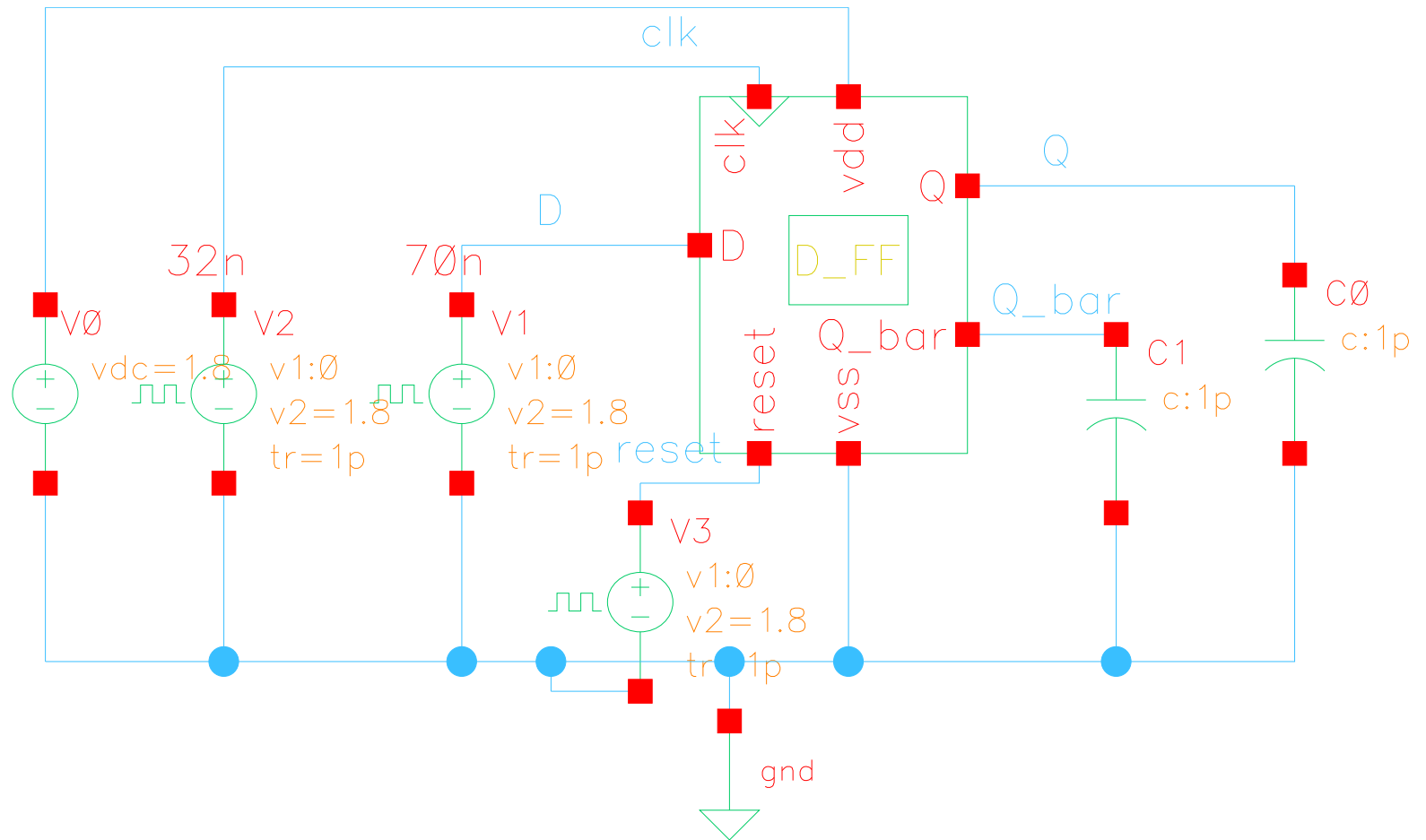


4. D Flip-Flop

4.1 Schematic:



4.2 D Flip-Flop Test Bench:



4.3 D Flip-Flop Simulation:

Transient Response

Thu Apr 18 20:13:19 2019

