Digital Electronics

Total Time taken - 18 days

~~Lect 01~~

3 July - 9 July

→ Boolean Algebra & logic Gate - 01 to 17

→ K- Map -

→ Combinational circuit - 18 to 35

~~Lect~~ -

→ Sequential circuit - 50 - 101

DAC & ADC

Rahul Bansod

Lect - 01

Boolean Theorem :-

1) $A + A = A$

$A + \bar{A} = 1$

$A + 0 = A$

$A + 1 = 1$

$A + B = B + A$

2) $A \cdot A = A$

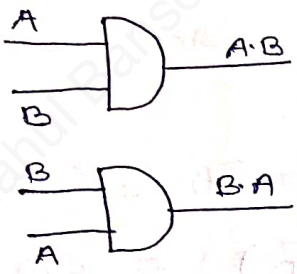
$A \cdot \bar{A} = 0$

$A \cdot 0 = 0$

$A \cdot 1 = A$

$A \cdot B = B \cdot A$ → commutative law (~~AND~~ all Gate holds commutative law)

e.g:-



3) $A \cdot [B + C] = (A \cdot B + A \cdot C)$ → Distributive law

AND is Distributive over OR

* $A + (B \cdot C) = (A + B) \cdot (A + C)$

* $A + \bar{A} \cdot B = (A + \bar{A}) \cdot (A + B)$

$= 1 \cdot (A + B)$

$= A + B$

* $\bar{A} + A \cdot B = (\bar{A} + A) \cdot (\bar{A} + B)$

$= 1 \cdot \bar{A} + B$

$= \bar{A} + B$

Note:- AND is Distribute over OR & vice versa.

Ex) Imp

$\bar{A}B + \bar{A}C + \underline{BC} = (AB + \bar{A}C)$

$\bar{A}B + AC + \underbrace{BC}_{\text{Redundant term}} = \bar{A}B + AC$

Lect-02

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$		1	1	
A			1	1

K MAP

e.g:- $\bar{A}B + AC + \underline{BC} = \bar{A}B + AC$

e.g:- $x(A+C) + \bar{x}(B+D) + \underbrace{(A+C)(B+D)}_{\text{Redundant term}}$

$= x(A+C) + \bar{x}(B+D)$

What is duality theorem

→ It is states that " If in a boolean expression ~~AND is~~

'AND' → 'OR', 'OR' → AND and 'NOT' → 'NOT'

Then the new boolean expression will also be true.

e.g:- $AB + \bar{A}C + BC = AB + \bar{A}C$ - SOP

$(A+B)\cdot(\bar{A}+C)\cdot(B+C) = (A+B)\cdot(\bar{A}+C)$ - POS

e.g:-

$\overline{AB} \longrightarrow \overline{A+B}$

$f(A,B) = AB + BC$

$f^D(A,B) = (A+B)\cdot(B+C)$

NAND $\xrightarrow{\text{dual}}$ NOR

NOR $\longrightarrow$ NAND

XOR $\longrightarrow$ XNOR

XNOR $\longrightarrow$ XOR

e.g:- $f(A,B) = A\bar{B} + \bar{A}B$

$f^D(A,B) = (A+\bar{B})\cdot(\bar{A}+B)$

$= AB + \bar{A}\bar{B}$

e.g:- $f(A,B,C) = AB + BC + CA$

$f^D(A,B,C) = (A+B)\cdot(B+C)\cdot(C+A)$

$= AB + BC + CA$ → self dual function

Lect-03

e.g:- n variable

3-variable $\longrightarrow 2^3 \rightarrow 8 \longrightarrow$

$\bar{A}\bar{B}\bar{C}$	0	0	0
$\bar{A}\bar{B}C$	0	0	1
$\bar{A}B\bar{C}$	0	1	0
$\bar{A}BC$	0	1	1
$A\bar{B}\bar{C}$	1	0	0
$A\bar{B}C$	1	0	1
$AB\bar{C}$	1	1	0
ABC	1	1	1

n variable $\rightarrow 2^n$

$\rightarrow 0 - (2^n - 1)$

$f(A,B,C) = 0$

$f(A,B,C) = \bar{A}\bar{B}\bar{C}$

$f(A,B,C) = \bar{A}\bar{B}C$

$f(A,B,C) = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C = \Sigma(0,1)$ SOP

$2^4\ 2^3\ 2^2\ 2^1\ 2^0$

$1\ 1\ 1\ 1\ 1 = 2^5 - 1 = 31$

$f(A,B,C) = \Sigma(0,1)$

$f(A,B,C) = \Sigma(1,2)$

$\pi\Sigma(2,3,4,5,6,7)$ POS

$\therefore$ n-variables

$N = 2^n \rightarrow$ Terms

$N_{C_0} + N_{C_1} + N_{C_2} + N_{C_3} + N_{C_4} + \cdots N_{C_N}$

$= 2^N$

$= (2^{2^n})$

disticnt boolean function $= \left[2^{2^n}\right]$

$\therefore 2^{2^3} = 2^8 = 256$

- If a dual of a boolean function then we will get dual boolean function of the initial boolean function

- The dual boolean function maybe or maynot be equal to the original boolean function. If the dual boolean function is equal to the original boolean function then we can say that this boolean function is self dual in nature.

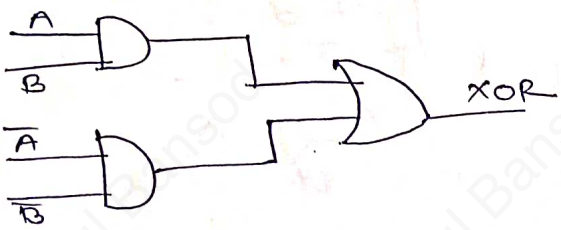
g:- n-variable
Boolean (distinct) function are possible $= 2^{2^n}$

number of self dual boolean functions $= 2^{2^{(n-1)}}$

3 variables
Total boolean function $= 2^{2^3} = 256$

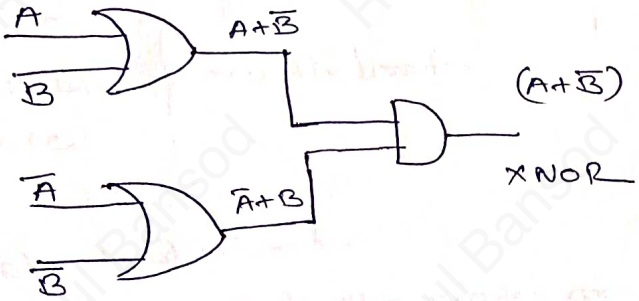
self boolean function $= 2^{2^{(n-1)}} = 2^{2^2} = 2^4 = 16$

e.g:-



$= A\bar{B} + \bar{A}B$
$= A \oplus B$

Dual



$(A+\bar{B})(\bar{A}+B) = \bar{A}\bar{B} + A \cdot B$
$= A \odot B$

Lect-04

Gates :→

Basic Gates → NOT, AND, OR

Arithmetic Gates → XOR, XNOR

Universal Gates → NAND, NOR

SOP - $\bar{A} \rightarrow 0$
$A \rightarrow 1$

POS - $0 \rightarrow A$
$1 \rightarrow \bar{A}$

101 → SOP → $A\bar{B}C$

101 → POS → $\bar{A}+B+\bar{C}$

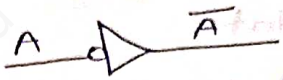
$\pi(1,2)$

$f(A,B,C) = (A+B+\bar{C}).(A+\bar{B}+C)$ - POS

$\Sigma(1,2) = f(A,B,C)$

$= \bar{A}\bar{B}C + \bar{A}B\bar{C}$ - SOP

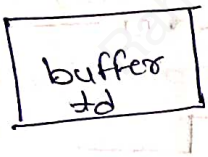
NOT :→

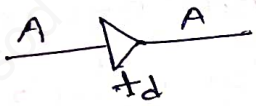


'inverting buffer'

I/P	O/P
A	$\overline{A}$
0	1
1	0

Imp → Buffer is a circuit that passes the input as it is the output with some delay





→ Bistable
monostable
Astable
} multivibrator

Bistable multivibrator

'0', '1' → both the states are stable.

$0 \xrightarrow{\text{trigger}} 1 \xrightarrow{\text{trigger}} 0$

e.g:- (F/F)

→ Monostable multivibrator

1 - stable state

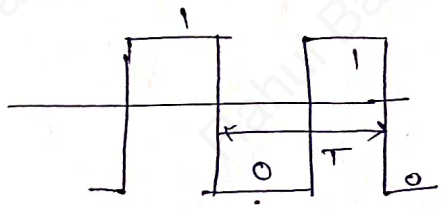
'0' → unstable or quasi stable state

'1' $\xrightarrow{\text{trigger}}$ '0' $\xrightarrow[\text{after some time}]{\text{No trigger}}$ '1'

→ Astable multivibrator

0, 1 are unstable state

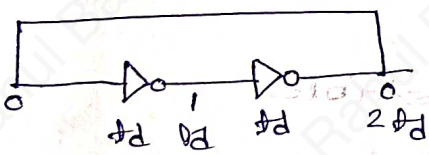
0 → '1' → 0 → 1 → 0 → 1

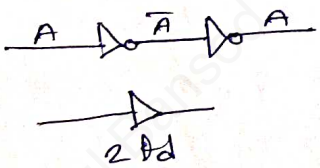


Lect-05

e.g:-

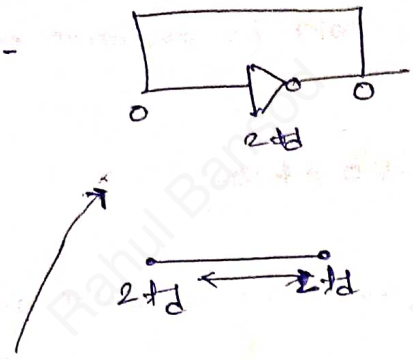
→





} Buffer.

e.g :-



even - 2, 4, 6, 8, 10
odd → 1, 3, 5, 7, 9, 11, 13

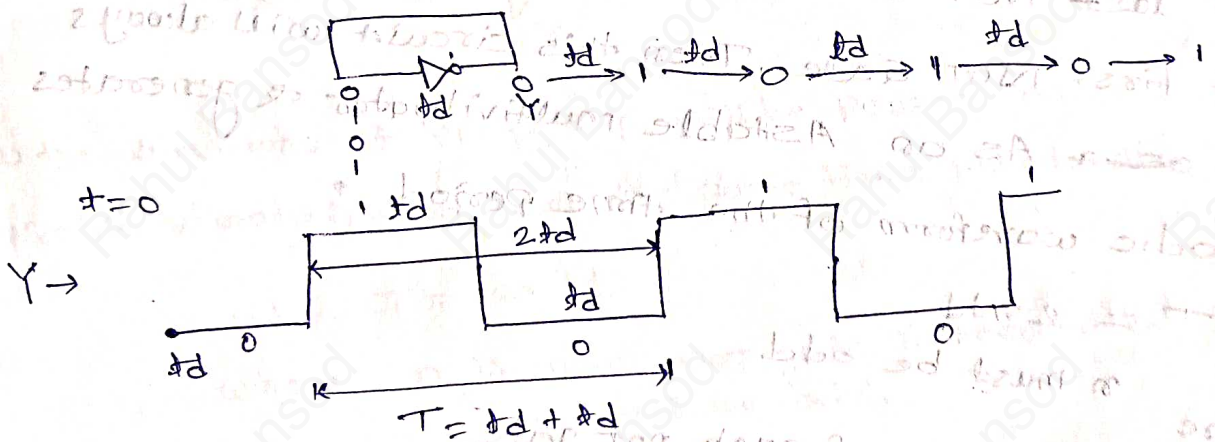
Bistable multivibrator

→ when even no. of NOT gates are in cascaded & The output of last NOT Gate is feed back into the input of first NOT Gate then this circuit will work as a bistable multivibrator.

→ If in feedback loop there are even no. of not gate in feedback loop then the circuit will work as a bistable multivibrator

Lect - 06

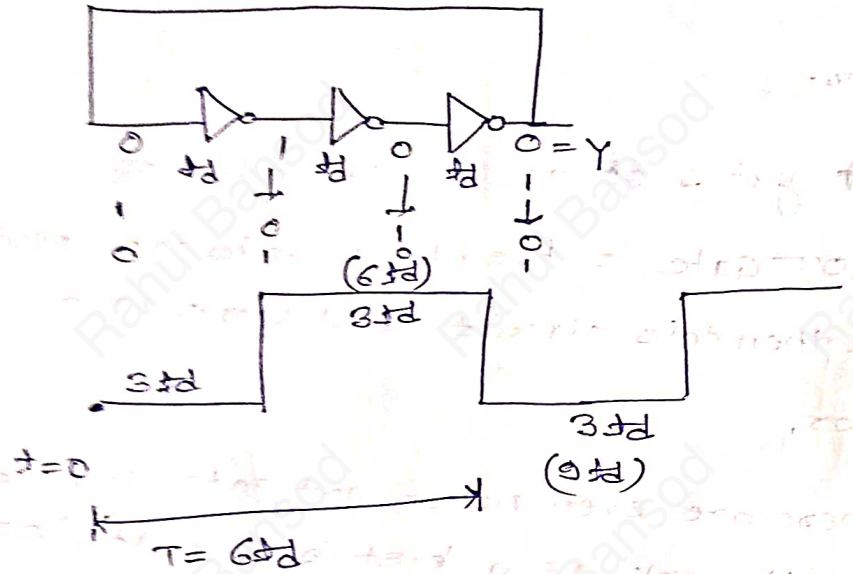
Astable multivibrator using not gate



$T = td + td$
$= 2td$

$$f = \frac{1}{T} = \frac{1}{2t_d}$$

Odd no. of not gates



$$f = \frac{1}{6t_d}$$

- when odd no. of not gates are cascaded and the o/p of last NOT Gate ~~to the i/p~~ is feedback into the i/p of first NOT Gate. Then this circuit will always work ~~as a~~ As an Astable multivibrator & generates a periodic waveform of the time period.

$$T = 2nt_d$$

n must be odd

where

t_d is delay of each not gate

$$f = \frac{1}{2nt_d} = \frac{1}{T}.$$

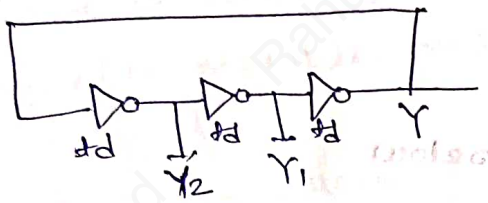
n → number of NOT Gates in feed back loop and must be odd.

Lect - 07

→ There must be odd no. of NOT Gate in feed back loop for the ckt to work as an Astable multivibrator.

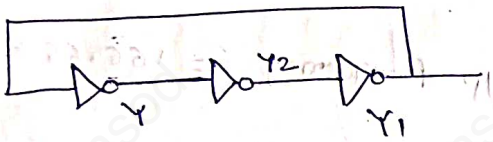
~~Astable~~

e.g:-



Y_1 →

Y_2 →



→ All the waveforms at Y_1 Y_2 & Y will be periodic nature (o/p of astable vibrator) with the same time period.

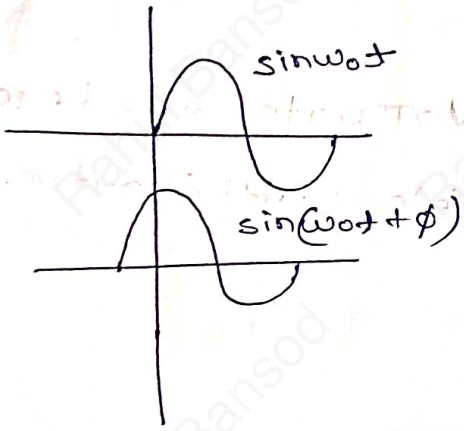
$$T = 2ntd$$

where n is no. of not gate in feed back loop & n must be odd.

$$f = \frac{1}{2ntd}$$

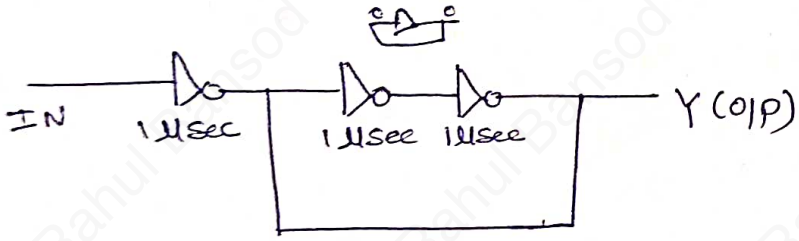
- but the waveforms at Y_2, Y_1, Y will not be same they will have phase difference ~~with~~ between them.

e.g:-



Lect-08

Q1) A digital circuit is given below



The circuit will work as a

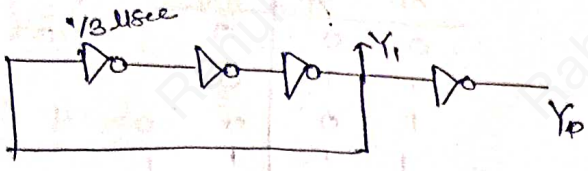
a) Astable multivibrator with o/p frequency $f = 166.66$ KHz

✓b) Bistable multivibrator

c) Astable multivibrator with o/p frequency $f = 333.33$ KHz

d) non-of these

Q2) A digital circuit is designed using NOT Gate, where delay of each NOT Gate is 1/3 μsec, the ckt is given below →



at o/p Y, we will get

a) square wave of ~~following~~ frequency 375 KHz

b) square wave of frequency 500 KHz

c) square wave of frequency 1000 KHz

d) o/p is o/p of a bistable multivibrator.

sol:-

$$T = 2 \times 3 \times \frac{1}{3} = 2\ \mu sec$$

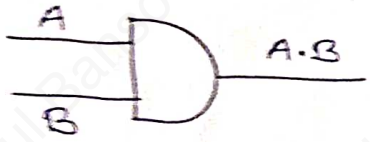
$$f = \frac{1}{2\ \mu sec} = \frac{1}{2} \times 10^6$$

$$= 500 \times 10^3$$

$$= 500\ KHz$$

$$\therefore Y = \overline{Y_1}$$

AND Gate :-



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

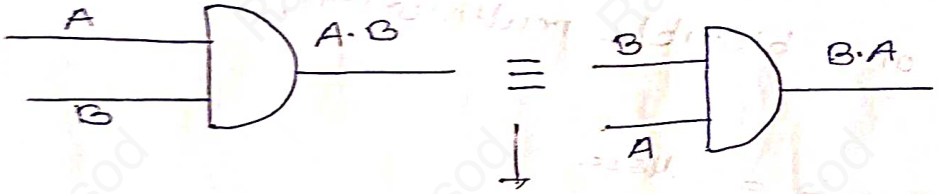
SOP

$Y = \Sigma(3)$

POS $\pi[0,1,2] = Y$

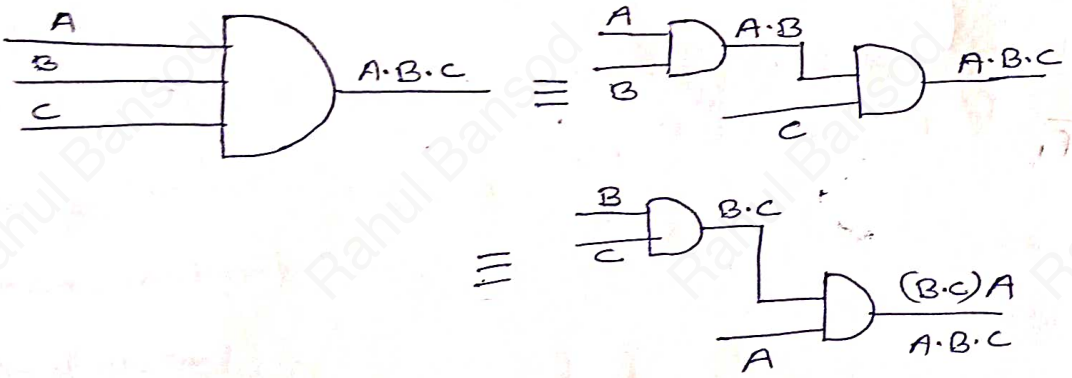
Lect - 09

Commutative law :- All the gates hold commutative law



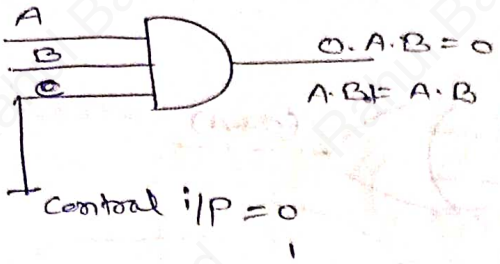
AND Gates holds commutative law

Associative law :-



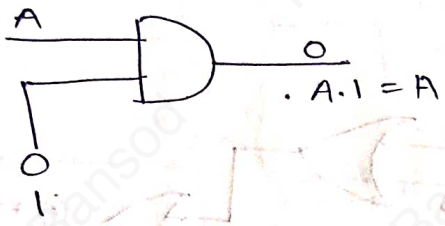
AND Gate is said to hold associative law

e.g:-

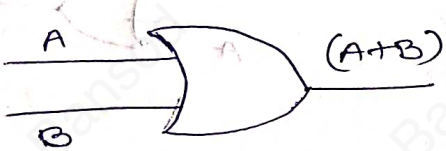


- for AND Gate '0' is disable i/p and '1' is enable i/p.

e.g:-



'OR' Gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

$Y = \Sigma(1,2,3)$ SOP

$\pi(0)$ POS

$= A+B$

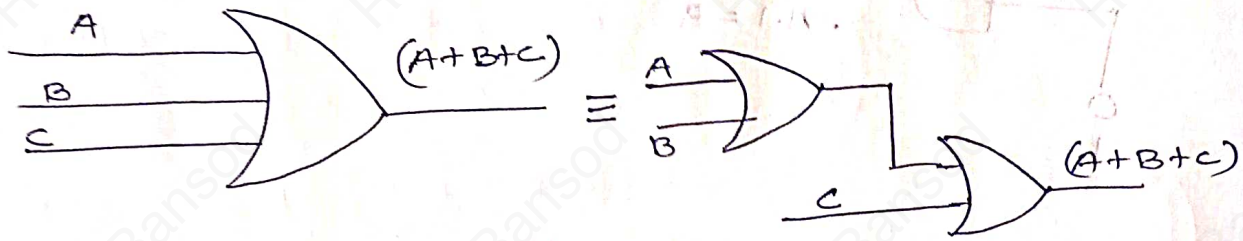
SOP: $Y = \overline{A}.B + A\overline{B} + A.B = A+B$

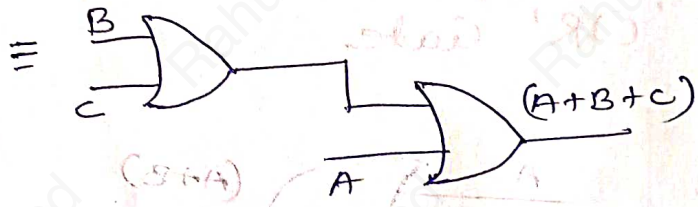
$B(\overline{A}+A) = B.1 = B \Rightarrow B + A\overline{B} = (B+A)(B+\overline{B}) = A+B$
$= B+A$

Commutative law :-

it holds commutative law

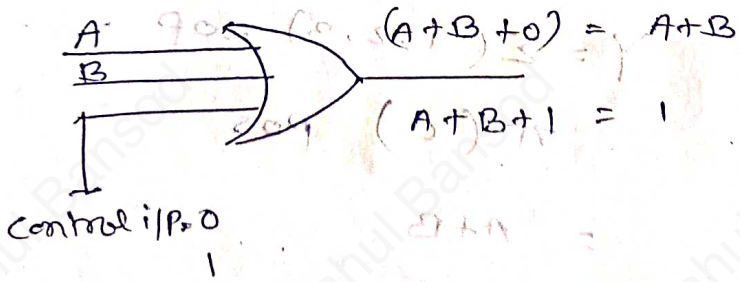
Associative law :-





∴ OR Gate holds associative law

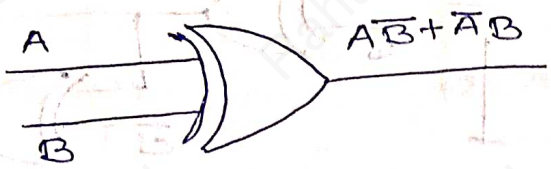
Commutative law :→



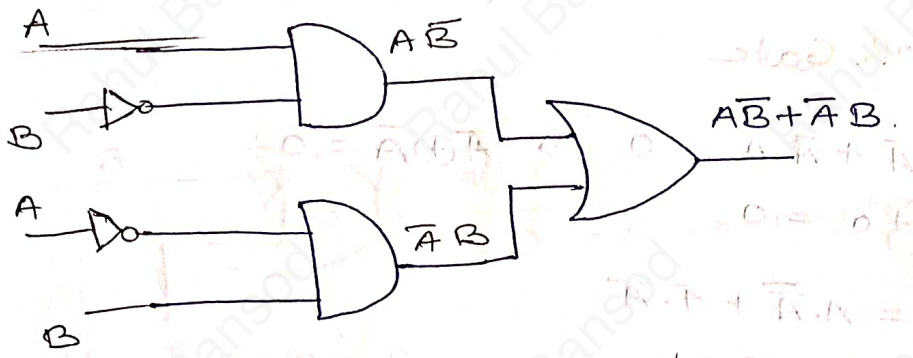
for OR Gate '0' is the enable i/p & 1 is the disable i/p

Lect - 10

XOR Gate :-



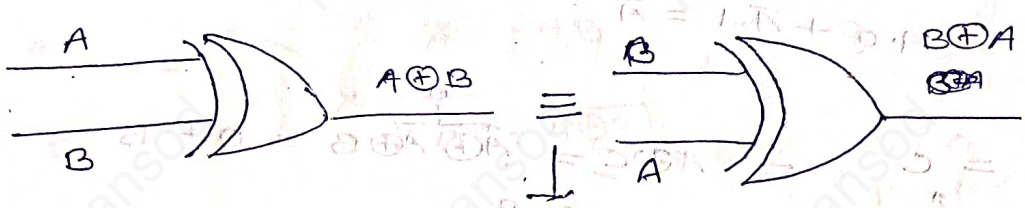
|||



A	B	$Y(A \oplus B)$
0	0	0
0	1	1
1	0	1
1	1	0

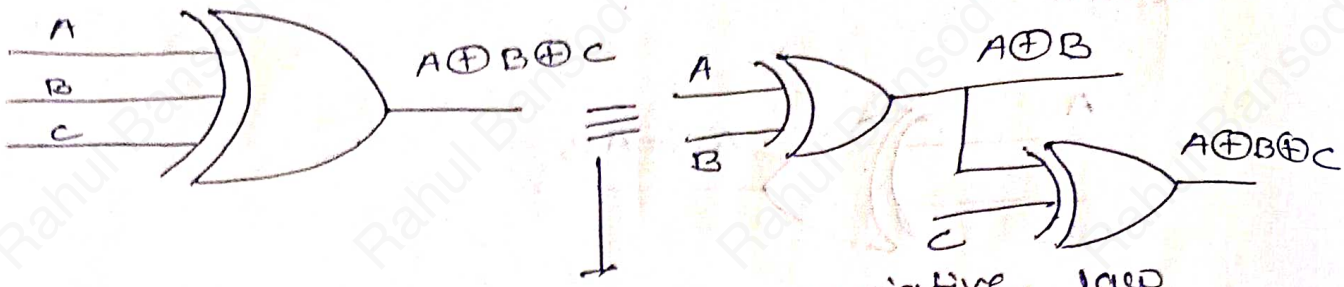
$Y(A,B) = \Sigma(1,2) = \bar{A}B + A\bar{B}$

Commutative law :-



It holds commutative law

Associative law :-



XOR Gate holds associative law

Properties of XOR Gate

i) $A \oplus A = A \cdot \bar{A} + \bar{A} \cdot A = 0 \Rightarrow \bar{A} \oplus \bar{A} = 0$

$= 0 + 0 = 0$

ii) $A \oplus \bar{A} = 1 = A \cdot \bar{\bar{A}} + \bar{A} \cdot \bar{A}$

$= A + \bar{A} = 1$

iii) $A \oplus A = 0$

$A \oplus 0 = A \Rightarrow A \cdot \bar{0} + \bar{A} \cdot 0$

$= A \cdot 1 + 0 = A$

iv) $A \oplus 1 = \bar{A} \Rightarrow \bar{A} \oplus 1 = \bar{\bar{A}} = A$

$= A \cdot \bar{1} + \bar{A} \cdot 1$

$= A \cdot 0 + \bar{A} \cdot 1 = \bar{A}$

v) $A \oplus B = C = A \oplus C = \overbrace{A \oplus A}^{0} \oplus B = 0 \oplus B$

given

$= B$

$A \oplus C = B$

$C \oplus B = A$

vi) $A \oplus A \oplus A \oplus \ldots$ n times $= 0 \longrightarrow$ n even

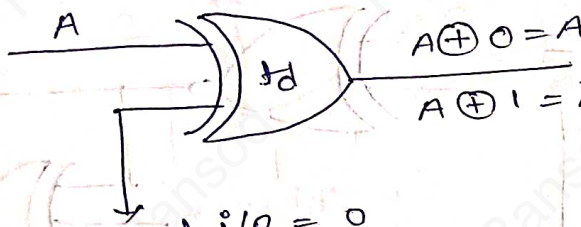
$A \longrightarrow$ n odd

Lect-11

$A \oplus A \oplus A \oplus A \oplus A \oplus A$ $\qquad 0 \oplus A = A$

$0 \oplus 0 \oplus 0 \oplus 0$

$0 \oplus 0 = 0$



$A \oplus 0 = A \longrightarrow$ buffer

$A \oplus 1 = \bar{A} \longrightarrow$ inverting

control i/p = 0

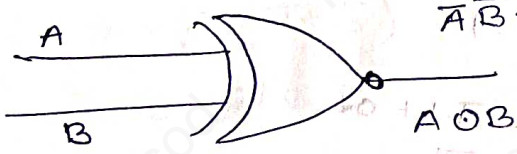
= 1

note:- Both 0 & 1 i/p are enable i/p for XOR Gate

$0 \longrightarrow$ buffer

$1 \longrightarrow$ Inverting buffer

XNOR Gate:-



$\bar{A}\bar{B} + AB$

$A \odot B = \overline{A \oplus B}$

$A \odot B$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

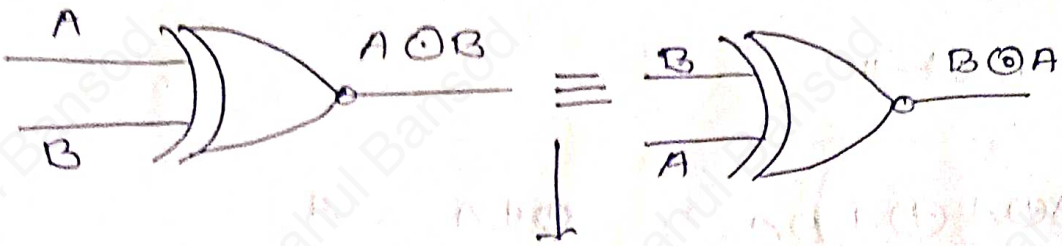
SOP

$Y \Sigma (0,3)$

$= \bar{A}\bar{B} + A \cdot B$

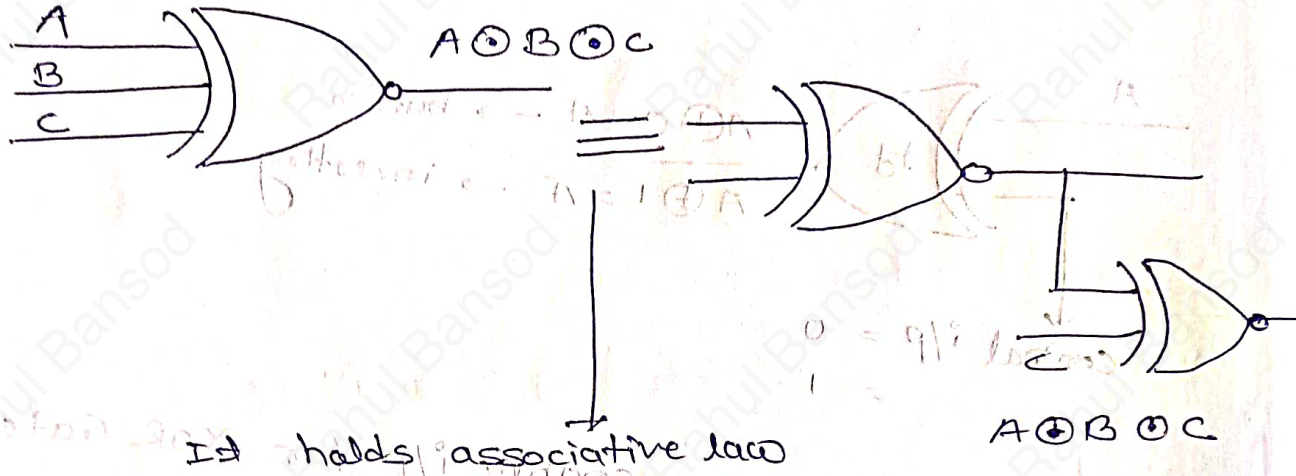
$= A \odot B$

Commutative law :-



It holds commutative law

Associative law :-



It holds associative law

XNOR Gate (properties) :-

i) $A \odot A = 1 = \bar{A}\cdot\bar{A} + A\cdot A = \bar{A} + A = 1$

ii) $A \odot \bar{A} = 0 = \bar{A}\cdot\bar{\bar{A}} + A\cdot\bar{A}$

$= \bar{A}\cdot A + A\cdot\bar{A} = 0$

iii) $A \odot 1 = A = \bar{A}\cdot 1 + A\cdot 1 = A$

iv) $A \odot 0 = \bar{A} = \bar{A}\cdot\bar{0} + A\cdot 0 = \bar{A}\cdot 1 + 0$
$= \bar{A}$

v) if $A \odot B = C$
then $A \odot C = B$ & $B \odot C = A$

$A \odot A \odot B = 1 \odot B = B$

VI) $A \odot A \odot A$ ---- n times $= 1 \rightarrow$ n even

$A \rightarrow$ n ~~odd~~ odd

even

$A \odot A \odot A \odot A$

$1 \odot 1 = 1$

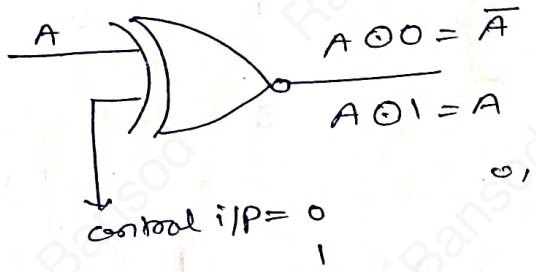
odd

$A \odot A \odot A \odot A \odot A$

$1 \odot 1 \odot A$

$1 \odot A = A$

VII)



0, 1 → enable i/p for XNOR gate

Lect-12

Mix property

1) $A \oplus B = \overline{A \odot B} = (\overline{\bar{A}\bar{B} + AB})$

$\overline{\cancel{A+B}} = \overline{\bar{A}\bar{B} \cdot \overline{AB}}$

$= (A+B)(\bar{A}+\bar{B})$

$= A\bar{B} + \bar{A}B$

$\overline{A \oplus B} = \overline{\overline{A \odot B}} = A \odot B$

$\overline{ABC} = \bar{A} + \bar{B} + \bar{C}$

$\overline{AB + BC} = \overline{A \cdot B} \cdot \overline{BC}$

$= (\bar{A} + \bar{B}) \cdot (\bar{B} + \bar{C})$

2.) $\overline{A} \oplus B = \overline{A}\,\overline{B} + \overline{\overline{A}} \cdot B$

$= \overline{A}\,\overline{B} + A \cdot B$

$= A \odot B$

$A \oplus \overline{B} = A \odot B$

$= A\overline{\overline{B}} + \overline{A} \cdot \overline{B}$

3) $\overline{A} \oplus \overline{B} = \overline{A}\,\overline{\overline{B}} + \overline{\overline{A}} \cdot \overline{B}$

$= \overline{A}B + A\overline{B}$

$= A \oplus B$

4) $A \odot \overline{B} = A\overline{\overline{B}} + \overline{A} \cdot \overline{B}$

$= A \oplus B$

$\overline{A} \odot B = \overline{\overline{A}} \cdot B + A \cdot \overline{B}$

$= A \oplus B$

$\overline{A} \odot \overline{B} = A \odot B$

Q) $A \oplus B \oplus C = \overline{A \odot B \odot C}$ False

A	B	C	$Y_1 (A \oplus B \oplus C)$	$Y_2 (A \odot B \odot C)$
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	0	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$Y_1 = Y_2$$

$$A \oplus B \oplus C = A \odot B \odot C$$

(SOP) (Imp)

$$= \Sigma (1, 2, 4, 7)$$

2's 1 → even

3's 1 → odd

0 → even

3's

→ XOR Gate always search for odd no. of one's at the i/p side, meaning is that if it gets total no. of 1s at the i/p side odd in no. then its generated output one otherwise o/p zero.

→ XNOR Gate search for even no. of one's at the i/p side for even no. of i/p lines while it searches for odd no. of one's for odd no. of i/p lines

Conclusion:- So for even no. of i/p lines XOR & XNOR are complement of each other while for odd no. of i/p lines XOR & XNOR are same.

Complement property

$$A \oplus B = \overline{A \odot B} = \overline{A} \odot B = A \odot \overline{B} = A \oplus B$$

$$A \odot B = \overline{A \oplus B} = \overline{A} \oplus B = A \oplus \overline{B} = A \odot B$$

$$\overline{A \oplus B \oplus C} = \overline{A} \oplus B \oplus C = A \oplus \overline{B} \oplus C = A \oplus B \oplus \overline{C}$$

$$= A \odot B \oplus C = A \oplus B \odot C = A \oplus B \odot C$$

$$\overline{\overline{A \oplus B \oplus C}} = \overline{A \odot B \oplus C} = \overline{A \odot B \oplus C} = \overline{A \oplus B \odot C}$$

$$= A \odot B \odot C$$

$$\overline{A \oplus B \oplus C} = A \oplus B \oplus C$$

Lect-13

e.g:- $\overline{A \oplus B \oplus C} = A \oplus \overline{B} \oplus C$

e.g:- $\overline{\overline{A} \oplus \overline{B} \oplus C} = \overline{\overline{\overline{A \oplus B \oplus C}}} = \overline{A \oplus B \oplus C}$

e.g:- $\overline{\overline{A \oplus B} \odot C} = \overline{\overline{A} \oplus B \odot C} = \overline{\overline{A \oplus B \odot C}}$

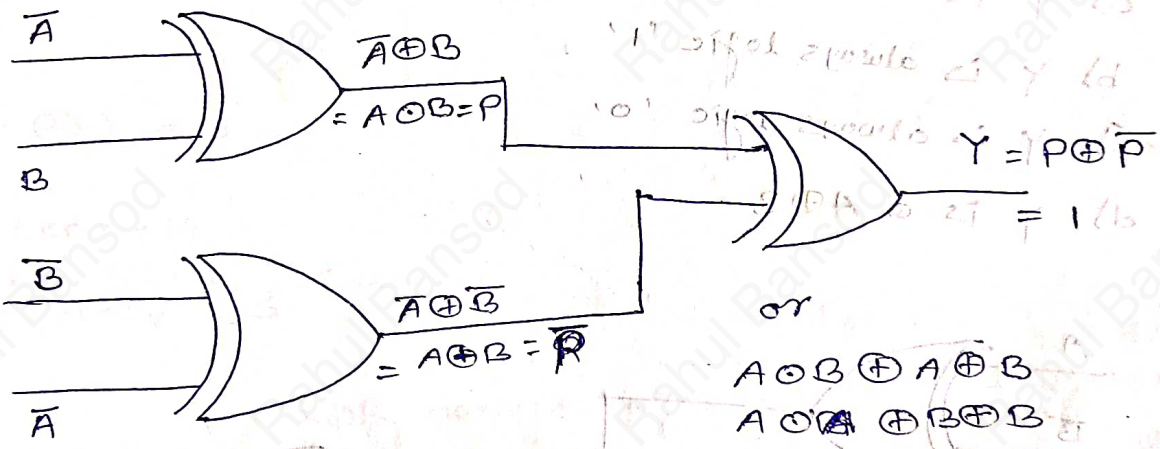
$= A \oplus B \odot C$

e.g:- $\overline{\overline{\overline{A} \oplus B} \odot C} = \overline{A \oplus B \odot C}$

$= A \odot B \odot C$

$= A \oplus B \oplus C$

Q)



or

$A \odot B \oplus A \oplus B$

$A \odot A \oplus B \oplus B$

$1 \oplus 0 = 1$

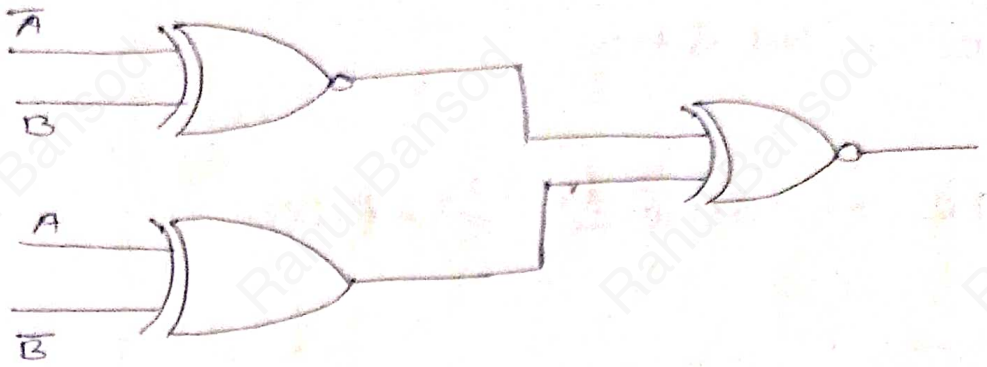
a) Y is $A \odot B$

b) Y is always at logic '1'

c) Y is always at logic '0'

d) Y is $A \oplus B$

Q)



$$\overline{\overline{A \oplus B}} = \overline{A \odot B} = A \oplus B = P$$

$$A \oplus \overline{B} = A \oplus B = \overline{P}$$

$$\overline{P \oplus \overline{P}} = \overline{1} = 0$$

$$P \odot \overline{P} = 0$$

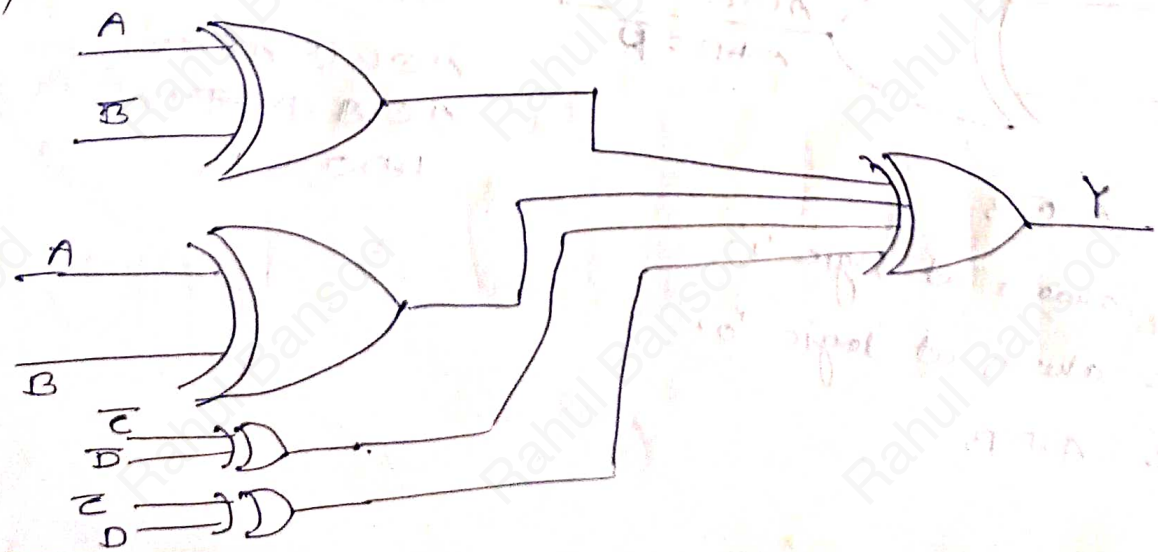
a) Y is $A \odot B$

b) Y is always logic '1'

✓ c) Y is always logic '0'

d) Y is $A \oplus B$

Q)



a) $A \oplus B \odot C \oplus D$

b) $A \odot B \oplus C \oplus D$

c) Y always at logic '0'.

d) Y is always at logic '1'

Sol^n:- 1) $A \oplus \overline{B} = A \odot B$

2) $A \oplus B$

3) $\overline{C} \oplus \overline{D} = C \oplus D$

4) $C \odot D$

$A \odot B \oplus A \oplus B \oplus C \oplus D \oplus C \odot D$

$\underbrace{A \odot B \oplus A \oplus B}_{1} \oplus \underbrace{C \oplus D \oplus C \odot B}_{1}$

$1 \oplus 1 = 0$

Lect - 14

Q) $Y = A \oplus (A+B)$ is

a) $A \oplus B$

b) $A \odot B$

c) $\overline{A} B$

d) $A \overline{B}$

XOR doesn't hold distributive law over OR Gate

Sol:-

$$Y = A \oplus (A+B)$$

$$= A \cdot (\overline{A+B}) + \overline{A}(A+B)$$

$$= A[\overline{A} \cdot \overline{B}] + 0 + \overline{A}B$$

$$= 0 + 0 + \overline{A}B$$

$$= \overline{A}B$$

also

A	B	A+B	$A \oplus (A+B)$ Y
0	0	0	0
0	1	1	1
1	0	1	0
1	1	1	0

$$Y = \Sigma(1)$$

$$= \overline{A}B$$

Note:- XOR Gate doesn't hold distributive law over OR

Q) $A \oplus B \oplus AB = (A+B)$

$$A \oplus [B \cdot \overline{AB} + \overline{B} \cdot AB]$$

$$= A \oplus [\overline{A}B]$$

$$= A \cdot \overline{\overline{A}B} + \overline{A} \cdot \overline{A}B = A(A+\overline{B}) + \overline{A}B = A + A\overline{B} + \overline{A}B$$

$= A(1+\overline{B}) + \overline{A}B$

$= A + \overline{A}B$

$= (A+\overline{A})(A+B)$

$= (A+B)$

* $A \oplus B \oplus AB = A+B$

$A \oplus B \oplus (A+B) = AB$

$A \oplus (AB) = (A \oplus A)(A \oplus B)$ ✗
$= 0\,(A \oplus B) = 0$

$A \cdot \overline{AB} + \overline{A}.(AB)$
$= A(\overline{A}+\overline{B})$
$= 0 + A\overline{B}$

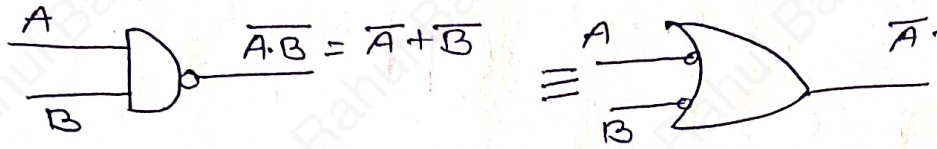
A	B	A·B	Y
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	0

$Y = A\overline{B} = \Sigma(2)$

Note:- XOR does not hold distributive law over 'AND' Gate also.

Univarsal Gates :-

NAND Gate

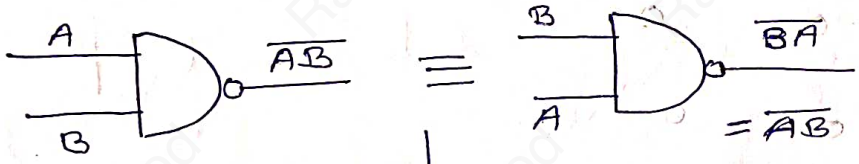


A	B	Y ($\overline{A \cdot B}$)
0	0	1
0	1	1
1	0	1
1	1	0

$= \Sigma(0,1,2) = \overset{pos}{\Pi}(3)$
$= (\overline{A} + \overline{B})$

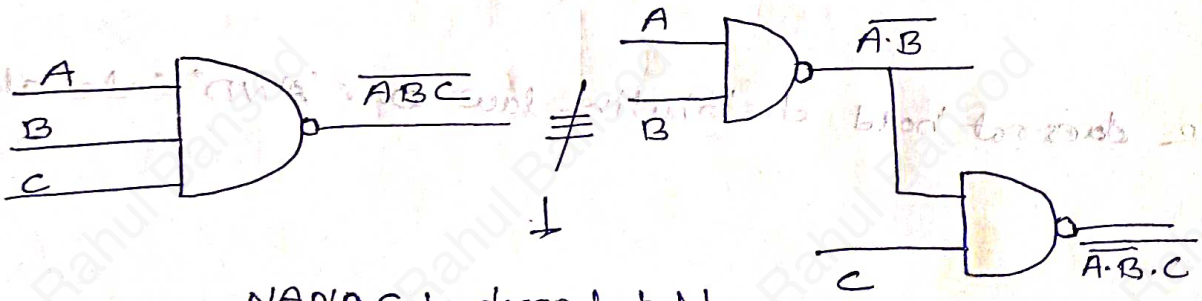
Commutative & associative law

Commutative law



It holds commutative law

Associative law :→



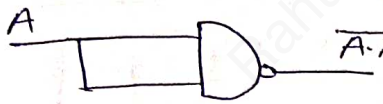
NAND Gate doesnot hold associative law

$= AB + \overline{C}$

Imp

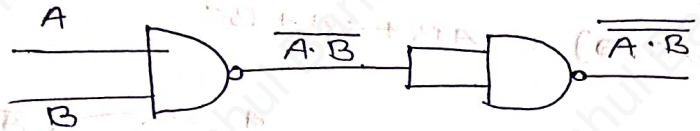
NAND as a universal circuit

NOT gate :→



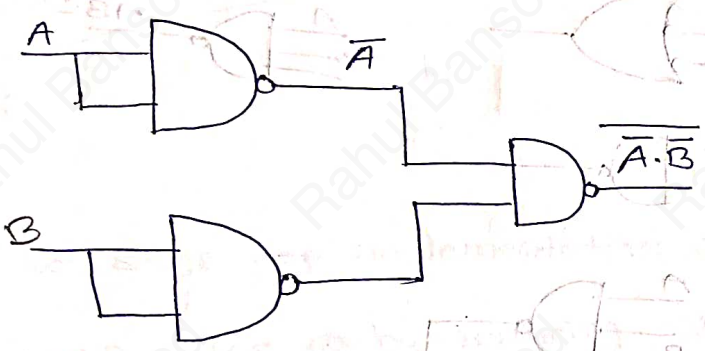
$\overline{A \cdot A} = \overline{A}$

AND Gate :→



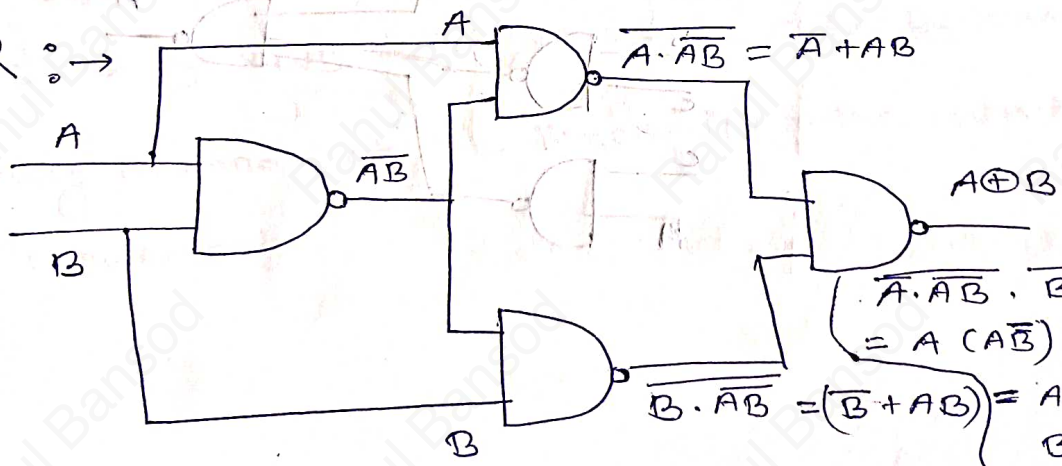
$\overline{\overline{A \cdot B}} = A \cdot B$

OR Gate :-



$\overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}}$
$= (A + B)$

XOR :→



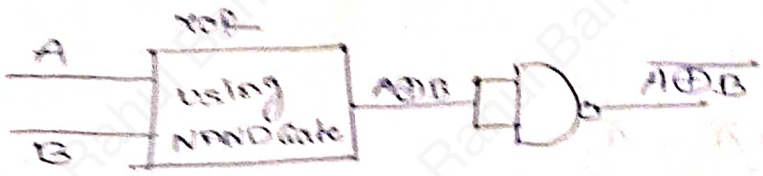
$\overline{A \cdot \overline{AB}} = \overline{A} + AB$

$\overline{B \cdot \overline{AB}} = (\overline{B} + AB)$

$\overline{\overline{A} \cdot \overline{AB}} \cdot \overline{B \cdot \overline{AB}}$
$= A(A\overline{B}) + B\overline{AB}$
$= A(\overline{A} + \overline{B}) + B(\overline{A} + \overline{B})$
$= A\overline{B} + \overline{A}B$

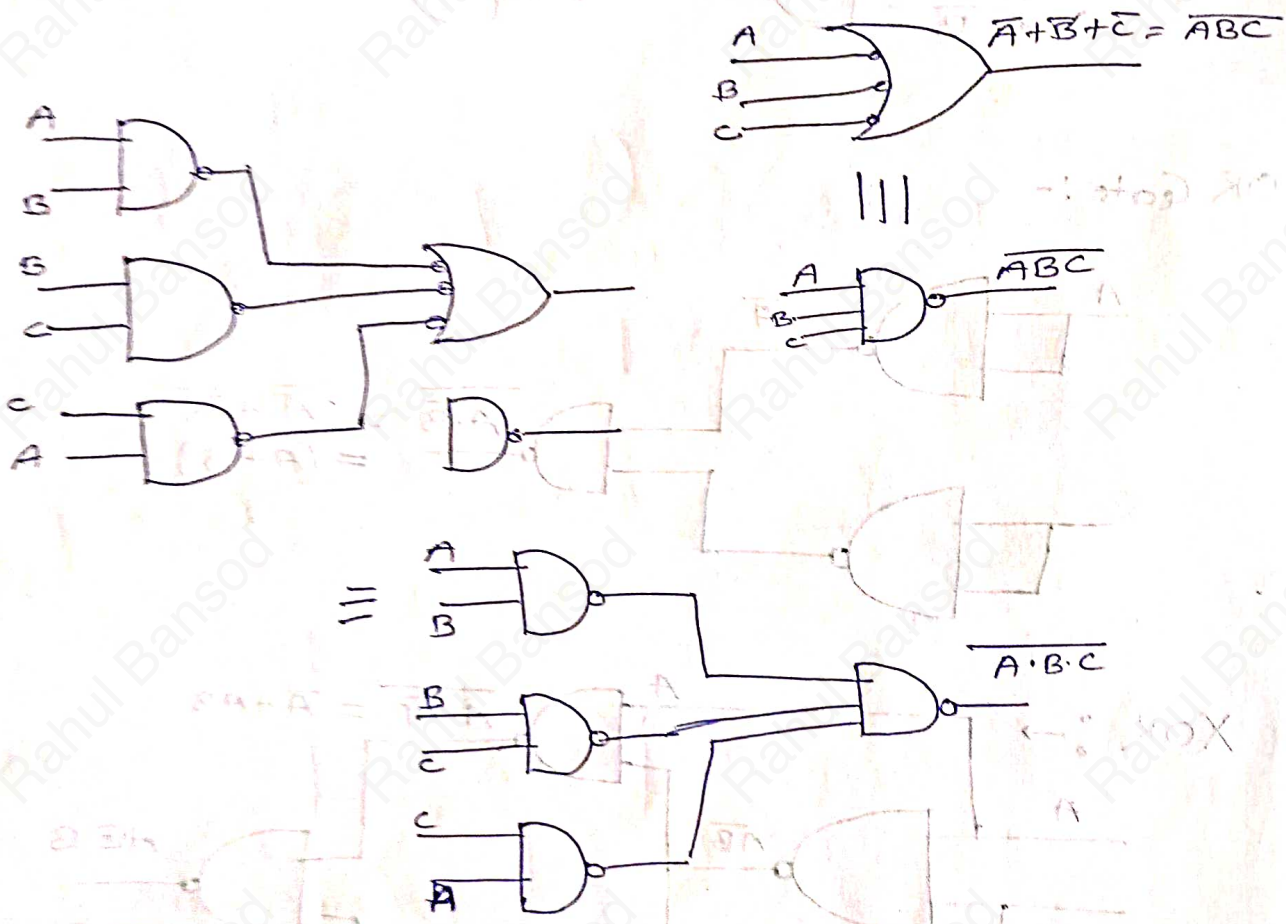
Lect-15

XNOR :- (5 gates) Required

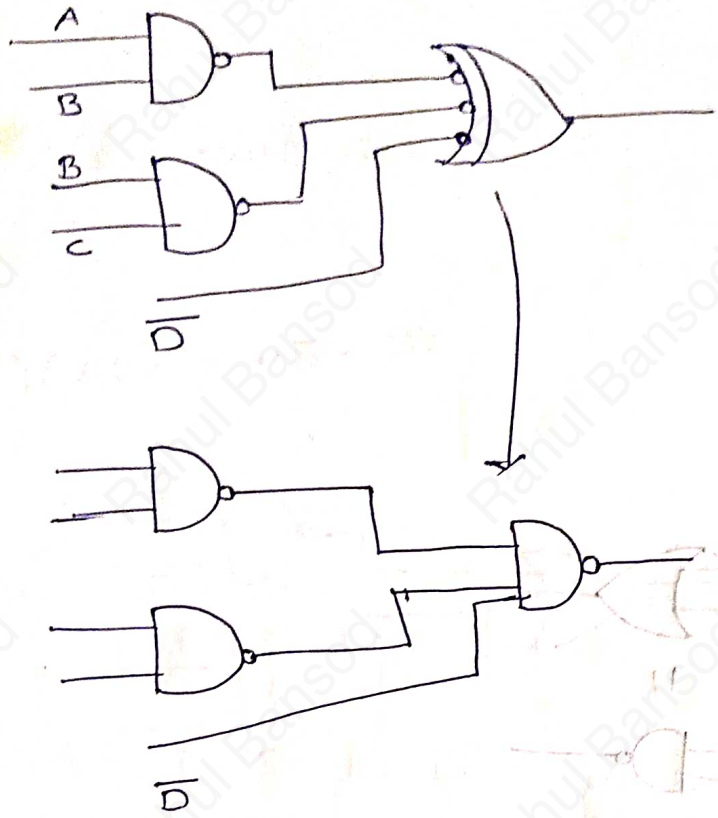


e.g:-

$$Y(A,B,C,D) = AB + CA + BC$$



e.g:- $Y = AB + BC + D$

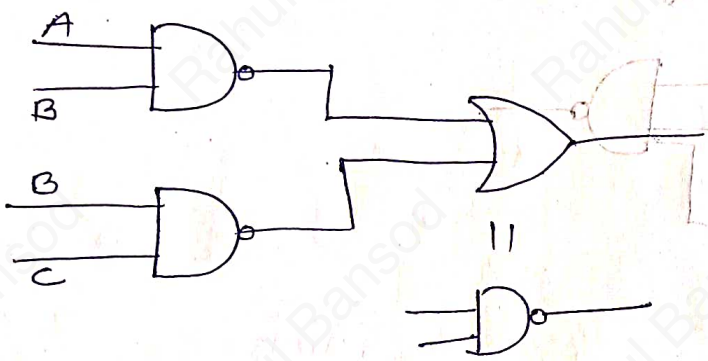


Note:- any two stage sop implementation can directly be implemented using NAND Gates by replacing all the input a AND Gates (1st stage) by NAND & single o/p OR Gate by NAND Gate just keeping in mind that the direct i/p to the output OR Gate will be complemented

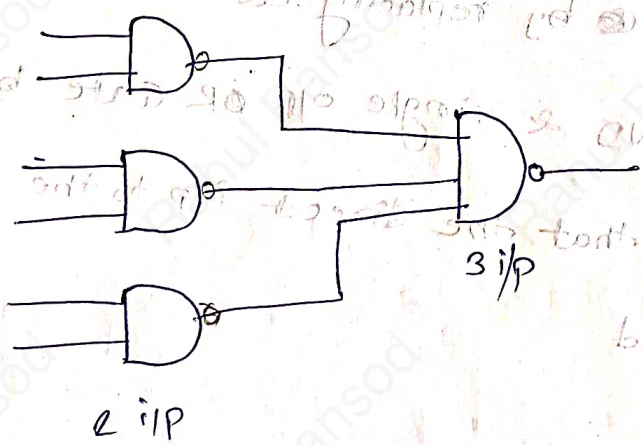
Q) $Y(A,B) = AB+BC$, minimum no. of 2 i/p NAND requires to implement above boolean function

a) 3
b) 7
c) 5
d) 4

sol:-

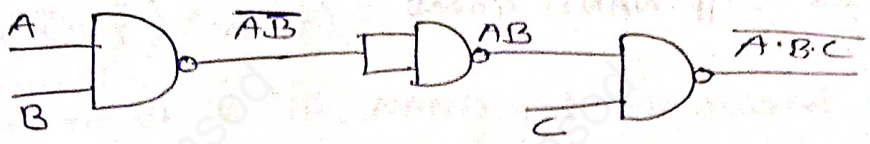


Q) $Y(ABC) = AB+BC+CA$



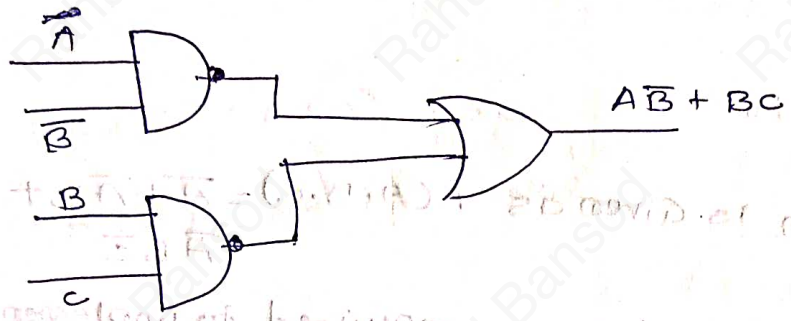
4 Gate

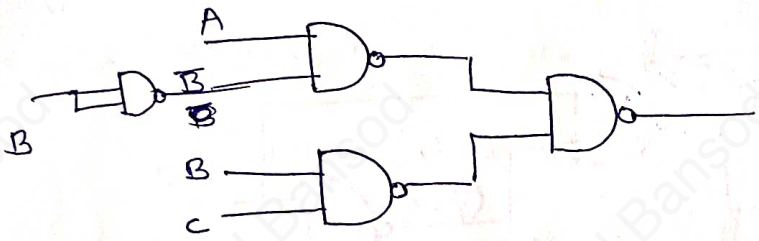
$\overline{A \cdot B \cdot C} = \overline{AB} + \overline{C}$



⇒ 6 i/p NAND Gate

Q) $Y(A,B,C) = A\overline{B} + BC$





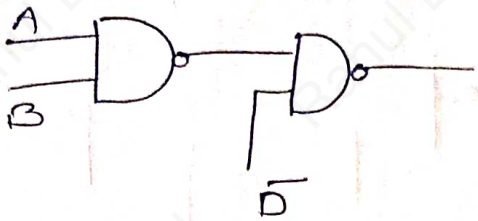
Q) $Y = AB + D \longrightarrow$ 3 i/p NAND Gates

$$\overline{Y} = \overline{AB+D}$$

$$= \overline{AB} \cdot D$$

$$Y = \overline{\overline{AB} \cdot \overline{D}}$$

$$= \overline{\overline{x} \cdot y}$$



always Do SOP implementation.

Lect-16

Q) A boolean function is Given as $f(A,B,C) = \overline{A} + \overline{A}B + \overline{A}B\overline{C}$

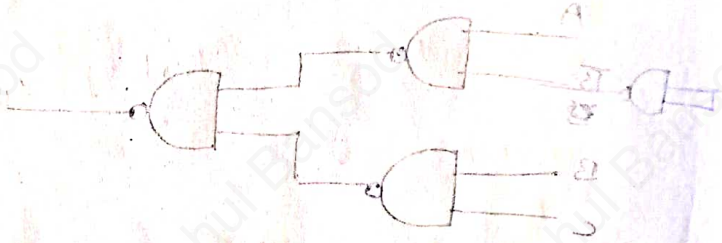
How many (minimum) two i/p NAND gates are required to implement above boolean function

a) 13

✓ b) 1

c) 5

d) 7



Sol:- $\overline{A} + \overline{A}B + \overline{A}B\overline{C} = \overline{A}\left[1 + B + B\overline{C}\right]$

$$= \overline{A} \cdot 1 = \overline{A}$$

Q) $F = (\overline{X}+\overline{Y})(W+Z)$

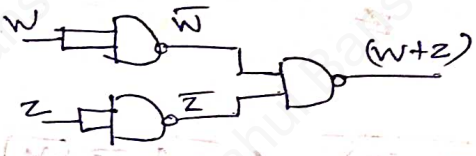
minimum no. of 2 i/p NAND gate required implement above boolean function?

a) 4 ✓ b) 6 c) 5, d) 7

Sol:-

$$F = \underbrace{(\overline{X\cdot Y})}_{\text{1 Nand}}\overbrace{(W+Z)}^{\text{2 Nand}}$$

3 Nand

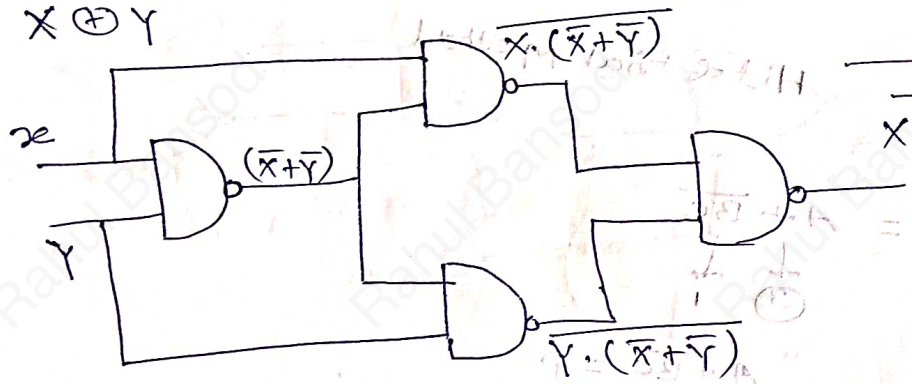


e.g:- $(\overline{A}+\overline{B})(A+B) = XOR$

$(A+\overline{B})(\overline{A}+B) = XNOR$

eg:- $(\overline{X}+\overline{Y})(X+Y)$

$= X \oplus Y$



$\overline{\overline{X(\overline{X}+\overline{Y})}\cdot\overline{Y(\overline{X}+\overline{Y})}}$

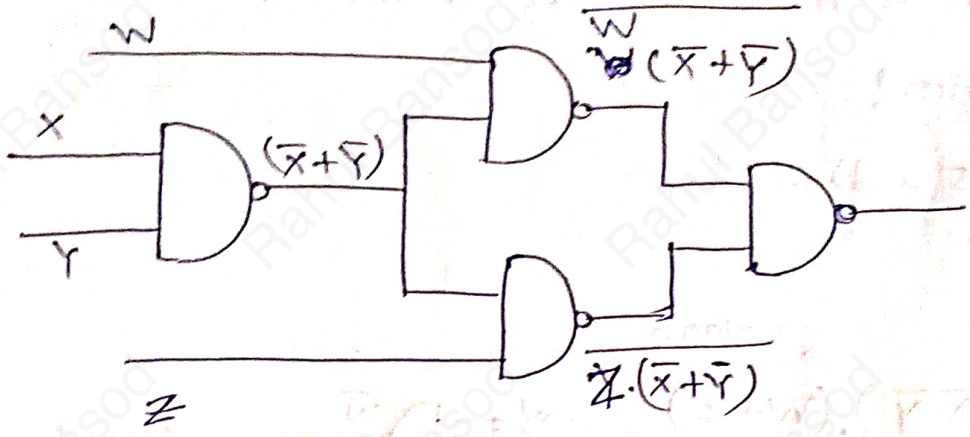
$= X(\overline{x}+\overline{y}) + y(\overline{x}+\overline{y})$

$= (X+Y)(\overline{X}+\overline{Y})$

$= X \oplus Y$

$(\overline{X}+\overline{Y})(W+Z)$

Sol^n :-



$$\overline{W(\bar{X}+\bar{Y})} + \overline{Z(\bar{X}+\bar{Y})}$$

$$= W(\bar{X}+\bar{Y}) + Z(\bar{X}+\bar{Y})$$

$$= (X+\bar{Y})(W+Z)$$

4 gates required

H.W

Q) $Y = \bar{A}BC$ Hit & trial Method

$$\bar{Y} = \overline{\bar{A}.BC} = A + \overline{BC}$$

3 1

$$Y = \overline{A+\overline{BC}}$$

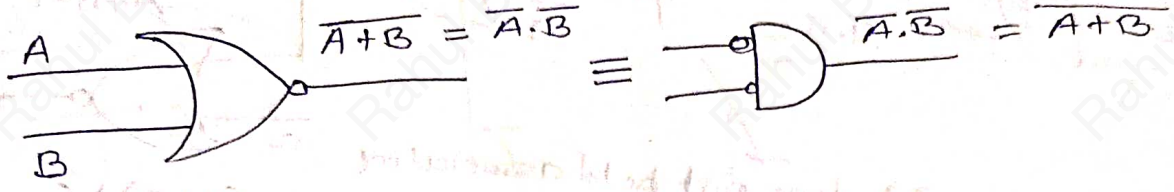
$$= \bar{P}$$

$A + \overline{BC} = P$

$$Y = \bar{A}BC$$

Lect-17

NOR Gate :→

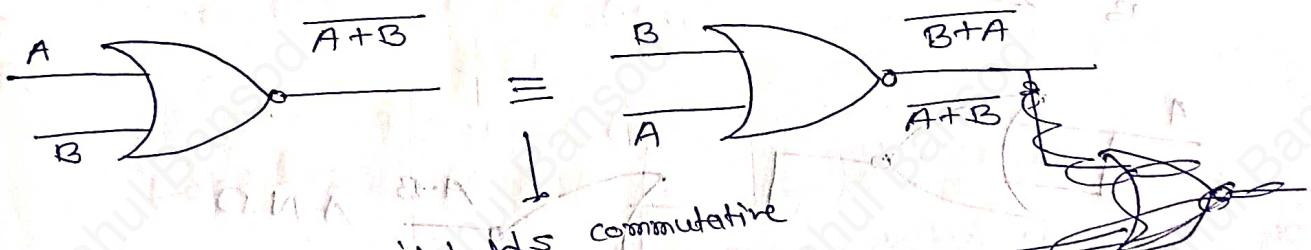


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

$Y = \overset{SOP}{\Sigma}(0) = \overline{A}.\overline{B}$

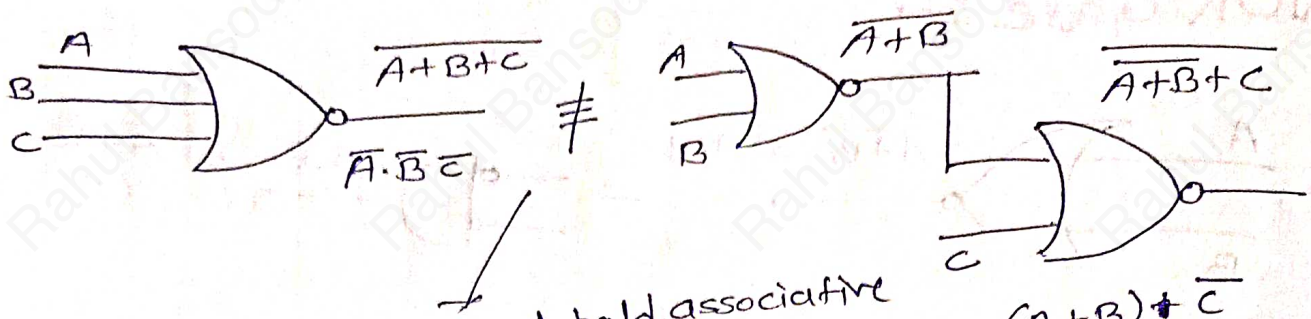
Commutative & associative law :-

Commutative law :-



it holds commutative law

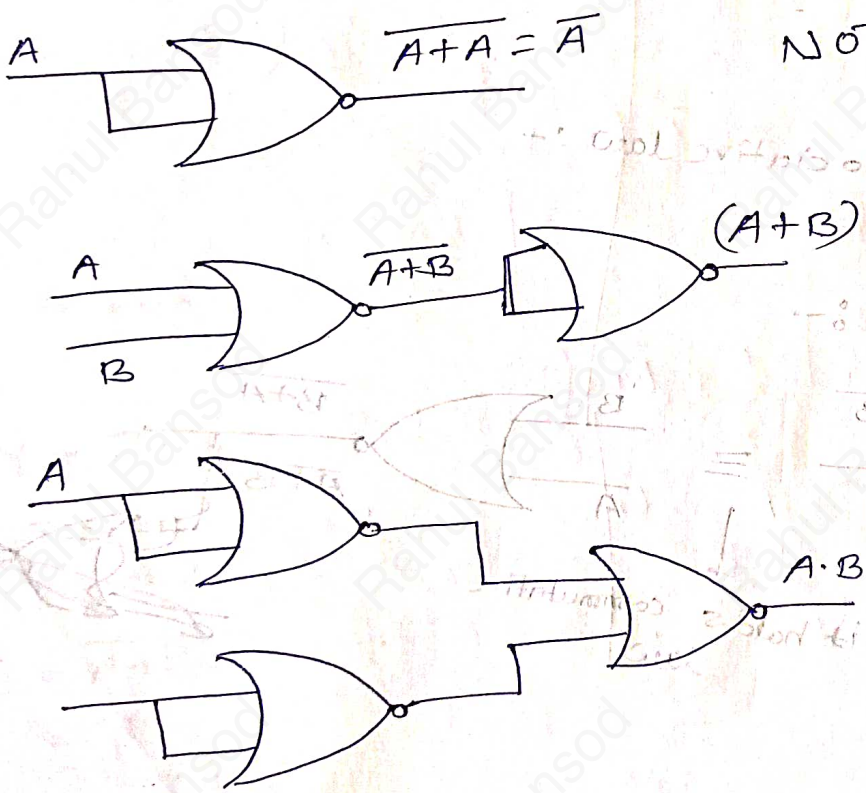
Associative law :-

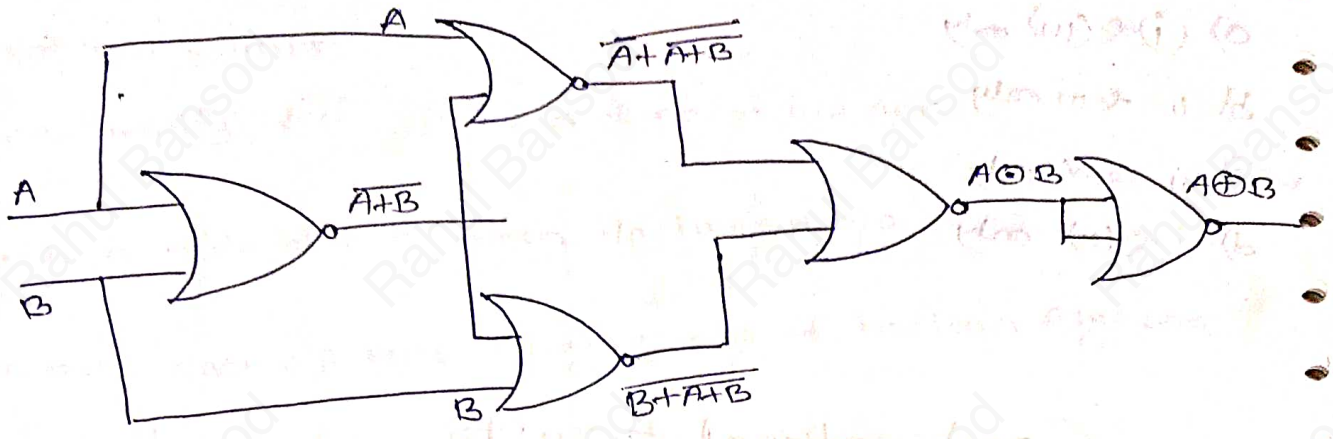


It does not hold associative law

$(A+B)+\overline{C}$

NOR as a Universal :-



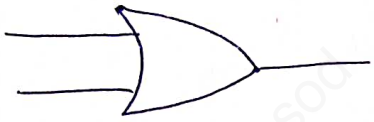


4 for XNOR
5 for XOR

	NAND	NOR
NOT	1	1
AND	2	3
OR	3	2
XOR	4	5
XNOR	5	4

Lect - 18

Q) which of the following circuit can work as universal gate

i) 

ii)

AND + NOT
OR + NOT

iii)

iv)

a) (i) & (iii) only

b) ii & iii only

c) ii & iv only

d) i & (ii) only

Combinational circuits

Combinational circuits	sequential circuits
i) o/p depends on present i/p only.	i) o/p depends on present i/p as well as past o/p.
ii) There is no feedback	ii) There is feedback
iii) static Hazards & dynamic Hazards.	iii) essential Hazard
iv) No memory	iv) There is memory
v) MUX, FA, HA, FS, HS, Encoder, Decoder	v) counter, FF, AS, SS, Register, shift Registers

Rahul Bansod

→ Combinational circuit

1) first we identify no. of i/p lines & no. of o/p lines

2) Then d-write a truth table between i/p lines & o/p lines

3) Then minimise each o/p lines using K-map or boolean Algebra.

4) Then implement using gates

Lect- 19

Half adder

HA

i/p lines		o/p lines	
x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

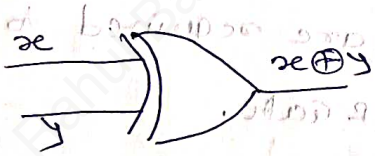
$$\begin{array}{rccc} A = & a_2 & a_1 & a_0 \\ B = & b_2 & b_1 & b_0 \\ & c_2 & c_1 & \\ \hline & s_2 & s_1 & s_0 \end{array}$$

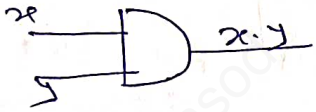
$s(x,y) =$

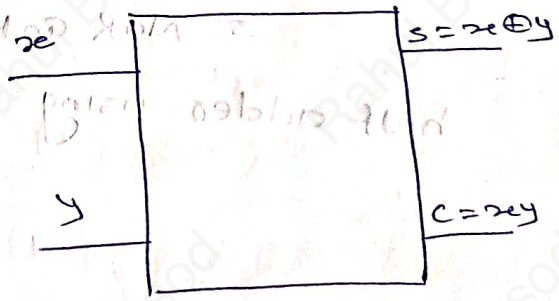
$S = \Sigma(1,2) = \bar{x}y + x\bar{y}$

$= x \oplus y$

$C = \Sigma(3)$



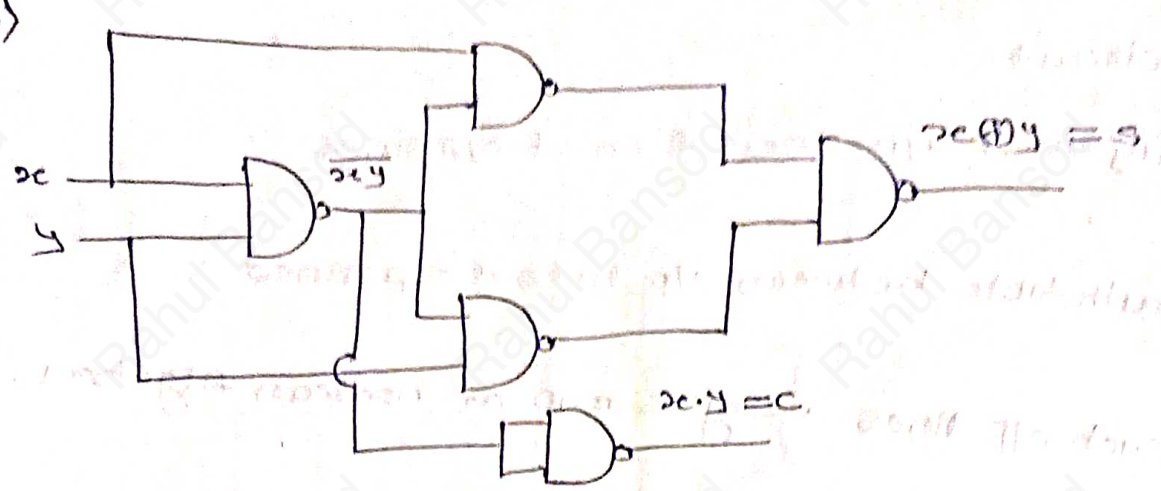




HA – 5 (NAND, NOR) 2i/p

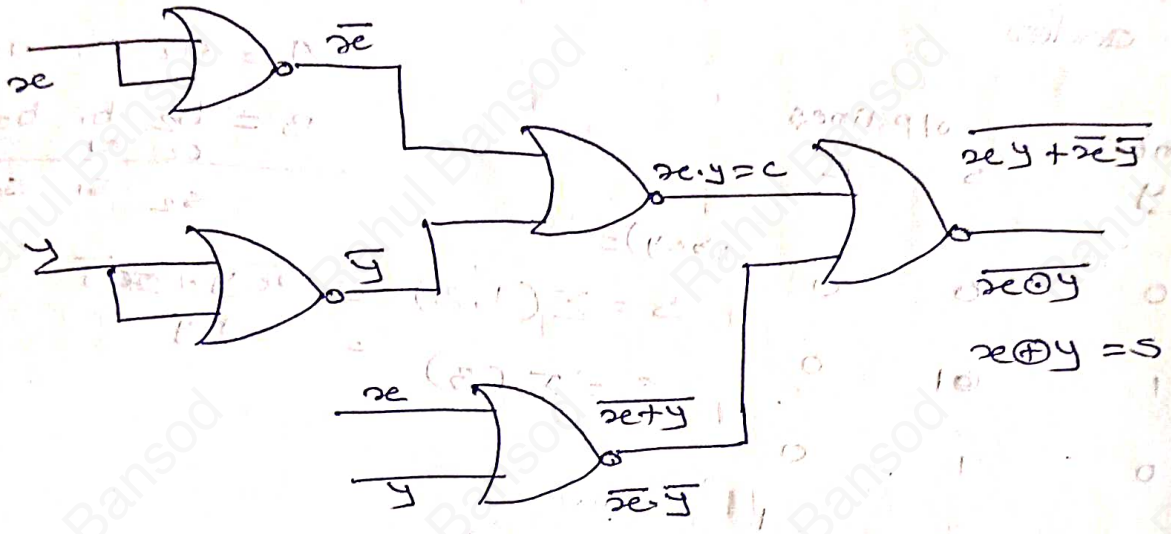
FA – 9 (NAND, NOR) 2i/p

1)



5 NAND Gates are required to implement half adder using NAND Gate

2)



5 NOR Gates are required to implement half adder using NOR Gate.

Half subtractor

x	y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$$\begin{array}{lcl} P & = & P_2 \quad P_1 \quad P_0 \\ Q & = & Q_2 \quad Q_1 \quad Q_0 \\ \hline & & D_0 \end{array}$$

b_1

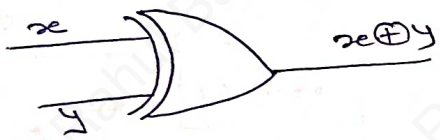
$P_1 - b_1 - Q_1$

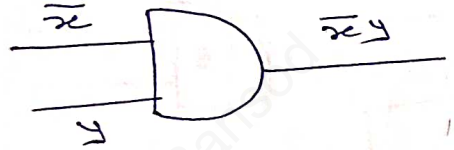
$$\begin{array}{ccc} 1 & 1 & 0 \\ 1 & 0 & 1 \\ \hline 0 & 0 & 0 \end{array} \qquad B=1$$

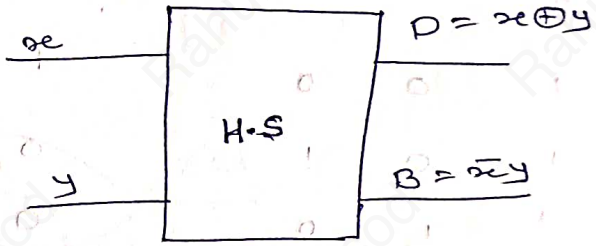
$$\begin{array}{c} 1 \\ 0 \\ \hline 1 \end{array} \qquad B=0$$

$D = \Sigma(1,2) = \bar{x}y + x\bar{y}$

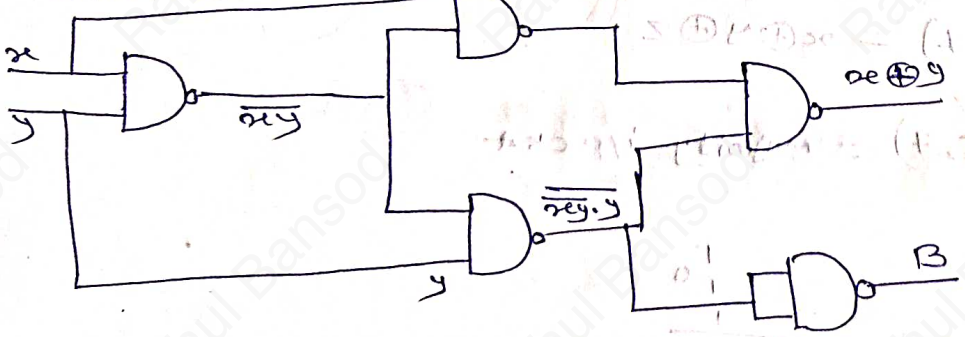
$B = \Sigma(1) = \bar{x}y$







NAND Gate



5 Gates

$\overline{\bar{x}y \cdot y} = (\bar{x}+\bar{y})\,y$

$= \bar{x}y$

- To implement Half adder or Half subtractor we require 5 - 2 i/p NAND Gates or 5 - 2 i/p NOR Gates.

Lect-20

(very Imp)

Full adder

x	y	z	s	c
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S = \Sigma(1,2,4,7) = x \oplus y \oplus z$

$C = \Sigma(3,5,6,7)$ = majority i/p ckt

$$C = \bar{x}yz + x\bar{y}z + xy\bar{z} + xyz$$

$$= xz + xy + yz = xy + yz + zx$$

(or)

$$= z[\bar{x}y + x\bar{y}] + xy$$

$$= xy + z(x \oplus y).$$

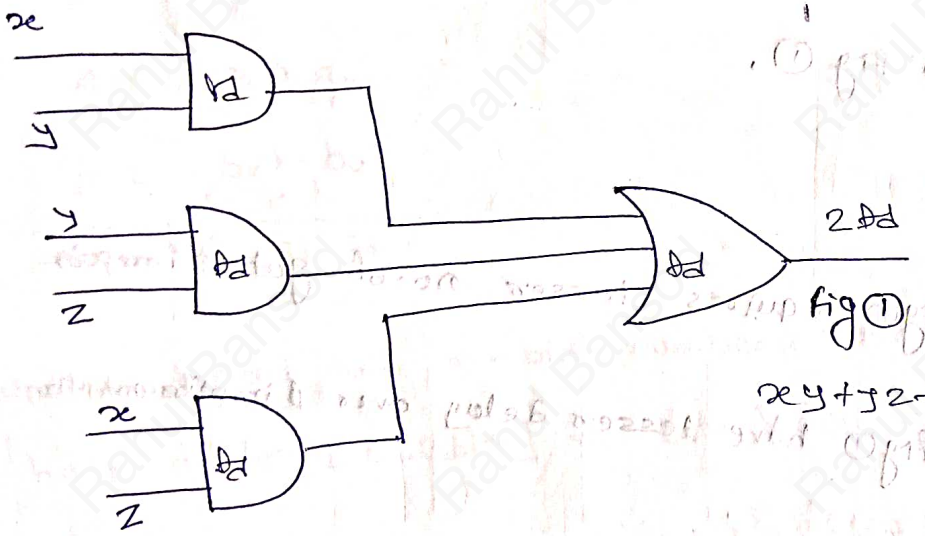
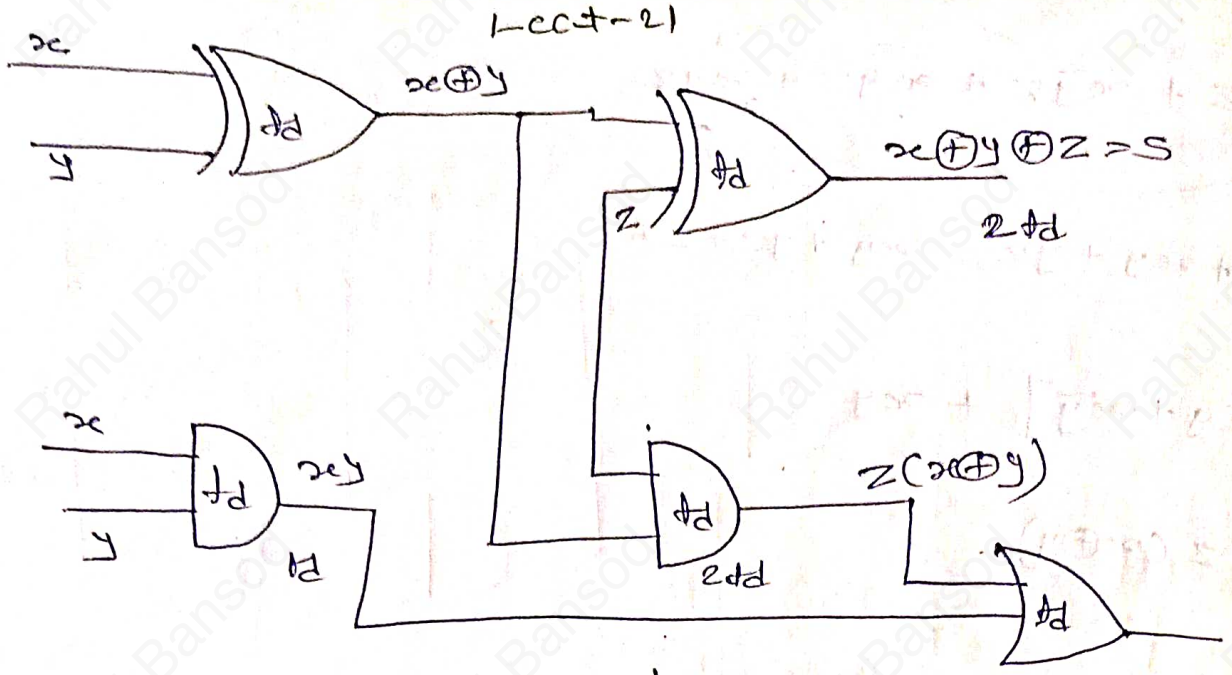


Fig ①

$xy + yz + zx = C$

Fig ①



Total 5 gates are required

$C = xy + z(x \oplus y)$

3td

fig ②

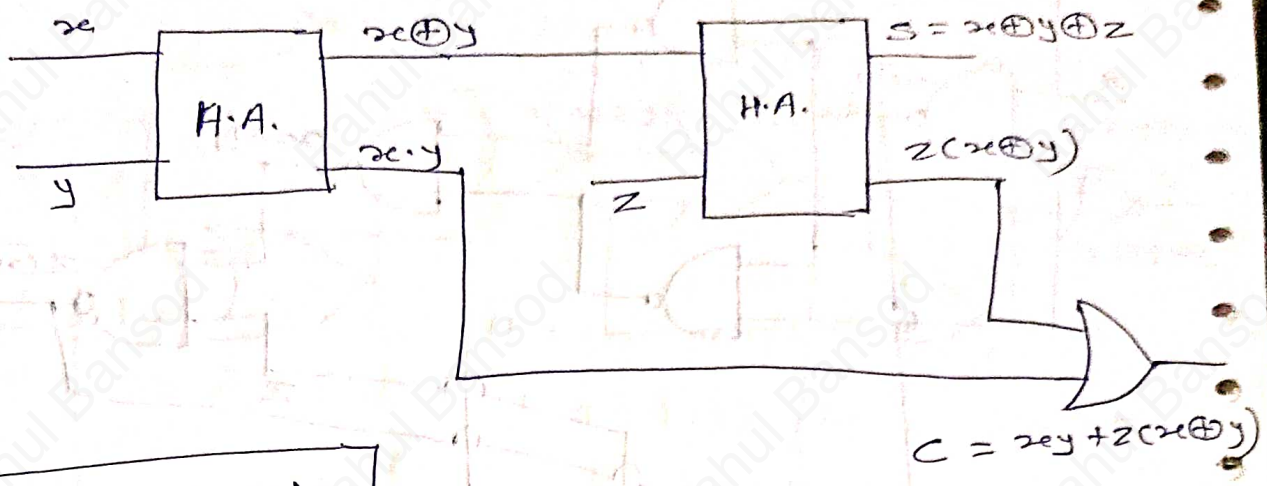
→ fig② have lesser no. of gates are required compare to implementation fig ①.

→ implimentation fig② requires lesser no. of gates compare to fig①.

→ implimentation fig① have lesser delay over implimentation fig ②

and this is advantage of fig① over fig②

Full adder using half Adder



$$\boxed{1\ F.A = 2\ H.A + 1\ OR\ Gate}$$

Lect - 22

e.g.:- $A = a_2 a_1 a_0$

$B = b_2 b_1 b_0$

$c_2\ c_1$

$c_3\ s_2\ s_1\ s_0$

If we have to add two n-bit numbers then ~~usi~~ we require 1 half adder [LSB bit] & (n-1) F.A for remaining bits

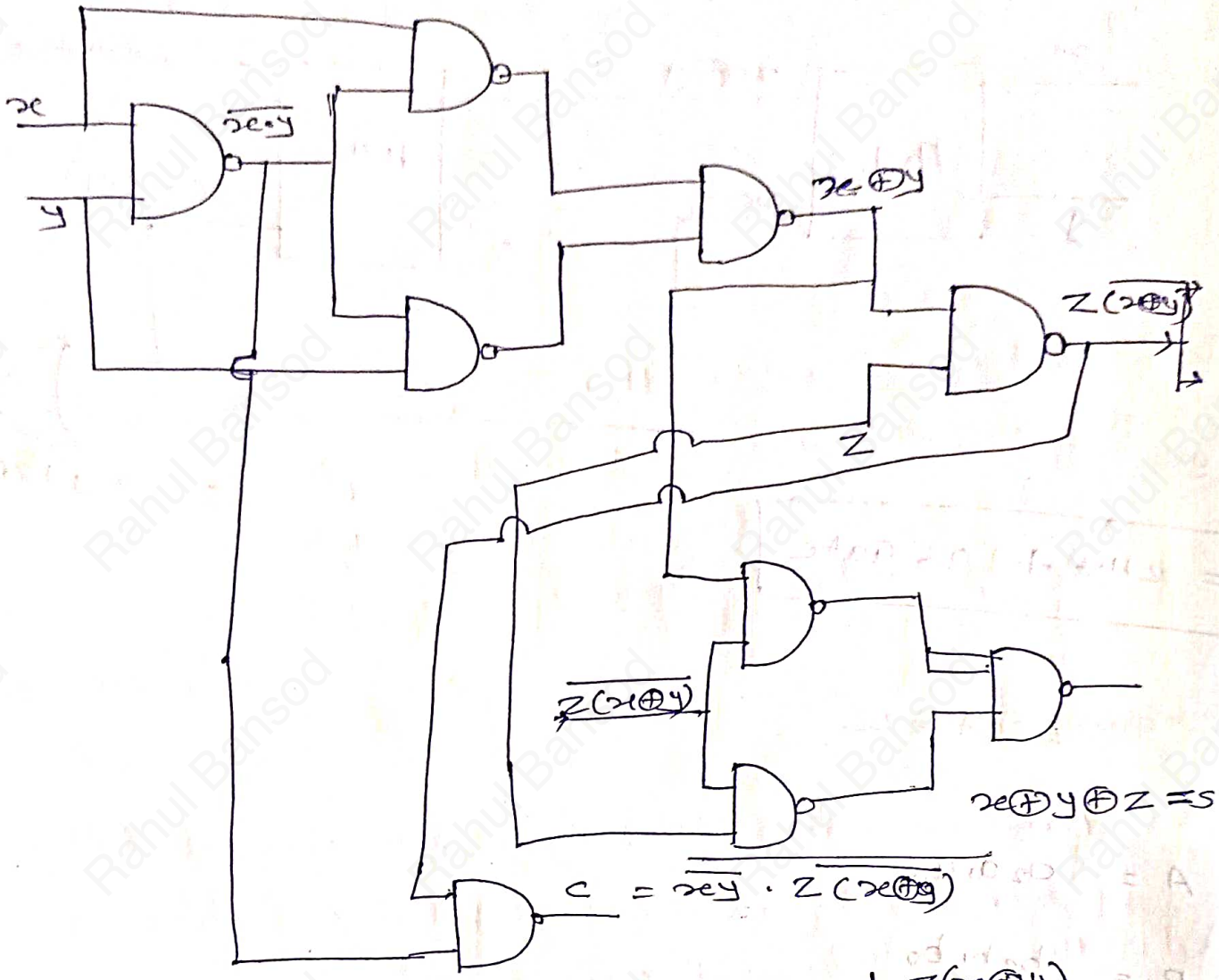
Total = 1 HA + (n-1) × 2 HA + (n-1) OR Gate

= 1 HA + (2n-2) HA + (n-1) OR Gate

= [2n-2+1] H.A + (n-1) OR Gate

= (2n-1) H.A + (n-1) OR Gate

Full Adder using 2 i/p NAND Gate



$$c = \overline{\overline{xy} \cdot \overline{z(x \oplus y)}}$$

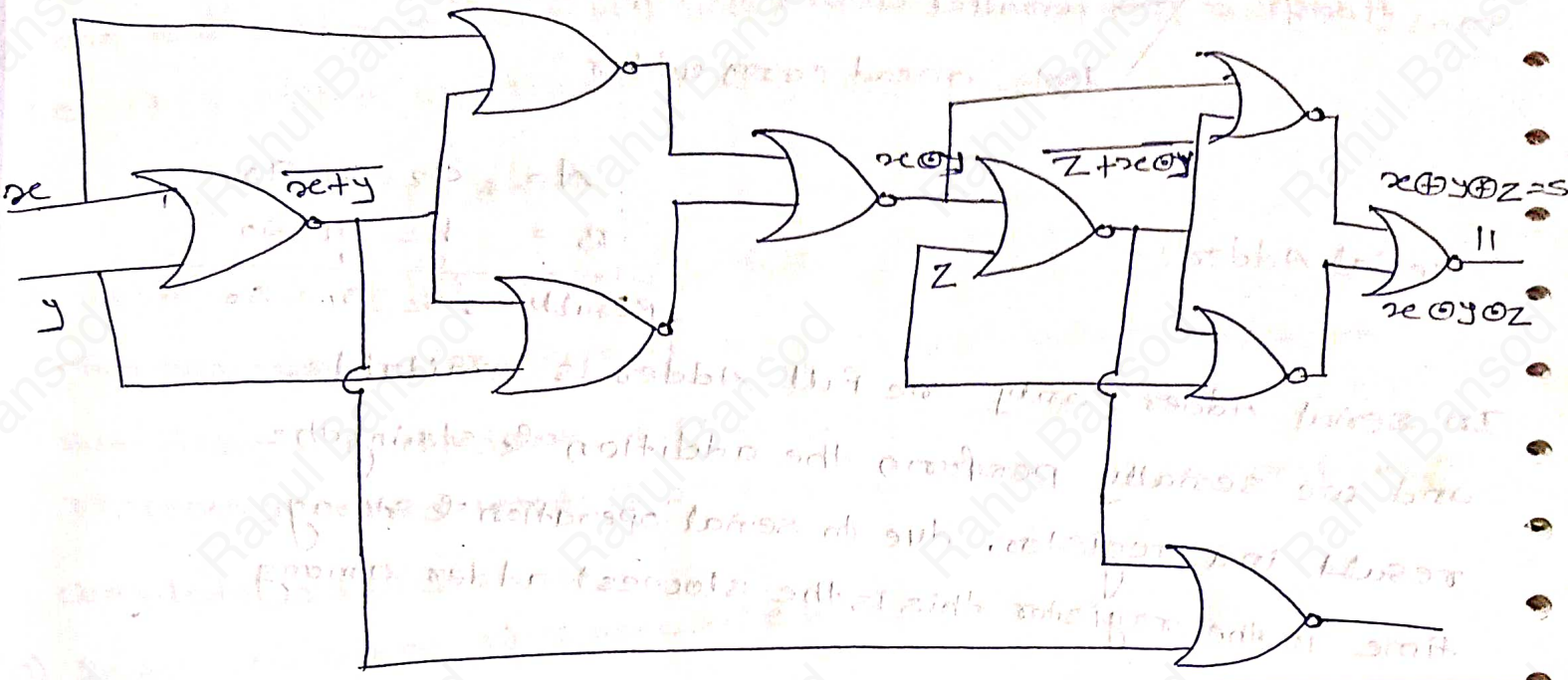
$$= xy + z(x \oplus y)$$

~~→ 2 i/p 9 Gates~~

→ for implementing a full adder we require ~~for implementing~~ 9 - 2 i/p NAND Gates.

H.W every NAND Gate Replace by ~~NAND~~ NOR Gate.

Lect-23



$$C = \overline{\overline{x+y} + \overline{z+x \odot y}}$$

$$= (x+y) \cdot (z + x \odot y)$$

$$= (x+y)(z + \bar{x}\bar{y} + xy)$$

$$C = xz + xy + yz + xy$$

$$= xy + yz + zx$$

- To implement a full Adder we required 9 - 2i/p NOR Gates.

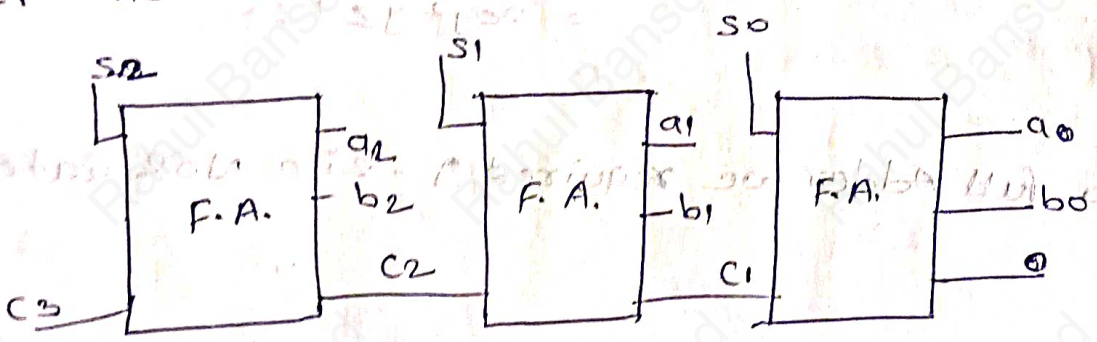
Adder :-
- serial adder
- parallel adder or ripple carry adder
- look ahead carry adder

$$\begin{array}{lcccc} A = & & a_2 & a_1 & a_0 \\ B = & & b_2 & b_1 & b_0 \\ & & c_2 & c_1 & \\ \hline \text{Result} = & c_3 & s_2 & s_1 & s_0 \end{array}$$

Serial Adder :-

In serial Adder only one full Adder is available and we serially perform the addition & storing the result in a register. due to serial operation & storage time in the register this is the slowest adder among the all adder.

Parallel Adder :- In parallel Adder there are full Adder for the each bit of the ~~n-bit~~ 2 n-bit numbers. If the no. are of n-bit then there will be n full adders.



$\boxed{C_3\ S_2\ S_1\ S_0}$

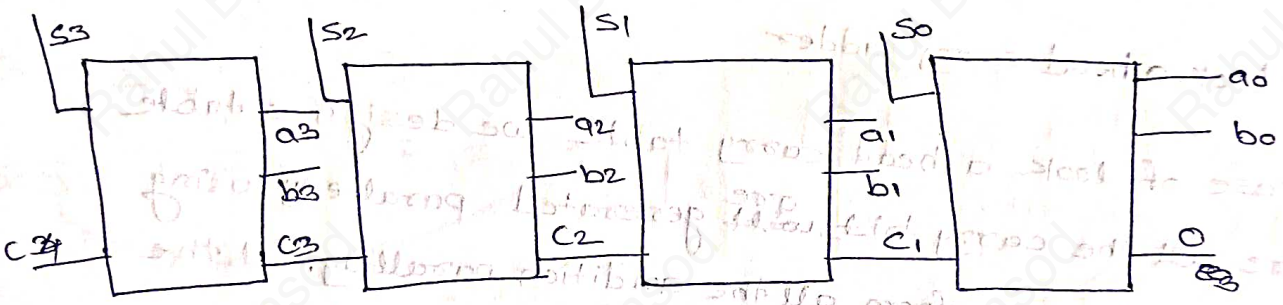
In case of parallel adder delay of carry gets added from one full adder to next full adder to their next full adder. ...so on.
i.e. it is called as rippeal carry adder

Lect-24

Q) we have two 4-bit numbers A & B. This two numbers are added using parallel adder. ~~delay~~ of sum delay & carry delay of each full adder are 3 ns & 2 ns respectively. then ~~what~~ How much time is required to perform complete addition.

a) 8 nsec b) 9 nsec c) 12 nsec d) 20 nsec.

Sol^n:-



$T_{delay} = (n-1)t_c + \max[\text{sum delay}, \text{carry delay}]$

$T_{delay} = (n-1)t_c + \max[t_c, t_s]$ → worst case delay

t_c → carry delay of each full adder

t_s → sum delay of each full adder

	6nsec	4nsec	2nsec	
A =	a_3	a_2	a_1	a_0
B =	b_3	b_2	b_1	b_0
	C_3	C_2	C_1	
	C_4	S_3	S_2	S_1	S_0
	8nsec	9nsec	7nsec	5nsec	3nsec

Lect-25

Q) We have two 100 bit numbers which addition is going to be perform using parallel adder. each full adder used in parallel adder has sum delay of 5 nsec & carry delay of 3 nsec. then worst case delay for performing the addition in nsec is 302 nsec.

Sol:-

$= 99 \times 3 + 5$

$= 297 + 5$

$= 302$ nsec.

look ahead carry adder

In case of look a head carry table we design a table where all the carry bits are generated parallely using Gate's & then perform all the addition parallely. all the bits simultaneously and i.e. it is fastest addition among all.

speed

Look a head carry > parallel > serial

delay

serial > parallel > Look ahead

Full subtractor :→

x	y	z	D	B
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$D = \Sigma(1,2,4,7) = x \oplus y \oplus z$$

$$B = \Sigma(1,2,3,7)$$

$$\bar{x}\bar{y}z + \bar{x}y\bar{z} + \bar{x}yz + xyz$$

$$B = \bar{x}z + \bar{x}y + yz$$

$$= \bar{x}y + z[x \odot y]$$

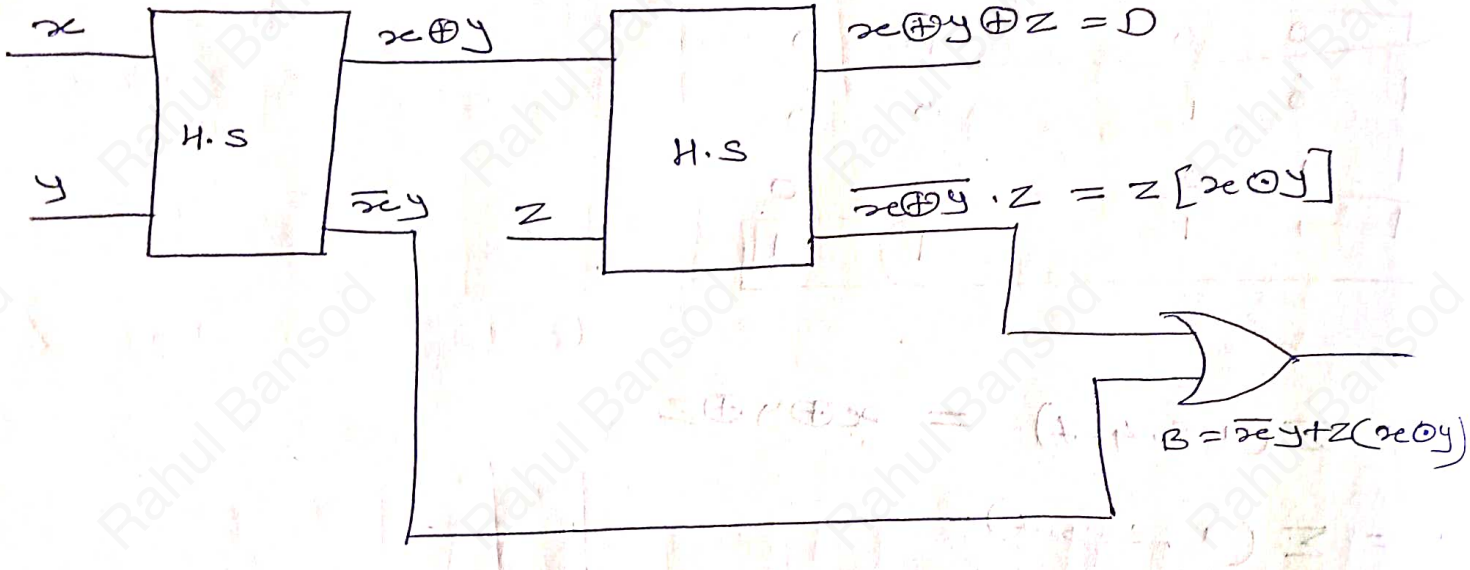
$$= \bar{x}y + z[\bar{x} \oplus y]$$

Lect-26

$D = x \oplus y \oplus z$

$B = \bar{x}y + yz + \bar{x}z$

$= \bar{x}y + z[x \odot y]$



$\boxed{\text{1. F.S.} \rightarrow \text{2 H.S \& 1 OR Gate}}$

Q) We have two n-bits numbers → A & B, subtraction

$A = a_2 \; a_1 \; a_0$

$B = b_2 \; b_1 \; b_0$

$B_2 \; B_1$

$B_3 \; D_2 \; D_1 \; D_0$

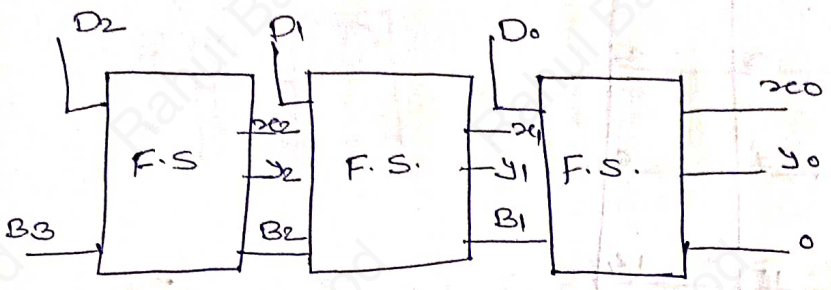
Total = 1 HS + (n-1) F.S.

= 1 HS + (n-1) × 2 HS + (n-1) OR

= [1 + 2n-2] HS + (n-1) OR = [2n-1] HS + (n-1) OR

Q) $X = x_2\ x_1\ x_0$

$Y = y_2\ y_1\ y_0$



$B_3\ D_2\ D_1\ D_0$

(1 ~~#~~ 2 Marks)

K-Map:-

1

0

X

		$\bar{B}$ (0)	B (1)
0	$\bar{A}$	0	1
1	A	2	3

$f(A,B) = \Sigma(1,2)$

Lec# - 27

A B C

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	0	1	3	2
A	4	5	7	6

Grey code

001 → 0

011 → 1

110 → 2

100 → 3

A B C D

$2^n - 1 = 2^4 - 1 = 15$

LSB

	$\overline{C}\,\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\,\overline{B}$	0	1	3	2
$\overline{A}B$	4	5	7	6
MSB AB	12	13	15	14
$A\overline{B}$	8	9	11	10

LEC* – 28

Q) $f(A,B) = \Sigma(1,3)$

	$\overline{B}$	B
$\overline{A}$	0	1
A	2	1 3

$= B$

Q) $f(A,B) = \Sigma(0,3) + d\Sigma 2 = \overline{B} + A$

	$\overline{B}$	B
$\overline{A}$	1 0	1
A	X 2	1 3

Q) $f(A,B) = \Sigma(0,2) + d\Sigma(1) = \overline{B}$

	$\overline{B}$	B
$\overline{A}$	1 (0)	X (1)
A	1 (2)	(3)

Q) $f(A,B,C) = \Sigma(0,1,6,7) = \overline{A}\,\overline{B} + AB = A \odot B$

	$\overline{B}\,\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	1	1		
A			1	1

Lect-29

Q) $f(A,B,C) = \Sigma(0,1,3,6,7)$

	$\overline{B}\,\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	1 (0)	1 (1)	1 (3)	(2)
A	(4)	(5)	1 (7)	1 (6)

$= \overline{A}\,\overline{B} + BC + AB$

pair, quard, octed

	$\overline{B}\,\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	1	1	1	
A			1	1

$= \overline{A}\,\overline{B} + \overline{A}C + AB$

- K-Map can have more than one solution but it is not necessary

Q) $f(A, B, C) = \Sigma(0, 1, 6, 7) + d(3, 5)$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1 (0)	1 (1)	X (3)	(2)
A	(4)	X (5)	1 (7)	1 (6)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	1	X	
A		X	1	1

$= \bar{A}\bar{B} + AB$

Q) $f(A, B, C) = \Sigma(1, 3, 6, 7)$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$		1	1	
A			1	1

$= \bar{A}C + AB + BC$

$= \bar{A}C + AB$

A pair have use than 1 then it is called as redundant pair or invalid pair.

Q) $f(A, B, C) = \Sigma(0, 1, 3, 6)$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	1	1	
A				1

$= \bar{A}\bar{B} + \bar{A}C$

Q) $f(A, B, C) = \Sigma(0, 1, 2, 4, 6)$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	1		1
A	1			1

$= \bar{C} + \bar{A}\bar{B}$

Q) $f(A, B, C, D) = \Sigma(0, 1, 3, 5, 7, 8, 9, 11, 13, 15)$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	
$\bar{A}B$		1	1	
AB		1	1	
$A\bar{B}$	1	1	1	

$= \bar{C}\bar{B} + D$

Q) $f(A, B, C, D) = \Sigma(0, 1, 4, 5, 8, 9, 13, 15)$

Lect-31

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1		
$\bar{A}B$	1	1		
AB		1	1	
$A\bar{B}$	1	1		

→ $\bar{C}D$ – is a redundant/ invalid quard

$= \bar{B}\bar{C} + \bar{A}\bar{C} + ABD$

Q) $f(A, B, C, D) = \Sigma(0, 4, 5, 7, 9, 13, 14, 15)$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$			1	
$\bar{A}B$	1	1	1	
AB		1	1	1
$A\bar{B}$		1		

$= \bar{A}B\bar{C} + \bar{A}CD + ABC + A\bar{C}D$

Q) $f(A, B, C, D) = \Sigma(0, 2, 4, 8, 9, 10)$

	$\overline{C}\,\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\,\overline{B}$	1			1
$\overline{A}B$	1			
AB				
$A\overline{B}$	1	1		1

$= \cancel{\overline{A}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{D} + A\,\overline{B}\,\overline{C}}$

$= \overline{B}\,\overline{D} + \overline{A}\,\overline{C}\,\overline{D} + A\,\overline{B}\,\overline{C}$

Q) $f(A, B, C, D) = \Sigma(0, 1, 2, 5, 7, 8, 9)$

	$\overline{C}\,\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\,\overline{B}$	1	1		1
$\overline{A}B$		1	1	
AB				
$A\overline{B}$	1	1		

$= \overline{A}\,\overline{B}\,\overline{D} + \overline{B}\,\overline{C} + \cancel{\overline{A}\,\overline{C}\,\overline{D}} + \overline{A}BD$

Lect- 32

Q) $F(A,B,C) = A\overline{C} + A\overline{B}C + BC$

	$\overline{B}\,\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$			1	
A	1	1	1	1

Pair - 1 variable reduse

quad → 2

octed → 3

$= A + BC$

Q) $F(A,B,C,D) = \overline{A}\,\overline{D} + BC\overline{D} + AC$

	$\overline{C}\,\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\,\overline{B}$	1			1
$\overline{A}B$	1			1
AB			1	1
$A\overline{B}$			1	1

$= \overline{A}\,\overline{D} + AC$

Q) $F(A, B, C, D) = A\bar{C} + B\bar{C} + AC\bar{D}$

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$				
$\bar{A}B$	1	1		
AB	1	1		1
$A\bar{B}$	1	1		1

$= B\bar{C} + A\bar{C} + A\bar{D}$

$= \Sigma(4, 5, 8, 9, 10, 12, 13, 14)$

Q) $F(A, B, C) = B + \overline{\bar{A}C + B\bar{C}}$

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$		1	1	1
A				1

$y_1 = \cancel{\bar{A}C + B\bar{C}}$

$\bar{A}C + B\bar{C}$

$\bar{y}_1 = \overline{\bar{A}C + B\bar{C}}$

	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	1		1	1
A	1	1	1	1

$= \overline{C} + A + B$

$= \overline{\overline{A}.\overline{B}.C}$

Q) $f(A,B,C) = A\overline{B} + \overline{B + \overline{C}\,\overline{A}}$

$y_1 = B + \overline{C}\,\overline{A}$

	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	1		1	1
A			1	1

$y = \overline{B + \overline{C}\,\overline{A}}$ & $A\overline{B}$

	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$		1		
A	1	1		

$= \overline{B}C + A\overline{B}$

Lect- 33

Q) If the function W, X, Y, Z are as

$$W = R + \bar{P}Q + \bar{R}S$$

$$X = PQ\bar{R}\bar{S} + \bar{P}\bar{Q}\bar{R}\bar{S} + P\bar{Q}\bar{R}\bar{S}$$

$$Y = RS + \overline{PR + P\bar{Q} + \bar{P}\bar{Q}}$$

$$Z = R + S + \overline{PQ + \bar{P}\bar{Q}\bar{R} + P\bar{Q}\bar{S}}$$

then

(a) $W = Z$, $X = \bar{Z}$

(b) $W = Z$, $X = Y$

(c) $W = Y$

(d) $W = Y = \bar{Z}$

Sol:-

W=

	$\bar{R}\bar{S}$	$\bar{R}S$	RS	$R\bar{S}$
$\bar{P}\bar{Q}$		1	1	1
$\bar{P}Q$	1	1	1	1
PQ		1	1	1
$P\bar{Q}$		1	1	1

$X =$

	$\overline{R}\,\overline{S}$	$\overline{R}S$	RS	$R\overline{S}$
$\overline{P}\,\overline{Q}$	1			
$\overline{P}Q$				
PQ	1			
$P\overline{Q}$	1			

$\therefore \quad W = \overline{X}$

(a) $W = Z$, $X = \overline{Z}$

$Y =$

	$\overline{R}\,\overline{S}$	$\overline{R}S$	RS	$R\overline{S}$
$\overline{P}\,\overline{Q}$			1	
$\overline{P}Q$	1	1	1	1
PQ	1	1	1	1
$P\overline{Q}$	1	1	1	

$Z =$

	$\overline{R}\,\overline{S}$	$\overline{R}S$	RS	$R\overline{S}$
$\overline{P}\,\overline{Q}$	1	1	1	1
$\overline{P}Q$	1	1	1	1
PQ	1	1	1	1
$P\overline{Q}$	1	1	1	1

Q) The boolean expression

$f(x, y, z) = \bar{x}y\bar{z} + x\bar{y}\bar{z} + xy\bar{z} + xyz$

converted into canonical product of sum of form is

✓ a) $(x+y+z)(x+y+\bar{z})(x+\bar{y}+\bar{z})(\bar{x}+y+\bar{z})$

b) $(x+\bar{y}+z)(\bar{x}+y+\bar{z})(\bar{x}+\bar{y}+z)(\bar{x}+\bar{y}+\bar{z})$

c) $(x+y+z)(\bar{x}+y+\bar{z})(x+\bar{y}+z)(\bar{x}+\bar{y}+\bar{z})$

d) $(x+\bar{y}+z)(\bar{x}+y+z)(\bar{x}+\bar{y}+z)(x+y+z)$

Soln:-

$f(x,y,z) = \Sigma(2,4,6,7)$ - sop → 0- bar, 1 non bar

pos $= \pi(0,1,3,5)$ → 0-non bar, 1-bar

$= (x+y+z)(\bar{x}+\bar{y}+\bar{z})(x+\bar{y}+\bar{z})(\bar{x}+y+\bar{z})$

	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{x}$			1	
x	1		1	1

sop form

$= x\bar{z} + yz$

	$\bar{Y}\bar{Z}$	$\bar{Y}Z$	YZ	$Y\bar{Z}$
$\bar{X}$	0	0		0
X		0		

pos form

$= \cancel{\bar{X}\bar{Z} + \bar{Y}Z}\ (\bar{X}+\bar{Z})(\bar{Y}+Z)$

$= XY + X\bar{Z} + YZ$

$= X\bar{Z} + YZ$

Lect-34

Q)

f	$\bar{B}$	B
$\bar{A}$		$\bar{C}$
A	C	1

$= \bar{A}\bar{B}\cdot 0 + \bar{A}B\cdot\bar{C} + A\bar{B}C + AB\cdot 1$

$= \bar{A}B\bar{C} + A\bar{B}C + AB$

	$\bar{B}$	B
$\bar{A}$	0	0
A	1	1

$= \bar{A}\bar{B}\cdot 0 + \bar{A}B\cdot 0 + A\bar{B}\cdot 1 + AB\cdot 1$

$= A\bar{B} + AB$

$= \Sigma(2,3)$

Q)

	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$				1
A		1	1	1

$= AC + B\bar{C}$

	$\overline{B}$	B
$\overline{A}$		1
A		1

$= B$

$C = 1$

	$\overline{B}$	B
$\overline{A}$		1
A	1	1

$= A$

$= B\overline{C} + AC$

Q)

Y	B	$\overline{B}$
	$\overline{B}$	B
A $\overline{A}$		1
$\overline{A}$ A		1

$Y = B \rightarrow$ SOP

$\overline{Y} = \overline{B}$

Q)

$(A+\overline{C})$

	$\overline{B}\,\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$		1	1	
A			1	1

$Y = \overline{A}.C + A.B$

$\overline{Y} = (A+\overline{C}).(\overline{A}+\overline{B})$ – clubing 1's & writing in sop form then we will get Y.

$Y = \overline{(A+\overline{C})(\overline{A}+\overline{B})}$

$Y = \overline{A+\overline{C}} + \overline{\overline{A}+\overline{B}}$

$= (\overline{A}+C) + (A.B)$

(Interview ask)

Comperator circuit :-

A	B	Y_2 (A > B)	Y_1 (A < B)	Y_0 (A = B)
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

Lect – 35

$y_2\ (A>B) = A\overline{B}$

$y_1\ (A<B) = \overline{A}B$

$y_0\ (A=B) = \overline{A}\,\overline{B} + A.B$

$= A \odot B$

Q) $A = a_2\ a_1\ a_0$

$B = b_2\ b_1\ b_0$

$y_2\ (A > B) = a_2 \cdot \overline{b_2} + (a_2 \oplus b_2) \cdot a_1 \overline{b_1} + a_2 \oplus b_2 \cdot a_1 \oplus b_1 + a_0 \overline{b_0}$

$y_1\ (A < B) = \overline{a_2} \cdot b_2 + (a_2 \oplus b_2) \cdot \overline{a_1}\ b_1 + a_2 \oplus b_2 \cdot a_1 \oplus b_1 \cdot \overline{a_0}\ b_0$

$y_0\ (A = B) = (a_2 \oplus b_2)(a_1 \oplus b_1)(a_0 \oplus b_0)$

a_2	a_1	a_0	b_2	b_1	b_0	y_2	y_1	y_0
0	0	0	0	0	0			
0	0	1	0	0	1			
0	1	0	0	1	0			
0	1	1	0	1	1			
1	0	0	1	0	0			
1	0	1	1	0	1			
1	1	0	1	1	0			
1	1	1	1	1	1			

→ M=B to LSB

Q) we have two no. a A & B and both are 2 bit numbers in how many combinations no. A > B

a) 5 b) 6 c) 7, d) 8

Sol^n ⇒ $A = a_1\ a_0$

$B = b_1\ a_0$

a_1	a_0	b_1	b_0
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

$A > B \rightarrow 1+1+1+1+1+1$
$= 6$

n- bit number

$A > B \rightarrow (2^n - 1)$

$N = 1+2+3+4+5+(2^n-1)$

2 bit $\rightarrow (2^2-1) = 3$
$= 1+2+3 \longrightarrow 6.$

4 bit $\rightarrow (2^4-1) = 15$
$= 1+2+3+ \ldots 15$

$= \frac{n(n+1)}{2} = \frac{15 \times 16}{2} = 15 \times 8 = 120$

* $A < B = B > A = (2^n - 1)$

b_1	b_0	a_1	a_0
0	0	0	0
0	1	0	1
1	0	1	0
1	1	1	1

* $A = B = 2^n$

A & B are n bit no.

Lect - 36

Q) Design a combinational ckt. having 3 i/p line & 1 o/p line the o/p is high when majority of the i/p lines are at logic zero.

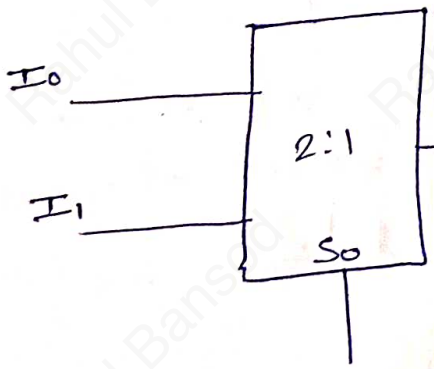
Q) Design a combinational ckt where input applying in BCD code as i/p & generates o/p '1' only when the i/p BCD code is divisible by 3.

Q) Design a combinational ckt where i/p is of 3 bit and ckt generates the square of the i/p no.

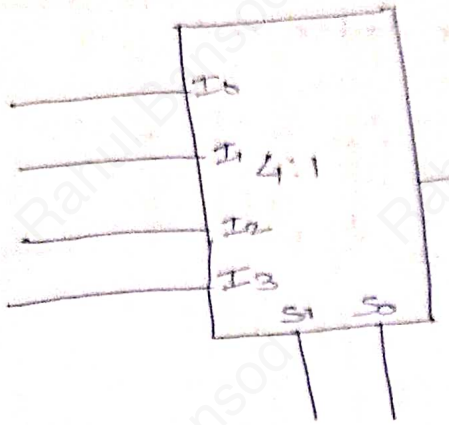
Imp

MUX :-

Mux is a combinational ckt having many i/p lines and single o/p line and on the basis of select line one of the i/p line is transfered to the o/p line.

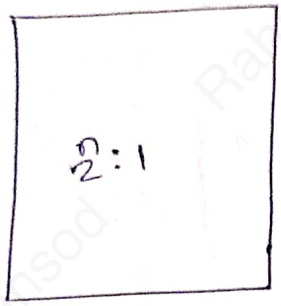


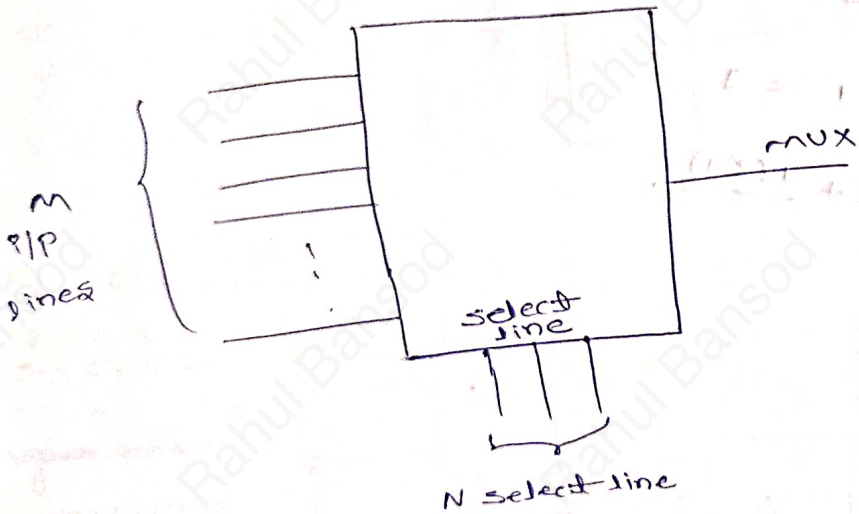
$Y = \bar{S}_0 I_0 + S_0 I_1$



$$Y = \bar{S}_1\bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1\bar{S}_0 I_2 + S_1 S_0 I_3$$

Q)





e^n for proper functioning of mux

$2^N \gg m$

$\log_2 2^N \geq \log_2 m$

$N \log_2 2 \geq \log_2 m$

$N \geq \log_2 m$

* higher order mux using lower lower order mux

$2^n:1 \quad 2^2:1 \longrightarrow 4:1 \xrightarrow{2:1} 2+1 = 3 = 2^2-1$

$2^3:1 \quad 8:1 \xrightarrow{2:1} 4+2+1 = 7 = 2^3-1$

$2^4:1 \quad 16:1 \xrightarrow{2:1} 8+4+2+1 = 15 = 2^4-1$

$$\boxed{2^n:1 \xrightarrow{2:1} (2^n-1)}$$

Lec# :- 37

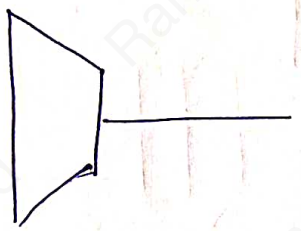
* $16:1 \xrightarrow{4:1} 4+1 = 5$

$64:1 \xrightarrow{4:1} 16+4+1 = 21$

$64:1 \xrightarrow{8:1} 8+1 = 9$

$16:1 \xrightarrow{8:1} 2 + 1(2:1)$

$2^{n-1} + 2^{n-2} + \cdots$



$32:1 \xrightarrow{8:1} 4 + 1(4:1)$

$\therefore 4(8:1) + 1(4:1)$

$32:1 \xrightarrow{4:1} 8 + 2 + 1(2:1)$

$10(4:1) + 1(2:1)$

Q) $8:1 \xrightarrow{2:1} 4+2+1$

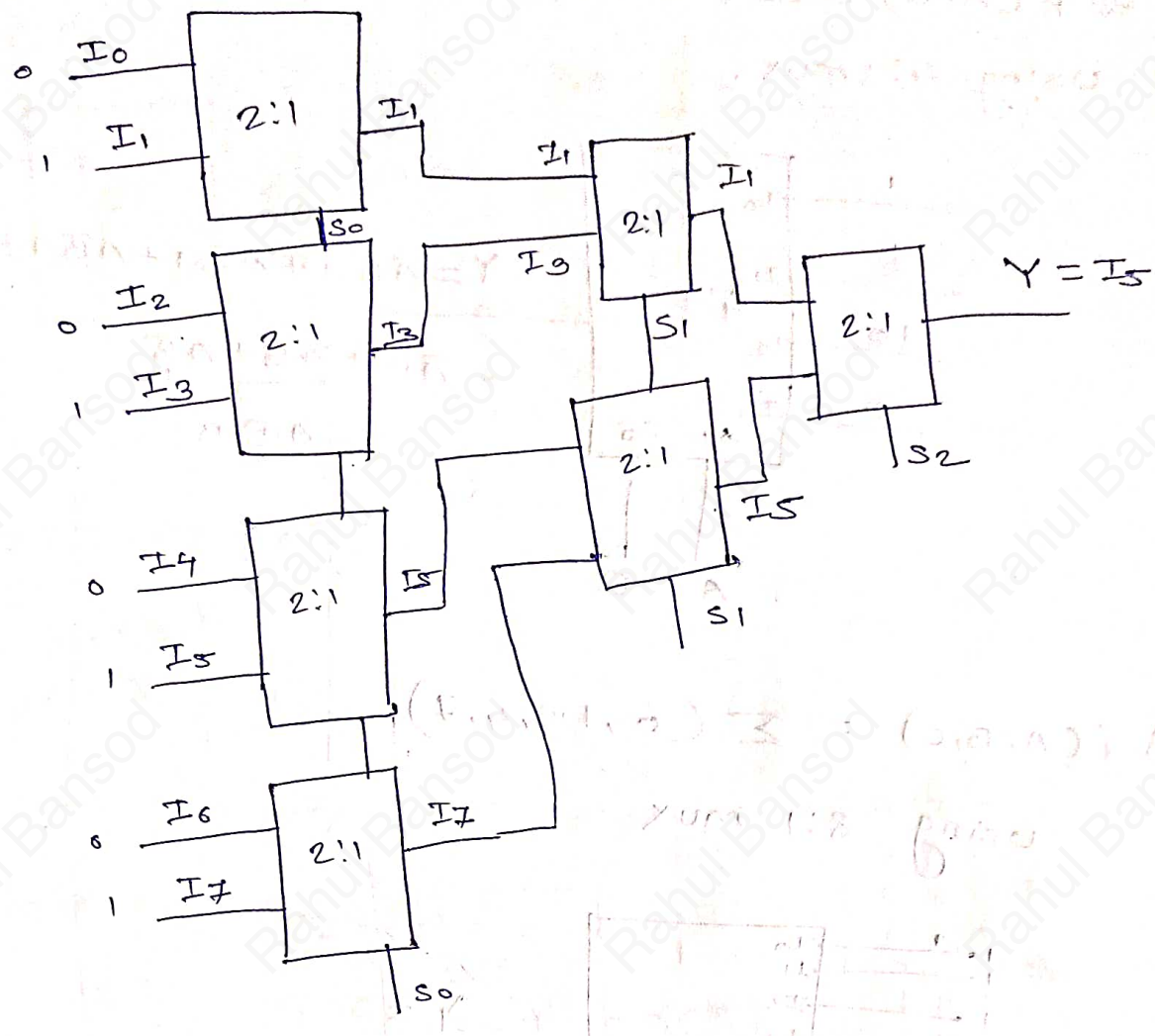
$S_2 S_1 S_0$

select line

lower to higher

$S_2\ S_1\ S_0$

$1\ \ 0\ \ 1 \rightarrow I_5$



Q) $16:1 \xrightarrow{4:1} 4+1$

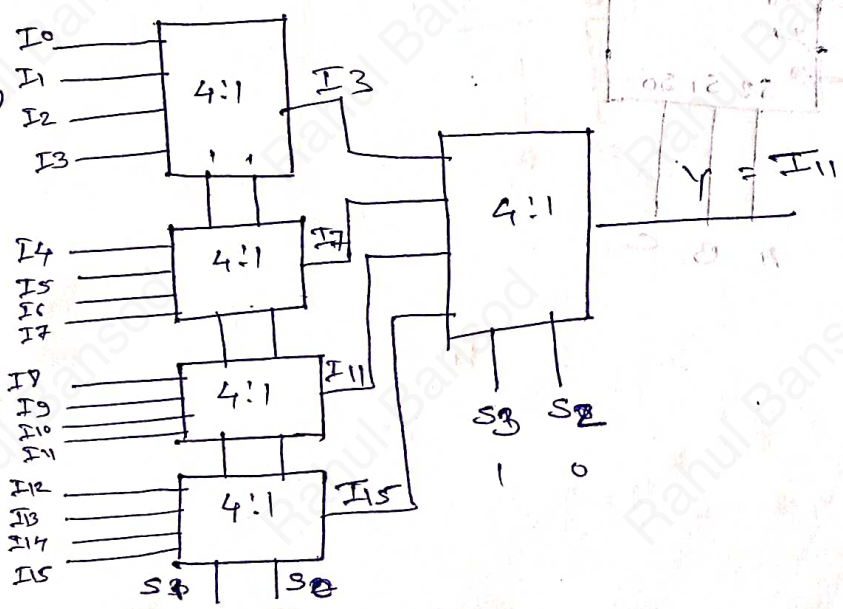
8 4 2 1

$S_3\ S_2\ S_1\ S_0$

$1\ \ 0\ \ 1\ \ 1 \rightarrow (11)$

~~higher → lower~~ 10

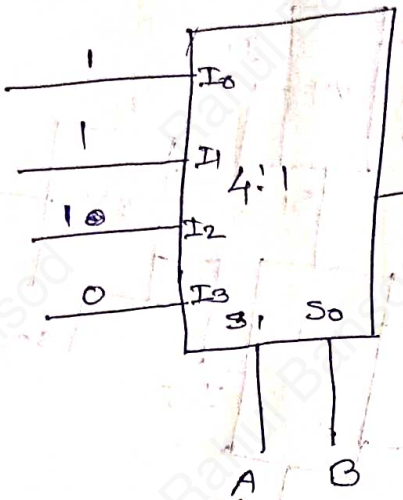
lower → higher



Lect-38

Q) $f(A,B) = \Sigma(0,1,2)$

Using 4:1 MUX.

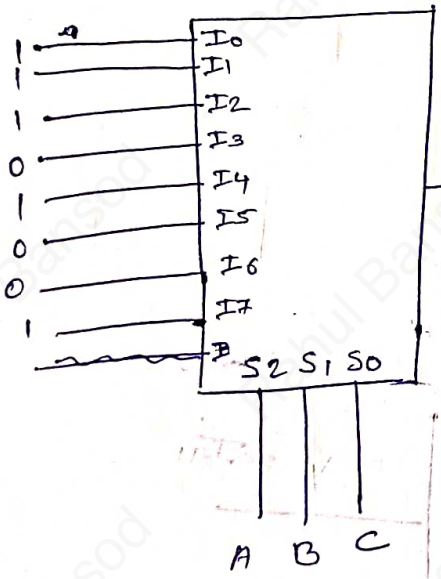


$Y = \bar{A}\bar{B}\cdot 1 + \bar{A}B\cdot 1 + A\bar{B}\cdot 1 + AB\cdot 0$

$= \bar{A}\bar{B} + \underbrace{\bar{A}B + A\bar{B}}_{A \oplus B}$

Q) $f(A,B,C) = \Sigma(0,1,2,4,7)$

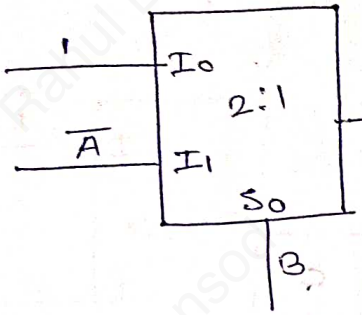
using 8:1 MUX



$Y =$

Q) $f(A,B) = \Sigma(0,1,2) =$

using 2:1 MUX



$Y = \bar{B}\cdot 1 + B\bar{A}$

	I_0	I_1
$\bar{A}$	0	1
A	2	3
	1	$\bar{A}$

A	B	
0	0	$\bar{A}\bar{B}$
0	1	$\bar{A}B$
1	0	$A\bar{B}$
1	1	AB

$Y = \bar{A}\bar{B} + \bar{A}B + A\bar{B}$

$= \bar{A} + A\bar{B}$

$= \bar{A} + \bar{B}$

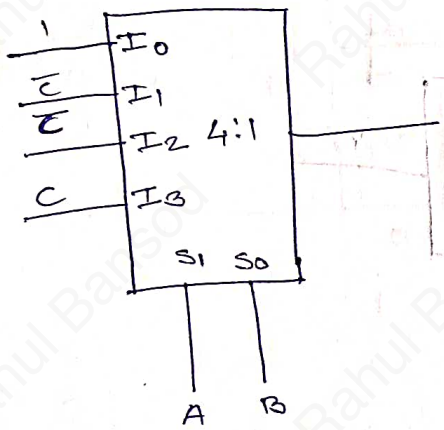
Q) $f(A,B,C) = \Sigma(0,1,2,4,7)$

using 4:1 MUX

a) AB select line

b) BC select line

c) AC select line

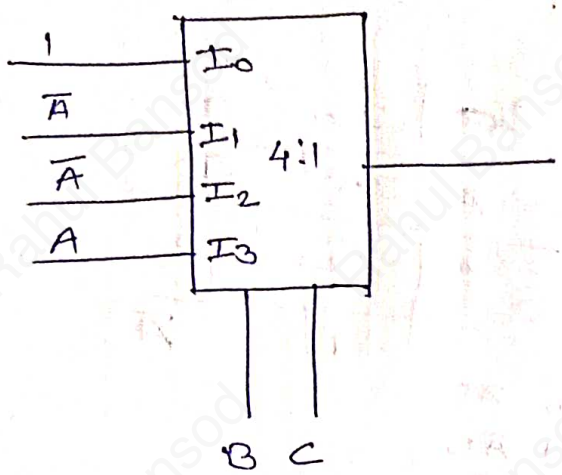


A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

a)

	I_0	I_1	I_2	I_3
$\bar{C}$	0	2	4	6
C	1	3	5	7
	1	$\bar{C}$	$\bar{C}$	C

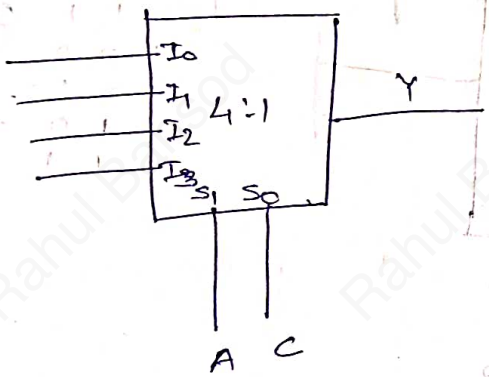
ⓑ BC select line



	I_0	I_1	I_2	I_3
$\bar{A}$	0	1	2	3
A	4	5	6	7
	1	$\bar{A}$	$\bar{A}$	A

A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

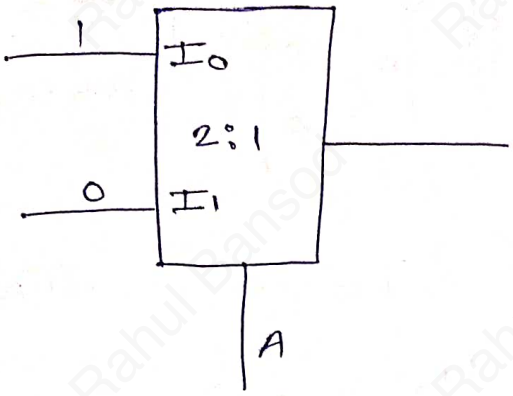
ⓒ AC select line



	I_0	I_1	I_2	I_3
$\bar{B}$	0	1	2	3
B	4	5	6	7
	1	$\bar{B}$	$\bar{B}$	B

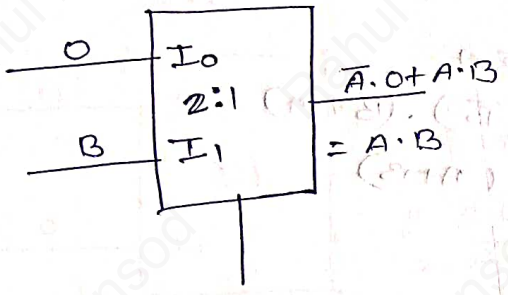
Lect-40

MUX as a universal circuit



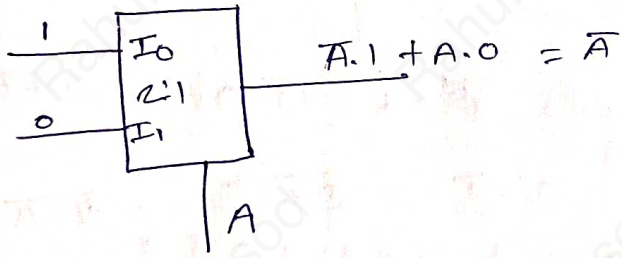
$F(A) = \Sigma(0) = \overline{A}$

AND Gate :- $f(A,B) = \Sigma(3)$



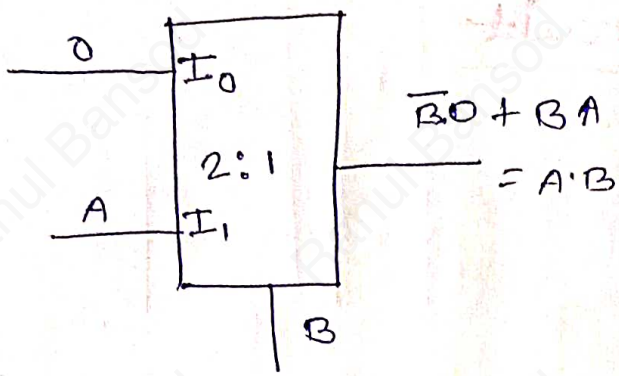
	I_0	I_1
$\overline{B}$	0	2
B	1	3
	0	B

NOT Gate



$A = 0 \xrightarrow[\overline{A}]{} 1$

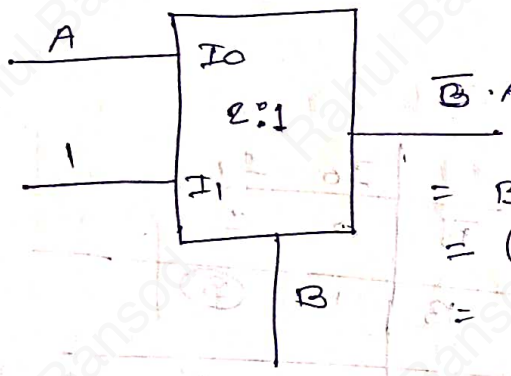
* AND Gate



$A \cdot B = A \cdot 0 = 0$

$A \cdot B = A \cdot 1 = A$

* OR Gate



$= B + \overline{B}A$

$= (B + \overline{B}) \cdot (B + A)$

$= (A + B)$

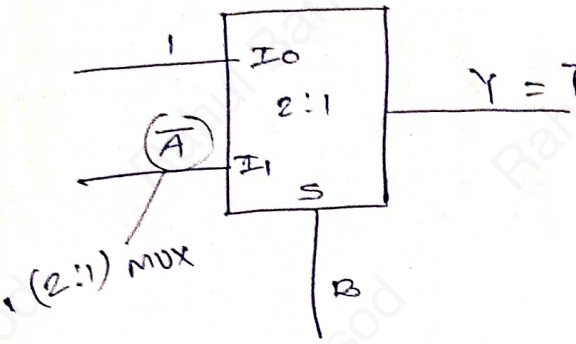
$f(A, B) = \Sigma(1, 2, 3)$

$B = 0, 1$

$A + 0 = A$

$A + 1 = 1$

* NAND Gate



$Y = B + \overline{A}B = (\overline{B} + B)(\overline{B} + \overline{A})$

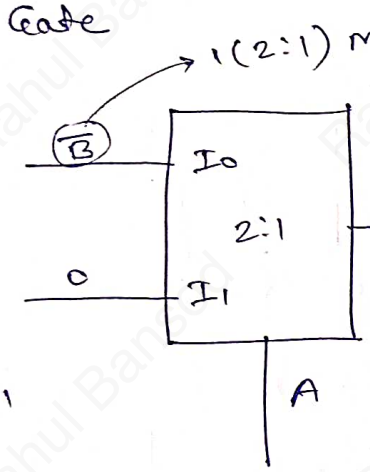
$= 1\,(\overline{A} + \overline{B})$

$= \overline{A \cdot B}$.

$\overline{A \cdot B} = \overline{A \cdot 0} = 1$

$\overline{A \cdot B} = \overline{A \cdot 1} = \overline{A}$

* NOR Gate



$= \overline{A} \cdot \overline{B} + A \cdot 0$

$= \overline{A}\,\overline{B}$

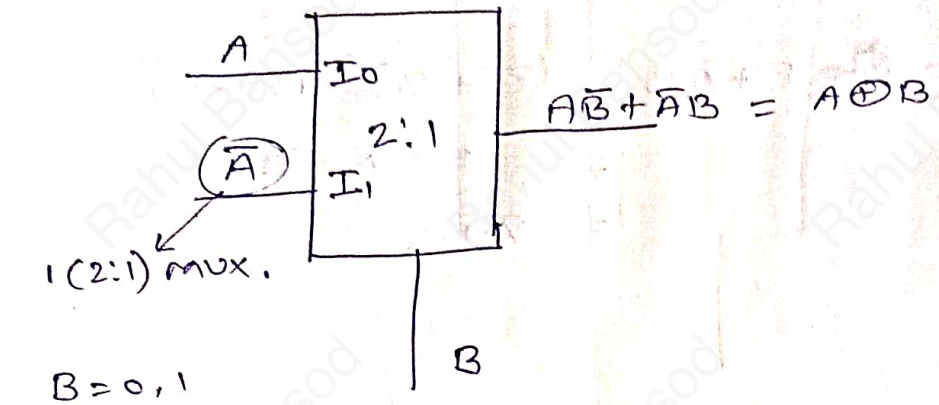
$= \overline{A+B}$.

$A = 0, 1$

$\overline{A+B} = \overline{0+B} = \overline{B}$

$\overline{A+B} = = \overline{1+B} = \overline{1} = 0$.

* XOR $A \oplus B$

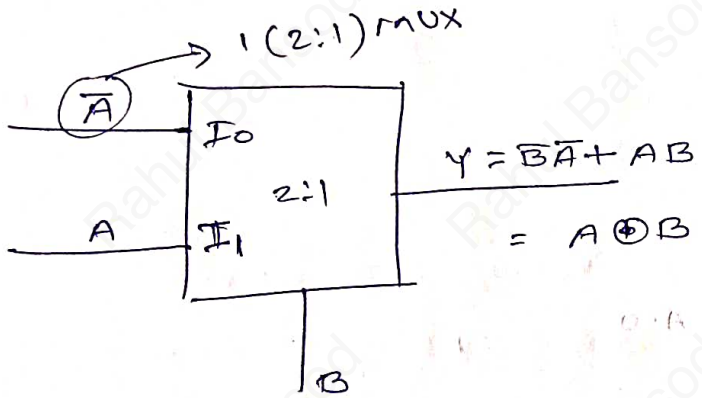


$B = 0, 1$

$A \oplus B = A \oplus 0 = A$

$A \oplus B = A \oplus 1 = \bar{A}$

* XNOR



$B = 0, 1$

$A \odot B = A \odot 0 = \bar{A}$

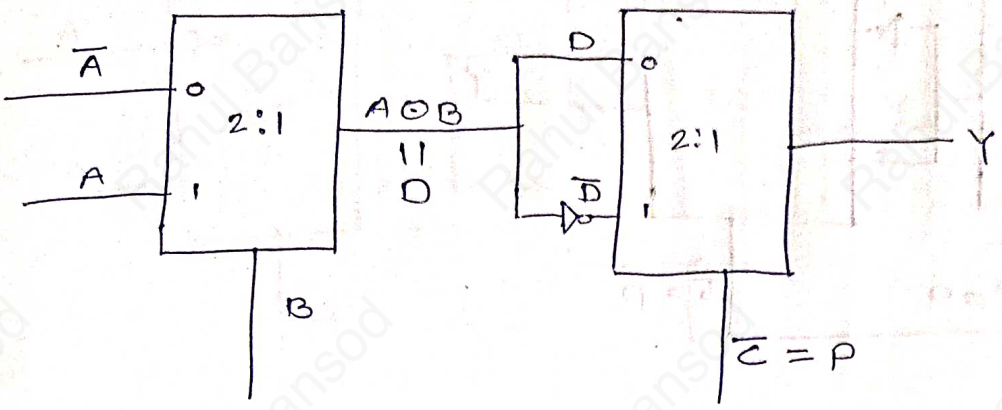
$A \odot 1 = A$

Note:- for implementation of Basic gates (NOT, AND, OR) one 2:1 MUX required.

- for implementation of non basic gates (NAND, NOR, XOR, XNOR) Two 2:1 MUX required.

Lect - 41

Q)



Y is

✓ a) $A \odot B \odot C$

b) $\overline{A \oplus B \oplus C}$

c) $A \odot B$

d) $B \oplus C$

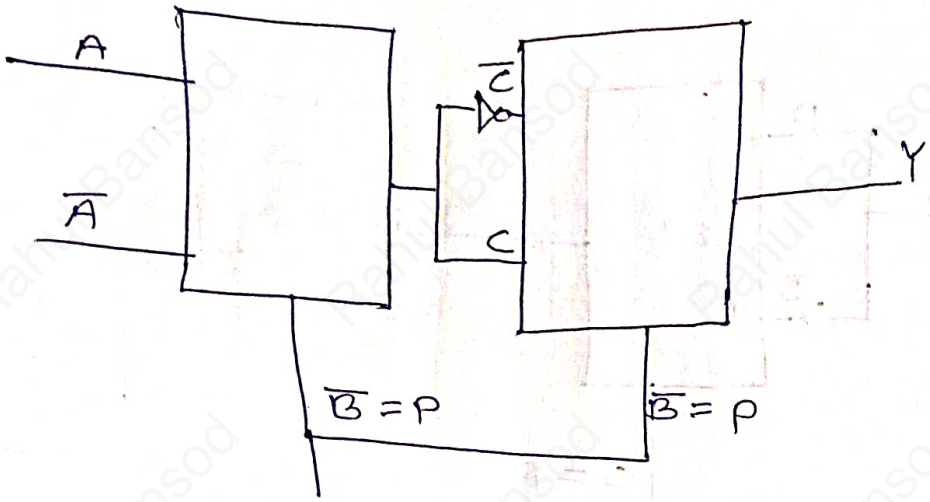
Solⁿ:-

$$Y = D\bar{P} + \bar{D}P$$

$$= D \oplus P = A \odot B \oplus \bar{C}$$

$$= A \odot B \odot C$$

Q)



Y is

a) $A \oplus B$

b) $A \odot B$

c) $\overline{A}$

d) A

Sol^n:-

$A\overline{B} + \overline{A}P$

$A \oplus P$

$A \oplus \overline{B}$

$A \odot B$

$\overline{C}\,\overline{P} + PC$

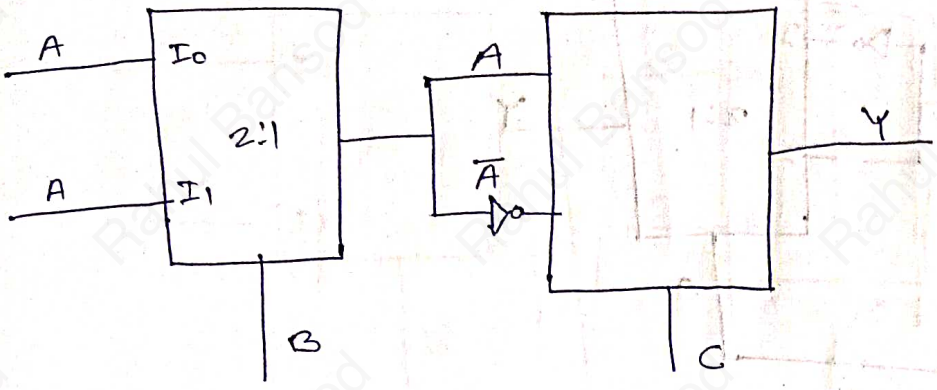
$\overline{C \oplus P} = C \odot P$

$= A \odot \underbrace{B \odot \overline{B}}_{0}$

$= A \odot 0$

$= \overline{A}.$

Q)



Solⁿ :-

$\bar{B}A + AB$

$A \cdot 1 = A$

$\bar{C}A + \bar{A}C = A \oplus C$

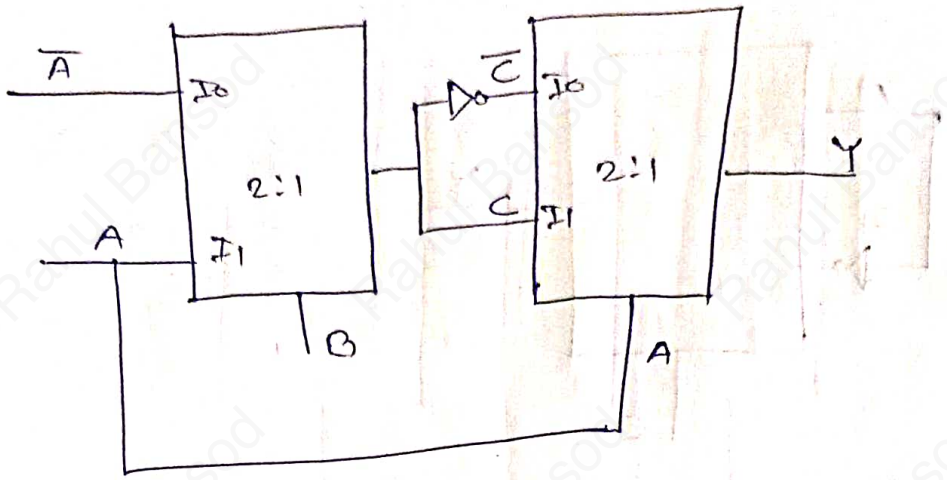
a) $A \oplus B \oplus C$

b) $A \odot B \odot C$

c) $A \oplus B$

d) $A \oplus C$

Q)



Sol^n:-

$$\overline{A}\,\overline{B} + AB = A \odot B = C$$

$$C\overline{A} + CA = A\ C \odot A$$

$$= A \odot B \odot A$$

$$= 1 \odot B$$

$$= B$$

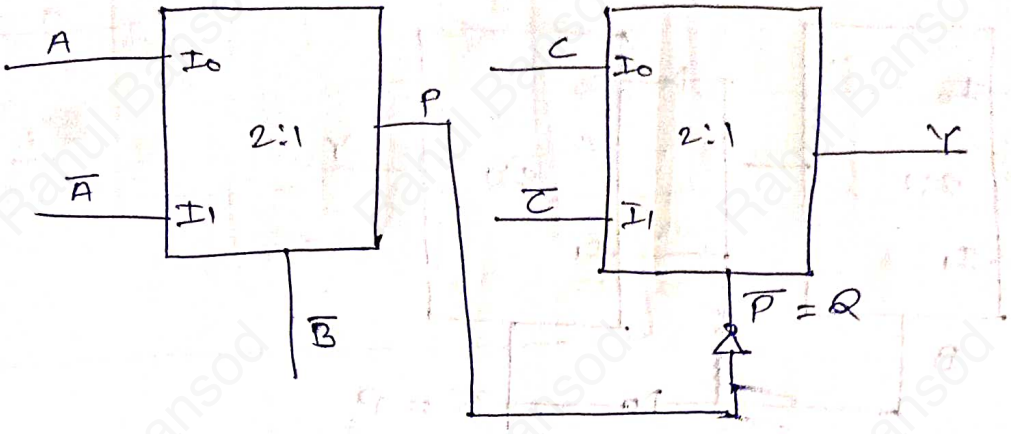
a) $A \oplus B$

b) $A \odot B$

✓ c) B

d) $\overline{A}$

Q)



a) $A \odot B \oplus C$

b) $A \oplus B \oplus C$

c) $A \odot B$

d) $A \oplus C$

soln:-

$$AB + \overline{A}\,\overline{B} = A \odot B = P$$

$$\overline{P} = Q$$

$$\therefore \; C\overline{Q} + \overline{C}Q$$

$$C \oplus Q$$

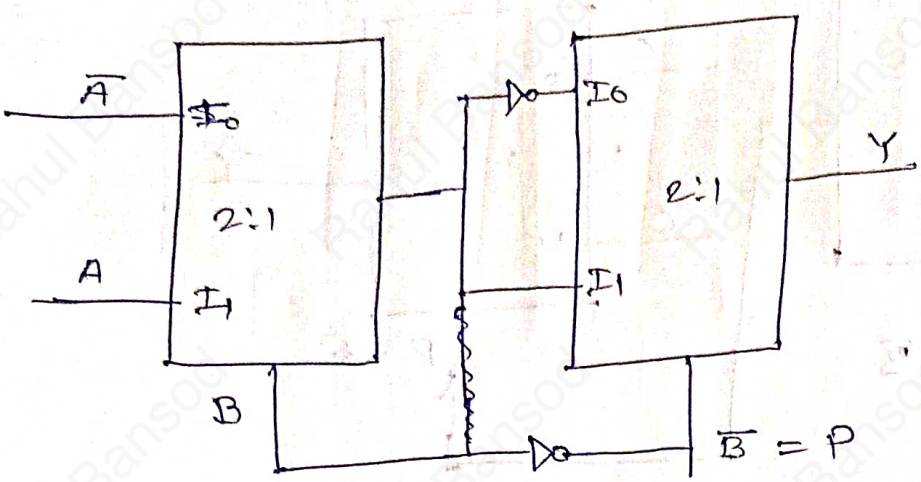
$$C \oplus \overline{A \odot B}$$

$$= C \oplus A \oplus B$$

$$= A \oplus B \oplus C$$

Lect - 42

Q)



Y is

a) $\bar{A}$

b) $A \odot B$

c) $A \oplus B$

d) A

$\bar{A}\bar{B} + AB = A \odot B = C$

$\bar{C}\bar{P} + CP$

$\bar{B} = P$

$C \odot P$

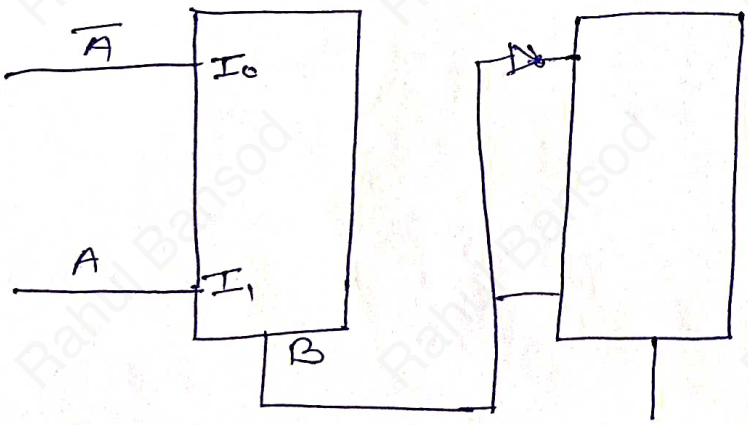
$A \odot B \odot \bar{B}$

0

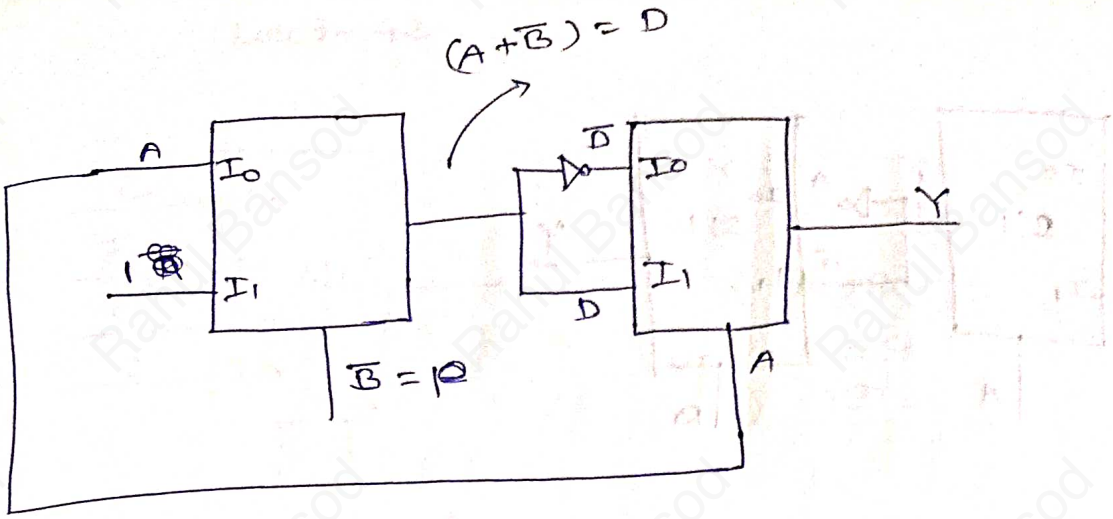
$A \odot 0$

$= \bar{A}$.

Q)



Q)



Sol^n :-

$A\overline{0} + 0.1$

$= AB + \overline{B}$

$= (A+\overline{B}).(B+\overline{B})$

$= (A+\overline{B}).\ 1$

$= (A+\overline{B}) = D$

$=$

$= \overline{A}\,\overline{D} + AD$

$= A \odot D$

$= A \odot [A + \overline{B}]$

$= \overline{A}\,\overline{(A+\overline{B})} + A(A+B)$

$= \overline{A}.\overline{A}B + A.A + A\overline{B}$

$= \overline{A}B + A(1+\overline{B}) = \overline{A}B + A$

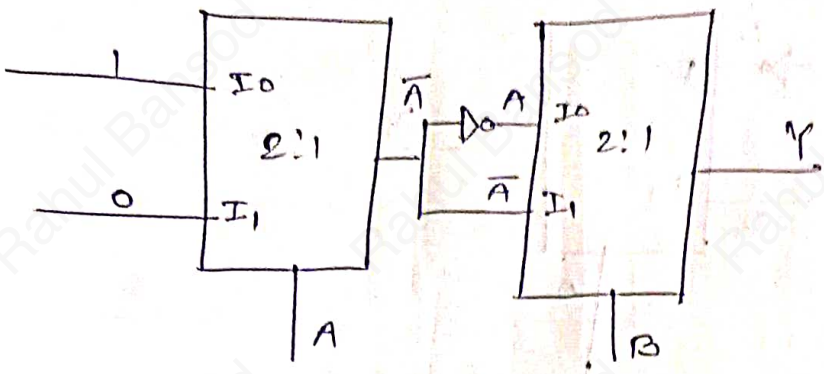
$= (A+\overline{A})(A+B)$

$= (A+B).$

Note:- $X.[X + _____] = x$

$x[x + xA + A\overline{x}C + Dxc] = x$

Q)



Y is

a) $A+B$

b) $A \cdot B$

c) $A \odot B$

D) $A \oplus B$

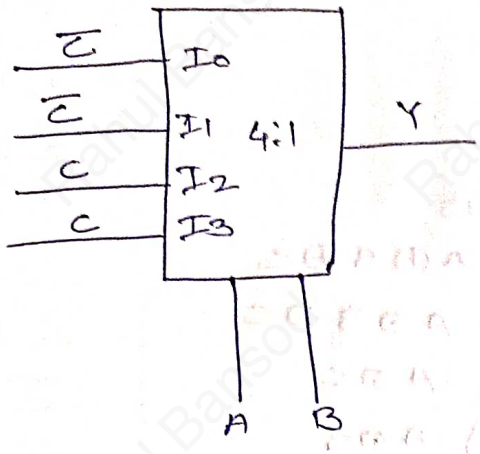
Sol^n:- $\bar{A} \cdot 1 + A \cdot 0 = \bar{A} + 0 = \bar{A}$

$= \bar{B}A + B\bar{A}$

$= A \oplus B$

Lect- 43

Q)



Y is

a) $A \oplus B \oplus C$

b) $A \oplus B \odot C$

c) $A \odot C$

d) $A \oplus B$

Sol:- $\overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,C + ABC$

st method 1:- K map

	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	1			1
A		1	1	

$= AC + \overline{A}\,\overline{C}$

$= A \odot C$

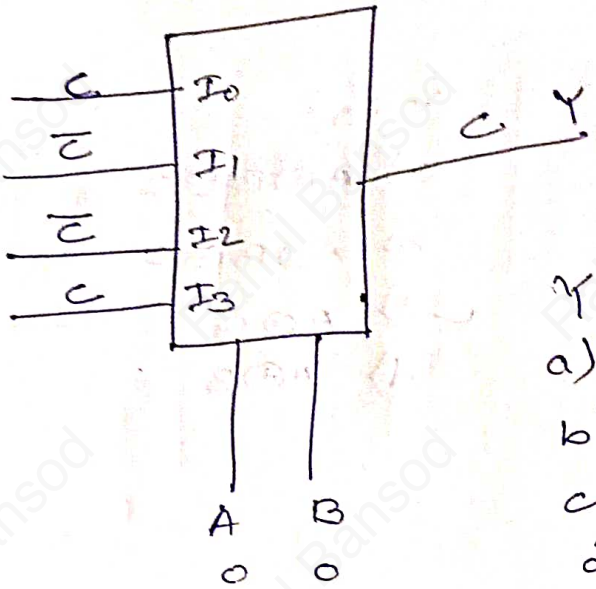
method 2:- Boolean function

$= \overline{A}\,\overline{C} + AC(\overline{B} + B)$

$= \overline{A}\,\overline{C} + AC$

$= A \odot C$

Q)



Y is

a) $A \oplus B \oplus C$

b) $A \odot B \oplus C$

c) $A \odot C$

d) $A \odot B$

$\overline{A}\,\overline{B}C + \overline{A}B\overline{C} + A\overline{B}\overline{C} + ABC$

	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$		1		1
A	1		1	

$= \cancel{\overline{A}\,\overline{B} + \overline{A}\,\overline{C} + ABC}$

$= \cancel{\overline{A}\,\overline{B} + \overline{A}\,\overline{C}} = \Sigma(1, 2, 4, 7)$

digonaly cross number / /

$\therefore$ its $A \oplus B \oplus C$

also practice boolean function.

$= \overline{B}\,[\overline{A}C + A\overline{C}] + B\,[\overline{A}\,\overline{C} + AC]$

$= \overline{B}\;A \oplus C + B\,(A \odot C)$

$= \overline{B}X + B\overline{X} = B \oplus X = B \oplus A \oplus C = A \oplus B \oplus C$

$0 \oplus 0 \oplus C = C$

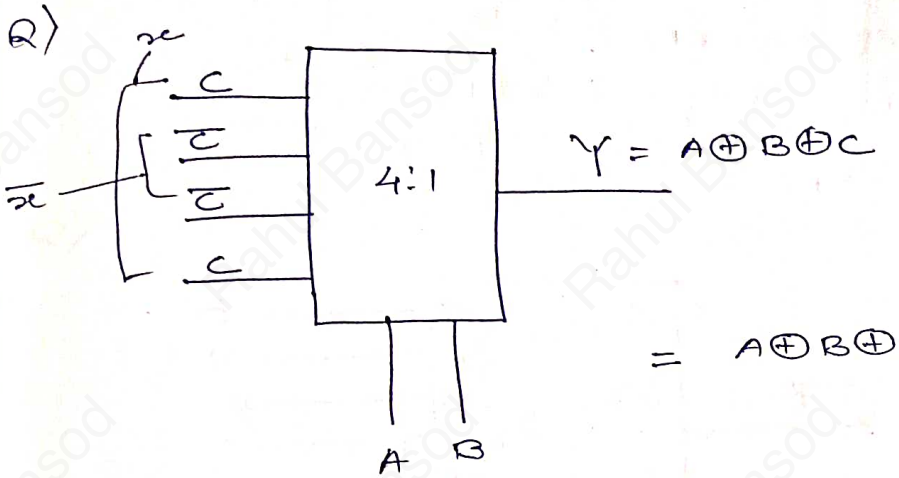
$0 \oplus 0 \oplus C = 1 \oplus C$

$= \overline{C}$

$0 \oplus C = \overline{C}$

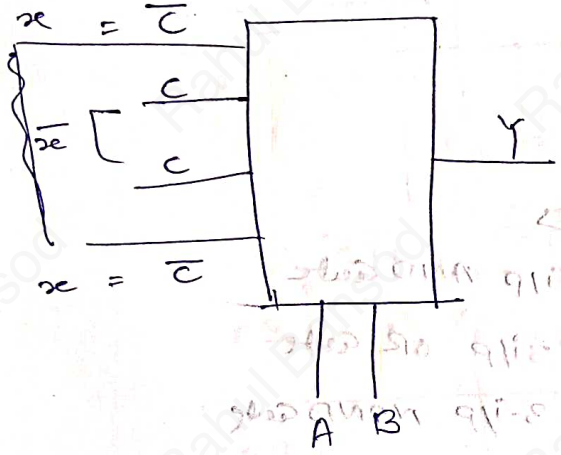
$0 \odot 0 = 1$

Q)



$Y = A \oplus B \oplus C$

$= A \oplus B \oplus x$



$A \oplus B \oplus x$

$A \oplus B \oplus \overline{C} = A \oplus B \oplus C'$

$= A \oplus B \odot C$

$= \overline{A \oplus B \oplus C}$.

$= \overline{A}\,\overline{B}C + \overline{A}B\overline{C} + AB\overline{C} + ABC$

K - map

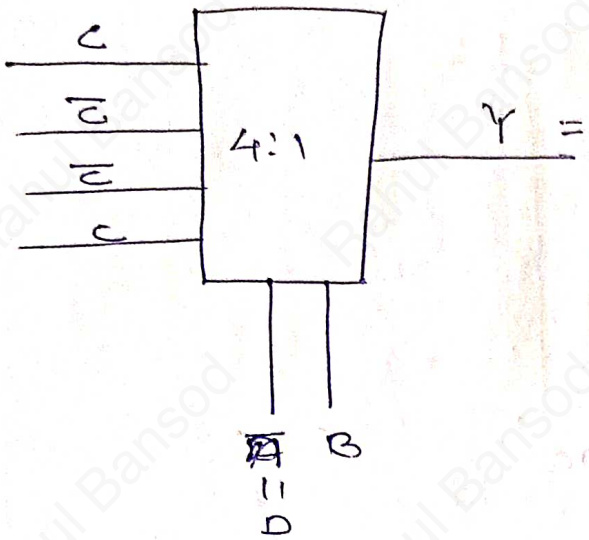
	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$		1		
A	1		1	1

$= \overline{A}\,\overline{B}C + AB + A\overline{C}$

$= \overline{A}[\overline{B}C] + A[B + \overline{C}]$

$= \overline{A \oplus B \oplus C}$

Q)



$\overline{A} = D$.

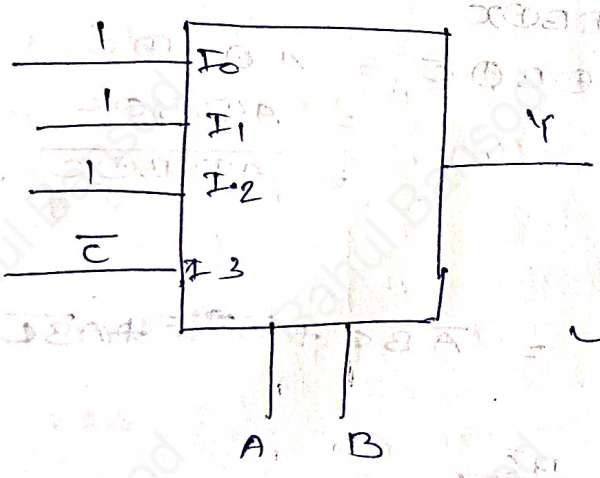
$D \oplus B \oplus C$

$\overline{A} \oplus B \oplus C$

$A \odot B \oplus C$

$\overline{A \oplus B \oplus C}$

Q)



Y is

a) A 3 i/p AND Gate

b) A 3 i/p OR Gate

c) A 3-i/p NAND Gate

d) A 3 i/p NOR Gate

Sol:- $Y = \overline{A}\,\overline{B}\,1 + \overline{A}\,B\,1 + A\,\overline{B}\,1 + A\,B\,\overline{C}$

	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$	1	1	1	1
A	1	1		1

$= \overline{A} + \overline{B} + \overline{C}$

$= \overline{A \cdot B \cdot C}$ = NAND Gate

Lec-44

a) AND Gate $A \cdot B \cdot C$ $\quad 0 \cdot 0 \cdot 1 = 0$ ✗

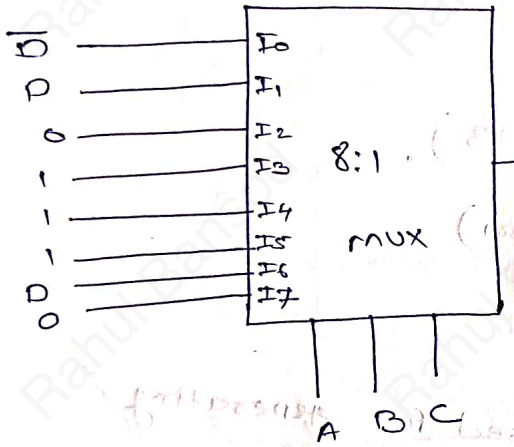
b) OR Gate $A + B + C$ $\quad 0 + 0 + 1 = 1$ ✗

c) NAND Gate $\overline{ABC}$ $\quad \overline{0 \cdot 0 \cdot 0} = 1$ ✓

d) OR Gate $\overline{A+B+C}$ $\quad \overline{0+0+0} = \overline{C}$ ✗

A	B
0	0
0	1

Q)



Y =

Y is

a) $\Sigma(0,1,2,3,6,7,8,9,10,11,13)$

b) $\Sigma(0,3,6,7,8,9,10,11,13)$ ✓

c) $\Sigma(0,1,2,6,7,9,10,11,13)$

d) $\Sigma(0,4,6,7,8,9,10,11,13)$

000 = $\overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$ =

001 = $\overline{A}\,\overline{B}C\,D$ =

010 = $\overline{A}B\overline{C} \cdot 0 = 0$

011 = $\overline{A}BC \cdot 1$ ✓

100 = $A\overline{B}\overline{C} \cdot 1$

101 = $A\overline{B}C \cdot 1$

110 = $AB\overline{C}\,D$

111 = $ABC\,0 = 0$

	$\overline{C}\,\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\,\overline{B}$	1 (0)	1 (1)	1 (3)	(2)
$\overline{A}B$	(4)	1 (5)	1 (7)	(6)
AB	1 (12)	1 (13)	(15)	1 (14)
$A\overline{B}$	1 (8)	1 (9)	1 (11)	1 (10)

$A B \overline{C}$.

$\Sigma(0, 3, 7, 6, 12, 13, 10, 8, 9)$

$Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D}$ $\quad \overline{A}\,\overline{B}\,C\,D$

0 0 0 0 $\quad$ 0 0 1 1

3

0 1 0	$\overline{A}\,B\,\overline{C}\cdot 0 = 0$
0 1 1	$\overline{A}\,B\,C\cdot 1 = 0111 + 0110 = 6, 7$
1 0 0	$A\,\overline{B}\,\overline{C}\cdot 1 = 1001 = A\,\overline{B}\,\overline{C}\,(D+\overline{D}) = 8, 9$
1 0 1	$A\,\overline{B}\,C\cdot 1 = 1011 + 1010 = 10, 11$
1 1 0	$A\,B\,\overline{C}\cdot D = 1101 = 13,$
1 1 1	$A\,B\,C\cdot 0 =$

$\Sigma(0, 3, 6, 7, 8, 9, 10, 11, 13)$.

(check again this problem)

Lect- 45

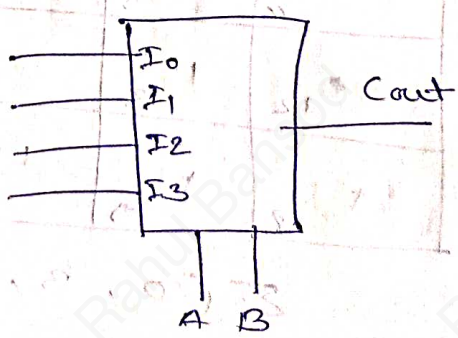
Q) A 4:1 multiplexer is to be used for generating the output carry of a full adder. A & B are bits to be added while cin is input carry & cout is o/p carry. which of the following statement describe the choice of signals at I_0, I_1, I_2, I_3

a) $I_0 = 0, I_1 = C_{in}, I_2 = C_{in}, I_3 = 1$

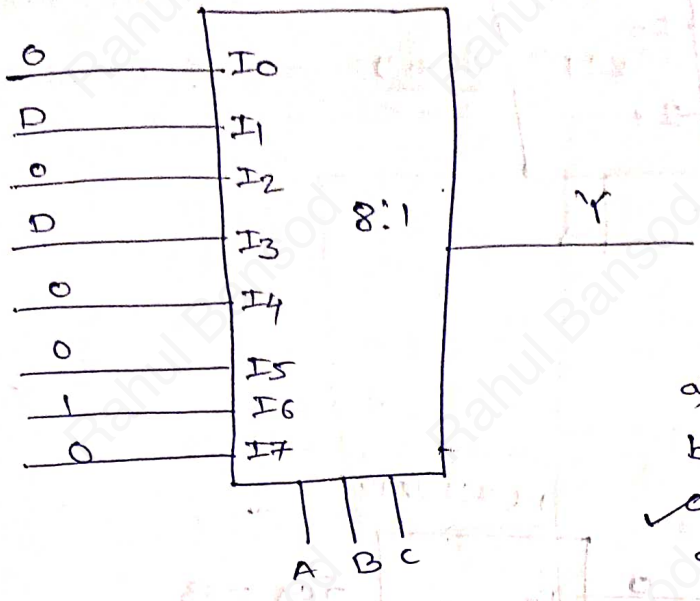
b) $I_0 = 1 \quad I_1 = C_{in} \quad I_2 = C_{in} \quad I_3 = 1$

c) $I_0 = C_{in} \quad I_1 = 0 \quad I_2 = 1 \quad I_3 = C_{in}$

d) $I_0 = 0 \quad I_1 = C_{in} \quad I_2 = 1 \quad I_3 = C_{in}$



Q2) An 8:1 mux as used to implement a logical function



Y is

a) $A\bar{B}C + A\bar{C}D$

b) $\bar{A}BC + A\bar{B}D$

✓ c) $AB\bar{C} + \bar{A}CD$

d) $\bar{A}\bar{B}D + A\bar{B}C$

Soln:- using K-map $= \bar{A}\bar{B}CD + \bar{A}BCD + AB\bar{C}D + AB\bar{C}\bar{D}$

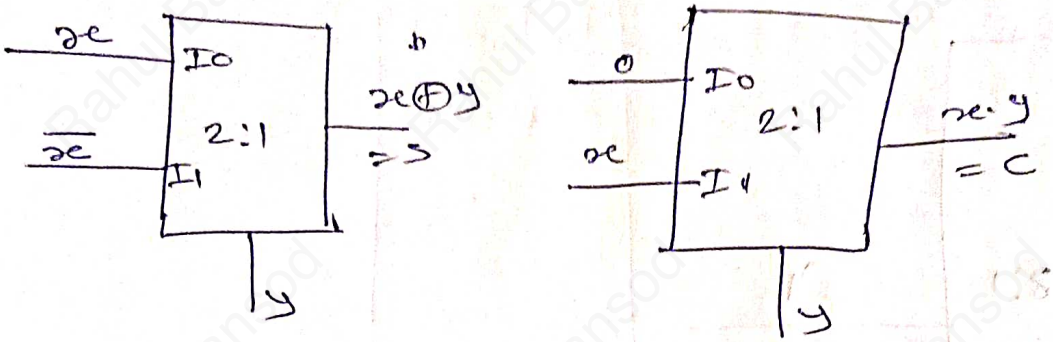
	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0		1	
$\bar{A}B$			1	
AB	1	1		
$A\bar{B}$				

$= \bar{A}CD + AB\bar{C}.$

H.A

$S = x \oplus y$

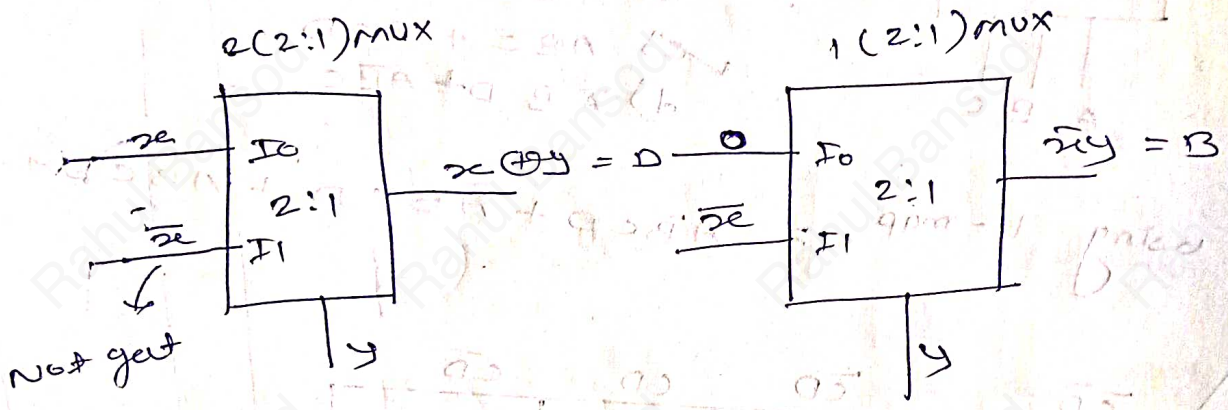
$C = xy$



Lect- 46

H.S $D = x \oplus y$

$B = \bar{x}y$

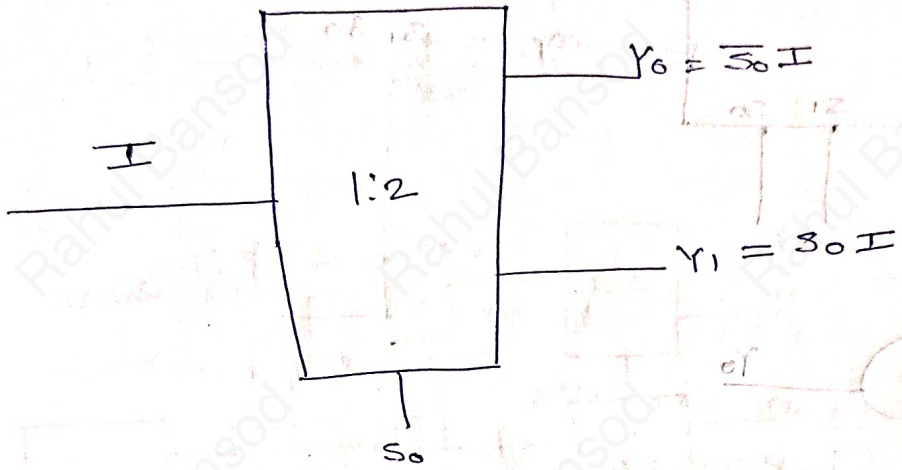


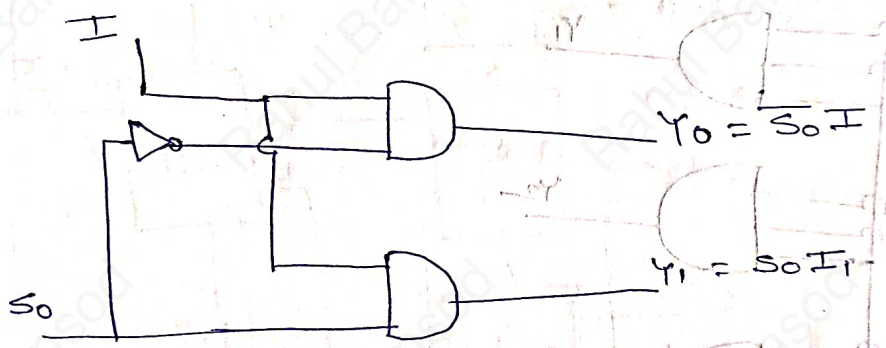
H.W $x \oplus y \oplus z = S$

$xy + z[x \oplus y] = C.$

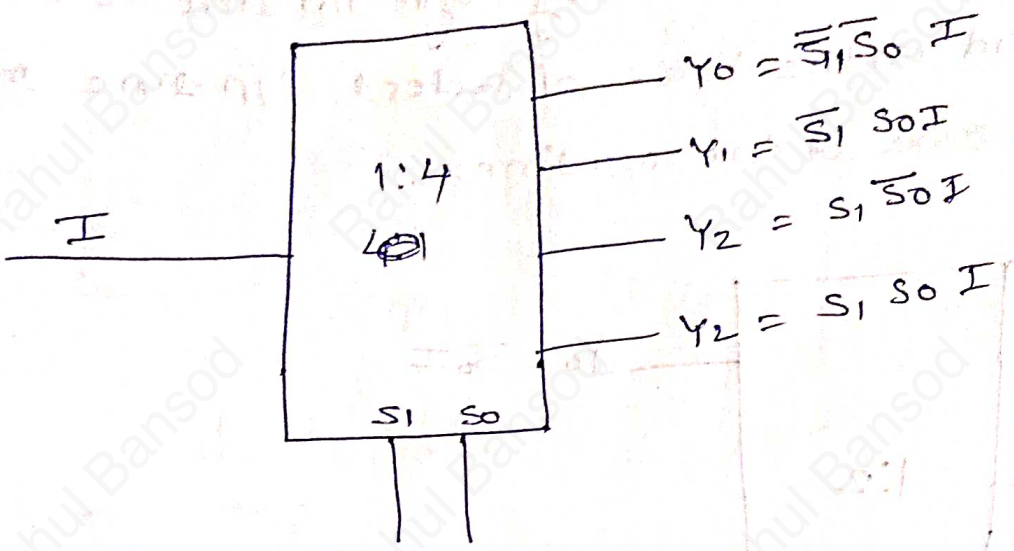
DeMUX

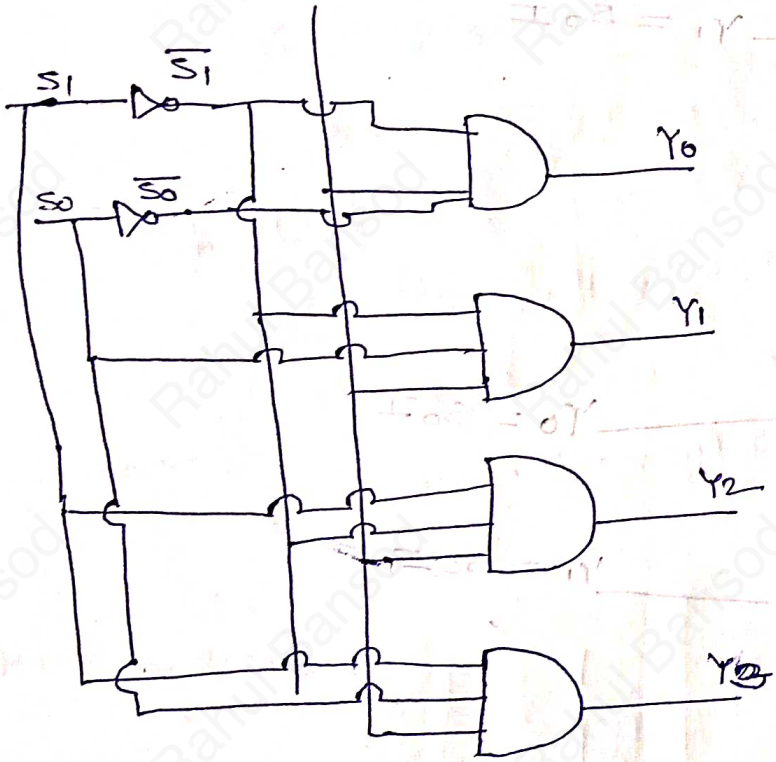
It is a combinational circuit having single i/p line & many output lines. and on the basis of select i/p line ~~it~~ transfered to the one of the o/p lines.





1:4 ~~4:1~~ Demux


1:4
I
S1 S0
Y0 = $\overline{S_1}\,\overline{S_0}$ I
Y1 = $\overline{S_1}$ S0 I
Y2 = S1 $\overline{S_0}$ I
Y2 = S1 S0 I


S1
$\overline{S_1}$
S0
$\overline{S_0}$
Y0
Y1
Y2
Y3

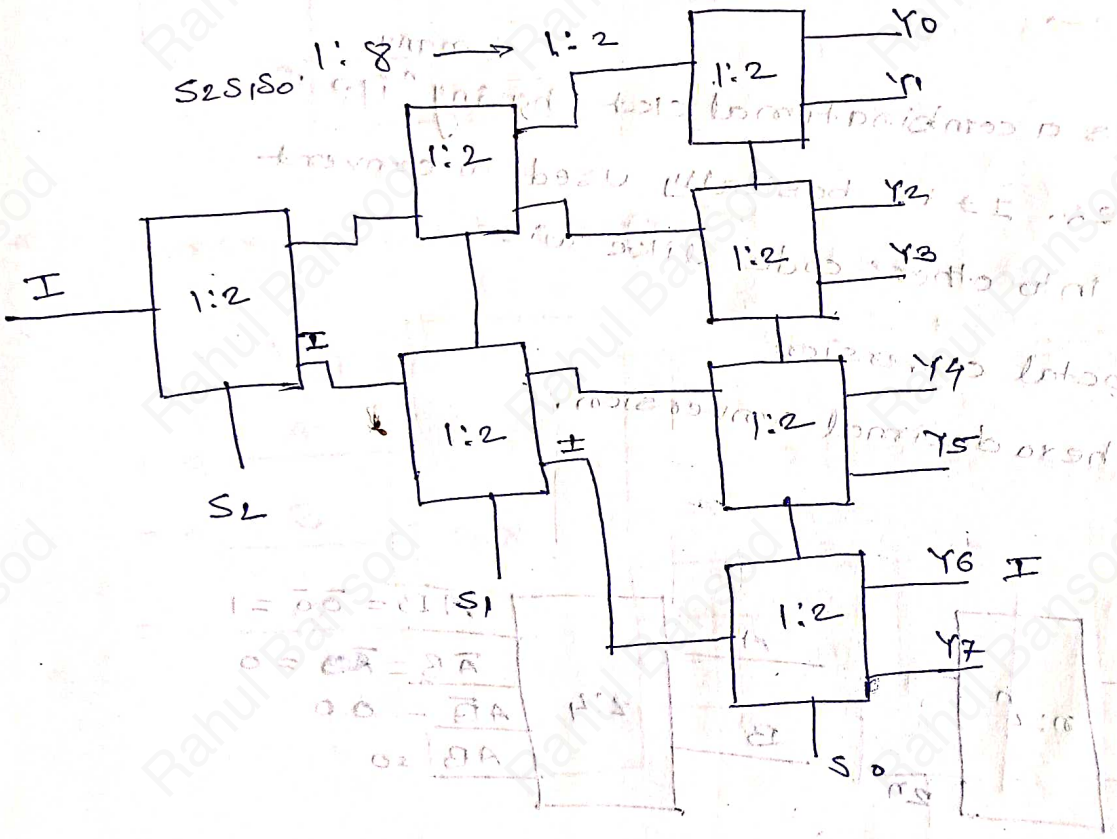
Higher order DeMUX using lower order DeMUX:-

$1:2^2$ $\quad 1:4 \xrightarrow{1:2} 2+1 = 2^2-1$

$1:2^3$ $\quad 1:8 \xrightarrow{1:2} 4+2+1 = 2^3-1$

$1:2^4$ $\quad 1:16 \xrightarrow{1:2} 8+4+2+1 = 2^4-1$

$1:2^n \xrightarrow{1:2} (2^n-1)$.



$1:16 \xrightarrow{1:4} 4+1 = 5$

$1:32 \xrightarrow{1:4} 8+2+1(1:2)$

$\downarrow$

$10(1:4)$

$1:32 \xrightarrow{1:8} 4+1(1:4)$

$\downarrow$

$4(1:8)+1(1:4)$

Lect-47

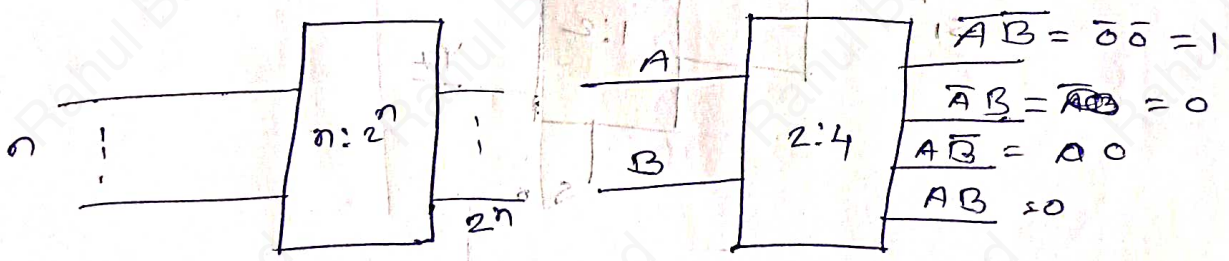
Decoder :→

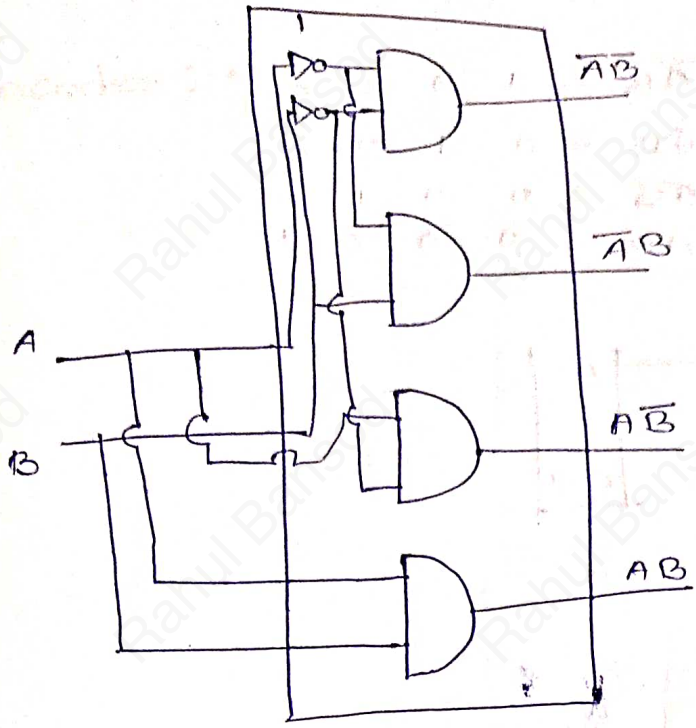
Decoder It is a combinational ckt having many i/p & many o/p lines. It is basically used to convert binary code into other code like wise

binary to octal conversion

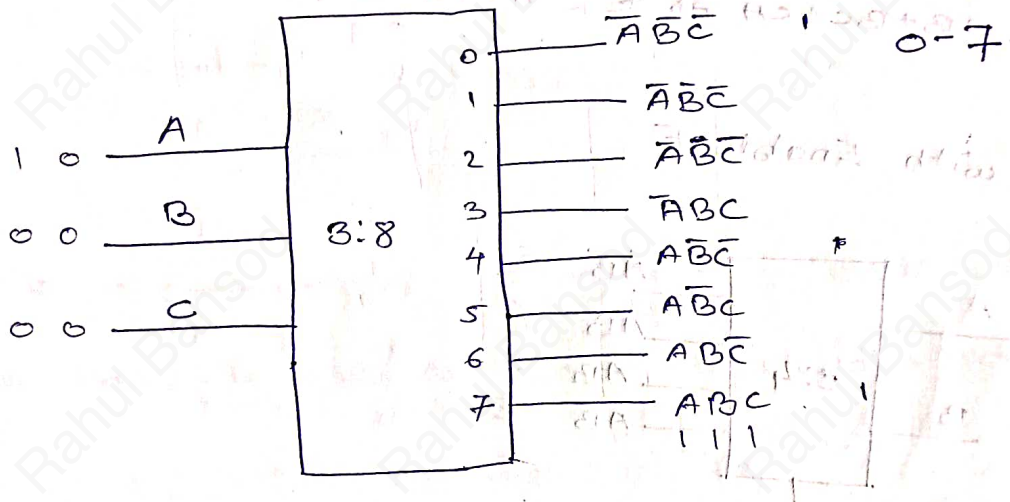
binary to hexadecimal conversion.

e.g:-





* binary to octal conversion



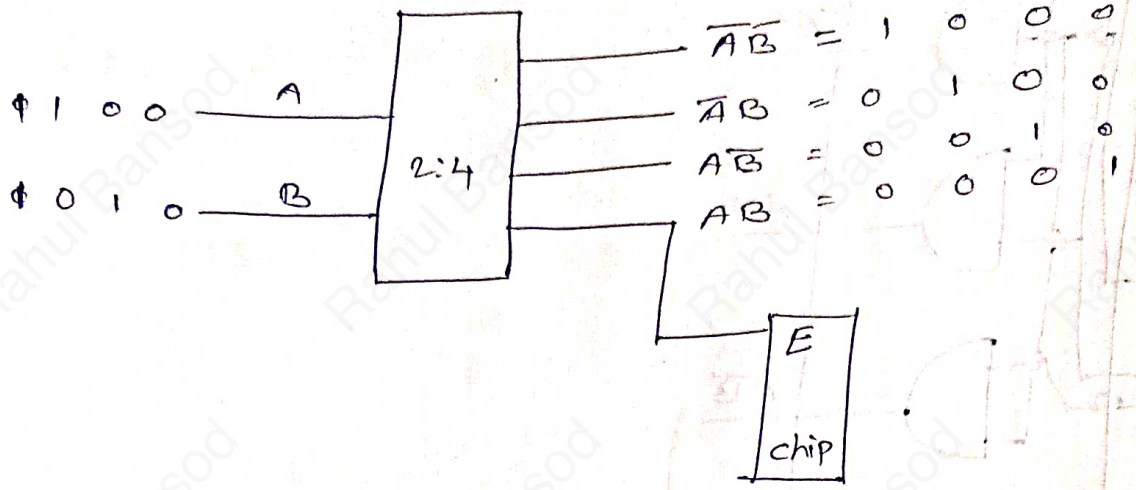
$(82)_8$ ×

$(110\ 011)_2$

(6 3)$_8$

010 111

(2 7)$_8$



Lect-48

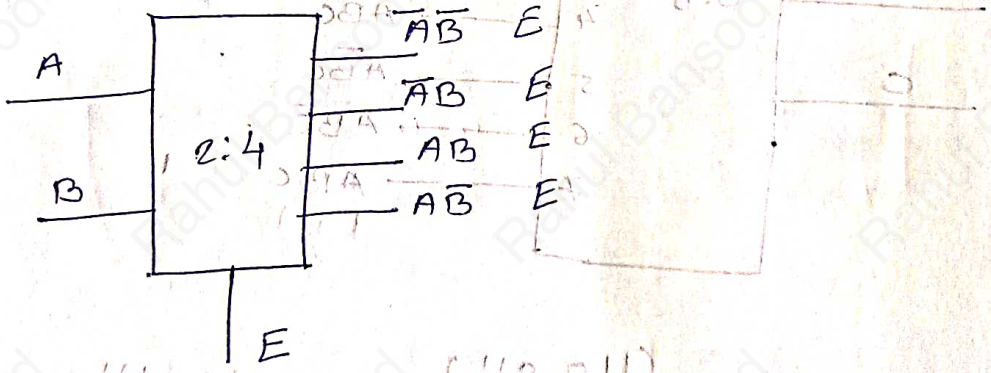
F(A,B,C)

Full adder →

$S = A \oplus B \oplus C = \Sigma(1,2,4,7)$ – SOP

$C = AB + BC + CA \Rightarrow \Sigma(3,5,6,7)$

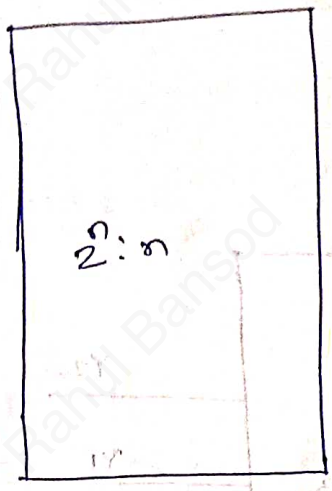
Decoder with Enable E

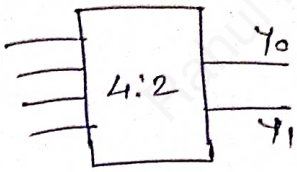


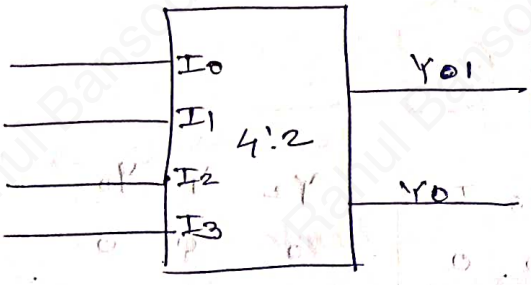
Lect-49

Imp

Encoder :→







- It is a combinational ckt having many inputs & many o/p lines.

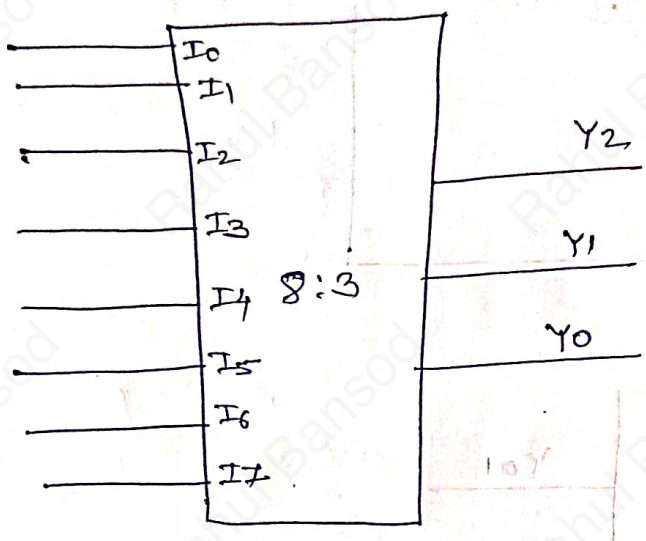
It is basically used to convert other codes into binary code.

I_0	I_1	I_2	I_3	Y_1	Y_0
1	0	0	0	0	0
0	1	0	0	0	1
0	0	1	0	1	0
0	0	0	1	1	1

$Y_1 = I_2 + I_3$

$Y_0 = I_1 + I_3$

*



I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$Y_2 = I_4 + I_5 + I_6 + I_7$

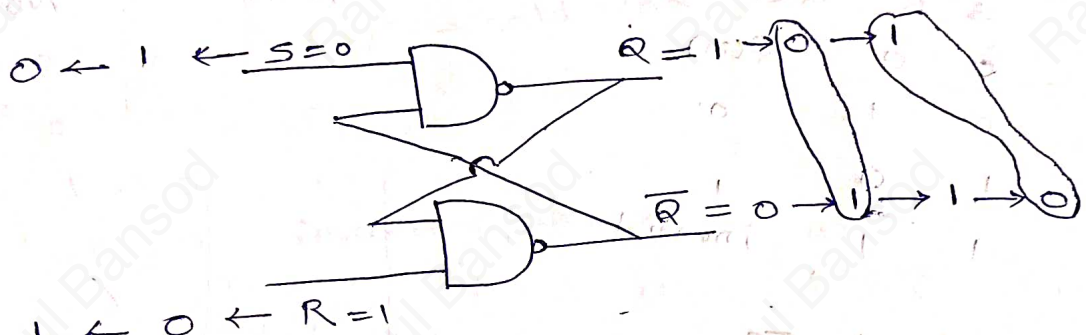
$Y_1 = I_2 + I_3 + I_6 + I_7$

$Y_0 = I_1 + I_3 + I_5 + I_7$

Lect- 50

Sequential circuits :-

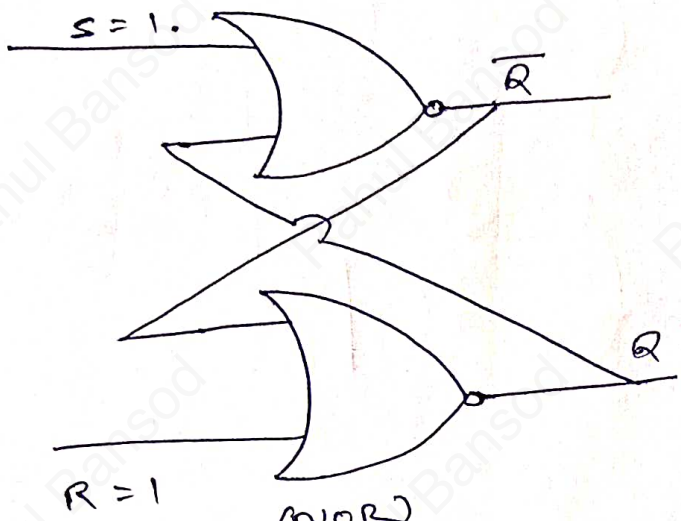
SR Latch :→



Nand

S	R	Q (n+1)
0	0	invalid state
0	1	1
1	0	0
1	1	Q (n) hold state

Lect-51



(NOR)

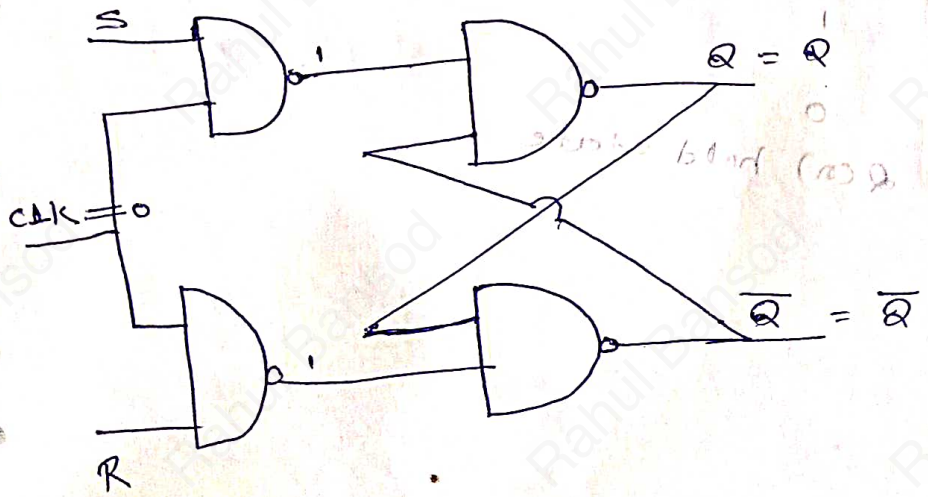
S	R	Q(n+1)
0	0	Q(n)
0	1	0
1	0	1
1	1	invalid

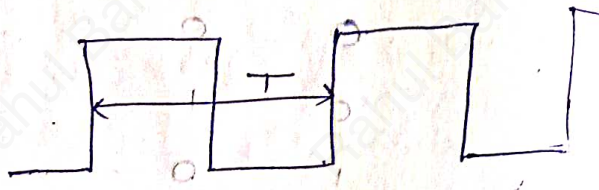
NAND is opposite of NOR latch

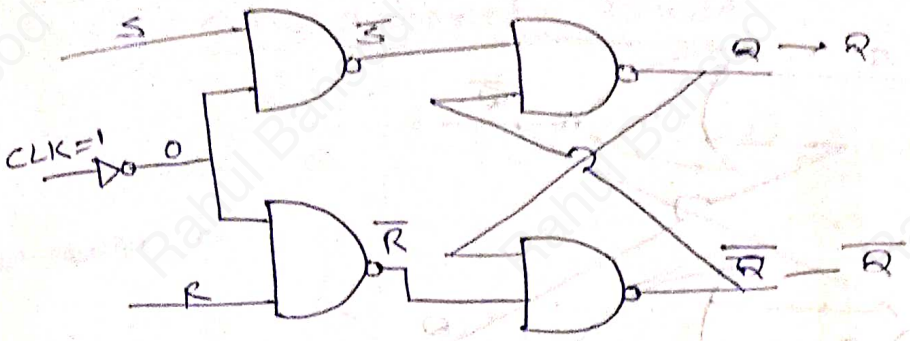
Lect-52

SR - flipflop

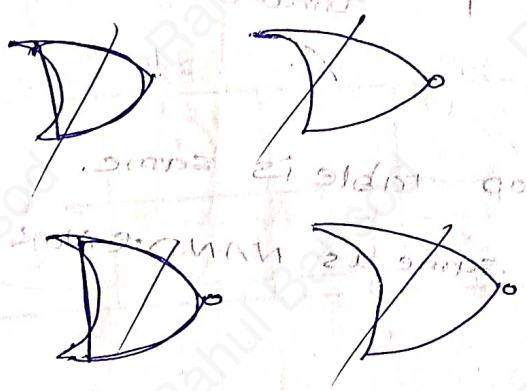
Using NAND

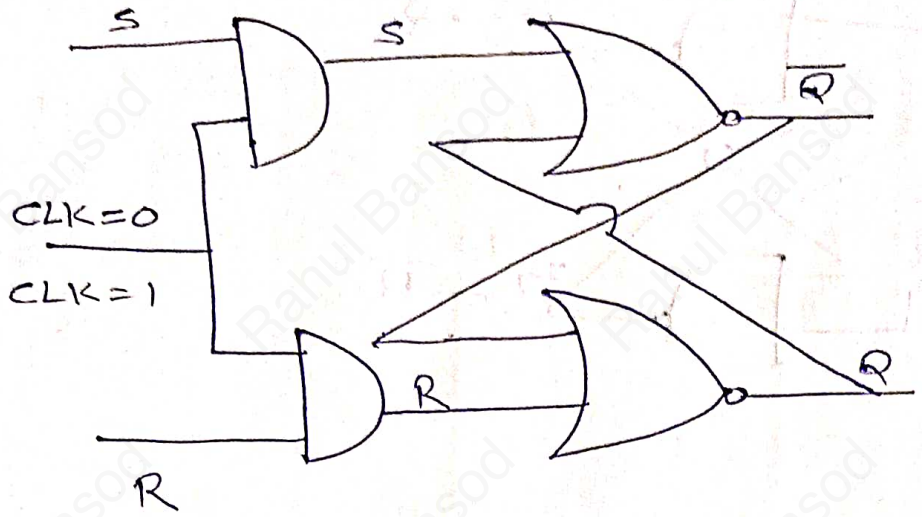






	S	R	Q(n+1)
CLK = Deactivate	X	X	Q(n)
CLK = 0			
CLK = activated	0	0	Q(n) → hold state
CLK = 1 = enable	0	1	0
"	1	0	1
"	1	1	invalid state
"			





CLK	S	R	Q(n+1)
=0	X	X	Q(n)
CLK =1	0	0	Q(n) → hold state
	0	1	0
	1	0	1
	1	1	Invalid state.

NAND & NOR flipflop Table is same.

NOR latch is also same as NAND & NOR f/f Table

Lect-53

Characteristic Table

	S	R	Q(n)	Q(n+1)
CLK = active	0	0	0	0
	0	0	1	1
	0	1	0	0
	0	1	1	0
	1	0	0	1
	1	0	1	1
	1	1	0	X
	1	1	1	X

Q(n+1)

	$\bar{R}\bar{Q}$	$\bar{R}Q$	$\bar{R}Q$	$R\bar{Q}$
$\bar{S}$		1		
S	1	1	X	X

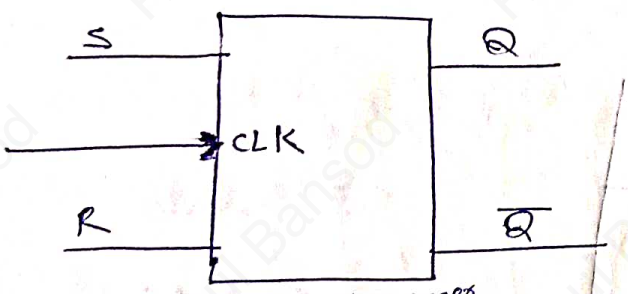
$Q(n+1) = \bar{R}Q + S$

$\boxed{Q(n+1) = S + \bar{R}Q(n)}$ — characteristic eqn of SR f/f

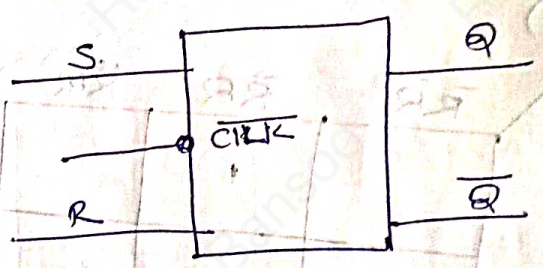
R(n)	Q(n+1)	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

S	R
0	0
1	0
X	0

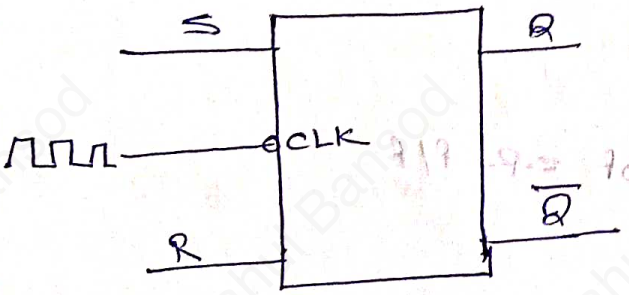
Lec#-54



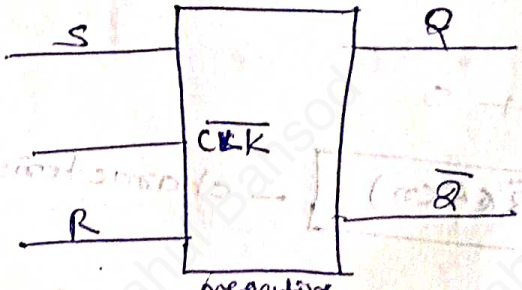
Positive level trigger



Negative

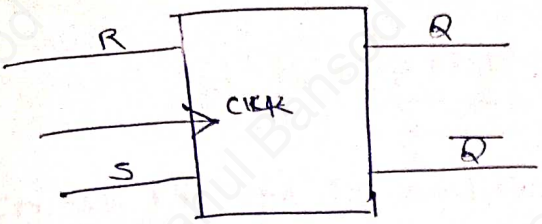


Negative

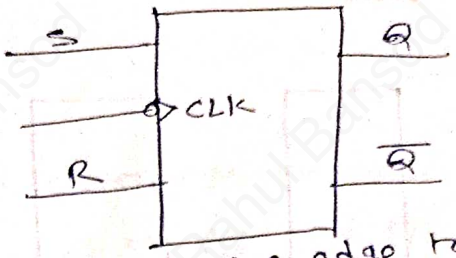


Negative

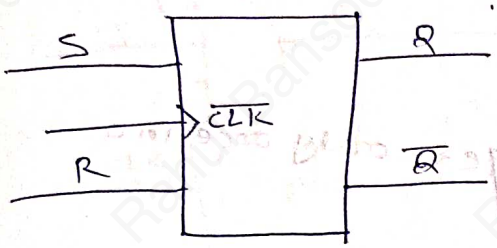
This all fours f/f are basically level trigger f/f.



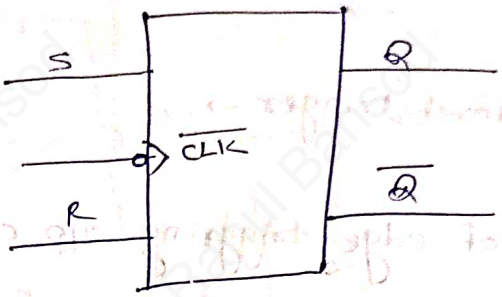
positive edge triggering



Negative edge trigger

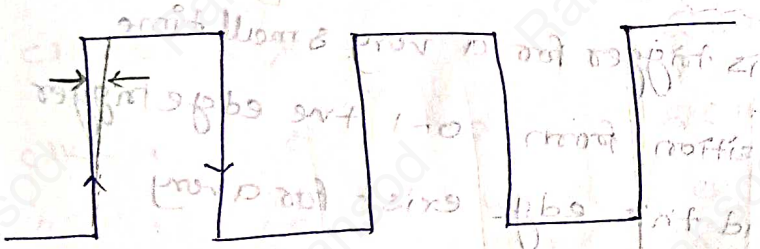


Negative



Negative

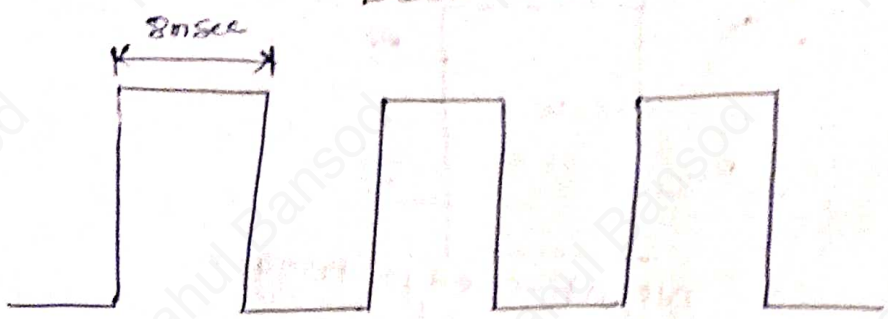
*



(0-1) → positive edge

1→0 → Negative edge

Lect - 55



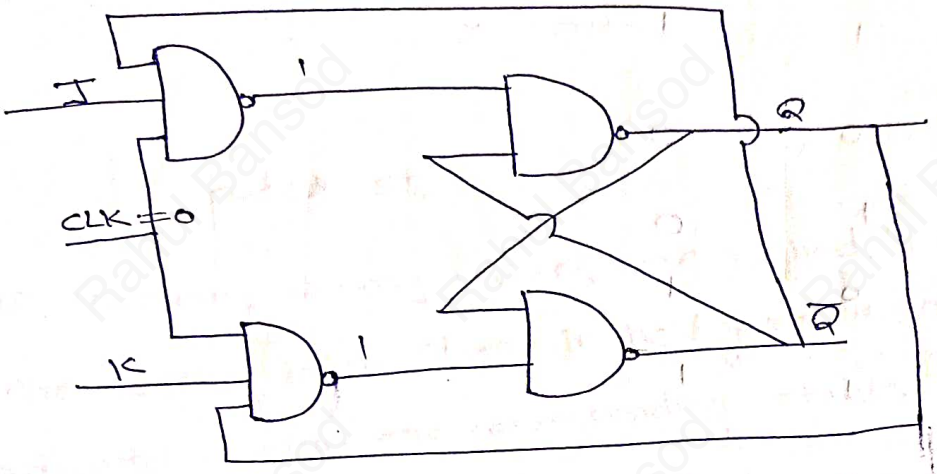
Positive level trigger →

- In case of edge triggring o/p can change only once in a single clock.
- In case of level triggring it can be possible that o/p can change more than once in a single clock (level is high or low for a larger time).
- In case of edge triggering ck is trigger for a very small time i.e. when clock is taking transition from 0-1 +ve edge trigg or 1-0 (-ve edge trigger). and this edge exist for a very small time i.e. the ck is trigger for a very small time
- In case of edge triggring ck is deactivated for clock value 1 or clock value 0.

Lect-56

J-K flip flop :→

- In SR f/f the i/p condition 11 is never use because it generates invalid o/p to shortout this problem of SR f/f JK f/f is made.



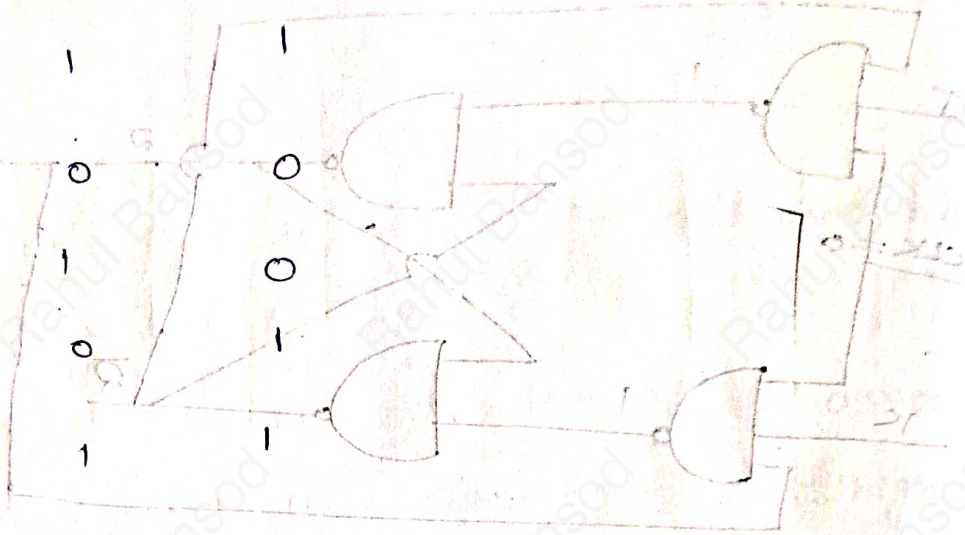
	J	K	Q(n+1)
CLK=0	X	X	Q(n)
CLK=1	0	0	Q(n) → hold state
" 1	0	1	0
" 1	1	0	1
" 1	1	1	$\overline{Q(n)}$ Toggle state

Lect# - 57

Characteristic Table

J	K	Q(n)	Q(n+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

CLK active



Q(n+1)	$\bar{K}\bar{Q}$	$\bar{K}Q$	KQ	$K\bar{Q}$
J	0	1 1	3	2
$\bar{J}$	1 4	1 5	7	1 6

$$\boxed{Q(n+1) = J\bar{Q}(n) + \bar{K}Q(n)}$$

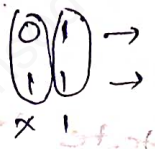
$1\,\bar{Q}(n) + 1\,Q(n)$

$= 1$

$Q(n+1) = \bar{Q}(n)$

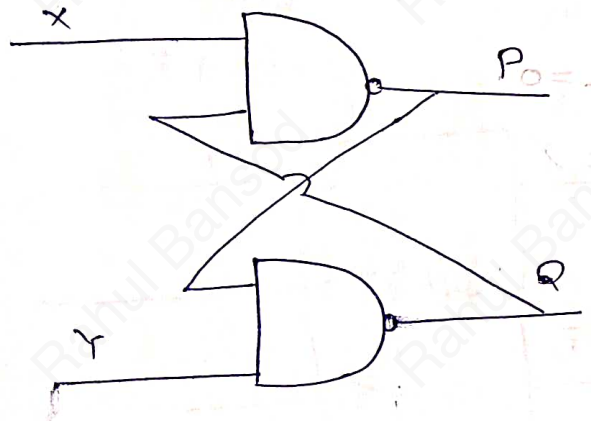
Excitation Table of JK F/F

Q(n)	Q(n+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0



Lect - 58

Q) The following binary values are applied to the x & y inputes of the NAND latch shown in the figure in the sequence indicated below the corresponding stable P, Q output will be



X=0, Y=1

X=0, Y=0

X=1, Y=1

a) P=1, Q=0, P=1, Q=0 or P=1, Q=0, P=0, Q=1

b) P=1 Q=0, P=0 Q=1 or P=1 Q=0, P=0 Q=1

✓ c) P=1 Q=0 P=1 Q=1 P=1 Q=0 or P=0 Q=1

d) P=1 Q=0, P=1 Q=1 P=1, Q=1.

soln:-

$X=0 \quad y=1, \quad S=0, \quad R=1 \longrightarrow P=1, Q=0$

$X=0, \quad y=0, \quad S=0 \quad R=0 \longrightarrow P=1, Q=1$

$X=1, \quad y=1, \quad S=1 \quad R=1 \longrightarrow P=1, Q=0$ or
$P=0, Q=1$

- hold state is valid only if the present o/p is a valid o/p [1,0 or 0,1].

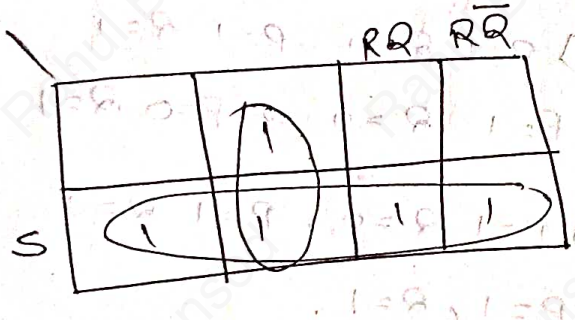
when present o/p state is invalid state is then after apply the i/p corresponding to hold state the o/p will change to Either 1, 0 valide state or 0, 1 valid state.

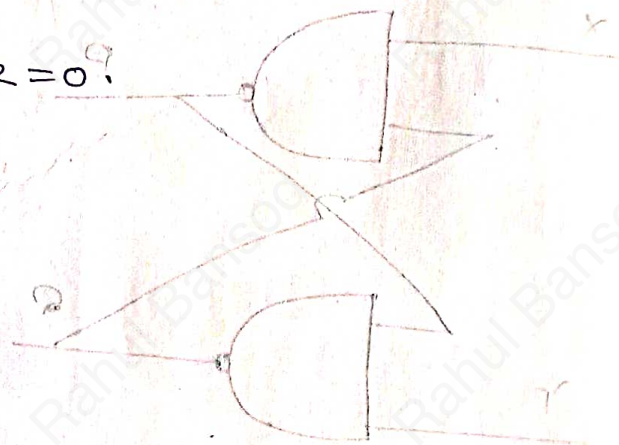
- it doesnot hold the invalid o/p state in next state.

- $Q(n+1) = S + \bar{R}Q(n)$

it is used only when $S \cdot R = 0$.

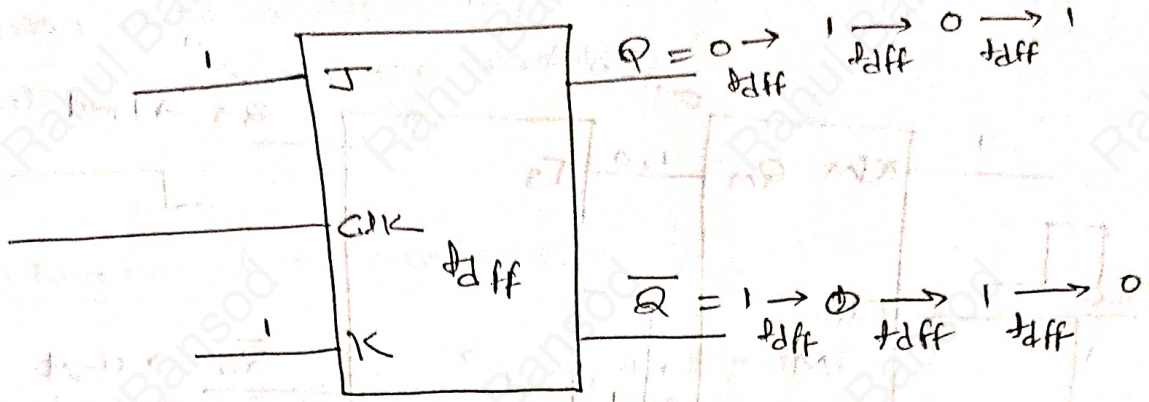
$Q(n+1) = 1 + \bar{1}Q(n) = 1$ ✗

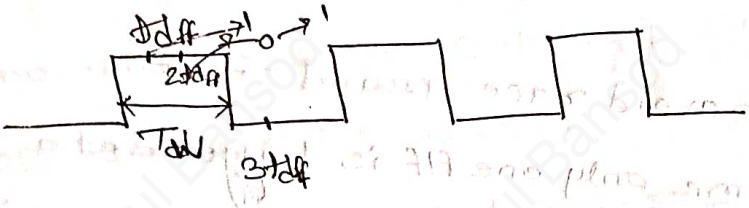


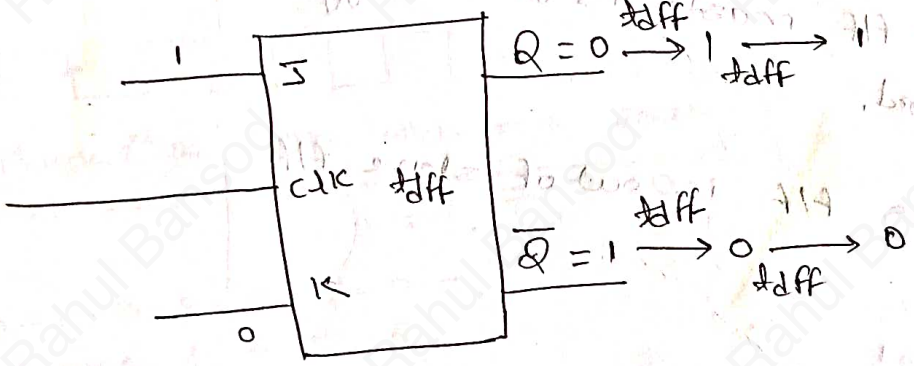


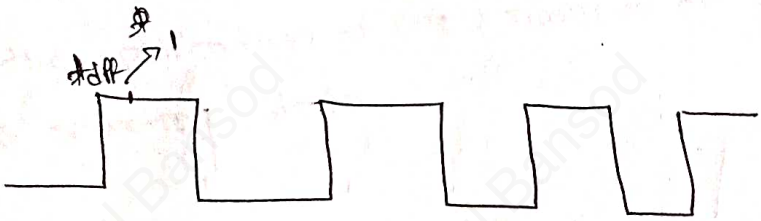
VOD - Lect. 29 - Lect 59

Race around condition





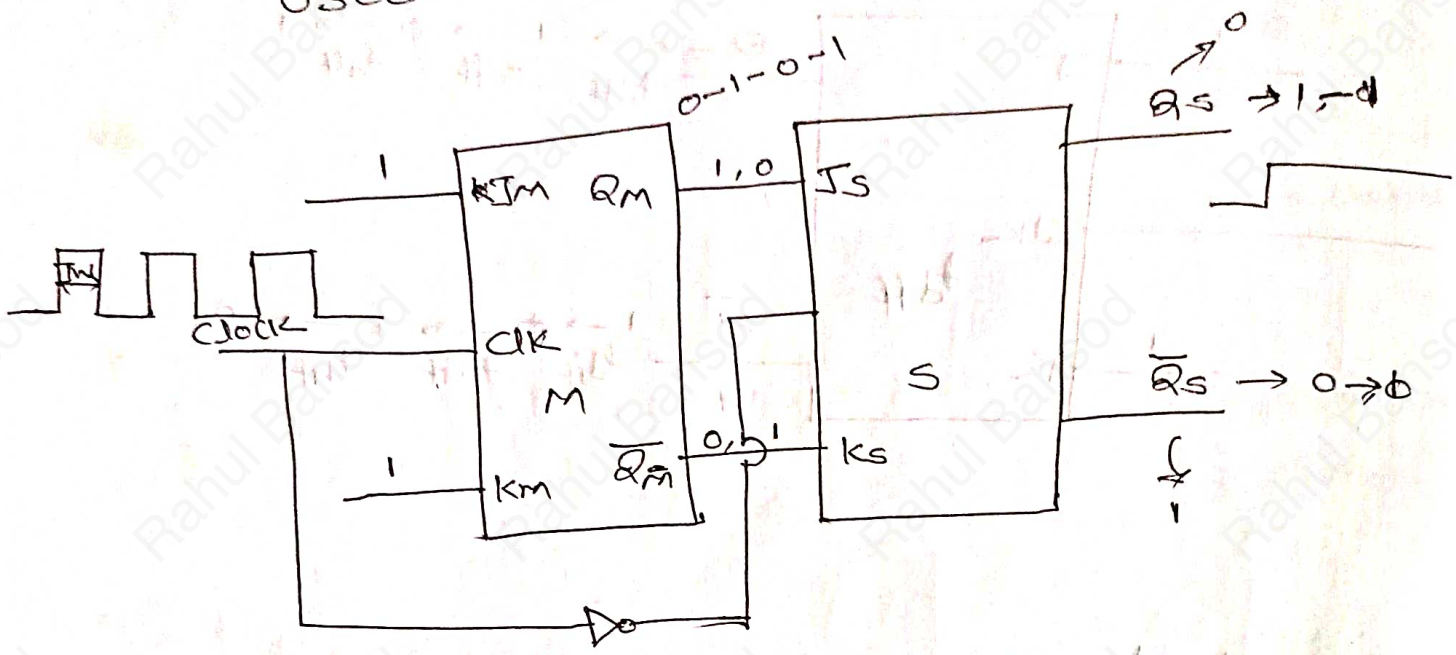




Lect-30 - (Lect-60)

ask in exam.

To avoid race around condition master-slave f/f is used



→ master slave f/f is used to avoid race around condition.

- In master slave f/f at a time only one f/f is triggered at a time
- In master slave f/f master is level triggered and slave is ~~ege~~ edge triggered.
- output of m-s f/f is out of slave f/f

Imp

Counters :-

- Counters are used to count number of clock pulses.
- It is also used for frequency division.
- It is also used for pulse streching.
-

Imp

MOD Number of the counter :-

0-1-3-2-5-7-0-1-3-2-5-7

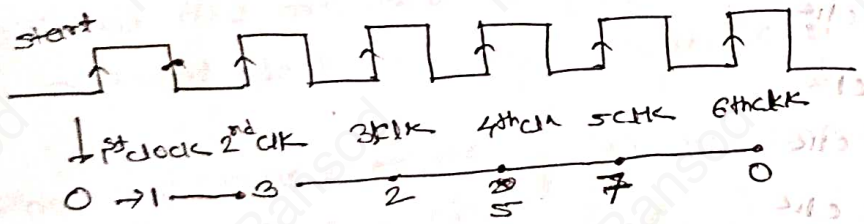
Start

Lect-61

MOD No: counter - 6

The no. of different state (distinct) in a counter is called as MOD number of the counter.

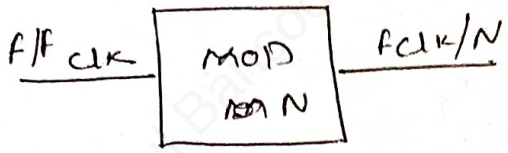
0-1-3-2-5-7 -0-1-3-2-5-7



0-1-3-2-5-7-0-

Start 1ck 2 3 4 5 6

- After the application of MOD number of clk pulses counter reaches to its starting state.

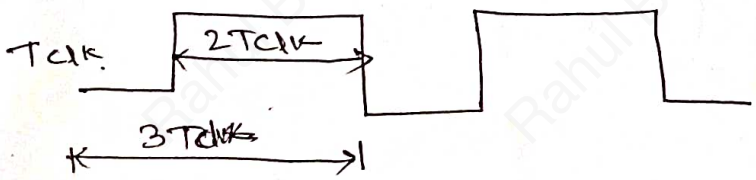


0-1-3-2-5-7-0-1-3-2-5-7

$Q_2 Q_1 Q_0$
000- 001-011-010-101-111

Q_2	Q_1	Q_0	
0	0	0	- 1 clk
0	0	1	- 2 clk
0	1	1	- 3 clk
0	1	0	- 4 clk
1	0	1	- 5 clk
1	1	1	- 6 clk
0	0	0	- 7 clk
0	0	1	- 8 clk
0	1	1	- 9 clk
0	1	0	- 10 clk
1	0	1	- 11 clk
1	1	1	- 12 clk

repeat

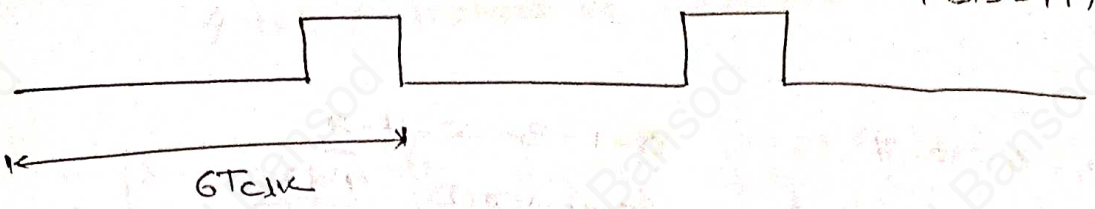


$T_{Q_0} = 3T_{clk}$

$f_{Q_0} = f_{clk}/3$

$= \frac{1}{T_{Q_0}} = \frac{1}{3T_{clk}}$

1 bit = 1 f/f

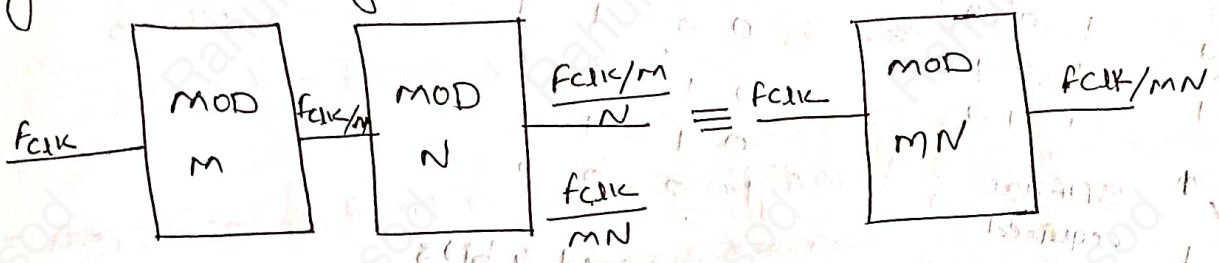


$T_{Q2} = 6T_{clK}$

$f_{Q2} = \frac{f_{clK}}{6}$

Lect- 62

e.g:- cascading MOD



Asynchronous counter	Synchronous counter
1) Different f/f's are supplied with Different clocks.	1) Different f/f's are supplied with same clock.
2) Either up sequence ~~or~~ or down sequence possible. (Fixed sequence < Either up / down)	2) any sequence is possible
3) Delay is high thats why frequency of operation is lesser/smaller	3) Delay is very small compare to asynchronous counter and thats why frequency of operation is higher side.
4) Decoding error (Essential hazzard) (transient error)	4) No decoding error.

e.g:-

0-1-3-4-5-7

Counter ①

MOD-6

0-1-3-5-7-8

Counter ②

4 bits

MOD-6

Lect-63

Q_2	Q_1	Q_0
0	1	1
1	0	0
1	0	1
1	1	0
1	0	1
1	1	1

0	0	0
0	1	1
1	0	0
1	0	1
1	1	1

3 f/f are required

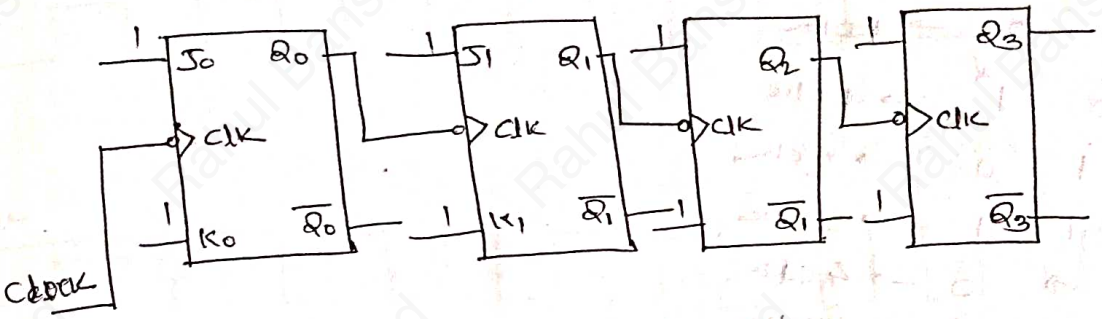
Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0

for 8 required 4 bits.

4 f/f are required

Lect-63

4 bit Asynchronus counter



$Q(n+1) = J\bar{Q}(n) + \bar{K}Q(n)$

$Q(n+1) = 1 \cdot \bar{Q}(n) + \bar{1}\,Q(n)$

$Q(n+1) = \bar{Q}(n) \rightarrow$ Toggle mode of operation

- ~~Asy~~ In case of Asyn. counter all the f/f's used are operated in toggel mode of operation.
- In case of Asyn. counter External clock is applied to one of the f/f and the clock i/p's ~~of~~ other f/f's are supplied by the output of previous f/f.
- Here, ~~A~~ respect to the ~~ckt~~ (All the f/f's used are negative as trigger
- Q_0 - toggles at every clock

  Q_1 - toggles when Q_0 (1-0)

  $Q_2 \rightarrow$ toggles when Q_1 goes from (1-0)

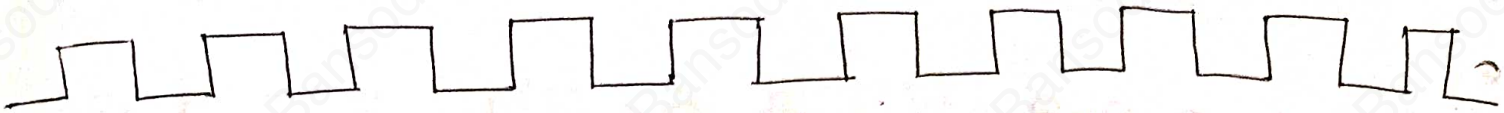
  $Q_3 \rightarrow$ toggles when Q_2 goes from (1-0)

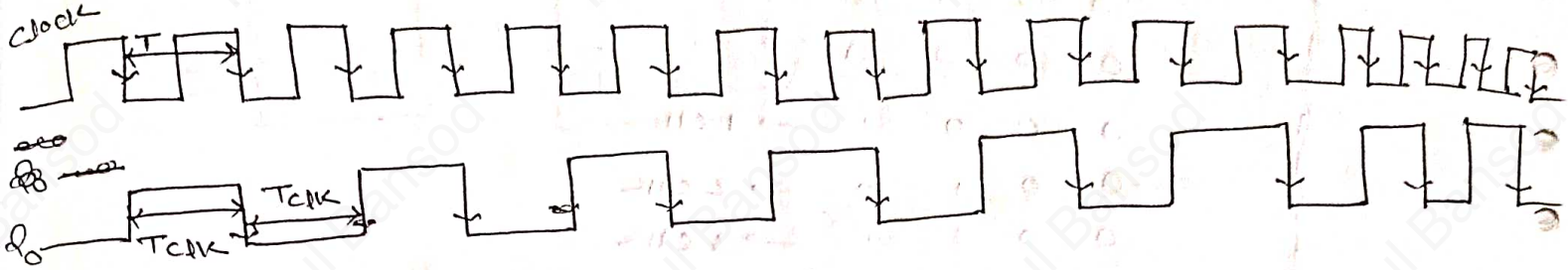
Lect - 64

Q_3	Q_2	Q_1	Q_0	
0	0	0	0	→ ~~1 clk~~
0	0	0	1	→ 1 clk
0	0	1	0	→ 2 clk
0	0	1	1	→ 3 clk
0	1	0	0	→ 4 clk
0	1	0	1	→ 5 clk
0	1	1	0	→ 6 clk
0	1	1	1	→ 7 clk
1	0	0	0	→ 8 clk
1	0	0	1	→ 9
1	0	1	0	→ 10
1	0	1	1	→ 11
1	1	0	0	→ 12
1	1	0	1	→ 13
1	1	1	0	→ 14
1	1	1	1	→ 15
0	0	0	0	→ 16

→ This is MOD - 16 up counter

Lect- 65

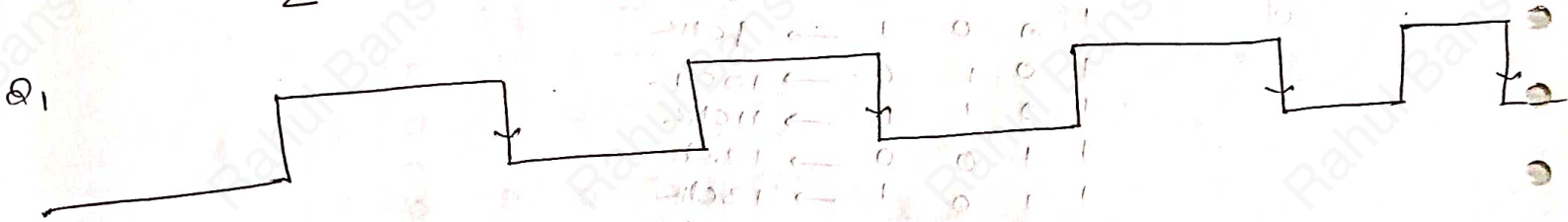




$T_0 = 2TCLK$

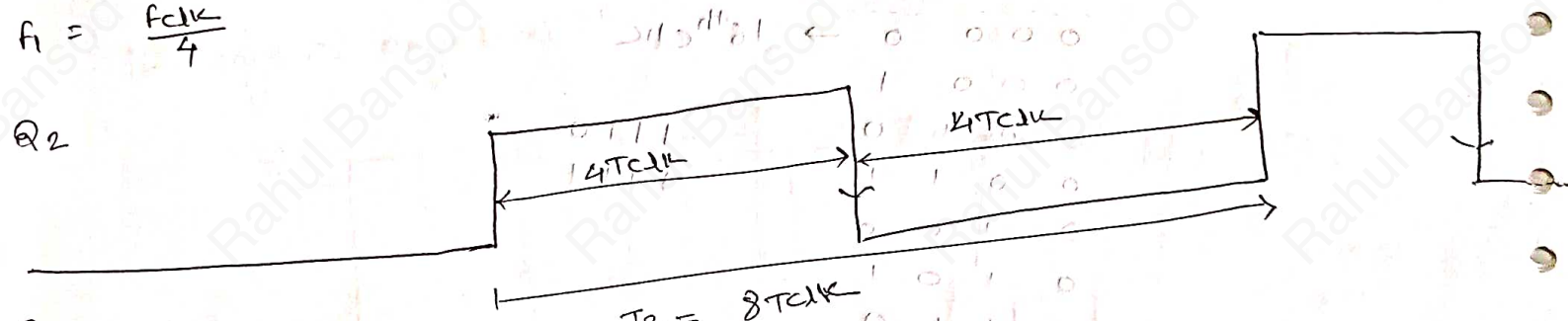
$f_0 = \frac{1}{T_0} = \frac{1}{2TCLK}$

$= \frac{fCLK}{2}$



$T_1 = 4\ TCLK$

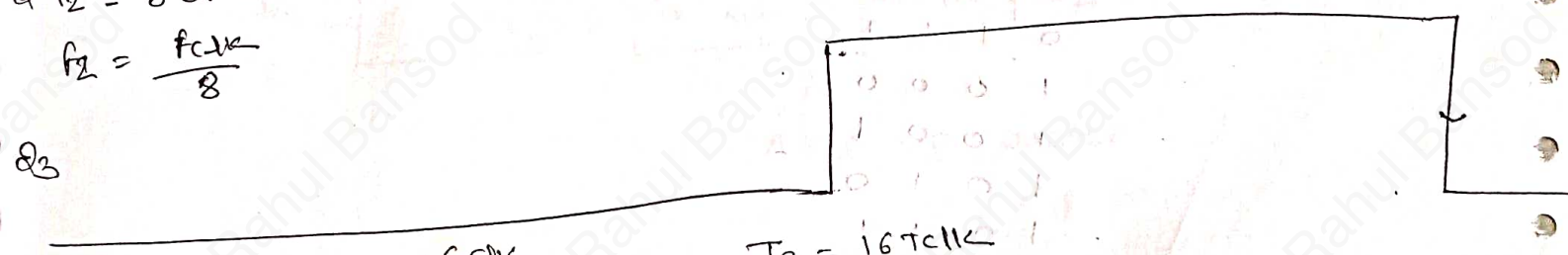
$f_1 = \frac{fCLK}{4}$



$T_2 = 8TCLK$

$T_2 = 8\ CLK$

$f_2 = \frac{fCLK}{8}$



$T_3 = 16\ CLK$

$f_3 = fCLK/16$

$T_3 = 16\ TCLK$

Lect - 66

~~Q_3 Q_2 Q_1 Q_0~~

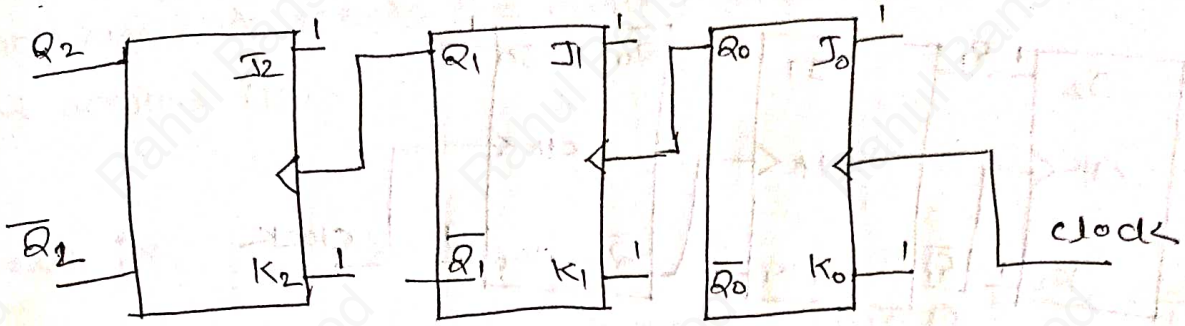
$f_{clk}/16$	$f_{clk}/8$	$f_{clk}/4$	$f_{clk}/2$	
Q_3	Q_2	Q_1	Q_0	
0	0	0	0	
0	0	0	1	→ 1 clk
0	0	1	0	→ 2 clk
0	0	1	1	→ 3 clk
0	1	0	0	→ 4 clk
0	1	0	1	→ 5 clk
0	1	1	0	→ 6 clk
0	1	1	1	→ 7 clk
1	0	0	0	→ 8 clk
1	0	0	1	→ 9 clk
1	0	1	0	→ 10 clk
1	0	1	1	→ 11 clk
1	1	0	0	→ 12 clk
1	1	0	1	→ 13 clk
1	1	1	0	→ 14 clk
1	1	1	1	→ 15 clk
0	0	0	0	→ 16th clk
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	

1110
1111

VOD – Lect-33

Asynchronous Counter

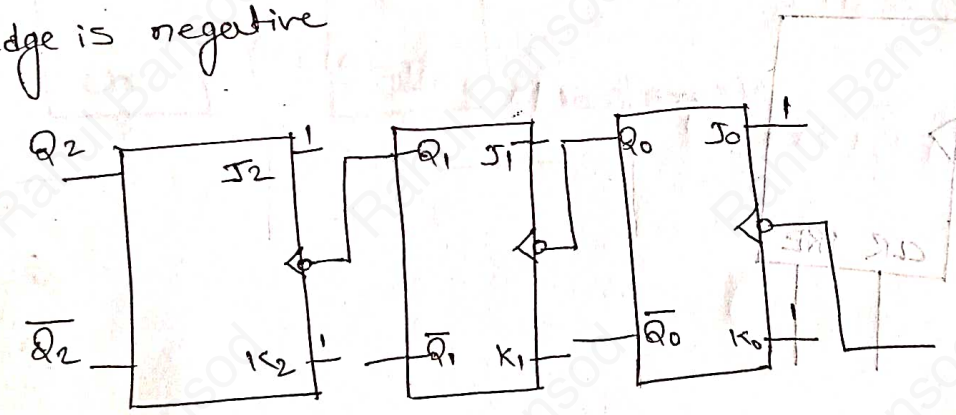
$Q_2 Q_1 Q_0$



Asyn. down counter.

Q_2	Q_1	Q_0	
0	0	0	
1	1	1	→ 1 clk
1	1	0	→ 2 clk
1	0	1	→ 3 clk
1	0	0	→ 4 clk
0	1	1	→ 5 clk
0	1	0	→ 6 clk
0	0	1	→ 7 clk
0	0	0	→ 8 clk
1	1	1	→ 9th clk

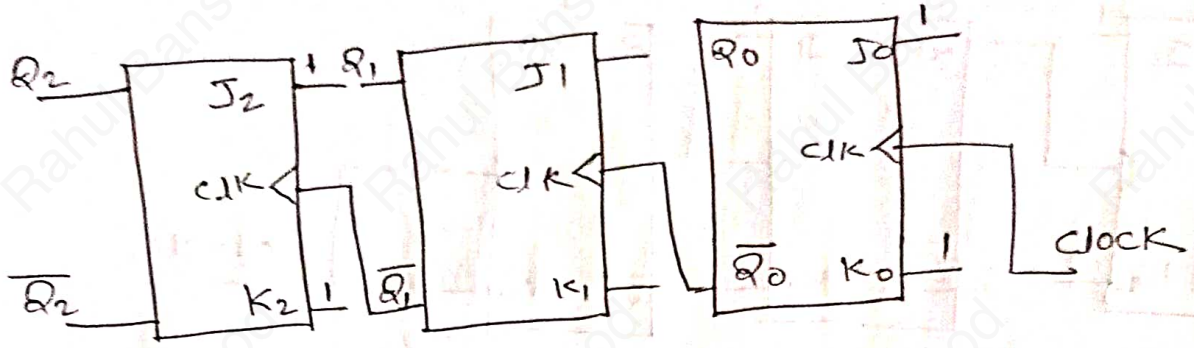
if edge is negative



0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

Asyn. up counter

if suppose



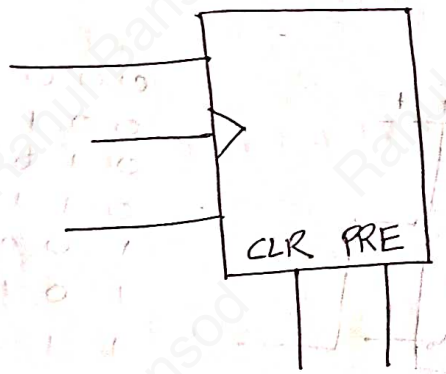
~~Q2 Q1 Q0~~
~~0 0 0~~

$\overline{Q_0} \rightarrow 0-1$

	Q_2	Q_1	Q_0	$\overline{Q_0}$	$\overline{Q_1}$	$\overline{Q_2}$
	0	0	0	1		
CLK	0	0	1	0		

Lect-34

Clear i/p :- (Asynchronous i/p)

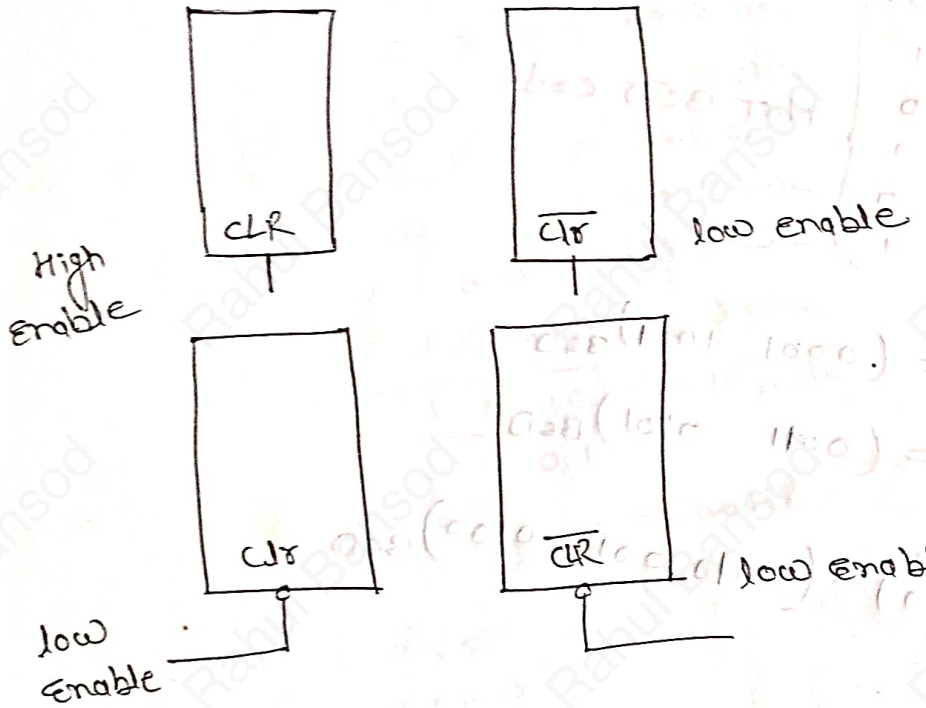


what is clear input (Asyn. clear i/p)

:- This is in general asynchronous in nature, when this pin get activated, it resets the output irrespective of clock i/p and applied i/p.

Preset i/p

it is in general Asynchronous in nature, when this pin gets activated it sets the output irrespective of clock i/p & applied i/p.



BCD counter :→

Binary coded Decimal (BCD)

(BCD is UP counter)

	Binary
0 –	0000
1 –	0001
2 –	0010
3 –	0011
4 –	0100
5 –	0101
6 –	0110
7 –	0111
8 –	1000
9 –	1001

Invalid BCD code

10 –	1010
11 –	1011
12 –	1100
13 –	1101
14 –	1110
15 –	1111

NOT BCD code

e.g:-

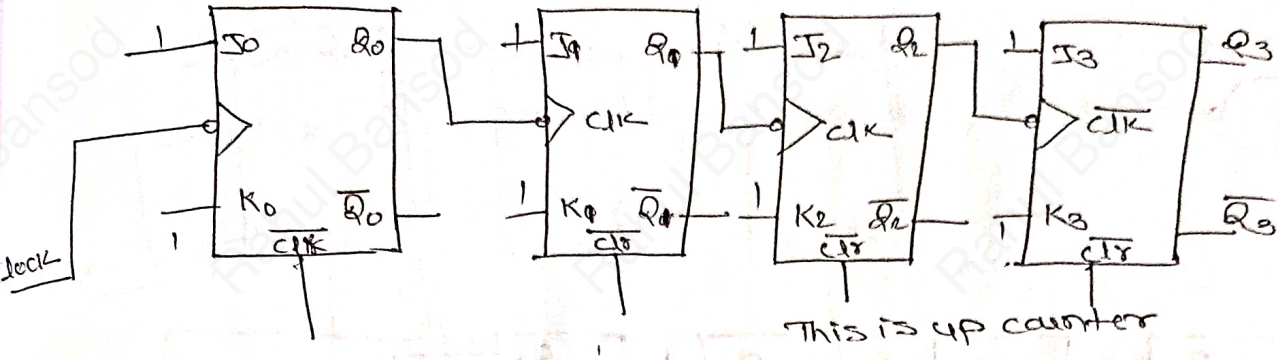
$(19)_{10} = (10011)_2 = (0001\ 1001)_{BCD}$

$(35)_{10} = (\overset{32\,16\,8\,4\,2\,1}{100011})_2 = (0011\ 0101)_{BCD}$

$(234)_{10} = (\overset{128\,64\,32\,16\,8\,4\,2\,1}{11\ 1010\ 10}) = (0010\ 0011\ 0100)_{BCD}$

~~(10)BCD~~

$(10)_{10} = (0001\ 0000)$



This is up counter

MSB LSB

Fclk/2

Q_3	Q_2	Q_1	Q_0	
0	0	0	0	
0	0	0	1	→ 1 clk
0	0	1	0	→ 2 clk
0	0	1	1	→ 3 clk
0	1	0	0	→ 4 clk
0	1	0	1	→ 5 clk
0	1	1	0	→ 6 clk
0	1	1	1	→ 7 clk
1	0	0	0	→ 8 clk
1	0	0	1	→ 9 clk
1	0	1	0	→ 10th clk
0	1	0	1	

clr pic activated

$Q_3 = 1$

$Q_2 = 0$

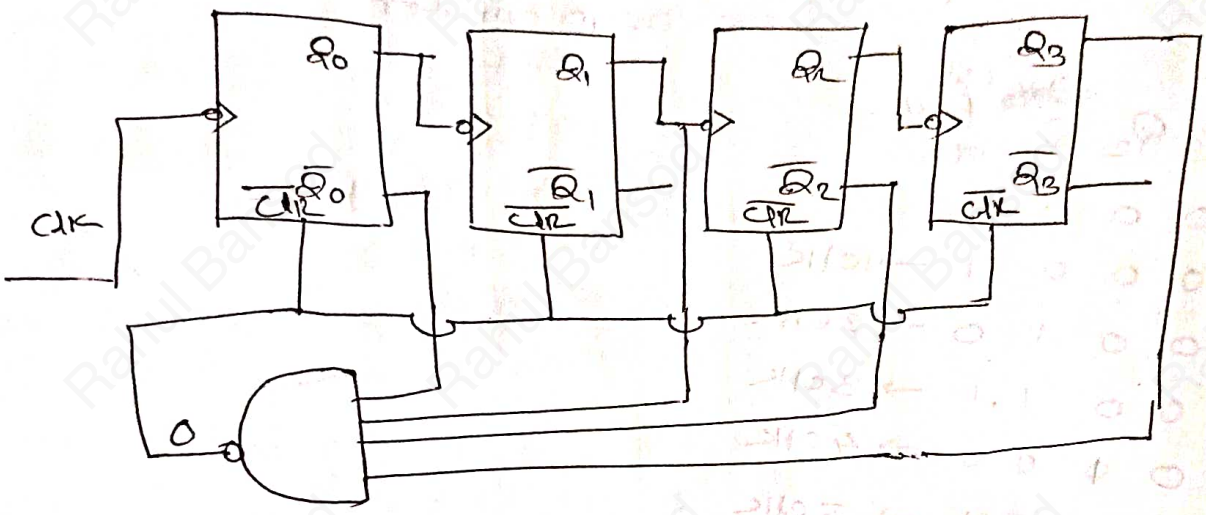
$Q_1 = 1$

$Q_0 = 0$

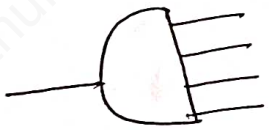
1010

$Q_3 \bar{Q}_2 Q_1 \bar{Q}_0$ ⟹ sop

Lect - 35



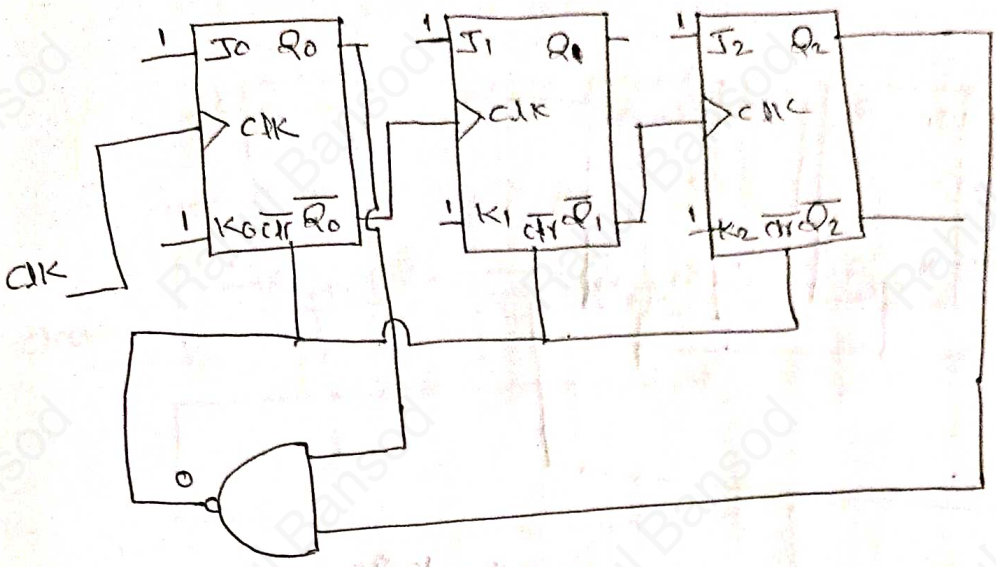
if CLR



- ~~all~~ BCD counter is a MOD 10 counter But all ~~BCD counter are not~~ MOD 10 counter are not BCD counter.

- BCD ~~MOD~~ counter ~~is~~ MOD 10 counter But vice versa not true.

Q)



a) MOD-6 up counter

b) MOD-5 down counter

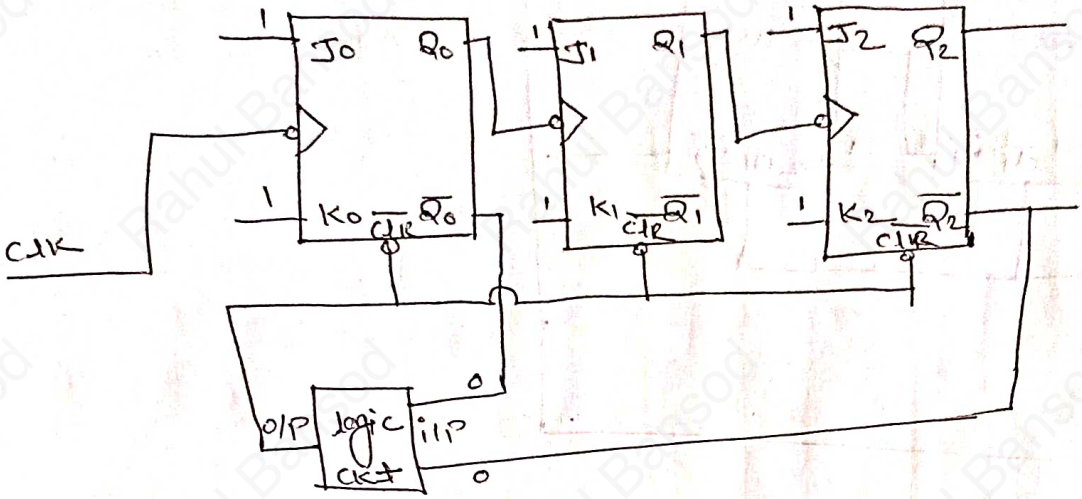
✓ c) MOD-5 up counter

D) MOD-6 down counter.

Sol:-

MSB		LSB	
Q_2	Q_1	Q_0	
0	0	0	
0	0	1	→ 1 clk
0	1	0	→ 2 clk
0	1	1	→ 3 clk
1	0	0	→ 4 clk
1	0	1	→ 5 clk
0	0	0	

Q)



This ~~ckt~~ counter is used as MOD-5 up counter, then the logic circuit is

a) 2 - i/p OR Gate 0+0 = 0

b) 2 - i/p AND Gate 0.0 = 0

c) 2 - i/p NOR Gate 1 ×

d) 2 - i/p NAND Gate 1 ×

up - counter

MSB Q_2	Q_1	LSB Q_0	
0	0	0	-
0	0	1	-
0	1	0	-
0	1	1	-
1	0	0	-
1	0	1	

$\overline{Q_2} = 0$

$\overline{Q_0} = 0$

Step :- identify LSB MSB bit

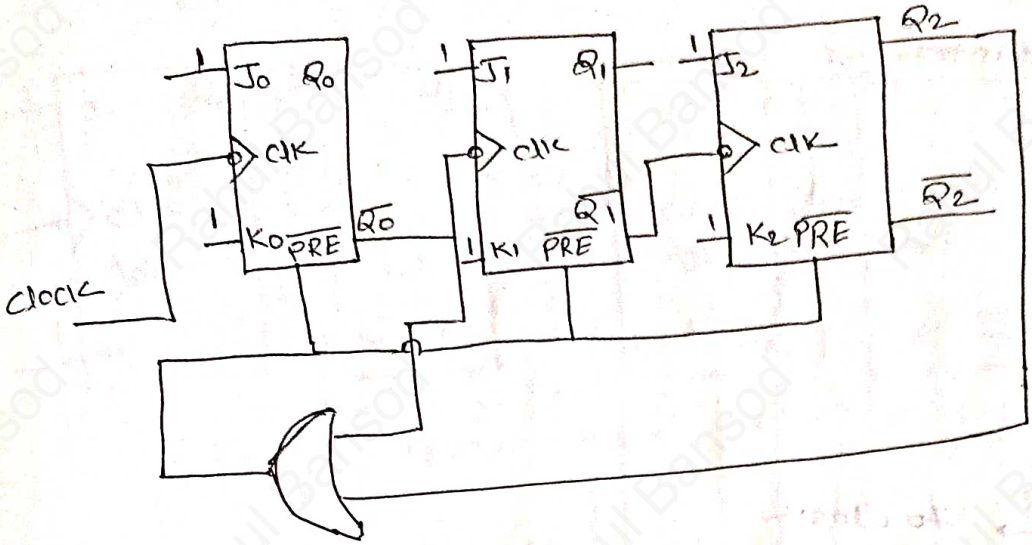
identify up/down counter

identify MOD

identify i/p of logic ckt

Lect - 36

Q)



The given counter is

a. MOD - 5 down counter

✓ b. MOD - 4 - down counter

c. MOD - 6 down counter

d. MOD - 5 UP counter

Sol:-

$Q_2 = 0 \rightarrow$

$\overline{Q_0} = 0 \rightarrow Q_0 = 1$

Q_2	Q_1	Q_0
0	0	0
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1

(4 MOD - down counter)

Q) we have a MOD 32 down counter its starting state is $(3)_{10}$, after application of 70 clock pulses what is the state of the counter.

a) $(30)_{10}$

b) $(29)_{10}$

c) $(9)_{10}$

d) $(27)_{10}$

Sol^n :→ $(3)_{10} \longrightarrow$ 70 clock

$$\underset{\text{clk}}{32} \cdot - (3)_{10} \xrightarrow[32\text{clr}]{} (3)_{10} \xrightarrow{6 \text{ clock}}$$

$2 \times 32 + 6$

$m \times 32$

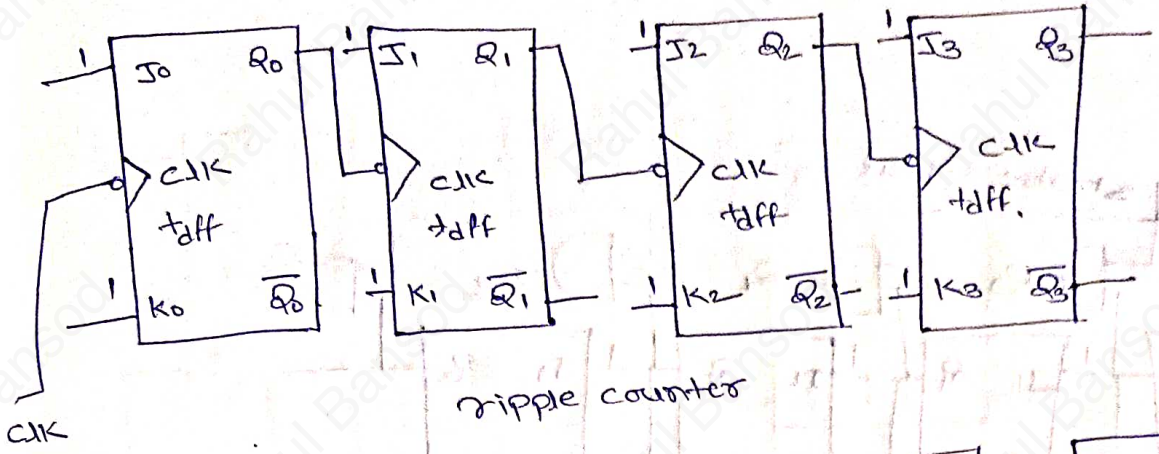
$$3 \xrightarrow[1\text{clk}]{} 2 \underset{2\text{clk}}{-} 1 \underset{3\text{clk}}{-} 0 \xrightarrow[4\text{clk}]{} (31)_{10} \longrightarrow 30 \longrightarrow (29)_{10}$$

$(00000) \longrightarrow (11111)$

$2^5 - 1 = 31$

Lect- 37

Q)



ripple counter

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1

$t = 0$

Total delay = $n\, t_{dff}$

Q_3	Q_2	Q_1	Q_0
0	0	1	1
0	0	1	0
0	1	0	0

t_{dff} → 0011 at $t = t_{dff}$

t_{dff} → 0010 at $t = 2t_{dff}$

at $t = 3t_{dff}$

decoding error / Transient error

correct/ for garantied operation

$T_{CLK} \geq n\, t_{dff}$

$\frac{1}{T_{CLK}} \leq \frac{1}{n\, t_{dff}}$

$\boxed{f_{CLK} \leq \frac{1}{n\, t_{dff}}}$

$\boxed{(f_{CLK})_{max} = \frac{1}{n\, t_{dff}}}$

(t_{dff}) CLK

0	1	1	1
0	1	1	0
0	1	0	0
0	0	0	0
1	0	0	0

$t = t_{dff}$

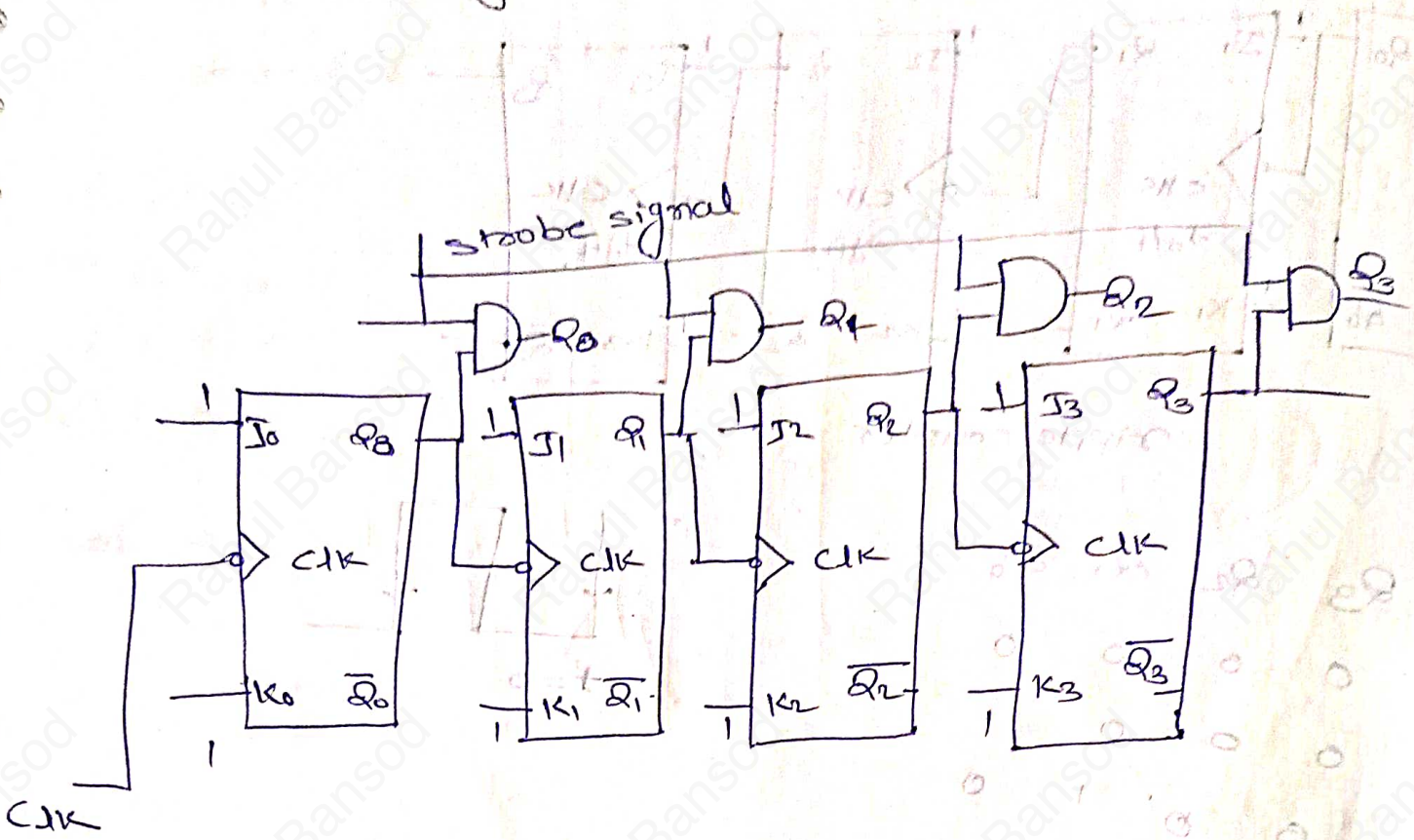
$t = 2t_{dff}$

$t = 3t_{dff}$

$t = 4t_{dff}$

decoding error / Transient error

To avoid decoding error strobe signal is used.

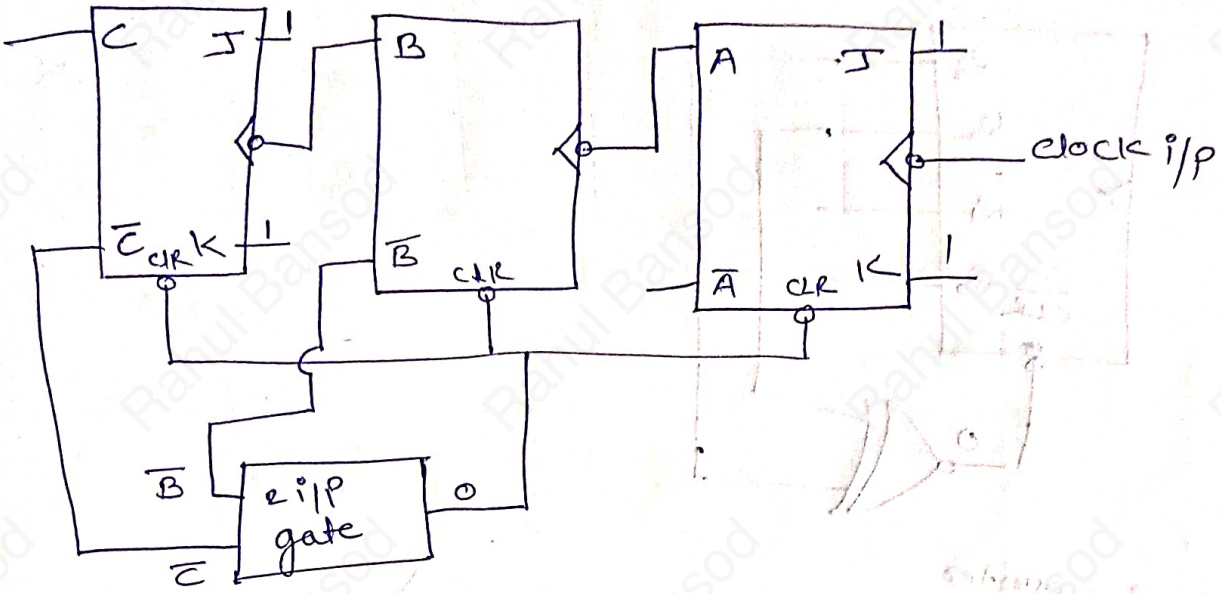


for proper operation $t_{clk} \geq (n t_{dff} + t_s)$

$$f_{clk} \leq \frac{1}{(n t_{dff} + t_s)}$$

$$\boxed{(f_{clk})_{max} = \frac{1}{n t_{dff} + t_s}}$$

Q) In the modulus - 6 ripple counter shown in the fig. The output of 2-input gate is used to clear the J-K flip-flop.



2 i/p gate is...

a) NAND X

b) NOR X

c) OR ✓

d) AND X

sol:-

C	B	A
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0

$\overline{B} = 0$

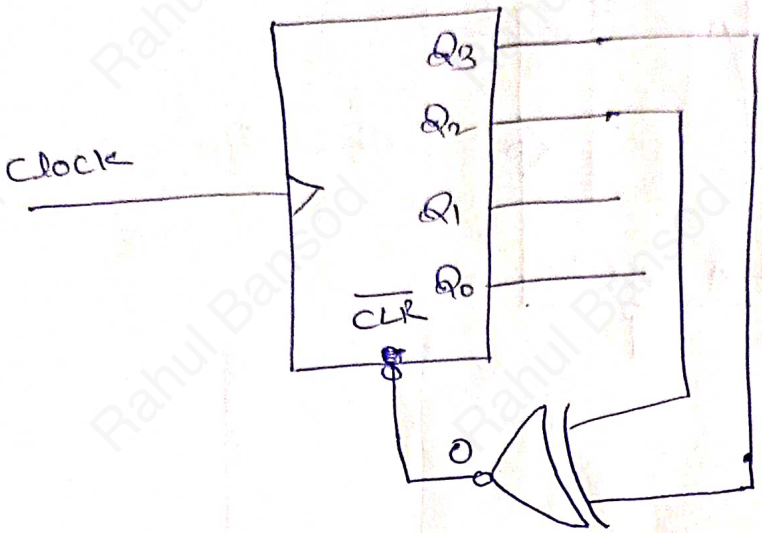
$\overline{C} = 0$

$\overline{C} \cdot \overline{B}$

$0 \cdot 0 = 0$

Lect - 38

Q) The figure shows a binary counter with synchronous clear i/p with the decoding logic shown the counter work as a –



a) MOD - 2 counter

b) MOD - 4 counter

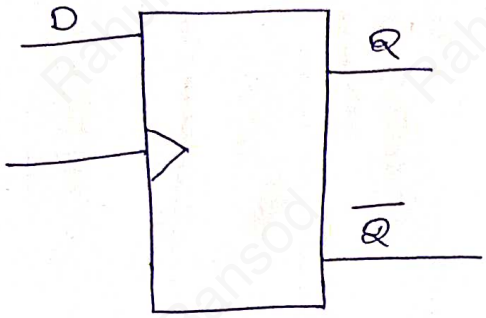
✓ c) MOD - 5 counter

d) MOD - 6 counter

Sol^n:-

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0

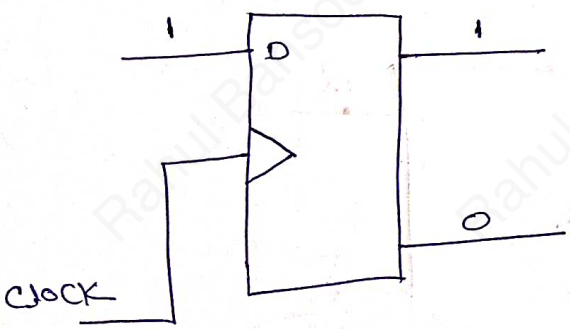
D - flip flop



D	Q(n)	Q(n+1)
0	0	0
0	1	0
1	0	1
1	1	1

Q(n+1)	$\overline{Q}(n)$	Q(n)
$\overline{D}$		
D	1	1

$Q(n+1) = D$



Excitation

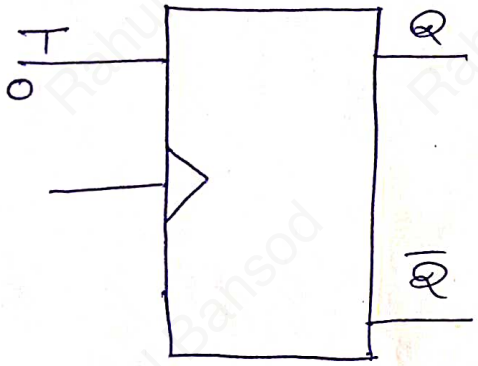
Q(n)	Q(n+1)	D
0	0	0
0	1	1
1	0	0
1	1	1

T- flip flop

T	Q(n)	Q(n+1)
0	0	0
0	1	1
1	0	1
1	1	0

XOR ka opposite

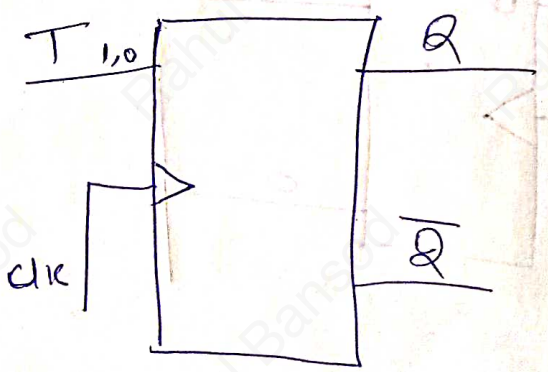
same - 0
different - 1



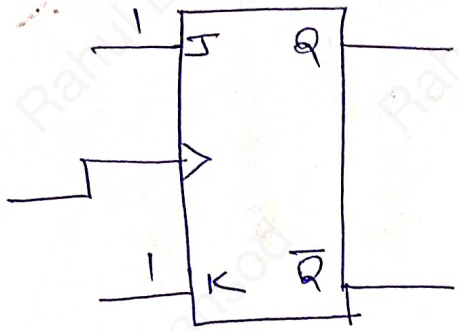
$Q(n+1) = T \oplus Q(n)$ Toggle mode of operation

Excitation table

Q(n)	Q(n+1)	T
0	0	0
0	1	1
1	0	1
1	1	0

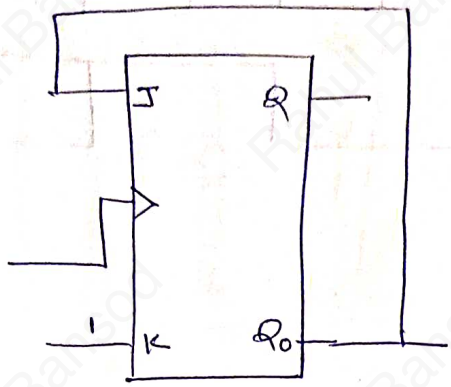


Toggle mode of operation



$Q(n+1) = J\overline{Q} + \overline{K}Q$

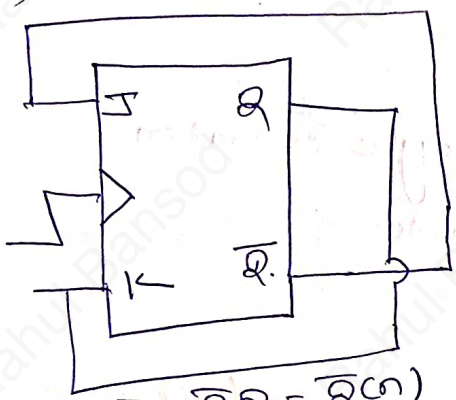
$Q(n+1) = 1\overline{Q} + 1Q = \overline{Q}(n)$



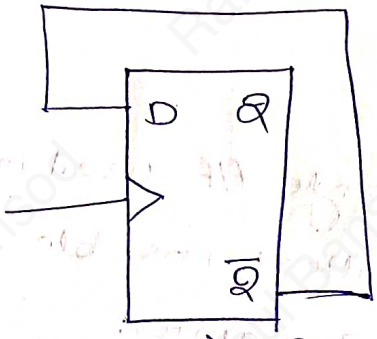
$Q(n+1) = J\overline{Q} + \overline{K}Q$

$= \overline{Q}.\overline{Q} + 1Q$

$Q(n+1) = \overline{Q}(n)$

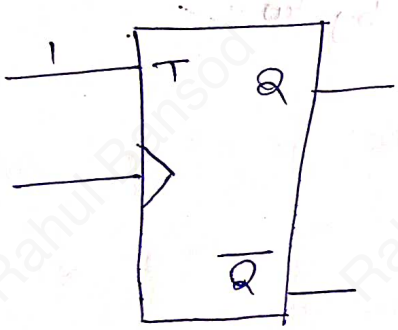


$Q(n+1) = \overline{Q}\,\overline{Q} + \overline{Q}Q = \overline{Q}(n)$



$Q(n+1) = D$

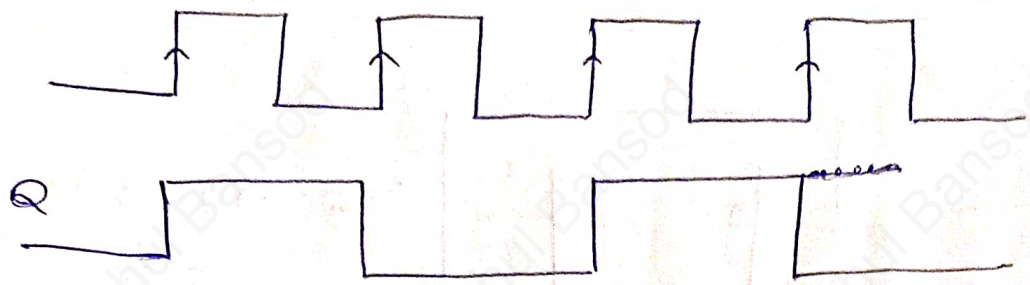
$= \overline{Q}(n)$

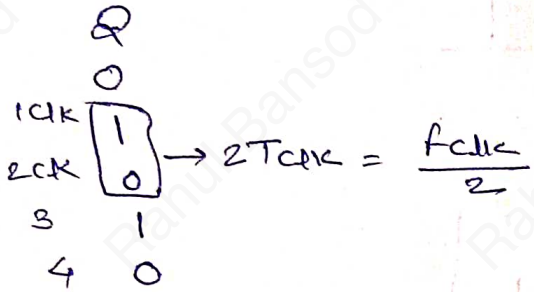


$Q(n+1) = T \oplus Q(n)$

$= 1 \oplus Q(n)$

$Q(n+1) = \overline{Q(n)}$



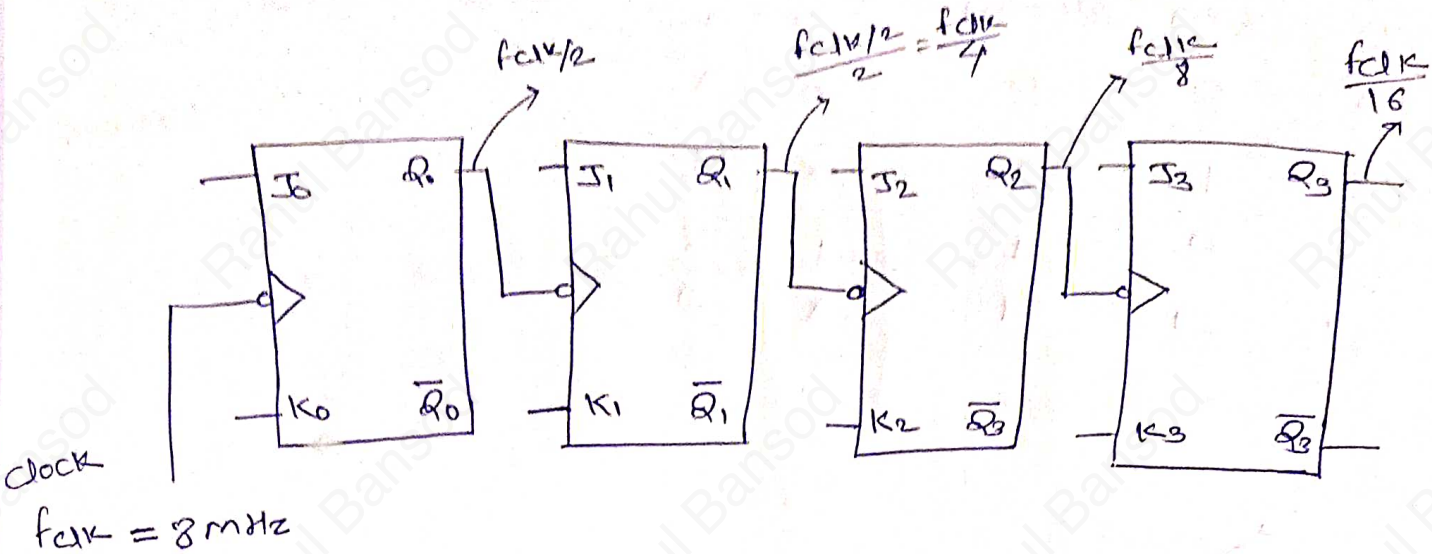


Note:- ~~Ano~~ A single f/f used in toggle mode of operation is the smallest possible counter i.e. MODE-2 counter.

~~and~~

- when a single f/f is used in toggle mode of operation then i/p clock frequency is divided by ~~two~~ 2 at a output of bad f/f.

Lect - 39



$f_{clk} = 8\,MHz$

Note:-

Conversion of one f/f into another f/f :→

1) write down the characterstic table of desired f/f at input side.

2) write down the exitation table of existing (available) f/f at o/p side

3) solve the truth table and implement it.

e.g:- JK TO D → desired f/f
↙ available

$Q(n)$

step ①

D	Q(n)	Q(n+1)
0	0	0
0	1	0
1	0	1
1	1	1

step ②

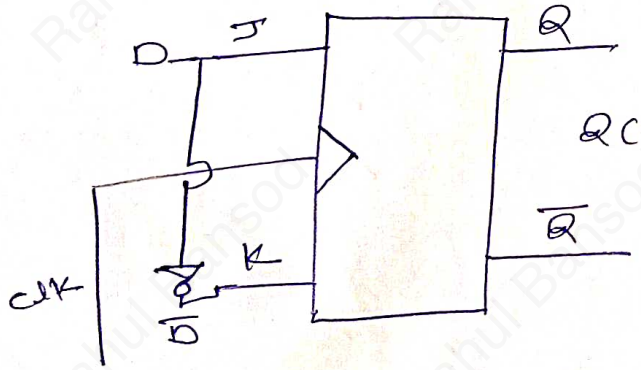
J	K
0	X
X	1
1	X
X	0

J	$\bar{Q}(n)$	$Q(n)$
$\bar{D}$		X
D	1	X

$J = D$

$K = \bar{D}$

K	$\bar{Q}$	Q
$\bar{D}$	X	1
D	X	



$Q(n+1) = \bar{J}\bar{Q} + \bar{K}Q \quad J = D$

$= D\bar{Q} + \bar{D}Q$

$= D\bar{Q} + DQ$

$= D(\bar{Q} + Q)$

$Q(n+1) = D$

SR to JK

available → SR, desired → JK

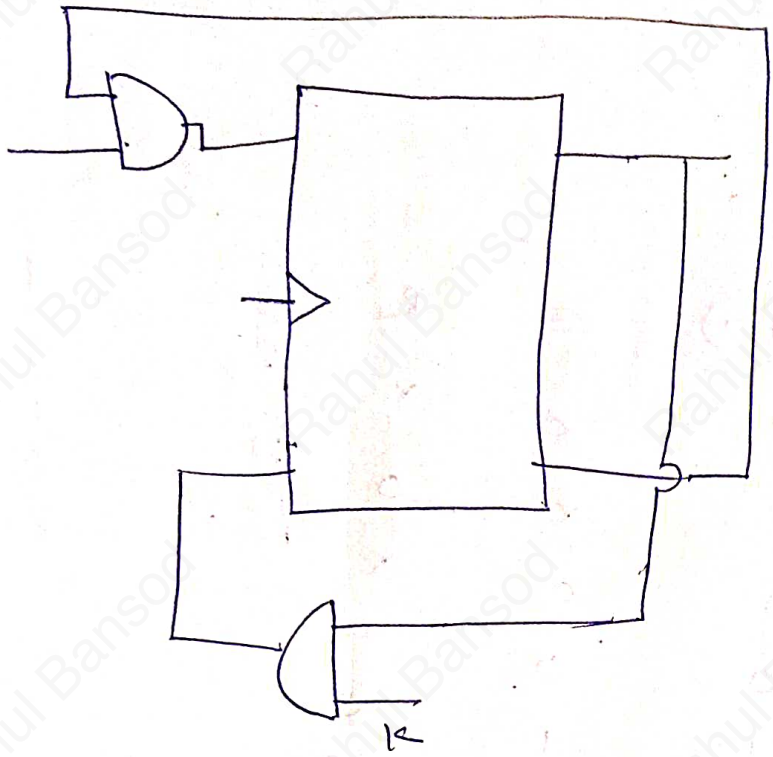
J	K	Q(n)	Q(n+1)	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

S \	$\bar{K}\bar{Q}$	$\bar{K}Q$	KQ	$K\bar{Q}$
$\bar{J}$		X		
J	1	X		1

$S = J\bar{Q}$

R \	$\bar{K}\bar{Q}$	$\bar{K}Q$	KQ	$K\bar{Q}$
$\bar{J}$	X		1	X
J			1	

$R = KQ$



$$Q(n+1) = S + \bar{R}Q$$
$$= J\bar{Q} + \overline{KQ}\,Q$$
$$= J\bar{Q} + (\bar{K} + \bar{Q})Q$$
$$Q(n+1) = J\bar{Q} + \bar{K}Q$$

SR - JK $\longrightarrow$ $S = J\bar{Q}$, $R = KQ$

SR - D $\longrightarrow$ $S = D$, $R = \bar{D}$

SR - T $\longrightarrow$ $S = T\bar{Q}$, $R = TQ$

JK - SR $\longrightarrow$ $J = S$, $K = R$

JK - D $\longrightarrow$ $J = D$, $K = \bar{D}$

JK - T $\longrightarrow$ $J = T$, $K = T$

$Q(n+1) = D$

$Q(n+1) = S + \bar{R}Q(n)$

$D \rightarrow SR \longrightarrow D = S + \bar{R}Q(n)$

$D \rightarrow JK \longrightarrow D = J\bar{Q} + \bar{K}Q$

$D - T \longrightarrow D = T \oplus Q(n)$

$T - JK \longrightarrow T = J\bar{Q} + KQ$

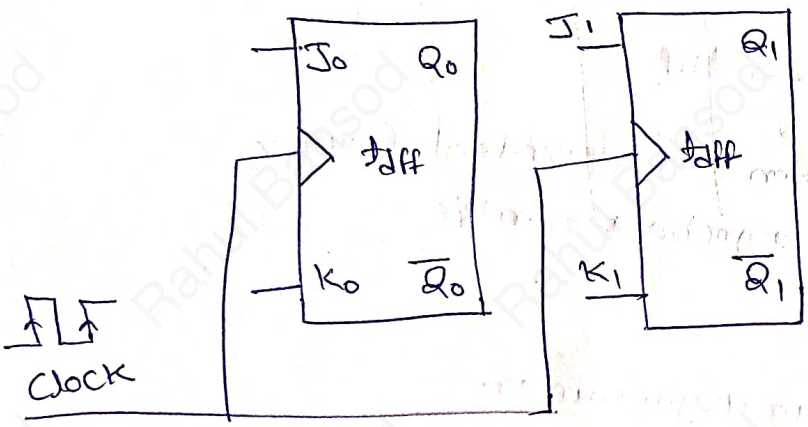
$T - SR \longrightarrow T = S\bar{R} + RQ$

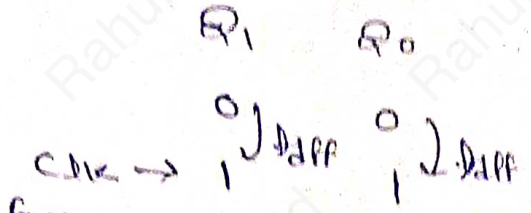
$T - D \longrightarrow T = \underbrace{D \oplus Q(n)}$

$Q(n+1) = T \oplus Q(n)$

Lect- 40

Synchronous counter





for proper operation of a synchronous counter having n f/f.

$$\boxed{T_{clk} \geq t_{dff}}$$ because overall delay

$T_{delay} = t_{dff}$.

$$\boxed{f_{clk} \leq \frac{1}{t_{dff}}}$$

$$\boxed{F_{max} = \frac{1}{t_{dff}}}$$

In case of synchronous counter designed with n f/f The overall delay of the ckt is

$$\boxed{T_{delay} = t_{dff}}$$

- So we can say that The delay is independent of no. of f/f and ~~delay~~ equal to delay of ~~singl~~ single ~~number~~ ~~of~~ f/f.

and proper operation $T_{clk} \leq t_{dff}$.

- here max. frequency of operation is independent of number of f/f (inversely proportion to no. of f/f) while in case of ~~asy~~ asynchronous counter

~~the~~

- synchronous counter are faster than asyn. counter.

- decoding error present only in Asyn. counter not in syn. counter.

e.g:- Design a counter

0 - 3 - 1 - 2 - 5 using JK, D, T.

MSB Q_2	Q_1	LSB Q_0	$Q_2(n+1)$	$Q_1(n+1)$	$Q_0(n+1)$

$Q_2(n)$	$Q_1(n)$	$Q_0(n)$	$Q_2(n+1)$	$Q_1(n+1)$	$Q_0(n+1)$	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	1	1	1					
0	1	1	0	0	1	X					
0	0	1	0	1	0	0					
0	1	0	1	0	1	X					
1	0	1	0	0	0	1					

J_2

1	0	X	X
	1		

Q_2	Q_1	Q_0	$Q_2(n+1)$	$Q_1(n+1)$	$Q_0(n+1)$	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	1	1	0	X	1	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	1	1	X	X	1	1	X
0	1	1	0	0	1	0	X	X	1	X	0
1	0	0	X	X	X	X	X	X	X	X	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

3-1-2-5-0-3

J_2	$\overline{Q_1}\,\overline{Q_0}$	$\overline{Q_1}Q_0$	Q_1Q_0	$Q_1\overline{Q_0}$
$\overline{Q_2}$				1
Q_2	X	X	X	X

$J_2 = Q_1\overline{Q_0}$

K_2	$\overline{Q_1}\,\overline{Q_0}$	$\overline{Q_1}Q_0$	Q_1Q_0	$Q_1\overline{Q_0}$
$\overline{Q_2}$	X	X	X	X
Q_2	X	1	X	X

$K_2 = 1$

J_1				
	1	1	X	X
	X		X	X

$J_1 = \overline{Q_2}$

K_1

X	X	1	1
X	X	X	X

$K_1 = 1$

J_0

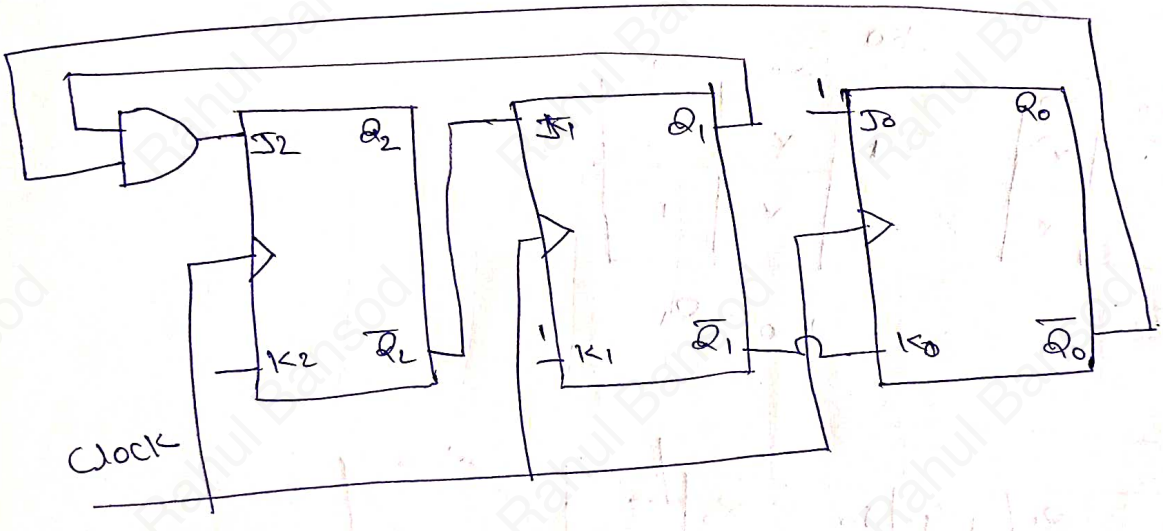
1 1	X 2	X 4	1 3
X 5	X 6	X 8	X 7

$J_0 = 1$

K_0

X	1		X
X	1	X	X

$K_0 = \overline{Q_1}$



e.g:- 0-1-3-2

Q_1	Q_0	$Q_1(n+1)$	$Q_0(n+1)$	J_1	K_1	J_0	K_0
0	0	0	1	0	X	1	X
0	1	1	1	1	X	X	0
1	0	0	0	X	1	0	X
1	1	1	0	X	0	X	1

J_1

	$\overline{Q_0}$	Q_0
$\overline{Q_1}$		1
Q_1	X	X

K_1

	$\overline{Q_0}$	Q_0
$\overline{Q_1}$	X	X
Q_1	1	

$J_1 = Q_0$

$K_1 = \overline{Q_0}$

J_0

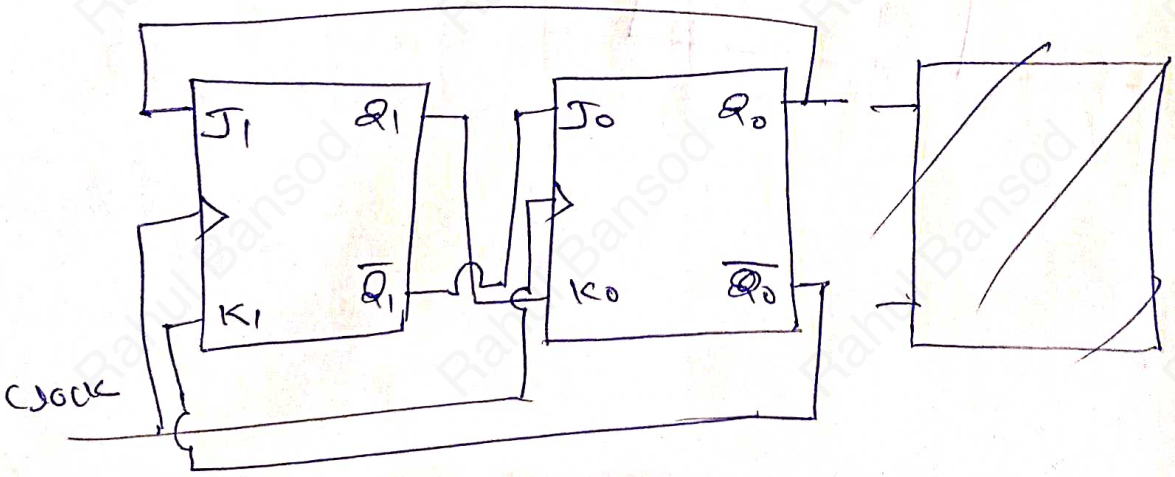
	$\overline{Q_0}$	Q_0
$\overline{Q_1}$	1	X
Q_1		X

K_0

	$\overline{Q_0}$	Q_0
$\overline{Q_1}$	X	
Q_1	X	1

$J_0 = \overline{Q_1}$

$K_0 = Q_1$



00 - 01 - 11 + 10

H.W 1) 0-1-2-5-4-6 using JK, D, T, SR
2) 0-3-1-9-2-6-5

Lect-41

Q) 0-3-1-9-2-6-5 using T f/f

Sol:- 4 f/f are required

Q_3	Q_2	Q_1	Q_0	$Q_{3(n+1)}$	$Q_{2(n+1)}$	$Q_{1(n+1)}$	$Q_{0(n+1)}$	T_3	T_2	T_1	T_0
0	0	0	0	0	0	1	1	0	0	1	1
0	0	0	1	1	0	0	1	1	0	0	0
0	0	1	0	0	1	1	0	0	1	0	0
0	0	1	1	0	0	0	1	0	0	1	0
0	1	0	0	X	X	X	X	X	X	X	X
0	1	0	1	0	0	0	0	0	1	0	1
0	1	1	0	0	1	0	1	0	0	1	1
0	1	1	1	X	X	X	X	X	X	X	X
1	0	0	0	X	X	X	X	X	X	X	X
1	0	0	1	0	0	1	0	1	0	1	1
1	0	1	0	X	X	X	X	X	X	X	X
1	0	1	1	X	X	X	X	X	X	X	X
1	1	0	0	X	X	X	X	X	X	X	X
1	1	0	1	X	X	X	X	X	X	X	X
1	1	1	0	X	X	X	X	X	X	X	X
1	1	1	1	X	X	X	X	X	X	X	X

T_3	$\overline{Q_1}\,\overline{Q_0}$	$\overline{Q_1}\,Q_0$	$Q_1 Q_0$	$Q_1\overline{Q_0}$
$\overline{Q_3}\,\overline{Q_2}$		1		
$\overline{Q_3}\,Q_2$	X		X	
$Q_3 Q_2$	X	X	X	X
$Q_3\overline{Q_2}$	X	1	X	X

$$T_3 = \overline{Q_2}\,\overline{Q_1}\,Q_0$$

T_2	$\overline{Q_1}\,\overline{Q_0}$	$\overline{Q_1}\,Q_0$	$Q_1 Q_0$	$Q_1\overline{Q_0}$
$\overline{Q_3}\,\overline{Q_2}$				1
$\overline{Q_3}\,Q_2$	X	1	X	
$Q_3 Q_2$	X	X	X	X
$Q_3\overline{Q_2}$	X		X	X

$$T_2 = Q_2 Q_0 + Q_1\overline{Q_0}\,Q_2$$

T_1	$\overline{Q_1}\,\overline{Q_0}$	$\overline{Q_1}\,Q_0$	$Q_1 Q_0$	$Q_1\overline{Q_0}$
$\overline{Q_3}\,\overline{Q_2}$	1		1	
$\overline{Q_3}\,Q_2$	X		X	1
$Q_3 Q_2$	X	X	X	X
$Q_3\overline{Q_2}$	X	1	X	X

$$T_1 = \overline{Q_1}\,\overline{Q_0} + Q_3 + Q_1 Q_0 + Q_2 Q_1$$

\$ quand invalid ~~c~~ ~~octaled~~.

may ask in exam

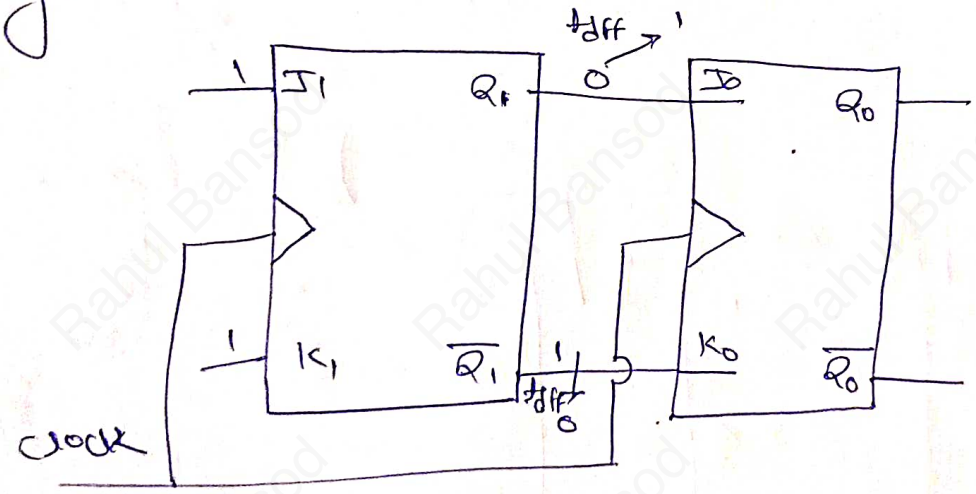
Q) 0-1-2-3-1-0-1-2-3-1

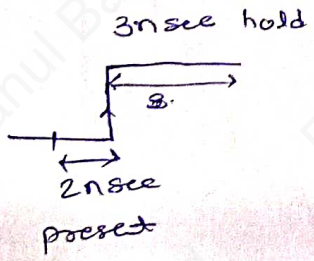
Preset time & hold time :-

Preset time:- It is the minimum time before arrival of clock before which input must be maintained at proper level for proper output generation.

hold time:- It is the minimum time after arrival of clock for which i/p must be maintained at proper level for proper output generation.

e.g:-





t_h = 3nsec

t_{dff} = 5nsec

$\boxed{t_{dff} > t_{hold}}$

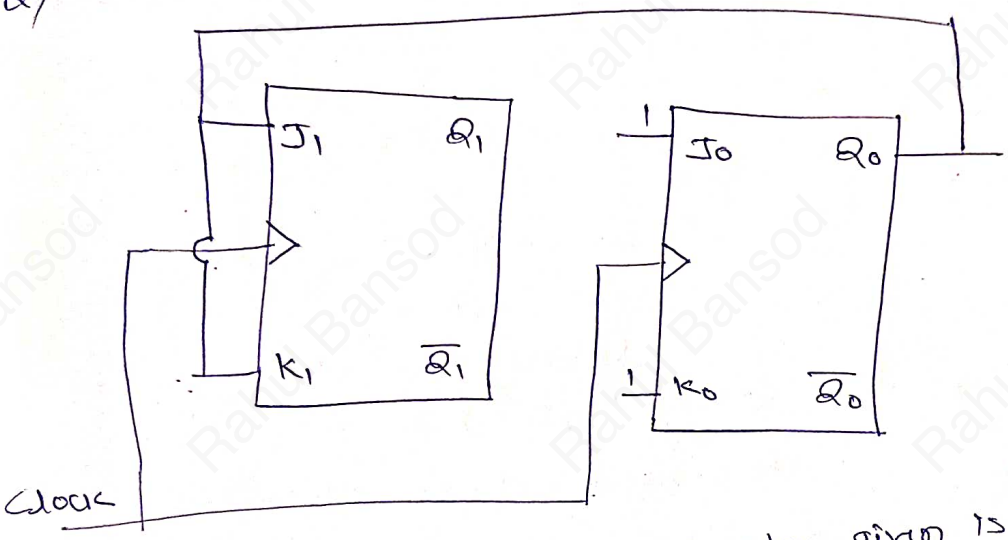
- For cascading operation in a syn. counter where o/p of 1 f/f is use as i/p of other f/f, then for this ckt to work properly the condition that must be satisfied is

$$\boxed{t_{dff} > t_h}$$

delay of the f/f must be greater than the hold f/f.

Lect - 42

Q)



initial state of the syn. counter given is $(Q_0 Q_1)$ - 00

what will the states of counter after applying clock pulses →

a) 00 - 10 - 01 - 11 - 00 ✓

b) 00 - 10 - 11 - 01 - 00

c) 00 - 11 - 10 - 01 - 00

d) 00 - 01 - 10 - 11 - 00

Sol:-

$$Q_1(n+1) = J_1\overline{Q_1} + \overline{K_1}Q_1$$
$$= Q_0\overline{Q_1} + \overline{Q_0}Q_1 = Q_1 \oplus Q_0$$

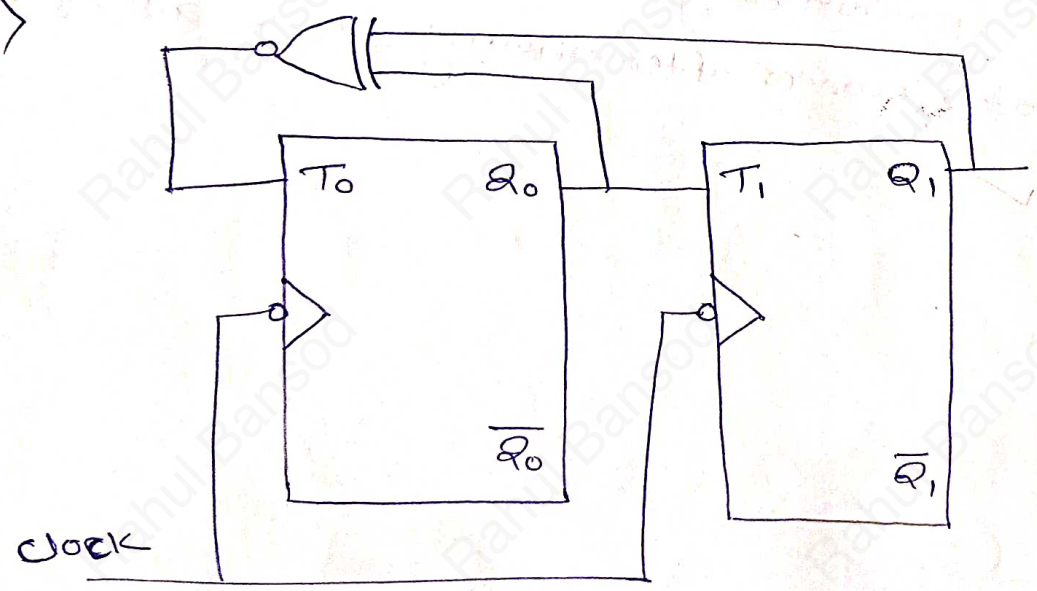
$$Q_0(n+1) = J_0\overline{Q_0} + \overline{K_0}Q_0$$
$$= 1\cdot\overline{Q_0} + \overline{1}\,Q_0$$
$$= \overline{Q_0} \text{ (toggle state)}$$

0-1-0-1-0-1-0

	$f_{clk}/2$ Q_0	$f_{clk}/4$ Q_1
	0	0
1 clk	1	0
2 clk	0	1
3 clk	1	1
4 clk	0	0

00 - 10 - 01 - 11 - 00

Q)



The initial state of the given counts is Q_1Q_0 - (0 0). what states will be generated at Q_1Q_0 after application of clock pulses.

a) 00 - 10 - 11 - 01 - 00

b) 00 - 01 - 11 - 00

c) 00 - 11 - 01 - 10 - 00

d) 00 - 01 - 10 - 00

sol^n:-

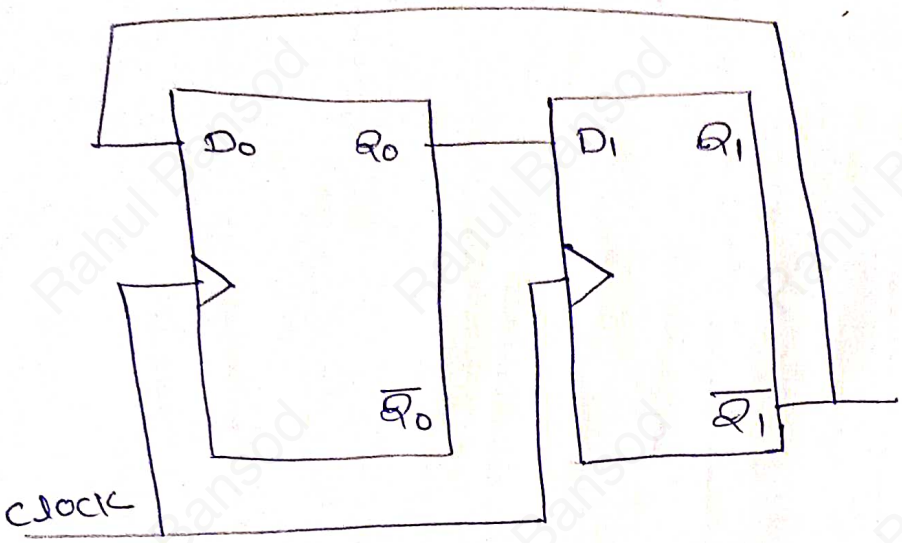
$$Q_1(n+1) = T_1 \oplus Q_1$$
$$= Q_0 \oplus Q_1$$

$$Q_0(n+1) = T_0 \oplus Q_0$$
$$= Q_0 \oplus Q_1 \oplus Q_0$$
$$= Q_0 \odot Q_0 \oplus Q_1$$
$$= 1 \oplus Q_1$$
$$Q_0(n+1) = \overline{Q_1} \rightarrow \text{toggle mode}$$

	Q_1	Q_0
	0	0
1 clk	0	1
2 clk	1	1
3 clk	0	0
	0	1
	1	1

00 - 01 - 11 - 00

Q)



Initial state of the given counts is $(Q_0 Q_1) - 00$. what states will be there after application of clock pulses.

a) 00-10-01-00
✓ b) 00-10-11-01-00
c) 00-11-10-01-00
d) 00-01-11-10-00

Sol^n:-

$$Q(n+1) = D$$

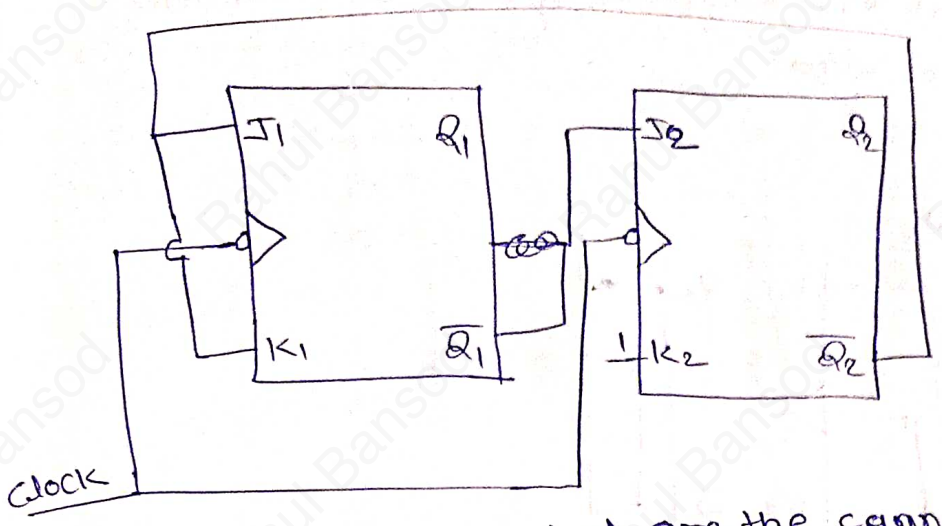
$$Q_0(n+1) = D_0 = \overline{Q_1}$$

$$Q_1(n+1) = D_1 = Q_0$$

Q_0	Q_1
0	0
1	0
1	1
0	1
0	0

00-10-11-01-00

Q)



what are the counting states (Q_1, Q_2) for counter shown in the figure.

a) 11, 10, 00, 11, 10, 00-11-10

b) 01, 10, 11, 00, 01

c) 00, 11, 01, 10, 00

d) 01, 10, 00, 01, 10

$$Q_1(n+1) = J_1 \overline{Q_1} + \overline{K_1} Q_1$$
$$= \overline{Q_2}\,\overline{Q_1} + Q_2 Q_1$$
$$= Q_1 \odot Q_2$$

$$Q_2(n+1) = J_2 \overline{Q_2} + \overline{K_2} Q_2$$
$$= \overline{Q_1}\,\overline{Q_2} + \overline{1} Q_2$$
$$= \overline{Q_1} . \overline{Q_2}$$
$$= \overline{Q_1 + Q_2}$$

$= \overline{0} . \overline{1} = 0 . 0 = 0$

$= 0 . 1 = 0$

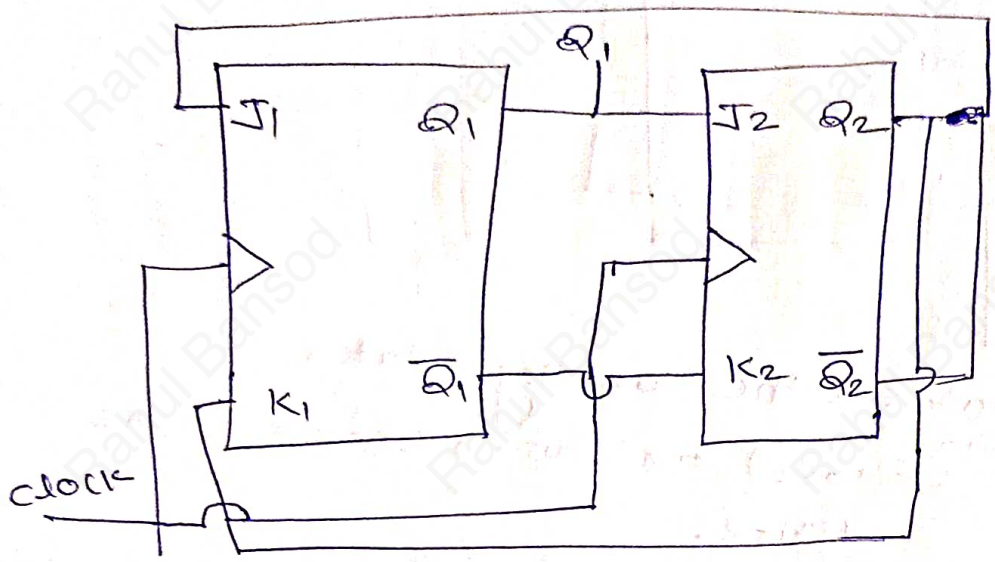
$\overline{1+1} = \overline{1} = 0$

$\overline{1+0} = 0$

	Q_1	Q_2
	0	0
1 clk	1	1
2 clk	1	0
3 clk	0	0

00 - 11 - 10 - 00

Q) The outputs of the two flipflops Q_1, Q_2 in the fig are initialize to (0,0) the sequence generated at Q_1 after application of clock signal



a) 01110 - - -

b) 01010 - - - -

c) 00110 - - -

✓d) 01100 - - - -

$$Q_1(n+1) = J_1\overline{Q_1} + \overline{K_1}Q_1$$
$$= \overline{Q_2}\,\overline{Q_1} + \overline{Q_2}Q_1$$
$$= \overline{Q_2}[\overline{Q_1} + Q_1]$$
$$= \overline{Q_2}$$

$$Q_1(n+1) = \overline{Q_2}$$

$$Q_2(n+1) = J_2\overline{Q_2} + \overline{K_2}Q_2$$
$$= Q_1\overline{Q_2} + \overline{\overline{Q_1}}Q_2$$
$$= Q_1\overline{Q_2} + Q_1Q_2$$
$$= Q_1(Q_2 + \overline{Q_2})$$

$$Q_2(n+1) = Q_1$$

Q_1	Q_2
0	0
1	0
1	1
0	1
0	0
1	0
1	1
0	1
0	0

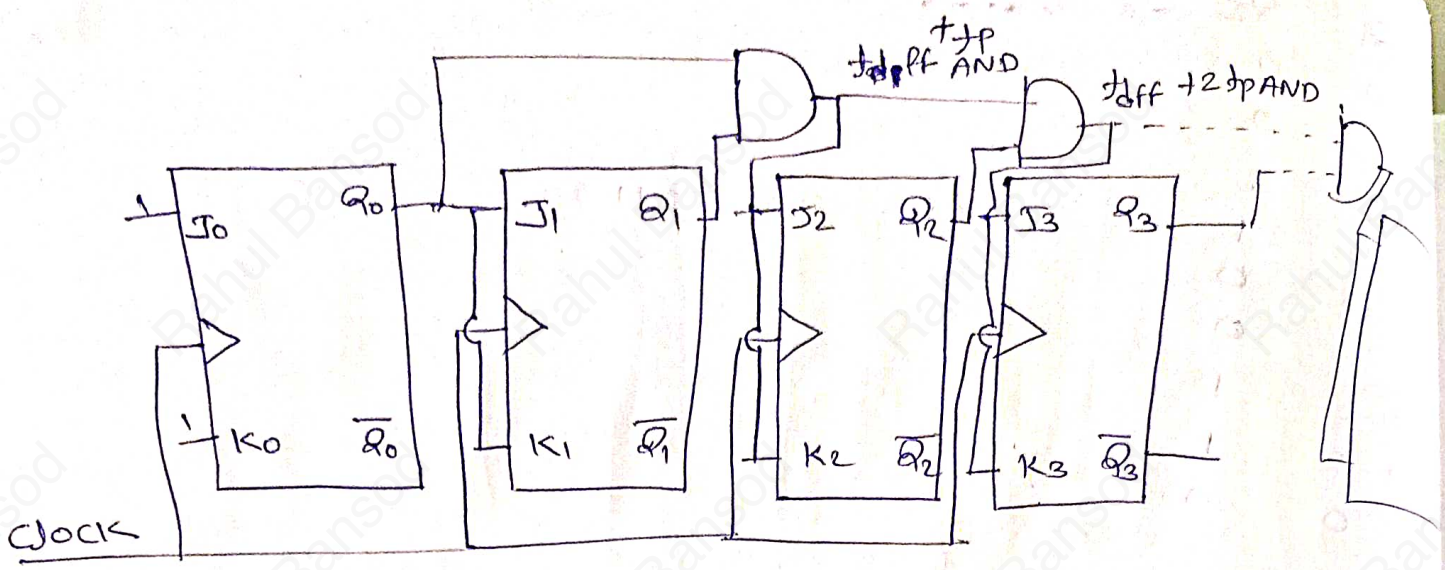
$Q_1 = 011001100$

Lect - 43

Synchronous series carry counter :→

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
0			

↑



→ Here 2 i/p 2 AND gate are required

- To design n-bit syn. series carry counter we require (n-2) AND gates (2 i/p AND gates)

$$\boxed{t_{dff} + (n-2)\, t_{pAND}}$$

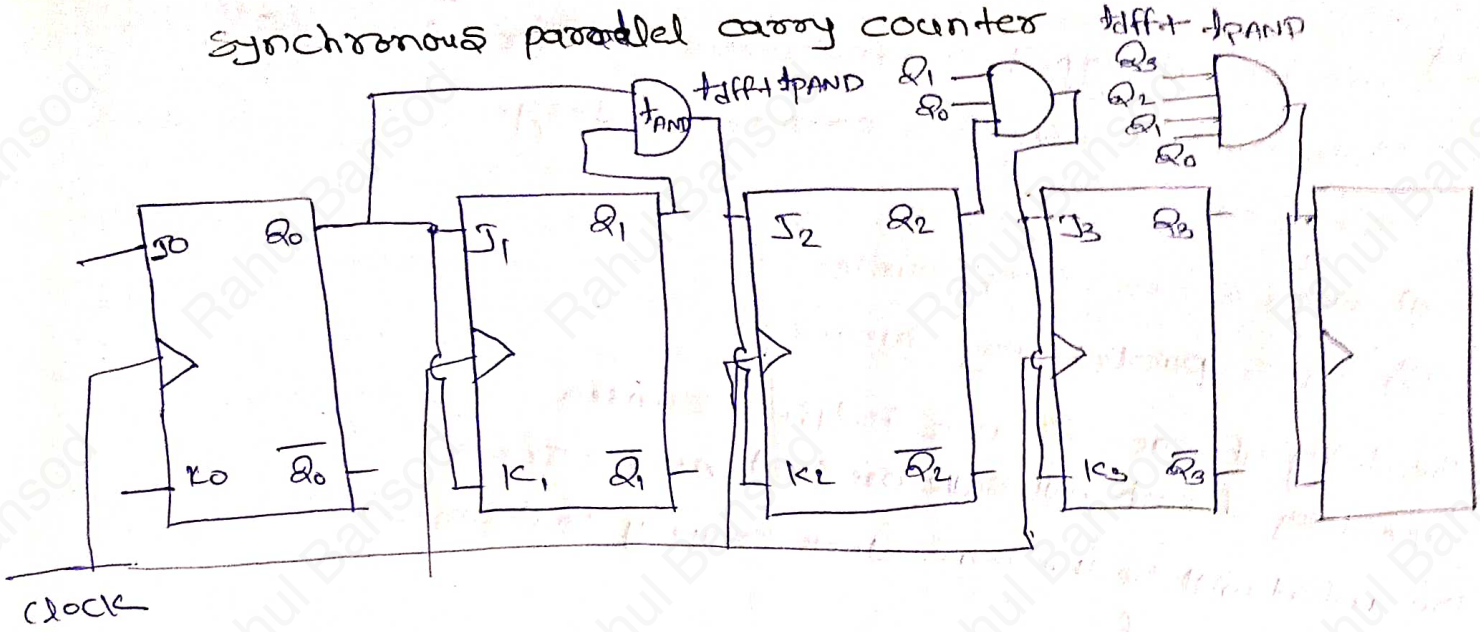
- In worst case delay of the ckt is $T_{delay} = T_{dff} + (n-2)t_{pA}$

- for proper operation $T_{clk} \geq t_{dff} + (n-2)\, t_{pAND}$

$$f_{clk} \leq \frac{1}{t_{dff} + (n-2)\, t_{pAND}}$$

$$\boxed{f_{max} = \frac{1}{t_{dff} + (n-2)\, t_{pAND}}}$$

Synchronous parallel carry counter



worst case delay $T_{delay} = t_{dff} + t_{PAND}$

$$T_{clk} \geq T_{dff} + t_{PAND}$$

$$f_{clk} \leq \frac{1}{t_{dff} + t_{PAND}}$$

$$\boxed{f_{max} = \frac{1}{t_{dff} + t_{PAND}}}$$ parallel

- In syns. parallel carry counter design with n flf number of AND Gate requires are $\{n-2\}$ AND Gate (multi input AND Gate)
- In syns. parallel carry counter due to parallel operation of all the AND Gates delay of only 1 AND Gate Added
- In case of syns. parallel carry counter the clock time period

$$\boxed{T_{clk} \geq T_{dff} + t_{PAND}}$$

Q) we have designed a synchronous counter of MOD number 64. This counter is design using sy

A) syns. series carry counter

B) syns. parallel carry counter

The delay of each flf use is $t_{dff} = 20$ nsec

The delay of each AND Gate use is $t_{PAND} = 5$ nsec

The what will be the max. clock frequency that can be used in case of

1) sys. series carry counter

2) sys. parallel carry counter.

Sol:-

A)

$n = 6$

$2^6 = 64 \Rightarrow 2^n$

$T_{ds} = 20 + 4 \times 5$ → worst case delay

$= 20 + 20$ $\quad t_{dff} + (n-2) t_{PAND}$

$= 40$ nsec

$T_{clk} \geq 40$ nsec

$f_{clk} \leq \frac{1}{40 \text{ nsec}}$

$f_{max} = \frac{1}{40 \text{ nsec}} = \frac{10^9}{40}$

$= 10^6 \times \frac{10^3}{40}$

$\boxed{f_{max} = 25 \text{ MHz (max)}}$

B) parallel

$n = 6$

$T_{delay} = 20 + 5 = 25\,nsec$

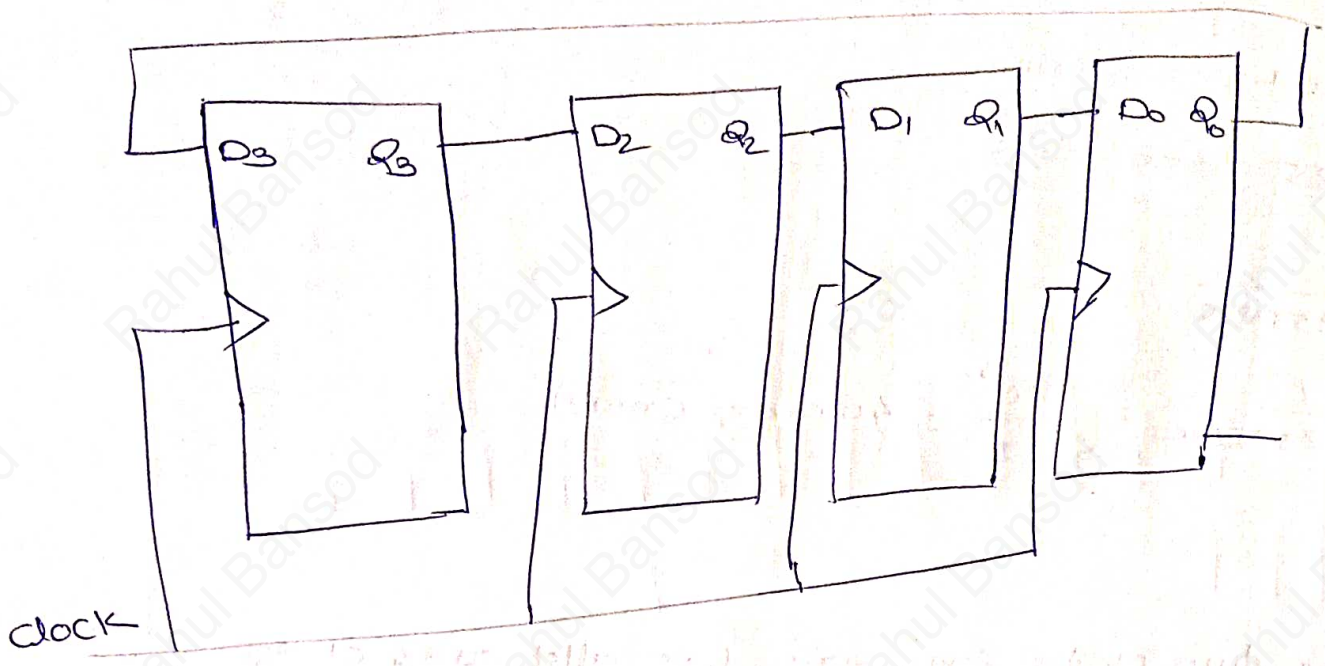
$T_{clk} \geq 25\,nsec$

$f_{clk} \leq \frac{1}{25\,nsec}$

$f_{max} = \frac{1}{25\,nsec} = \frac{10^9}{25} = 40\,MHz$ (max)

If in above two ckts syn. series & parallel carry ckts if all i/p's of all AND Gates will be driven by complementry* outputs of flip then above two ckts behave as a down counter (MODE 16 down counter)

Ring counter :→



4 bit ring counter

$Q_3(n+1) = D_3 = Q_0(n)$

$Q_2(n+1) = D_2 = Q_3(n)$

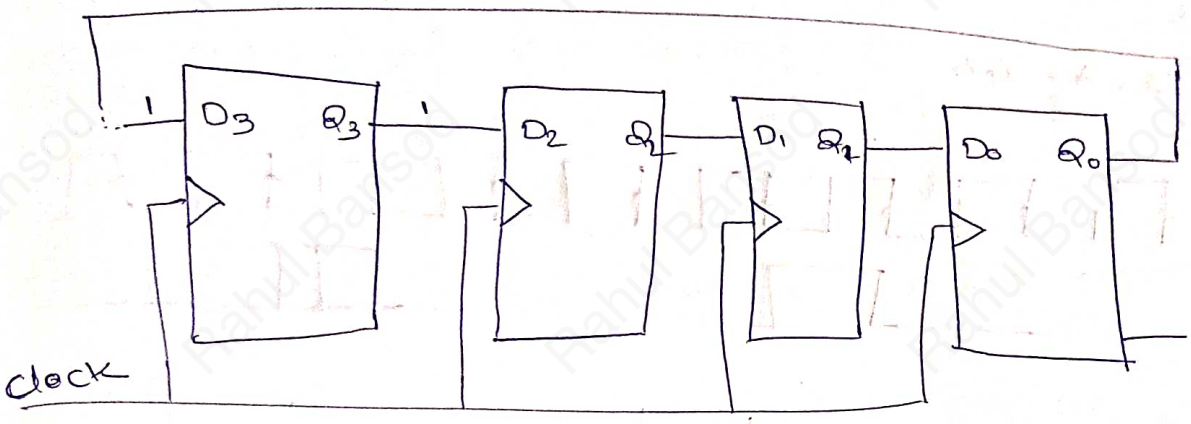
$Q_1(n+1) = D_1 = Q_2(n)$

$Q_0(n+1) = D_0 = Q_1(n)$

	Q_3	Q_2	Q_1	Q_0
	0	0	0	0
clk	0	0	0	0

This is self starting

	Q_3	Q_2	Q_1	Q_0
	0	0	0	0
1 clk	0	0	0	0

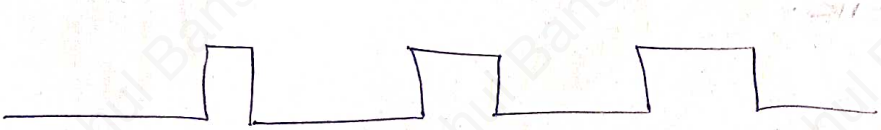


	Q_3	Q_2	Q_1	Q_1
	fclk/4	fclk/4	fclk/4	fclk/4
	1	0	0	0
1 clk	0	1	0	0
2 clk	0	0	1	0
3 clk	0	0	0	1
4 clk	1	0	0	0
5 clk	0	1	0	0 → repeat
	0	0	1	0
	0	0	0	1
	1	0	0	0

(MOD 4)

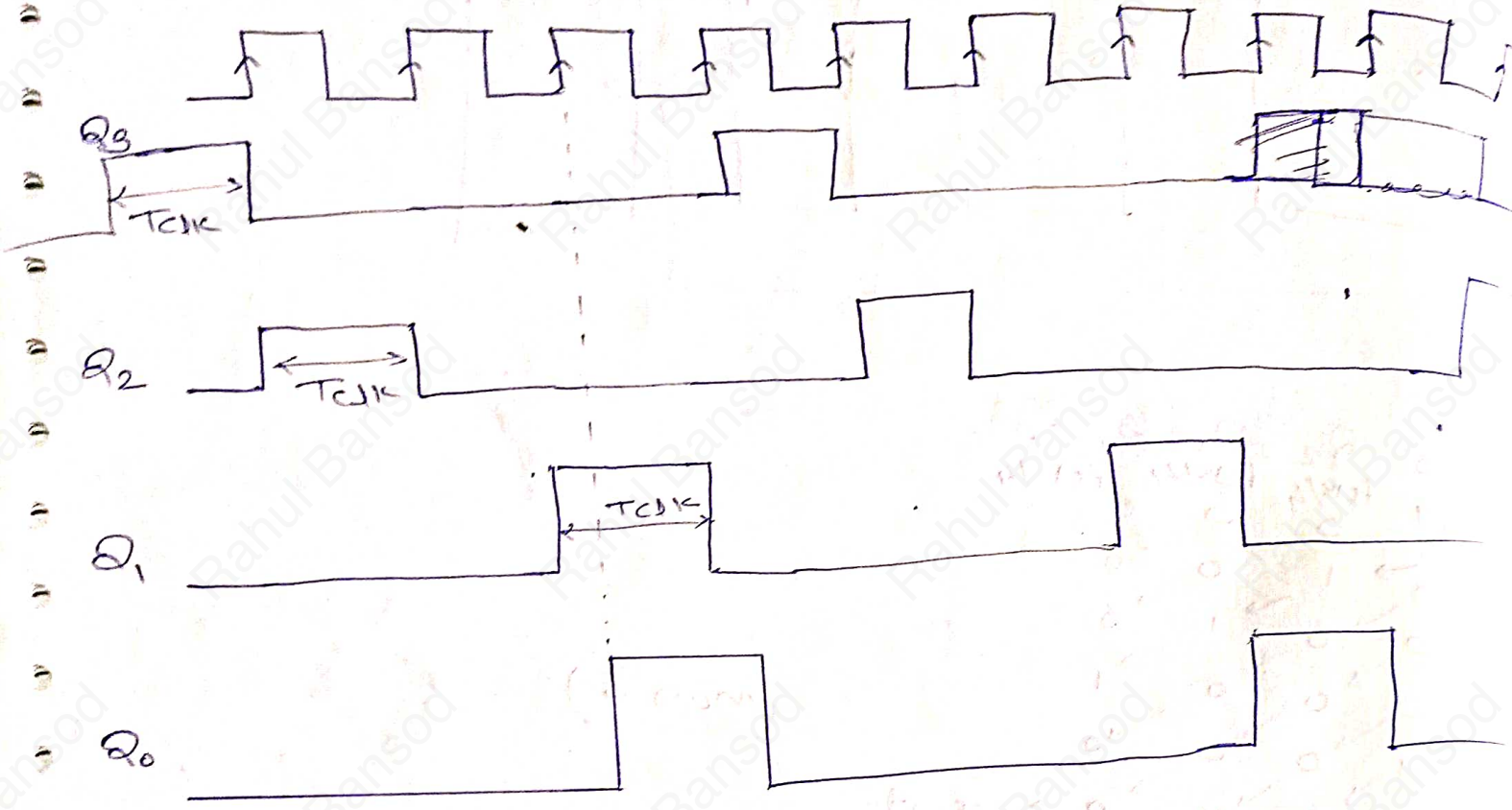
A ring counter design ~~durin~~ using n f/f then the MOD number of the counter will be → n

- unused states in ring counter is → $(2^n - n)$



Note:- In case of ring counter designed with n F/F (MOD no. n) then at the o/p of each F/F the i/p clock frequency will be divided by the mod number of the counter.

Lect - 44



Time period of waveforms at Q_3, Q_2, Q_1 & Q_0 will be

$$T = nT_{CLK}$$

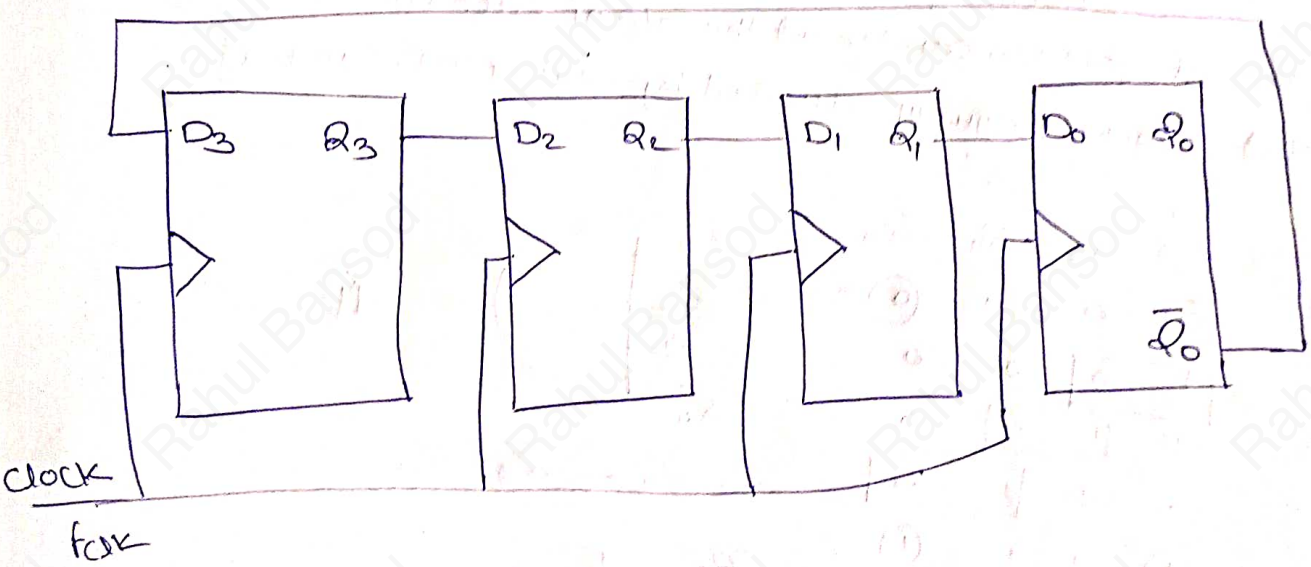
- successive waveforms at the o/p of F/F's of a ring counter has time shift of T_{CLK}.

- $nT_{clk} \rightarrow 2\pi = 360^\circ$
- $T_{clk} \rightarrow \frac{2\pi}{n}$ phase $= \frac{360^\circ}{n}$

- in ring counter design using n f/f the successive waveforms at the o/p of f/f has a phase shift of 360° or 2π radian.

- ring counter is basically use in motor controls in Electrical circuit.

4 bit Johnson counter :→ (switch tail counter)



	$f_{clk}/8$ Q_3	$f_{clk}/8$ Q_2	$f_{clk}/8$ Q_1	$f_{clk}/8$ Q_0
	0	0	0	0
1 clk	1	0	0	0
2 clk	1	1	0	0
3 clk	1	1	1	0
4 clk	1	1	1	1
5 clk	0	1	1	1
6 clk	0	0	1	1
7 clk	0	0	0	1
8 clk	0	0	0	0

$Q_3(n+1) = D_3 = \overline{Q_0}(n)$

$Q_2(n+1) = D_2 = Q_3(n)$

$Q_1(n+1) = D_1 = Q_2(n)$

$Q_0(n+1) = D_0 = Q_1(n)$

MOD-8

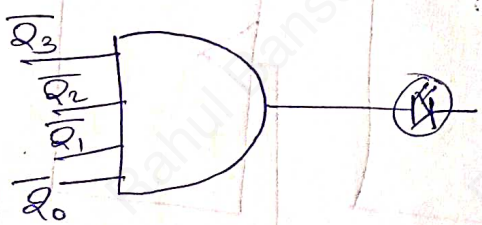
- Johnson counter designed using n f/f will have MOD number equal to 2^n

Unused state in Johnson counter is $\rightarrow (2^n - 2n)$

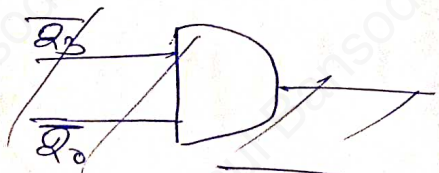
Lect-45

- In case of Johnson counter at the o/p of each f/f the input clock frequency divided by 2n [MOD number]

Q_3	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
0	0	0	0



$\overline{Q_3}\,\overline{Q_0} = \overline{Q_3 + Q_0}$



$Q_3\overline{Q_2} = \overline{\overline{Q_3} + Q_2}$

$Q_2\overline{Q_1} = \overline{\overline{Q_2} + Q_1}$

$Q_1\overline{Q_0} = \overline{\overline{Q_1} + Q_0}$

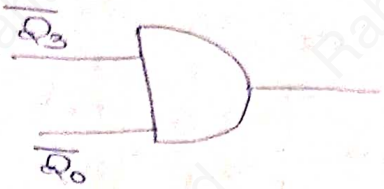
$Q_3 Q_0 = \overline{\overline{Q_3} + \overline{Q_0}}$

$\overline{Q_3} \cdot Q_2 = \overline{Q_3 + \overline{Q_2}}$

$\overline{Q_2} Q_1 = \overline{Q_2 + \overline{Q_1}}$

$\overline{Q_1} Q_0 = \overline{Q_1 + \overline{Q_0}}$

0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1



- To decode each state of Johnson counter we require two i/p AND gate or 2 i/p NOR Gate

Note:- There is no decoding ckt require in ring counter to decode a state. The decoding ckt in johnson counter is less complex compaire to asynchronous counter decoding circuitary.

Q) we have a 3-bit Johnson counter, whose starting state is 0/0. The input clock frequency is 6MHz, then the o/p frequency will be

a) 3MHz b) 1MHz c) 6MHz. d) 1.5MHz.

Sol^n:-

	Q_2	Q_1	Q_0
	0	1	0
1 clk	1	0	1
2 clk	0	1	0
	0	0	0
	1	0	0
	1	1	0
	1	1	1
	0	1	1
	0	0	1
	0	0	0

$f_{clk}/2$

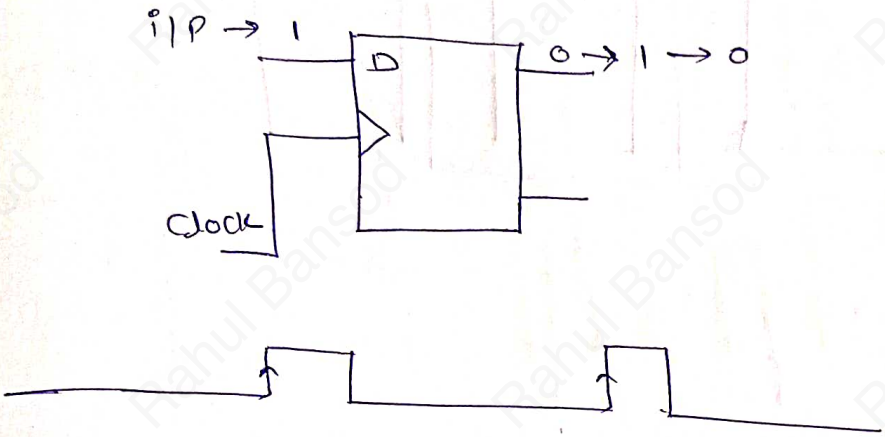
	Q_2	Q_1	Q_0
	0	1	0
1 clk	1	0	1
2 clk	0	1	0
3 clk	1	0	1
4 clk	0	1	0

MOD-2

$$\therefore f_{clk}/2 = \frac{6\,MHz}{2} = 3\,MHz$$

Shift Register :→

single f/f is smallest memory element

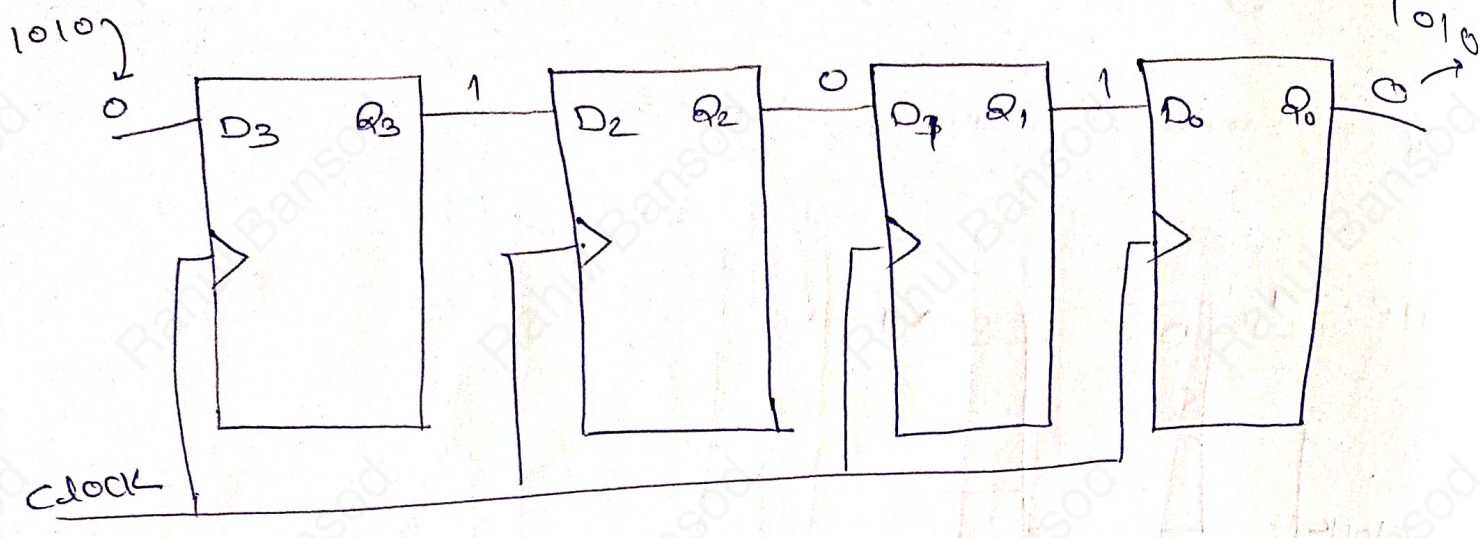


→ Registers are use to store the information.

- A single f/f is used to store 1 bit of information
- to store n bit information a register is used having n f/f.
- ~~Aon~~ and on the basis of i/p & o/p there are 4 types of shift register:-

- 1) SISO - serial in serial out
  2) SIPO → serial in parallel out
  3) PIPO → parallel in parallel out
  4) PISO → parallel in serial outs

1) SISO



1010

SI

1 clk	0 0 0 0
2 clk	1 0 0 0
3 clk	0 1 0 0
4 clk	1 0 1 0

~~1 clk 0 0 0 0~~
~~2 clk 1 1 1 1~~
~~3 clk 0 0 0 0~~

SISO → serially i/p ~~dat~~ the data n-clock are required.

n-bit → n clocks required.

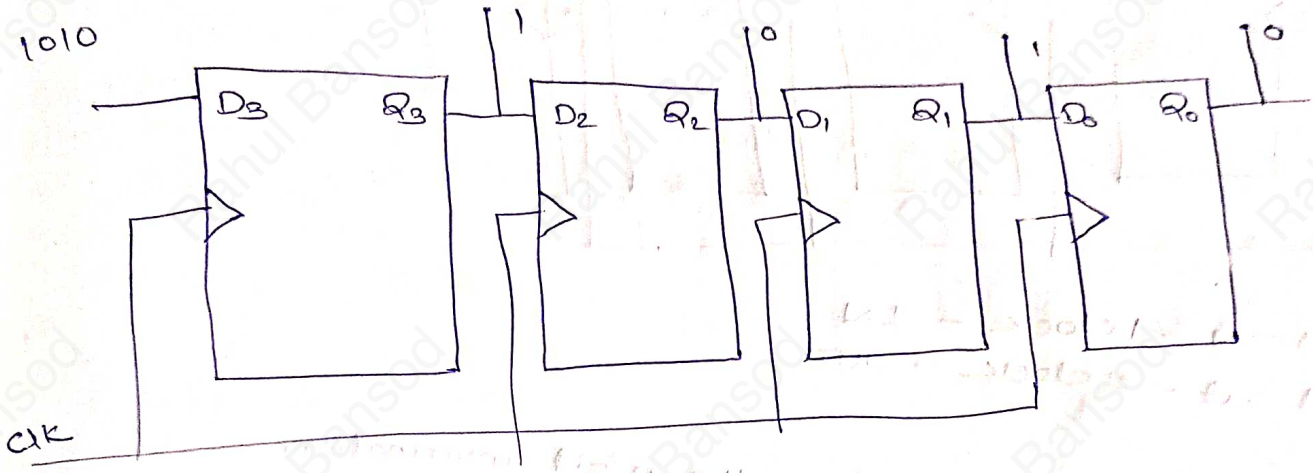
SO

1 clk	1 0 1 0
2 clk	1 0 0
3 clk	1

- for serially out the data - (n-1) clocks are required.

- In serial in serial out register to store (to in) n bit information we require n clocks. (n·Tclk Time)
- To serially out the data we require n-1 clock

2) SIPO

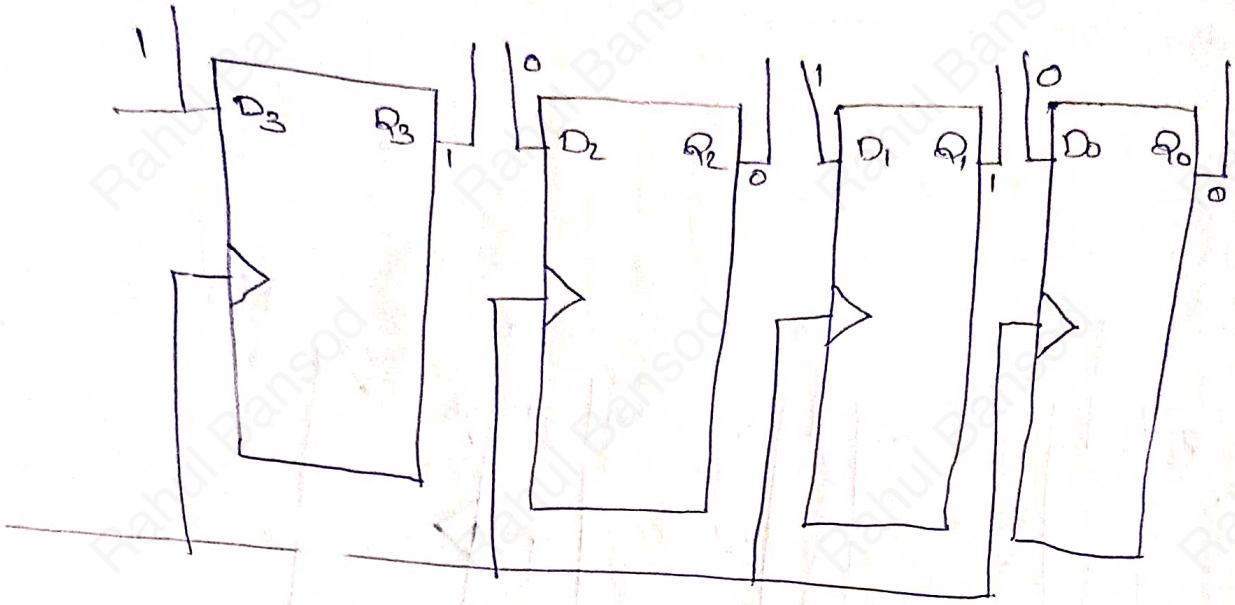


- To serially In the data ~~to~~ we require ~~for~~ n bit for n bit serial in parallal out register.
- To parallel out the data we require 0 clock.
- SIPO – n clock – IN
  0 clock – out.

3) PIPO Lect-46

Parallel in parallel out.

1010

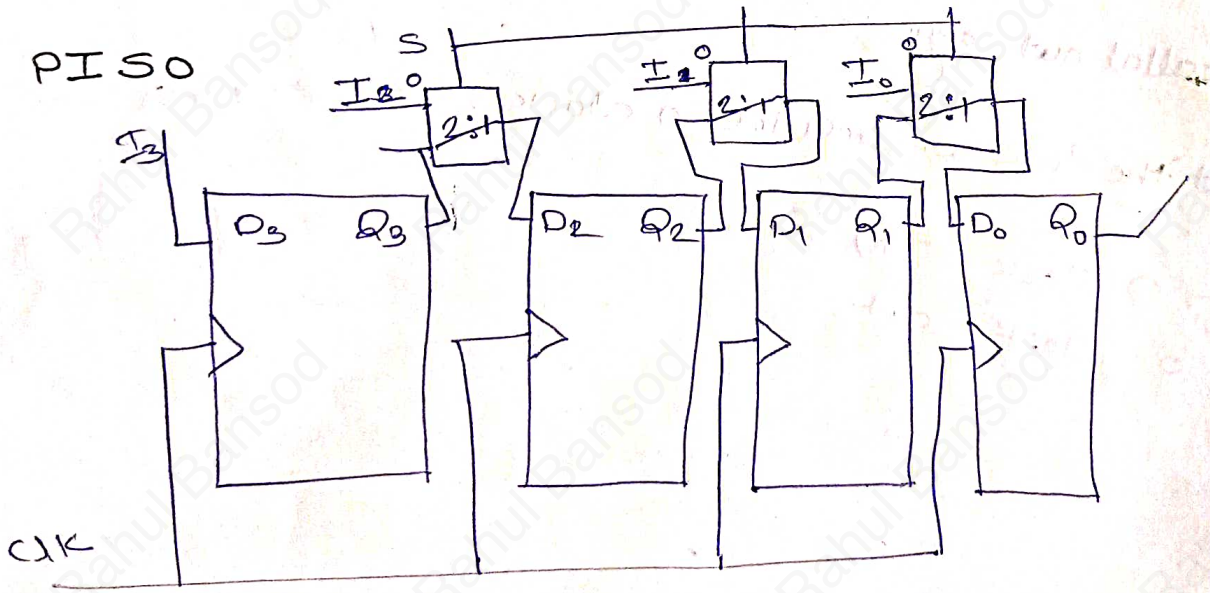


Parallel IN - 1 clock - IN

Parallel out - 0 clock - OUT

- To PIPO register to store the n bit information we require 1 clock & to out the data parallely we require 0 clock

4) PISO



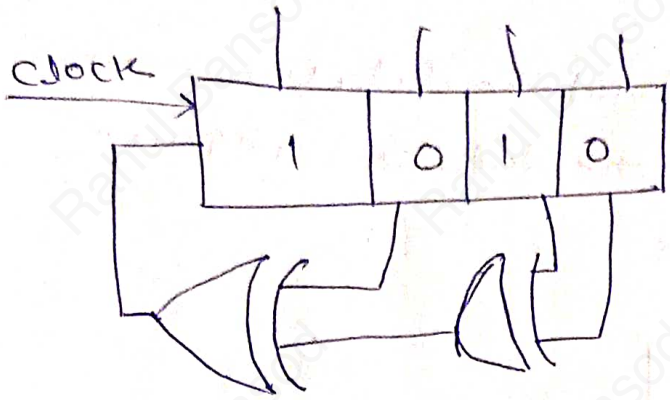
$S_0 = 0$ for parallaly i/p the data

$S = 1$ for serially out the data

In PISO register for parallely input the data we require 1 clock. while for serially o/p the data we require ~~IO~~ (n-1) clocks.

Register	IN	OUT
SISO	n-clock	(n-1) clock
SIPO	n-clock	0
PIPO	1-clock	0
PISO	1-clock	(n-1) clock

Q) (2 M) A four bit SIPO register is shown in given fig. with starting state 1010



After application of how many clock pluses the content of SIPO will again be 1010

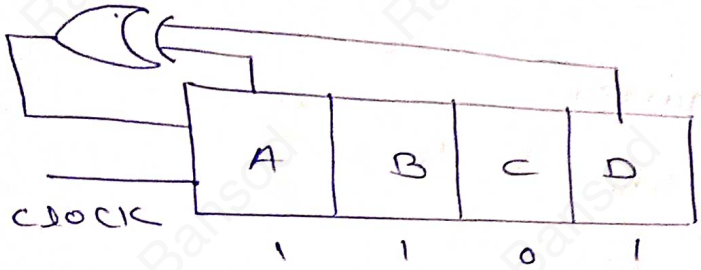
a) 7 b) 9 c) 8 d) 12

Sol:-

		XOR
	1010	0 1 0 → 1
1 clk	1101	1 0 1 → 0
2 clk	0110	1 1 0 → 0
3 clk	0011	011 → 0
4 clk	0001	001 → 1
5 clk	1000	000 → 0
6 clk	0100	100 → 1
7 clk	$\boxed{1010}$	

7 clk

Q) A 4-bit shift register ckt configured the right shift operation i.e. Din - A, A - B, B - C, C - D is shown, if the present state of shift register is ABCD = 1101, the number of clock cycles required to reach the state ABCD = 1111 (10 clk)



XOR

1 1 = 0

Soln:-

	1101
1 clk	0110
2 clk	0011
3	1001
4	0100
5	0010
6	0001
7	1000
8	1100
9	1110
10	1111 → ABCD = 1111
11	0111
12	1011
13	0101
14	1010
15 clk	1101

Q) 0-1-2-3-1-0-1-2-3-1-0

MOD 5 counter

Sol:-

~~Q_3 Q_2 Q_1 Q_0~~

There are 3 flf are required

	Q_2	Q_1	Q_0
000	0	0	0
01	0	0	1
10	0	1	0
11	0	1	1
01	1	0	1
00	0	0	0

Q_2 Q_1 Q_0

Q_2	Q_1	Q_0	$Q_2(n+1)$	$Q_1(n+1)$	$Q_0(n+1)$	T_2	T_1	T_0
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	1	1	1	0
1	0	0	X	X	X	X	X	X
1	0	1	0	0	0	0	0	1
1	1	0	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X

Q) 0-1-2-1-0-2-1-0

Lect- 47

DAC & ADC

DAC :→

1) weighted Resister type

2) R-2R ladder
   - Normal ladder
     - NON inverting type
     - Inverting type
   - Inverted ladder

Imp

ADC :→

i) counter type ADC

Imp ii) SAR type ADC

iii) parallel type ADC

iv) Dual slope type ADC

Rahul Bansod

Digital to Analogue converter (DAC)

~~Definition~~

Resolution :→ It is defined as the change in output voltage corresponding to 1 LSB change in the digital input.

For n-bit digital to Analogue converter

$$\text{Resolution} = \frac{V_r}{(2^n - 1)},$$

where V_r is refference voltage used for logic '1'.

e.g :- resolution = 0.25V

000 → 0V
001 → 0.25V = 1 × 0.25
010 → 0.50V = 2 × 0.25
011 → 0.75V = 3 × 0.25

IMP

- Analog o/p voltage (V_a)

V_a = Resolution × decimal equivalent of i/p digital data.

$$V_a = \frac{V_r}{(2^n - 1)} \times \text{decimal equivalent of i/p digital data.}$$

Full scale voltage of a DAC :- (V_{FS})

it is defined as the maximum possible o/p voltage corresponding to maximum digital input

$$V_{FS} = \frac{V_r}{(2^n-1)} \times (2^n-1)$$

↳ decimal equivalent of max. digital i/p. i.e. (111---n times)

$1111 \rightarrow (2^4-1) \rightarrow$ decimal equi.

$11111 \rightarrow (2^5-1)$

$11111---1n \Rightarrow (2^n-1)$

$$\boxed{V_{FS} = V_r}$$

what is % Resolution :-

% Resolution of a DAC :→ $= \dfrac{\frac{V_r}{(2^n-1)}}{V_{FS}} \times 100\%$

$$= \frac{\frac{V_r}{2^n-1}}{V_r} \times 100\%$$

% Resolution of a DAC $= \dfrac{1}{2^n-1} \times 100\%$

Note:- Two DAC's having same No. of bits but different refference voltages will have different resolution but same percent resolution.

Q) we have a 4 bit ~~di~~ DAC, corresponding to digital i/p $(0101)_2$ ~~Anagl~~ Analog o/p voltage is 2.5V.

~~Refference voltage used for logic '1' is~~

Then find out

1) Resolution of DAC
2) Analog o/p voltage for digital i/p $(1100)_2$
3) % Resolution of DAC

Solⁿ:-

4 bit

i) V_a = Resolution × decimal equivalent

2.5 = Resolution × 5

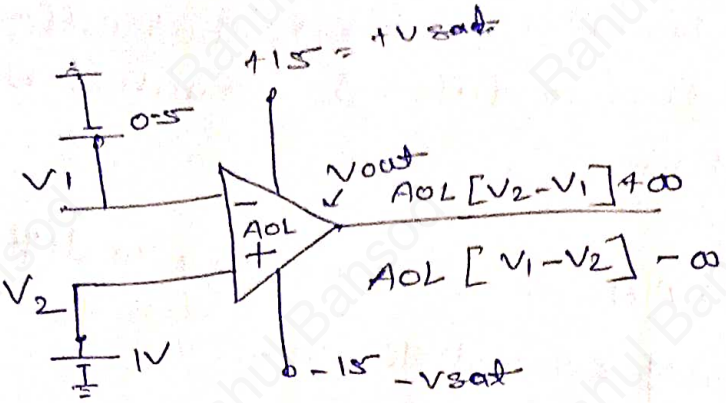
$\frac{2.5}{5}$ = Resolution

$\boxed{0.5V = \text{Resolution}}$

ii) $V_a = 0.5 \times 12 = 6V$

iii) % Resolution $= \frac{1}{(2^4-1)} \times 100 = \frac{100\%}{15} = 6.67\%$.

e.g:-



$A_{OL} \to +\infty$

$\to -\infty$

i) $V_2 = 0.3V$, $V_1 = 0.1V$

$V_{out} = A_{OL} \times 0.2 = \infty = +V_{sat}$

ii) $V_2 = 0.4V$, $V_1 = 0.1V$

$V_{out} = A_{OL} \times 0.3 = \infty = +V_{sat}$

iii) ~~Vout = AOL X~~

$V_2 = 0.5$ $V_1 = 0.1V$

$V_{out} = A_{OL} \times 0.4 = \infty = +V_{sat}$

iv) $V_2 = 0.1$, $V_1 = 0.3$

$V_{out} = A_{OL} \times (-0.2) = -\infty = -V_{sat}$

v) $V_2 = 0.1$, $V_2 = 0.4$

$V_{out} = A_{OL} (-0.3) = -\infty = -V_{sat}$

$y = kx$

$V_{out} = kV_{in}$

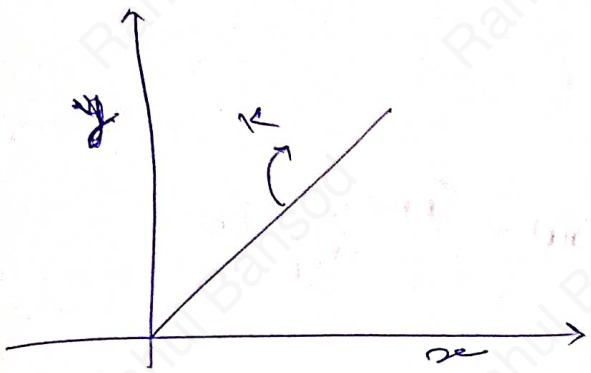
finite

$\boxed{k = 10}$

$V_{out} = 10 \times 0.2 = 2$

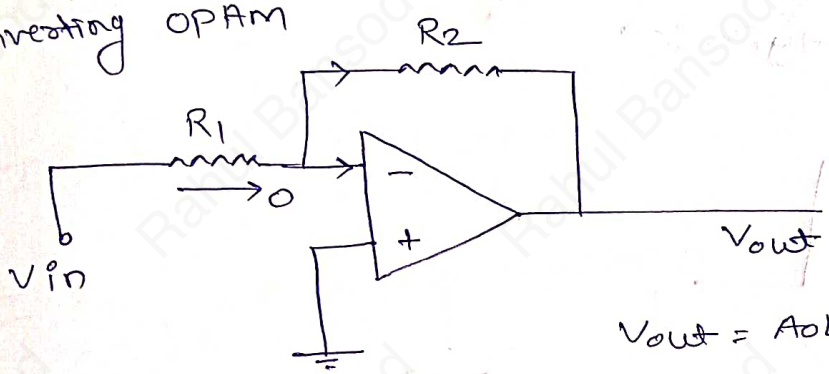
$V_{out} = 10 \times 0.3 = 3$

$V_{out} = 10 \times 0.4 = 4$



Lect - 48

inverting OPAM



$V_{out} = \text{finite}$

$V_{out} = A_{OL}\,[V_+ - V_-]$

$$\frac{V_{out}}{A_{OL}} = [V_+ - V_-]$$

$$(V_+ - V_-) = \rightarrow 0$$

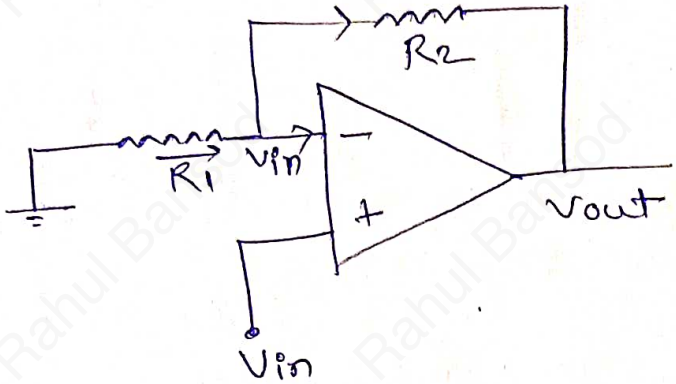
$$\frac{\infty}{\infty} = \text{finite}$$

$$\text{finite} = (V_+ - V_-)$$

$$V_+ = [V_- + \text{finite}]$$

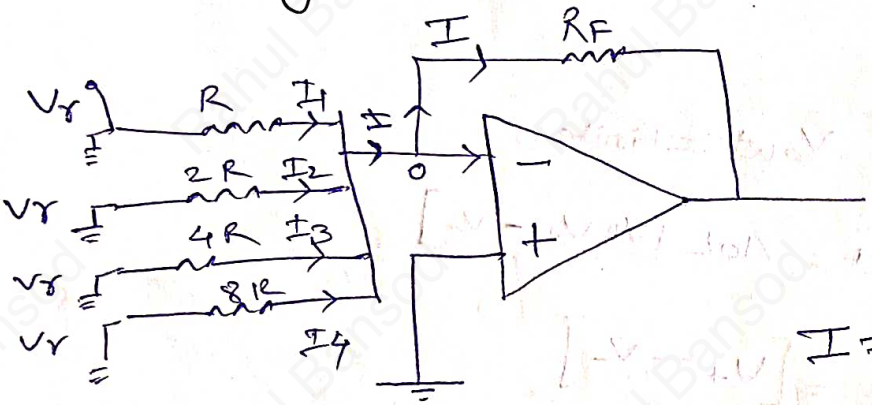
$$\frac{V_{in} - 0}{R_1} = \frac{0 - V_{out}}{R_2}$$

$$\boxed{V_{out} = \frac{-R_2}{R_1} V_{in}}$$



$$V_{out} = \left[1 + \frac{R_2}{R_1}\right] V_{in}$$

Weighted Resister type :→



$$I = I_1 + I_2 + I_3 + I_4$$

4 bit

2^3 2^2 2^1 2^0

b_3 b_2 b_1 b_0

$$I_1 = b_3 \frac{V_r}{R}$$

$$I =$$

$$I_2 = b_2 \frac{V_r}{2R}$$

$$I_3 = b_1 \frac{V_r}{4R}$$

$$I_4 = b_0 \frac{V_r}{8R}$$

$$I = b_3 \frac{V_r}{R} + b_2 \frac{V_r}{2R} + b_1 \frac{V_r}{4R} + b_0 \frac{V_r}{8R}$$

$$I = \frac{V_r}{8R}\left[b_3 \times 2^3 + b_2 \times 2^2 + b_1 \times 2^1 + b_0 \times 2^0\right]$$

$$I = \frac{V_r}{8R} \times \text{decimal Equivalent of input digital data}$$

$$I = \frac{0 - V_{out}}{R_F}$$

$$V_{out} = -I R_F = -\frac{V_r}{8} \cdot \frac{R_F}{R} \times \text{decimal equivalent of i/p digital data}$$

4 - bit

LSB resistance $= 2^3 \times$ MSB resistance

$$\boxed{\text{n-bit LSB resistance} = 2^{(n-1)} \times \text{MSB resistance}}$$

for n-bit DAC.

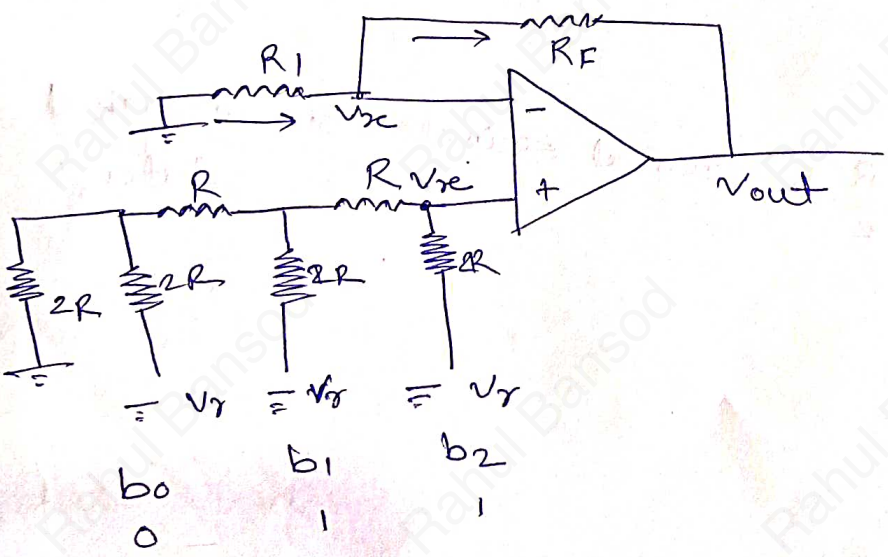
In weighted Resister type DAC if number of bits are high then to match all the Resistances (weighted Resistance) is not possible

∴ There will be error in o/p.

- To avoid this we use R-2R Ladder

R-2R - Normal Ladder

1) Non-inverting R-2R ladder



- Ladder - $(n+1)\,2R$

n-bit — $(n+1)\,2R$
$(n-1)\,R$.

Lect- 49

V_x = Resolution × decimal Equivalent of i/p digital data.

$V_x = \frac{V_r}{2^n}$ × decimal Equivalent i/p digital data

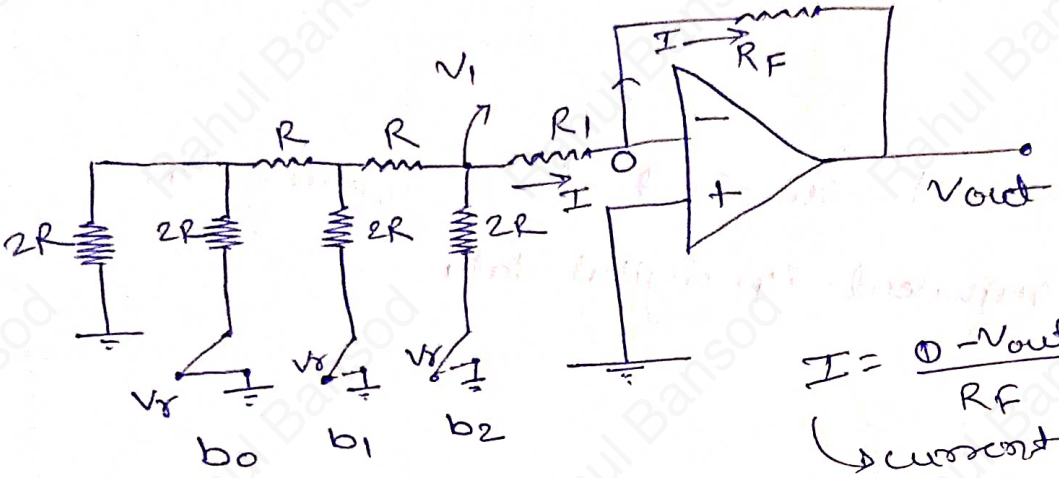
$\cancel{\frac{V_x - V_{out}}{R_F}}$ $\quad \frac{0 - V_x}{R_1} = \frac{V_x - V_{out}}{R_F}$

$$\boxed{V_{out} = \left(1 + \frac{R_F}{R_1}\right) V_x = \left(1 + \frac{R_F}{R_1}\right)\left(\frac{V_r}{2^n}\right) \times \text{decimal Equivalent of i/p digital data.}}$$

$b_2\, b_1\, b_0 \rightarrow 110 \rightarrow (6)_{10}$

- No. of 2R used in R-2R ladder in case of n-bits is $(n+1)$ and no. of R used in R-2R ladder in case of n-bit DAC is $(n-1)$

2) Inverting type R-2R Normal ladder



$I = \frac{0 - V_{out}}{R_F}$

↳ current across R_1 or R_F

$$V_{out} = \frac{-R_F}{(R_1+R)} \left(\frac{V_r}{2^n}\right) \times \text{decimal eq. of i/p digital data}$$

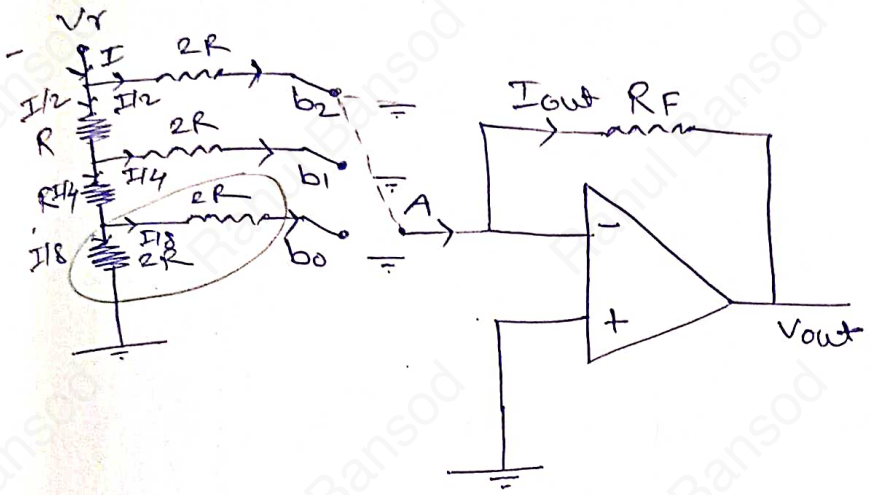
↓ resolution of DAC

$$I = \frac{V_1 - 0}{R_1}$$

$$\boxed{V_1 = IR_1}$$

2) R-2R Inverted ladder

- ~~due to switing dealy Normal Inverting ladder~~
- In case of Normal ladder due to switching delay there will be transient error's in the o/p to avoid this we have designed inverted R-2R ladder.



- The i/p bit which has to be zero will be connected to be ~~normal ground~~ A (virtual ground)

$I_{out} =$