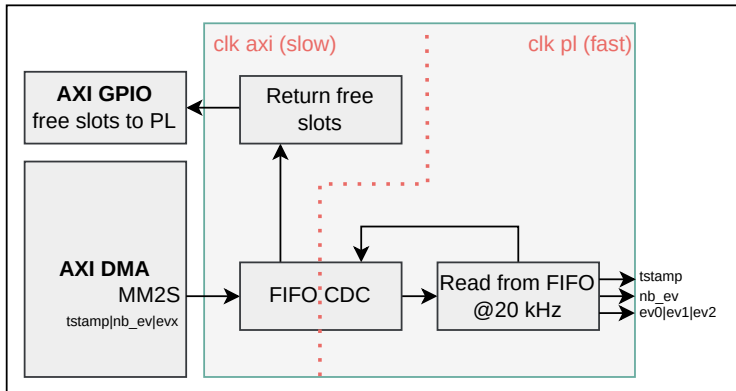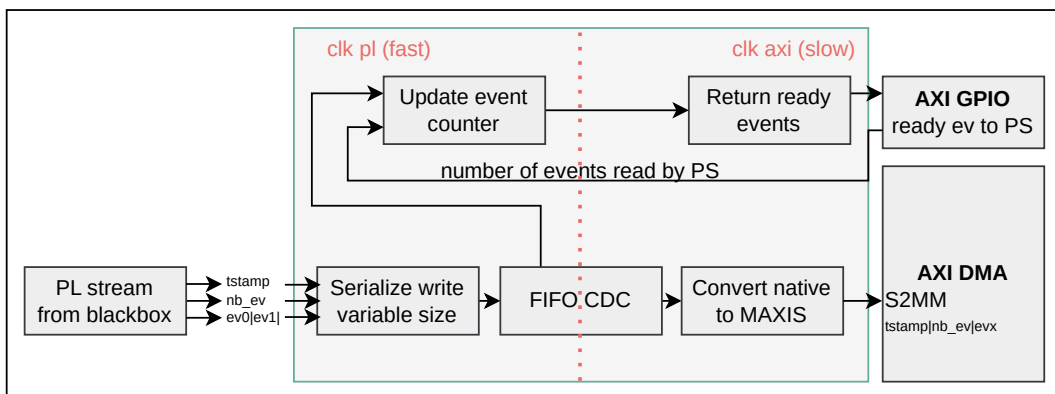SAXIS 2 NAT — Convert AXI-Stream sent by PS through DMA in AXI clock domain (slow) to native in PL clock (fast) domain

clk axi (slow)   clk pl (fast)

AXI GPIO free slots to PL

Return free slots

AXI DMA MM2S
tstamp|nb_ev|evx

FIFO CDC → Read from FIFO @20 kHz → tstamp / nb_ev / ev0|ev1|ev2

NAT 2 MAXIS — Convert stream generated by PL in PL clock (fast) domain to AXI-Stream in AXI clock (slow) to AXI DMA

clk pl (fast)   clk axi (slow)

Update event counter → Return ready events → **AXI GPIO** ready ev to PS

number of events read by PS

PL stream from blackbox → tstamp / nb_ev / ev0|ev1| → Serialize write variable size → FIFO CDC → Convert native to MAXIS → **AXI DMA** S2MM
tstamp|nb_ev|evx

Intr PL to PS — Interrupts from PL to PS are generated either on programmable threshold

In *top.vhd*

PL to PS interrupts handled withg UIO driver

AXI Lite Control

Return ready events
REGW_INTR_THRESH_FREE_SLOTS_TO_PL
>
`axi_gpio_free_slots_to_pl`

Return free slots
REGW_INTR_THRESH_READY_EV_TO_PS
>
`axi_gpio_ready_ev_to_ps`