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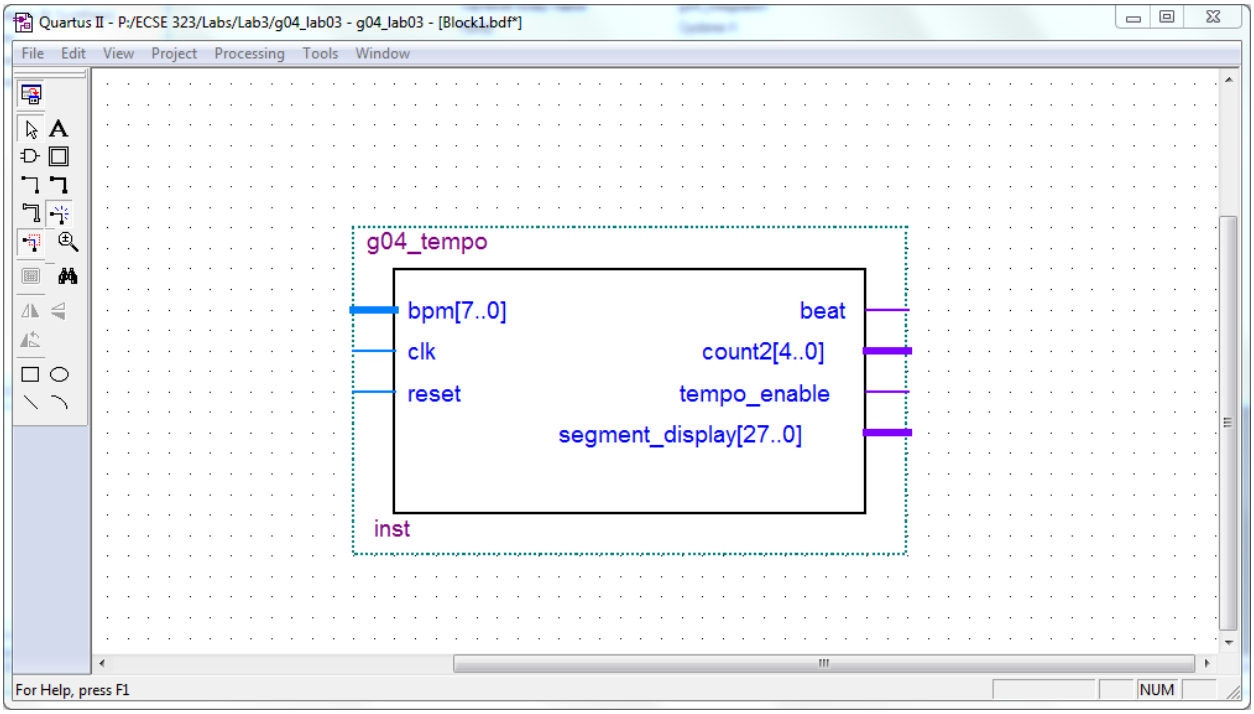
g04_tempo

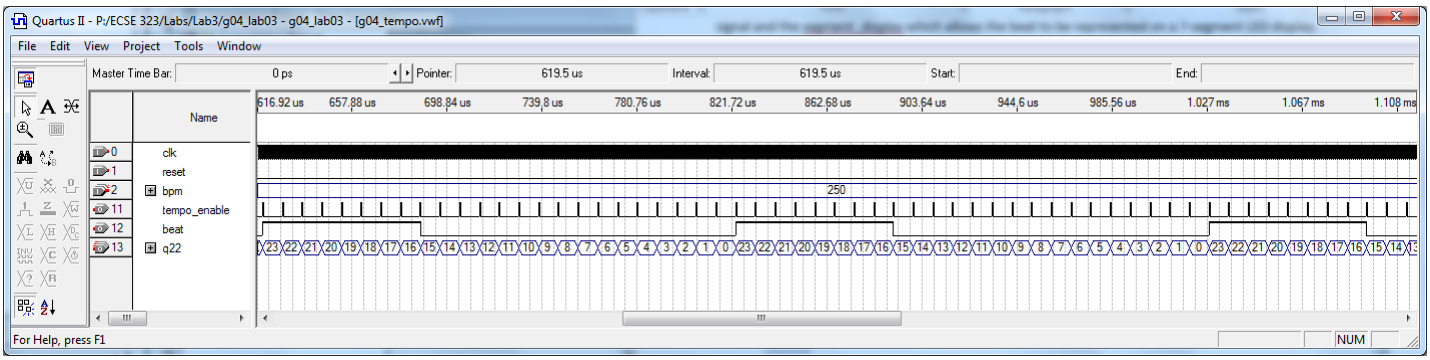
Description of Circuit Functions

The purpose of the tempo circuit is to provide a tempo for musical applications given an input of the desired beats-per-minute (bpm). The inputs are the bpm value, a clock and a reset toggle. The outputs include a beat signal representing the tempo, a tempo_enable which is a subdivision of the beat signal and the segment_display which allows the beat to be represented on a 7-segment LED display.



Testing and Simulation

The tempo circuit was tested via a timing simulation. We input 4 different bpm values to check that the tempo_enable and beat signals were responding appropriately. Below are two of the values we used to test the circuit.



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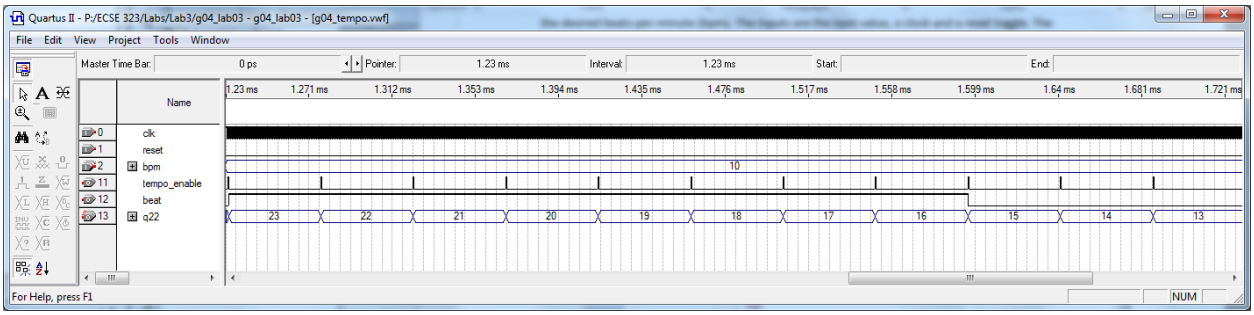
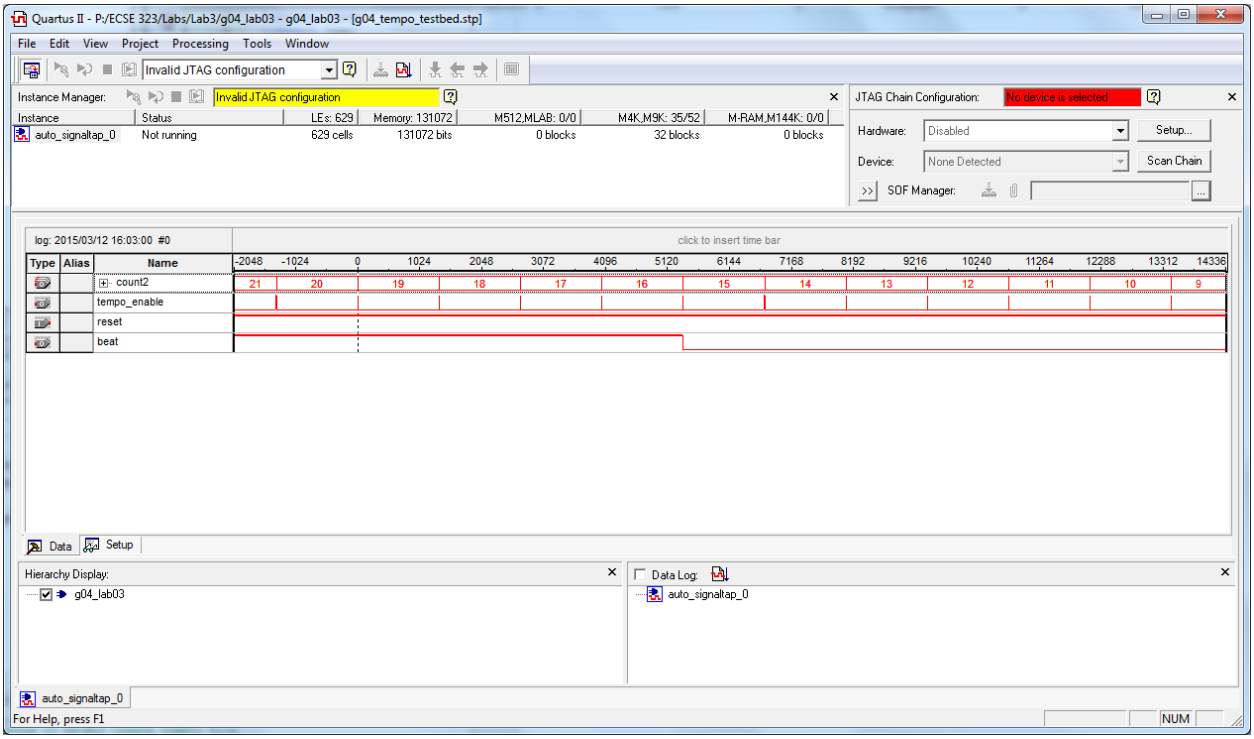


After the timing simulation, we performed a SignalTap II Logic Analysis. This would check that the circuit behaved correctly on the FPGA board. Similarly to the timing analysis results, the tempo_enable signal acts as a subdivision of the beat.



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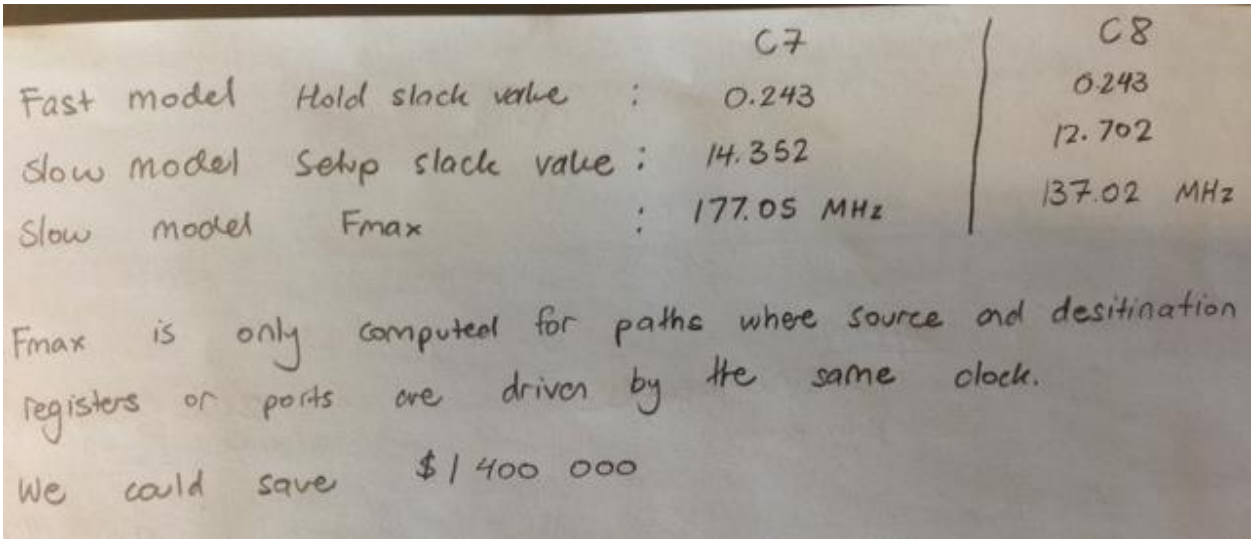
Timing performance summary –notes from in the lab:



The propogation delay of the circuit was 12.5 ns.

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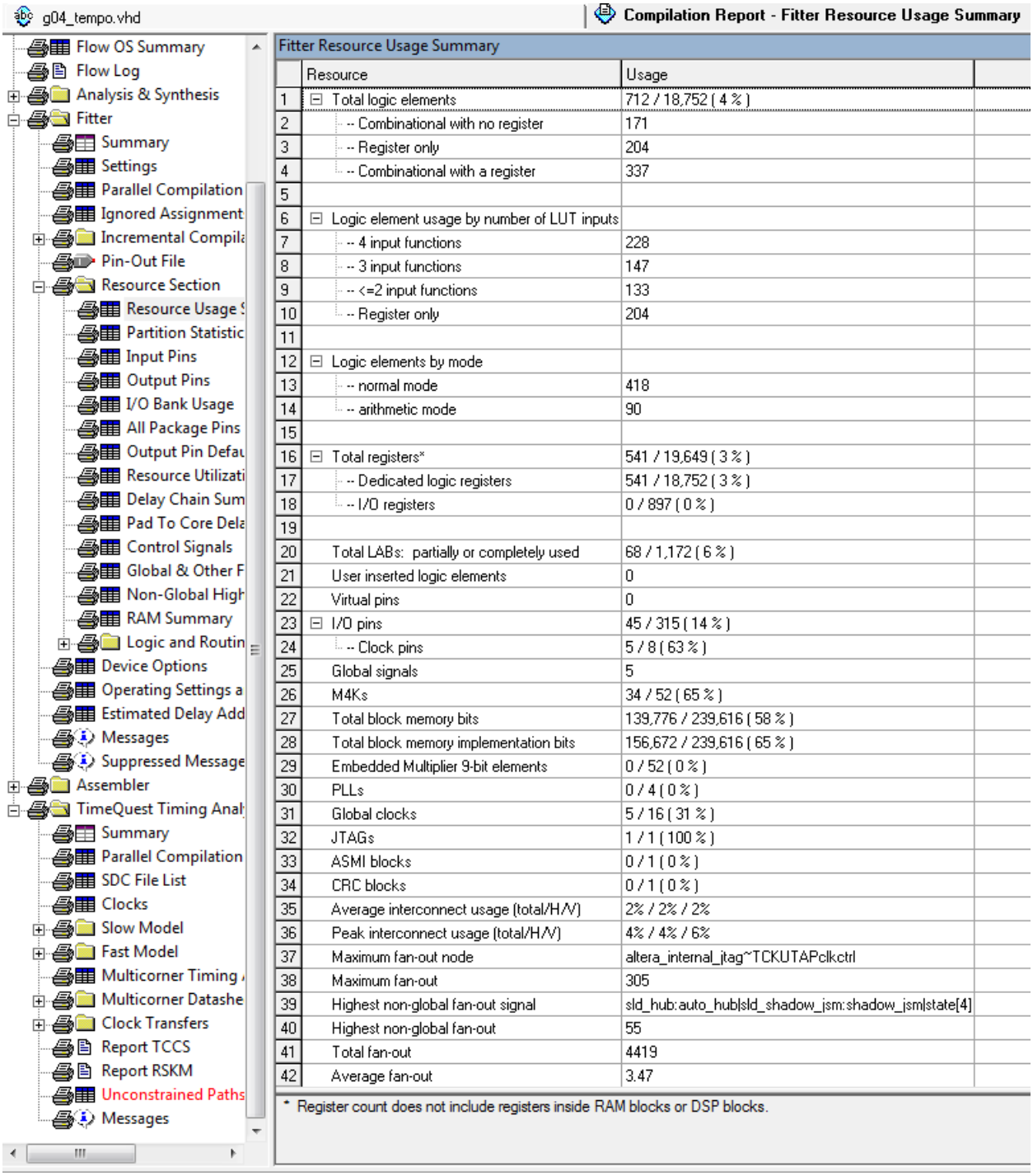
FPGA Resource Utilisation Summary:



	Resource	Usage
1	Total logic elements	712 / 18,752 (4 %)
2	-- Combinational with no register	171
3	-- Register only	204
4	-- Combinational with a register	337
5		
6	Logic element usage by number of LUT inputs	
7	-- 4 input functions	228
8	-- 3 input functions	147
9	-- <=2 input functions	133
10	-- Register only	204
11		
12	Logic elements by mode	
13	-- normal mode	418
14	-- arithmetic mode	90
15		
16	Total registers*	541 / 19,649 (3 %)
17	-- Dedicated logic registers	541 / 18,752 (3 %)
18	-- I/O registers	0 / 897 (0 %)
19		
20	Total LABs: partially or completely used	68 / 1,172 (6 %)
21	User inserted logic elements	0
22	Virtual pins	0
23	I/O pins	45 / 315 (14 %)
24	-- Clock pins	5 / 8 (63 %)
25	Global signals	5
26	M4Ks	34 / 52 (65 %)
27	Total block memory bits	139,776 / 239,616 (58 %)
28	Total block memory implementation bits	156,672 / 239,616 (65 %)
29	Embedded Multiplier 9-bit elements	0 / 52 (0 %)
30	PLLs	0 / 4 (0 %)
31	Global clocks	5 / 16 (31 %)
32	JTAGs	1 / 1 (100 %)
33	ASMI blocks	0 / 1 (0 %)
34	CRC blocks	0 / 1 (0 %)
35	Average interconnect usage (total/H/V)	2% / 2% / 2%
36	Peak interconnect usage (total/H/V)	4% / 4% / 6%
37	Maximum fan-out node	altera_internal_jtag~TCKUTAPclkctrl
38	Maximum fan-out	305
39	Highest non-global fan-out signal	sld_hub:auto_hub|sld_shadow_jsm:shadow_jsm|state[4]
40	Highest non-global fan-out	55
41	Total fan-out	4419
42	Average fan-out	3.47

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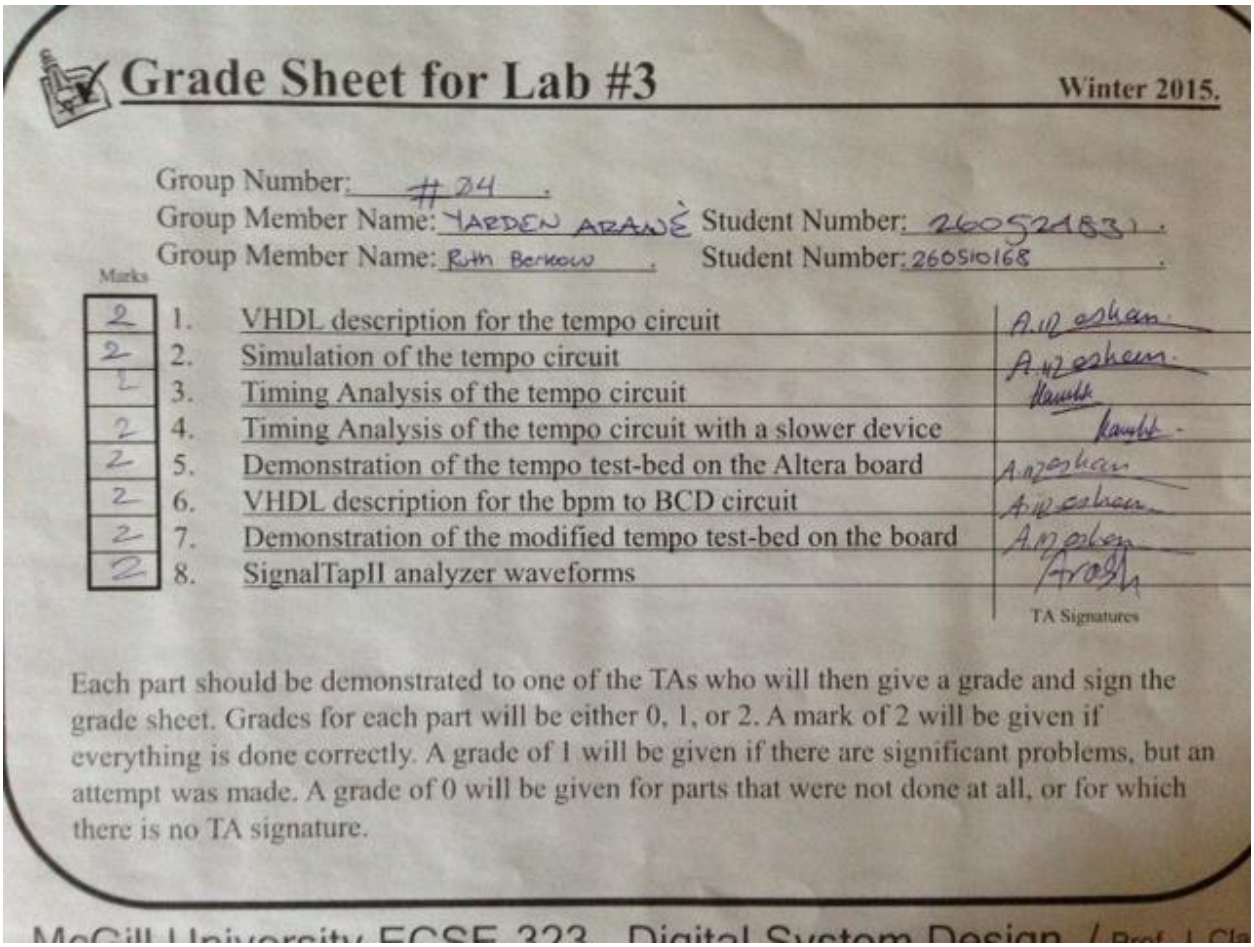

Grade Sheet for Lab #3

Winter 2015.

Group Number: #24.
Group Member Name: YARDEN ARANÉ Student Number: 260524831.
Group Member Name: Ruth Berkow. Student Number: 260510168.

Marks			TA Signatures
2	1.	VHDL description for the tempo circuit	A.Azsharn
2	2.	Simulation of the tempo circuit	A.Azsharn
2	3.	Timing Analysis of the tempo circuit	
2	4.	Timing Analysis of the tempo circuit with a slower device	
2	5.	Demonstration of the tempo test-bed on the Altera board	A.Azsharn
2	6.	VHDL description for the bpm to BCD circuit	A.Azsharn
2	7.	Demonstration of the modified tempo test-bed on the board	A.Azsharn
2	8.	SignalTapII analyzer waveforms	

Each part should be demonstrated to one of the TAs who will then give a grade and sign the grade sheet. Grades for each part will be either 0, 1, or 2. A mark of 2 will be given if everything is done correctly. A grade of 1 will be given if there are significant problems, but an attempt was made. A grade of 0 will be given for parts that were not done at all, or for which there is no TA signature.

McGill University ECSE 323 Digital System Design / Prof. J. Cl