Ruben Purdy

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EDUCATION

Carnegie Mellon University, Pittsburgh, PA   **August 2019 - Present**
PhD, Electrical and Computer Engineering
Research Advisor: Shawn Blanton
GPA: 3.93

University of Arizona, Tucson, AZ   **August 2015 - May 2019**
B.S., Computer Engineering, minor in Mathematics
Research Advisor: Ali Akoglu
Honors, *summa cum laude*

RESEARCH EXPERIENCE

Research Assistant   **August 2019 – Present**
Carnegie Mellon University Advanced Chip Test Laboratory, Pittsburgh, PA
- Researching IC manufacturing test, hardware security, and energy-efficient machine learning architectures.
- Mentored multiple undergraduate and master's students research projects.
- Served as head TA for graduate level classes, developing digital design projects and a novel auto-grader system using commercial EDA tools.

Undergraduate Research Assistant   **January 2018 – May 2019**
University of Arizona Reconfigurable Computing Laboratory, Tucson, AZ
- Explored and implemented neuromorphic architectures and algorithms.

PROFESSIONAL HISTORY

Ph.D. DFT Intern   **June 2023 – August 2023**
Apple, Cupertino, CA   **June 2024 – August 2024**
- Developed novel fault models and applied them to silicon.

Summer Academy for Math and Sciences Instructor   **June 2021**
Carnegie Mellon University, Pittsburgh, PA
- Instructed high school students and developed compute engineering curriculum

Software Developer Intern   **June 2018 – August 2018**
American Express, Scottsdale, AZ

Student iOS Developer   **November 2016 – March 2018**
University of Arizona, Tucson, AZ

PUBLICATIONS

[1]   R. Purdy, C. Nigh, W. Li and R.D. Blanton, "CHEF: CHaracterizing Elusive Logic Circuit Failures," VLSI Test Symposium. IEEE, 2025. [To Appear]

[2]   C. Nigh, R. Purdy, W. Li, S. Mitra and R.D. Blanton, "Faulty Function Extraction for Defective Circuits," European Test Symposium. IEEE, 2024.

[3]   Wei Li, Ruben Purdy, Jose Moura, Shawn Blanton, "Characterize the ability of GNNs in attacking logic locking", Workshop on Machine Learning for CAD. ACM/IEEE, 2023.

[4]   Y. Qin, R. Purdy, A. Probst, C. Lin, and J. Zhu. "Non-linear CNN-based Read Channel for Hard Disk Drive with 30% Error Rate Reduction and Sequential 200Mbits/second Throughput in 28nm CMOS," *Journal of Solid-State Circuits*. IEEE, 2023.

[5]   Y. Qin, R. Purdy, A. Probst, C. Lin, and J. Zhu. "ASIC Implementation of Non-linear CNN-based Data Detector for TDMR System in 28nm CMOS at 200Mbits/s Throughput," *Transactions on Magnetics*. IEEE, 2022.

[6]   Y. Qin, R. Purdy, A. Probst, C. Lin, and J. Zhu. "Non-linear CNN-based Read Channel for Hard Disk Drive with 30% Error Rate Reduction and Sequential 200Mbits/second Throughput in 28nm CMOS," *Symposium on VLSI Circuits*. IEEE, 2022.

[7]   R. Purdy and R.D. Blanton. "Large-Scale Logic-Locking Attacks via Simulation," *International Symposium on Quality Electronic Design*. IEEE, 2022.

[8]   J. Sweeney, R. Purdy, R.D. Blanton, and L. Pileggi. "CircuitGraph: A Python Package for Boolean Circuits," *Journal of Open Source Software.* 2020.

[9]   J. Mack, et al. "RANC: Reconfigurable Architecture for Neuromorphic Computing." *Transactions on Computer-Aided Design of Integrated Circuits and Systems*. IEEE, 2020.

[10] S. Valancius, et al. "FPGA Based Emulation Environment for Neuromorphic Architectures," *International Parallel and Distributed Processing Symposium Workshops*. IEEE, 2020.

POSTERS

[11] R.D. Blanton, D. Duvalsaint, R. Purdy, "Security Metrics for Logic Circuits", *International Symposium on Hardware Oriented Security and Trust*. IEEE, 2022.

[12] R. Purdy, et al. "Architectures and Applications of Neuromorphic Computing", *I/UCRC on Cloud and Autonomic Computing, Semiannual Industry Advisory Board Meeting*. NSF, 2018.

HONORS & AWARDS

Carnegie Mellon University, Pittsburgh, PA
Qualcomm Innovation Fellowship   **2024**

Carnegie Mellon University, Pittsburgh, PA
Apple PhD Fellowship in Integrated Systems   **2024**

Carnegie Mellon University, Pittsburgh, PA

David H. Barakat and LaVerne Owen-Barakat Dean's Fellowship   **2021**

University of Arizona, Tucson, AZ
Wildcat Excellence Scholarship   **2015 - 2019**

University of Arizona, Tucson, AZ
Dean's List with Distinction   **2016-2017**

SKILLS

- Extensive experience in Python (both scripting and creation/maintenance of codebases)
- Extensive experience with SystemVerilog, TCL, and various EDA tools including:
  - Cadence Xcelium and Synopsys VCS
  - Cadence Genus, Cadence Innovus, Synopsys DesignCompiler. And Vivado
  - Siemens Tessent
  - Various open-source tools such as Verilator, Icarus Verilog, ABC, and Yosys
- Experience with shell scripting, C, C++, Java, TypeScript