Ruben Purdy

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EDUCATION

Carnegie Mellon University, Pittsburgh, PA **August 2019 – September 2025**
Ph.D., Electrical and Computer Engineering
Research Advisor: Shawn Blanton
GPA: 3.93

University of Arizona, Tucson, AZ **August 2015 - May 2019**
B.S., Computer Engineering, minor in Mathematics
Research Advisor: Ali Akoglu
Honors, *summa cum laude*

RESEARCH EXPERIENCE

Research Assistant **August 2019 – September 2025**
Carnegie Mellon University Advanced Chip Test Laboratory, Pittsburgh, PA

- Dissertation on logic circuit test and diagnosis.
  - Investigated novel physically-aware fault model.
  - Invented novel diagnosis methodology that outperforms state-of-the-art commercial offerings.
  - Created comprehensive interactive diagnosis tool that seamlessly integrates with EDA software to perform novel diagnosis on modern large-scale industrial designs with various functionalities including:
    - Novel SPICE-based failure characterization
    - Diagnostic test pattern generation
    - Flexible, user-driven fault modeling and localization
    - Performant layout visualization
  - Developed novel test pattern generation flow to optimize and scale test pattern generation for large-scale industrial designs targeting complex fault models.
    - Uses distributed computing to scale across multiple compute nodes
    - Integrates with existing commercial EDA tools for optimal performance
    - Includes other significant optimizations enabled by custom flow
- Additional research in hardware security and energy-efficient machine learning
  - Investigated cryptography-informed methodologies for hardware reverse-engineering and overproduction protection with provable security.
  - Designed, implemented, verified, and taped-out novel ASIC for hard disk drive data detection. Successfully verified post-silicon performance.
- Mentored over ten undergraduate and master's students research projects.
- Served as head TA for graduate level classes, developing digital design projects and a novel auto-grader system using commercial EDA tools.

Undergraduate Research Assistant **January 2018 – May 2019**
University of Arizona Reconfigurable Computing Laboratory, Tucson, AZ

- Explored and implemented neuromorphic architectures and algorithms.

PROFESSIONAL HISTORY

Ph.D. DFT Intern **June 2023 – August 2023**
Apple, Cupertino, CA **June 2024 – August 2024**

- Developed novel fault models and applied them to silicon.
- Developed various improvements to DFT flow, *e.g.*, to improve post-silicon debug.

Summer Academy for Math and Sciences Instructor **June 2021**
Carnegie Mellon University, Pittsburgh, PA

- Instructed high school students
- Developed computer engineering and AI curriculum from scratch.

Software Developer Intern **June 2018 – August 2018**
American Express, Scottsdale, AZ

Student iOS Developer **November 2016 – March 2018**
University of Arizona, Tucson, AZ

PUBLICATIONS

[1] R. Purdy, et al. "Region-based Characterization of Defective Logic Circuits," International Symposium for Testing and Failure Analysis. ACM, 2025. [To appear]

[2] Wei Li, et al. "BRIDGES: Bridging Graph Modality and Large Language Models within EDA Tasks," International Conference on LLM-Aided Design. IEEE, 2025.

[3] C. Nigh, R. Purdy, W. Li, S. Mitra, and R.D. Blanton, "IC-PEPR: PEPR Testing Goes Intra-Cell," International Test Symposium. IEEE, 2025.

[4] R. Purdy, C. Nigh, W. Li and R.D. Blanton, "CHEF: CHaracterizing Elusive Logic Circuit Failures," VLSI Test Symposium. IEEE, 2025.

[5] C. Nigh, R. Purdy, W. Li, S. Mitra and R.D. Blanton, "Faulty Function Extraction for Defective Circuits," European Test Symposium. IEEE, 2024.

[6] Wei Li, Ruben Purdy, Jose Moura, Shawn Blanton, "Characterize the ability of GNNs in attacking logic locking", Workshop on Machine Learning for CAD. ACM/IEEE, 2023.

[7] Y. Qin, R. Purdy, A. Probst, C. Lin, and J. Zhu. "Non-linear CNN-based Read Channel for Hard Disk Drive with 30% Error Rate Reduction and Sequential 200Mbits/second Throughput in 28nm CMOS," *Journal of Solid-State Circuits*. IEEE, 2023.

[8] Y. Qin, R. Purdy, A. Probst, C. Lin, and J. Zhu. "ASIC Implementation of Non-linear CNN-based Data Detector for TDMR System in 28nm CMOS at 200Mbits/s Throughput," *Transactions on Magnetics*. IEEE, 2022.

[9] Y. Qin, R. Purdy, A. Probst, C. Lin, and J. Zhu. "Non-linear CNN-based Read Channel for Hard Disk Drive with 30% Error Rate Reduction and Sequential 200Mbits/second Throughput in 28nm CMOS," *Symposium on VLSI Circuits*. IEEE, 2022.

[10] R. Purdy and R.D. Blanton. “Large-Scale Logic-Locking Attacks via Simulation,” *International Symposium on Quality Electronic Design*. IEEE, 2022.

[11] J. Sweeney, R. Purdy, R.D. Blanton, and L. Pileggi. “CircuitGraph: A Python Package for Boolean Circuits,” *Journal of Open Source Software.* 2020.

[12] J. Mack, et al. "RANC: Reconfigurable Architecture for Neuromorphic Computing." *Transactions on Computer-Aided Design of Integrated Circuits and Systems*. IEEE, 2020.

[13] S. Valancius, et al. “FPGA Based Emulation Environment for Neuromorphic Architectures,” *International Parallel and Distributed Processing Symposium Workshops*. IEEE, 2020.

POSTERS

[14] R.D. Blanton, D. Duvalsaint, R. Purdy, “Security Metrics for Logic Circuits”, *International Symposium on Hardware Oriented Security and Trust*. IEEE, 2022.

[15] R. Purdy, et al. "Architectures and Applications of Neuromorphic Computing", *I/UCRC on Cloud and Autonomic Computing, Semiannual Industry Advisory Board Meeting*. NSF, 2018.

HONORS & AWARDS

Carnegie Mellon University, Pittsburgh, PA
Qualcomm Innovation Fellowship **2024**

Carnegie Mellon University, Pittsburgh, PA
Apple PhD Fellowship in Integrated Systems **2024**

Carnegie Mellon University, Pittsburgh, PA
David H. Barakat and LaVerne Owen-Barakat Dean's Fellowship **2021**

University of Arizona, Tucson, AZ
Wildcat Excellence Scholarship **2015 - 2019**

University of Arizona, Tucson, AZ
Dean’s List with Distinction **2016-2017**

SKILLS

- Extensive experience in Python
  - Created and maintained large libraries and codebases that have integrated EDA-tool interaction and scripting, complex custom logic, database interaction, and distributed computing
  - Built tooling and automation around these codebases, including modern Python package management, monorepo management and continuous integration
- Extensive experience with SystemVerilog, TCL, and various EDA tools including:
  - Cadence Xcelium and Synopsys VCS
  - Cadence Genus, Cadence Innovus, Synopsys DesignCompiler. And Vivado
  - Siemens Tessent
  - Various open-source tools such as Verilator, Icarus Verilog, ABC, and Yosys
- Experience with end-to-end chip tape-out and testing
  - Taped out a machine-learning accelerator in TSMC 28nm technology with published results (publications 6,7,8)
  - Wrote RTL, performed commercial synthesis and place-and-route and chip finishing
  - Used FGPA to interface with and test fabricated chips
- Industrial and research experience with DFT insertion, ATPG using commercial tools
- Experience with shell scripting, C, C++, Java, TypeScript, Cadence SKILL
- Well versed with LLM coding tools and agentic development
- Passionate about code quality, automation, and productivity for silicon development