Section 22. Basic 8-bit A/D Converter

HIGHLIGHTS

This section of the manual contains the following major topics:

22.1 Introduction 22-2
22.2 Control Registers 22-3
22.3 A/D Acquisition Requirements 22-6
22.4 Selecting the A/D Conversion Clock 22-8
22.5 Configuring Analog Port Pins 22-10
22.6 A/D Conversions 22-11
22.7 A/D Operation During Sleep 22-14
22.8 A/D Accuracy/Error 22-15
22.9 Effects of a RESET 22-16
22.10 Connection Considerations 22-16
22.11 Transfer Function 22-16
22.12 Initialization 22-17
22.13 Design Tips 22-18
22.14 Related Application Notes 22-19
22.15 Revision History 22-20

Note: Please refer to Appendix C.2 or the device Data Sheet to determine which devices use this module.

22.1 Introduction

This Analog-to-Digital (A/D) converter module has four analog inputs.

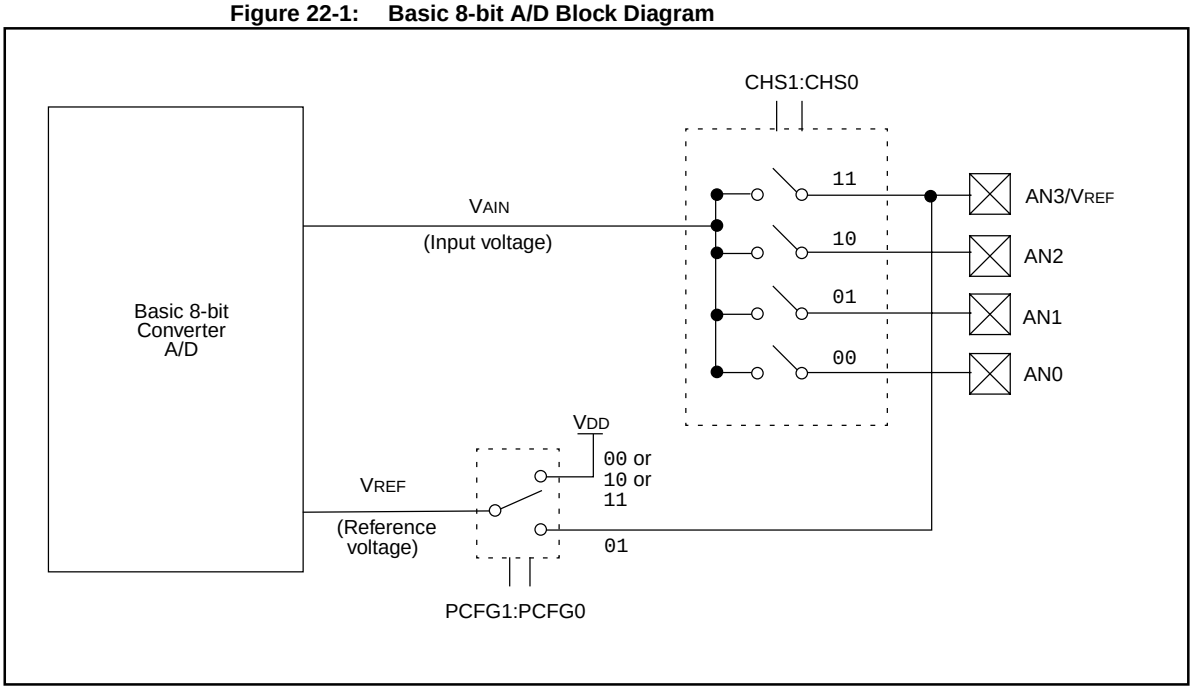
The A/D allows conversion of an analog input signal to a corresponding 8-bit digital number. The output of the sample and hold is the input into the converter, which generates the result via successive approximation. The analog reference voltage is software selectable to either the device's positive supply voltage (V_{DD}) or the voltage level on the AN3/V_{REF} pin. The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode.

The A/D module has three registers. These registers are:

- A/D Result Register (ADRES)
- A/D Control Register0 (ADCON0)
- A/D Control Register1 (ADCON1)

The ADCON0 register, shown in Figure 22-1 controls the operation of the A/D module. The ADCON1 register, shown in Figure 22-2, configures the functions of the port pins. The port pins can be configured as analog inputs (or a voltage reference) or as digital I/O.

Figure 22-1: Basic 8-bit A/D Block Diagram



22.2 Control Registers

Register 22-1: ADCON0 Register

R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADCS1	ADCS0	— (1)	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADIF / — (2)	ADON
bit 7							bit 0

bit 7:6 **ADCS1:ADCS0:** A/D Conversion Clock Select bits
00 = FOSC/2
01 = FOSC/8
10 = FOSC/32
11 = FRC (clock derived from the internal A/D RC oscillator)

bit 5 **Unimplemented**: Read as '0'.

bit 4:3 **CHS1:CHS0**: Analog Channel Select bits
00 = channel 0, (AN0)
01 = channel 1, (AN1)
10 = channel 2, (AN2)
11 = channel 3, (AN3)

bit 2 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
If ADON = 1
1 = A/D conversion in progress (setting this bit starts the A/D conversion)
0 = A/D conversion not in progress (This bit is automatically cleared by hardware when the A/D conversion is complete)

bit 1 **ADIF (2):** A/D Conversion Complete Interrupt Flag bit
1 = conversion is complete (must be cleared in software)
0 = conversion is not complete

bit 0 **ADON:** A/D On bit
1 = A/D converter module is operating
0 = A/D converter module is shutoff and consumes no operating current

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

Note 1: For the PIC16C71, Bit5 of ADCON0 is a General Purpose R/W bit. For the PIC16C710/711/715, this bit is unimplemented, read as '0'.

Note 2: For the PIC12CXXX devices, this bit is reserved. The ADIF bit is implemented in the PIR register. Use of this bit a a general purpose R/W bit is not recommended. Always maintain this bit cleared.

Register 22-2: ADCON1 Register

U-0	U-0	U-0	U-0	U-0	U-0 / R/W-0	R/W-0	R/W-0
—	—	—	—	—	— / PCFG2 (1)	PCFG1	PCFG0
bit 7							bit 0

bit 7:2 **Unimplemented:** Read as '0'

Note: Some devices implement bit2 as the PCFG2 bit.

bit 1:0 **PCFG1:PCFG0**: A/D Port Configuration Control bits

PCFG1:PCFG0	AN3	AN2	AN1	AN0
00	A	A	A	A
01	VREF+	A	A	A
10	D	D	A	A
11	D	D	D	D

A = Analog input

D = Digital I/O

Note: When AN3 is selected as VREF+, the A/D reference is the voltage on the AN3 pin. When AN3 is selected as an analog input (A), then the voltage reference for the A/D is the device VDD.

bit 2:0 **PCFG2:PCFG0**: A/D Port Configuration Control bits (1)

PCFG2:PCFG0	AN3	AN2	AN1	AN0
000	A	A	A	A
001	A	A	VREF+	A
010	D	A	A	A
011	D	A	VREF+	A
100	D	D	A	A
101	D	D	VREF+	A
110	D	D	D	A
111	D	D	D	D

A = Analog input

D = Digital I/O

Note: When AN1 is selected as VREF+, the A/D reference is the voltage on the AN1 pin. When AN1 is selected as an analog input (A), then the voltage reference for the A/D is the device VDD.

Legend

R = Readable bit W = Writable bit

U = Unimplemented bit, read as '0' - n = Value at POR reset

Note 1: Some devices add an additional Port configuration bit (PCFG2). This allows the minimum number of analog channels to be one. This is of most benefit to the 8-pin devices with the A/D converter, since in an 8-pin device I/O is a premium resource. In the other devices this bit is unimplemented, and read as '0'.

Note 2: On any device reset, the Port pins multiplexed with analog functions (ANx) are forced to be an analog input.

The ADRES register contains the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRES register, the GO/$\overline{\text{DONE}}$ bit (ADCON0<2>) is cleared, and A/D interrupt flag bit ADIF is set. The block diagram of the A/D module is shown in Figure 22-1.

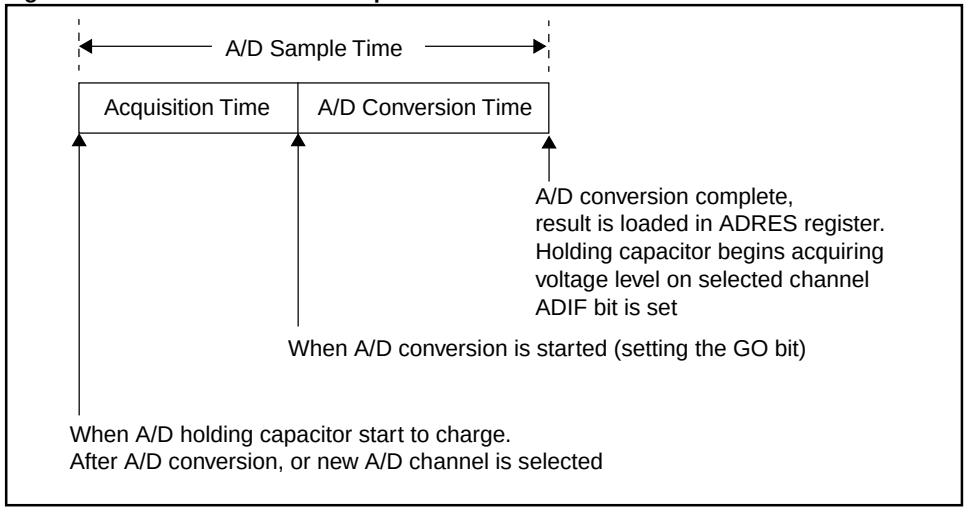
After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine sample time, see Subsection **22.3 "A/D Acquisition Requirements"** After this acquisition time has elapsed the A/D conversion can be started. The following steps should be followed for doing an A/D conversion:

1. Configure the A/D module:
   - Configure analog pins / voltage reference / and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D conversion clock (ADCON0)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear the ADIF bit
   - Set the ADIE bit
   - Set the GIE bit
3. Wait the required acquisition time.
4. Start conversion:
   - Set the GO/$\overline{\text{DONE}}$ bit (ADCON0)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared

   OR
   - Waiting for the A/D interrupt
6. Read A/D Result register (ADRES), clear the ADIF bit, if required.
7. For next conversion, go to step 1 or step 2 as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2TAD is required before next acquisition starts.

Figure 22-2 shows the conversion sequence, and the terms that are used. Acquisition time is the time that the A/D module's holding capacitor is connected to the external voltage level. Then there is the conversion time of 10 TAD, which is started when the GO bit is set. The sum of these two times is the sampling time. There is a minimum acquisition time to ensure that the holding capacitor is charged to a level that will give the desired accuracy for the A/D conversion.

Figure 22-2: A/D Conversion Sequence



22.3 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 22-3. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 22-3. **The maximum recommended impedance for analog sources is 10 kΩ.** After the analog input channel is selected (changed) this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 22-1 may be used. This equation assumes that 1/2 LSb error is used (512 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Equation 22-1: Acquisition Time

$$\begin{aligned} T_{ACQ} &= \text{Amplifier Settling Time} + \\ &\quad \text{Holding Capacitor Charging Time} + \\ &\quad \text{Temperature Coefficient} \\ &= T_{AMP} + T_C + T_{COFF} \end{aligned}$$

Equation 22-2: A/D Minimum Charging Time

$$V_{HOLD} = (V_{REF} - (V_{REF}/512)) \cdot (1 - e^{(-T_C/C_{HOLD}(R_{IC} + R_{SS} + R_S))})$$

or

$$T_C = -(51.2\ pF)(1\ k\Omega + R_{SS} + R_S) \ln(1/511)$$

Example 22-1 shows the calculation of the minimum required acquisition time TACQ. This calculation is based on the following system assumptions.

Rs	=	10 kΩ	
Conversion Error	≤	1/2 LSb	
VDD	=	5V → Rss = 7 kΩ	(see graph in Figure 22-3)
Temperature	=	50°C (system max.)	
VHOLD	=	0V @ time = 0	

Example 22-1: Calculating the Minimum Required Acquisition Time

$$T_{ACQ} = T_{AMP} + T_C + T_{COFF}$$

$$T_{ACQ} = 5\ \mu s + T_C + [(Temp - 25°C)(0.05\ \mu s/°C)]$$

$$\begin{aligned} T_C &= -C_{HOLD}(R_{IC} + R_{SS} + R_S) \ln(1/512) \\ &= -51.2\ pF\ (1\ k\Omega + 7\ k\Omega + 10\ k\Omega) \ln(0.0020) \\ &= -51.2\ pF\ (18\ k\Omega) \ln(0.0020) \\ &= -0.921\ \mu s\ (-6.2146) \\ &= 5.724\ \mu s \end{aligned}$$

$$\begin{aligned} T_{ACQ} &= 5\ \mu s + 5.724\ \mu s + [(50°C - 25°C)(0.05\ \mu s/°C)] \\ &= 10.724\ \mu s + 1.25\ \mu s \\ &= 11.974\ \mu s \end{aligned}$$

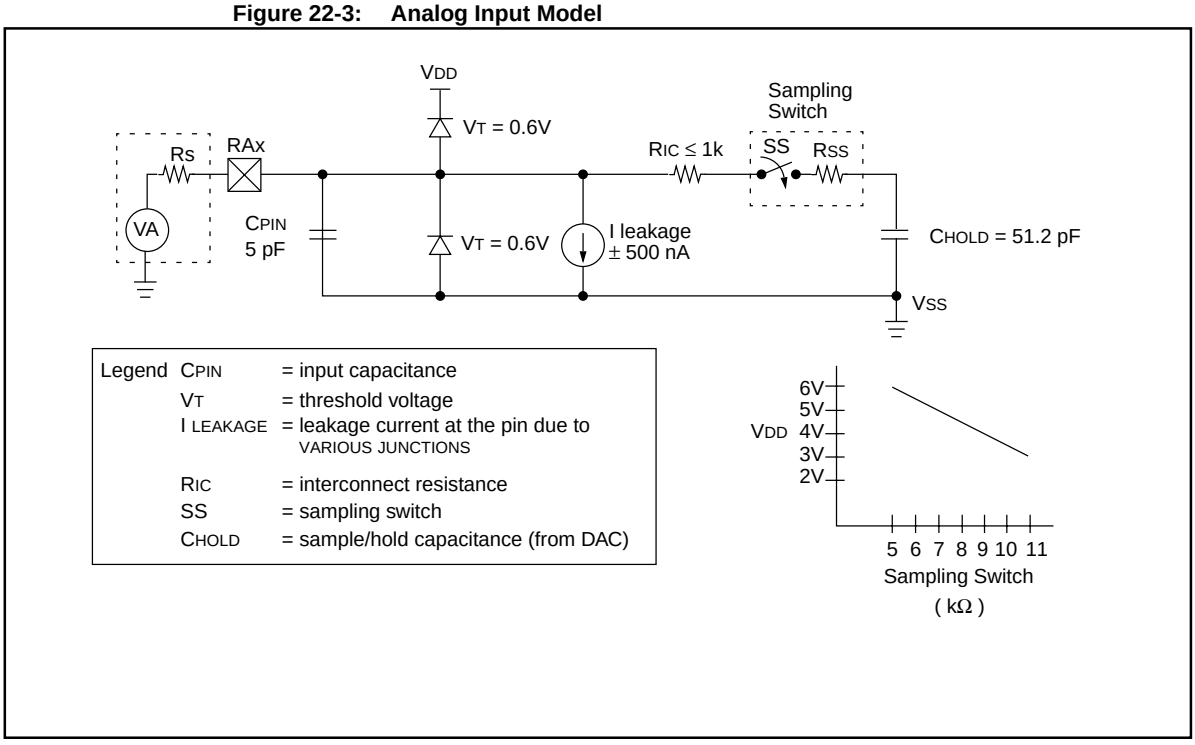
Note 1: The reference voltage (VREF) has no effect on the equation, since it cancels itself out.

Note 2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

Note 3: The maximum recommended impedance for analog sources is 10 kΩ. This is required to meet the pin leakage specification.

Note 4: After a conversion has completed, a 2.0 TAD delay must complete before acquisition can begin again. During this time the holding capacitor is not connected to the selected A/D input channel.

Figure 22-3: Analog Input Model



22.4 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 9.5 TAD per 8-bit conversion. The source of the A/D conversion clock is software selected. The four possible options for TAD are:

- 2TOSC
- 8TOSC
- 32TOSC
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of:

2.0 µs for the PIC16C71, as shown in parameter 130 of devices electrical specifications.

1.6 µs for all other devices, as shown in parameter 130 of devices electrical specifications.

Table 22-1 through Table 22-4 show the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

Table 22-1: TAD vs. Device Operating Frequencies, All Devices (except PIC16C71) (C Devices)

AD Clock Source (TAD)		Device Frequency			
Operation	**ADCS1:ADCS0**	**20 MHz**	**5 MHz**	**1.25 MHz**	**333.33 kHz**
2TOSC	00	100 ns(2)	400 ns(2)	1.6 µs	6 µs
8TOSC	01	400 ns(2)	1.6 µs	6.4 µs	24 µs(3)
32TOSC	10	1.6 µs	6.4 µs	25.6 µs(3)	96 µs(3)
RC(5)	11	2 - 6 µs(1,4)	2 - 6 µs(1,4)	2 - 6 µs(1,4)	2 - 6 µs(1)

Note 1: The RC source has a typical TAD time of 4 µs.
2: These values violate the minimum required TAD time.
3: For faster conversion times, the selection of another clock source is recommended.
4: For device frequencies above 1 MHz, the device must be in SLEEP for the entire conversion, or the A/D accuracy may be out of specification.

Table 22-2: TAD vs. Device Operating Frequencies, All Devices (except PIC16LC71) (LC Devices)

AD Clock Source (TAD)		Device Frequency			
Operation	**ADCS1:ADCS0**	**4 MHz**	**2 MHz**	**1.25 MHz**	**333.33 kHz**
2TOSC	00	500 ns(2)	1.0 µs(2)	1.6 µs(2)	6 µs
8TOSC	01	2.0 µs(2)	4.0 µs	6.4 µs	24 µs(3)
32TOSC	10	8.0 µs	16.0 µs	25.6 µs(3)	96 µs(3)
RC(5)	11	3 - 9 µs(1,4)	3 - 9 µs(1,4)	3 - 9 µs(1,4)	3 - 9 µs(1)

Note 1: The RC source has a typical TAD time of 6 µs.
2: These values violate the minimum required TAD time.
3: For faster conversion times, the selection of another clock source is recommended.
4: For device frequencies above 1 MHz, the device must be in SLEEP for the entire conversion, or the A/D accuracy may be out of specification.

Table 22-3: TAD vs. Device Operating Frequencies, PIC16C71 (C Devices)

AD Clock Source (TAD)		Device Frequency				
Operation	**ADCS1:ADCS0**	**20 MHz**	**16 MHz**	**4 MHz**	**1 MHz**	**333.33 kHz**
2TOSC	00	100 ns(2)	125 ns(2)	500 ns(2)	2.0 µs	6 µs
8TOSC	01	400 ns(2)	500 ns(2)	2.0 µs	8.0 µs	24 µs(3)
32TOSC	10	1.6 µs(2)	2.0 µs	8.0 µs	32.0 µs(3)	96 µs(3)
RC	11	2 - 6 µs(1,4)	2 - 6 µs(1,4)	2 - 6 µs(1,4)	2 - 6 µs(1)	2 - 6 µs(1)

Legend: Shaded cells are outside of recommended range.
Note 1: The RC source has a typical TAD time of 4 µs.
2: These values violate the minimum required TAD time.
3: For faster conversion times, the selection of another clock source is recommended.
4: For device frequencies above 1 MHz, the device must be in SLEEP for the entire conversion, or the A/D accuracy may be out of specification.

Table 22-4: TAD vs. Device Operating Frequencies, PIC16LC71 (LC Devices)

AD Clock Source (TAD)		Device Frequency			
Operation	**ADCS1:ADCS0**	**4 MHz**	**2 MHz**	**1.25 MHz**	**333.33 kHz**
2TOSC	00	500 ns(2)	1.0 µs(2)	1.6 µs(2)	6 µs
8TOSC	01	2.0 µs(2)	4.0 µs	6.4 µs	24 µs(3)
32TOSC	10	8.0 µs	16.0 µs	25.6 µs(3)	96 µs(3)
RC	11	3 - 9 µs(1,4)	3 - 9 µs(1,4)	3 - 9 µs(1,4)	3 - 9 µs(1)

Legend: Shaded cells are outside of recommended range.
Note 1: The RC source has a typical TAD time of 6 µs.
2: These values violate the minimum required TAD time.
3: For faster conversion times, the selection of another clock source is recommended.
4: For device frequencies above 1 MHz, the device must be in SLEEP for the entire conversion, or the A/D accuracy may be out of specification.

22.5 Configuring Analog Port Pins

The ADCON1 and TRISA registers control the operation of the A/D port pins. The port pins that are desired as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (V_{OH} or V_{OL}) will be converted.

The A/D operation is independent of the state of the CHS1:CHS0 bits and the TRIS bits.

Note 1: When reading the port register, all pins configured as analog input channel will read as cleared (a low level). Pins configured as digital inputs, will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

Note 2: Analog levels on any pin that is defined as a digital input (including the AN3:AN0 pins), may cause the input buffer to consume current that is out of the devices specification.

22.6 A/D Conversions

Example 22-2 show how to perform an A/D conversion. The RA pins are configured as analog inputs. The analog reference (VREF) is the device VDD. The A/D interrupt is enabled, and the A/D conversion clock is FRC. The conversion is performed on the RA0 channel.

Note:	The GO/$\overline{\text{DONE}}$ bit should **NOT** be set in the same instruction that turns on the A/D, due to the required acquisition time.

Clearing the GO/$\overline{\text{DONE}}$ bit during a conversion will abort the current conversion. The ADRES register will NOT be updated with the partially completed A/D conversion sample. That is, the ADRES register will continue to contain the value of the last completed conversion (or the last value written to the ADRES register). After the A/D conversion is aborted, a 2TAD wait is required before the next acquisition is started. After this 2TAD wait, an acquisition is automatically started on the selected channel.

Example 22-2: Doing an A/D Conversion

```
     BSF     STATUS, RP0    ; Select Bank1
     CLRF    ADCON1         ; Configure A/D inputs
     BCF     STATUS, RP0    ; Select Bank0
     MOVLW   0xC1           ; RC Clock, A/D is on, Channel 0 selected
     MOVWF   ADCON0         ;
     BSF     INTCON, ADIE   ; Enable A/D Interrupt
     BSF     INTCON, GIE    ; Enable all interrupts
;
;  Ensure that the required sampling time for the selected input
;  channel has elapsed. Then the conversion may be started.
;
     BSF     ADCON0, GO     ; Start A/D Conversion
       :                    ; The ADIF bit will be set and the GO/DONE bit
       :                    ;    is cleared upon completion of the
                            ;    A/D Conversion.
```

Figure 22-4: A/D Conversion TAD Cycles

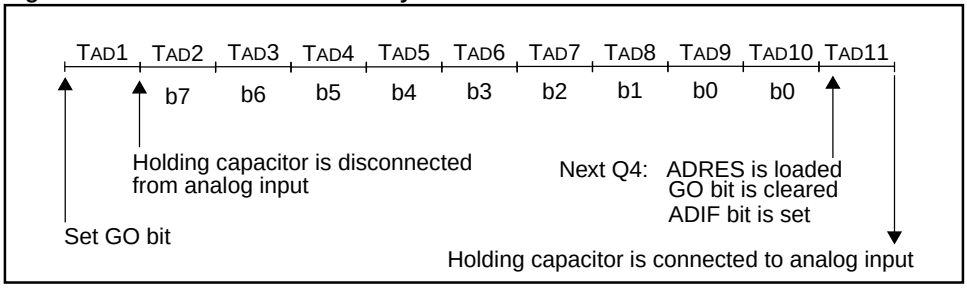
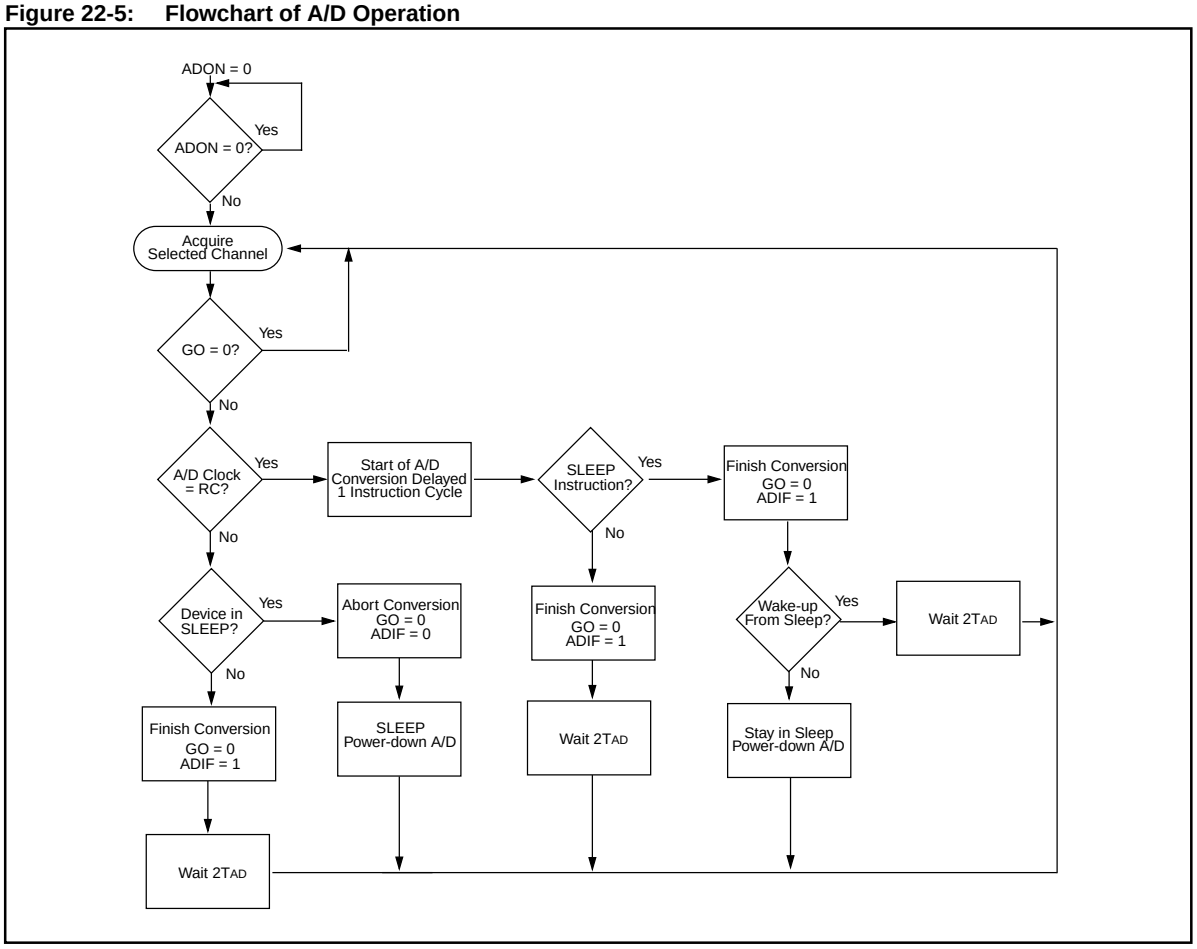


Figure 22-5: Flowchart of A/D Operation



22.6.1 Faster Conversion - Lower Resolution Trade-off

Not all applications require a result with 8-bits of resolution, but may instead require a faster conversion time. The A/D module allows users to make the trade-off of conversion speed to resolution. Regardless of the resolution required, the acquisition time is the same. To speed up the conversion, the clock source of the A/D module may be switched so that the TAD time violates the minimum specified time (see the applicable electrical specification). Once the TAD time violates the minimum specified time, all the following A/D result bits are not valid (see A/D Conversion Timing in the Electrical Specifications section.) The clock sources may only be switched between the three oscillator versions (cannot be switched from/to RC). The equation to determine the time before the oscillator can be switched is as follows:

Conversion time = TAD + N • TAD + (10 - N)(2TOSC)
Where: N = number of bits of resolution required.

Since the TAD is based from the device oscillator, the user must use some method (a timer, software loop, etc.) to determine when the A/D oscillator may be changed. Example 22-3 shows a comparison of time required for a conversion with 4-bits of resolution, versus the 8-bit resolution conversion. The example is for devices operating at 20 MHz and 16 MHz (The A/D clock is programmed for 32TOSC), and assumes that immediately after 5TAD, the A/D clock is programmed for 2TOSC.

The 2TOSC violates the minimum TAD time since the last 4-bits will not be converted to correct values.

Example 22-3: 4-bit vs. 8-bit Conversion Times

	Freq. (MHz)(1)	Resolution	
		4-bit	8-bit
TAD	20	1.6 µs	1.6 µs
	16	2.0 µs	2.0 µs
TOSC	20	50 ns	50 ns
	16	62.5 ns	62.5 ns
TAD + N • TAD + (10 - N)(2TOSC)	20	8.6 µs	17.6 µs
	16	10.75 µs	22 µs

Note 1: The PIC16C71 has a minimum TAD time of 2.0 µs.
All other devices have a minimum TAD time of 1.6 µs.
2: If the full 8-bit conversion is required, the A/D clock source should not be changed.

22.7 A/D Operation During Sleep

The A/D module can operate during SLEEP mode. This requires that the A/D clock source be set to RC (ADCS1:ADCS0 = 11). When the RC clock source is selected, the A/D module waits one instruction cycle before starting the conversion. This allows the SLEEP instruction to be executed, which eliminates all internal digital switching noise from the conversion. When the conversion is completed the GO/$\overline{\text{DONE}}$ bit will be cleared, and the result loaded into the ADRES register. If the A/D interrupt is enabled, the device will wake-up from SLEEP. If the A/D interrupt is not enabled, the A/D module will then be turned off, although the ADON bit will remain set.

When the A/D clock source is another clock option (not RC), a SLEEP instruction will cause the present conversion to be aborted and the A/D module to be turned off, though the ADON bit will remain set.

Turning off the A/D places the A/D module in its lowest current consumption state.

Note:	For the A/D module to operate in SLEEP, the A/D clock source must be set to RC (ADCS1:ADCS0 = 11). To perform an A/D conversion in SLEEP, the GO/$\overline{\text{DONE}}$ bit must be set, followed by the SLEEP instruction.

22.8 A/D Accuracy/Error

In systems where the device frequency is low, use of the A/D RC clock is preferred. At moderate to high frequencies, TAD should be derived from the device oscillator.

The absolute accuracy specified for the A/D converter includes the sum of all contributions for quantization error, integral error, differential error, full scale error, offset error, and monotonicity. It is defined as the maximum deviation from an actual transition versus an ideal transition for any code. The absolute error of the A/D converter is specified at < ±1 LSb for VDD = VREF (over the device's specified operating range). However, the accuracy of the A/D converter will degrade as VDD diverges from VREF.

For a given range of analog inputs, the output digital code will be the same. This is due to the quantization of the analog input to a digital code. Quantization error is typically ± 1/2 LSb and is inherent in the analog to digital conversion process. The only way to reduce quantization error is to increase the resolution of the A/D converter.

Offset error measures the first actual transition of a code versus the first ideal transition of a code. Offset error shifts the entire transfer function. Offset error can be calibrated out of a system or introduced into a system through the interaction of the total leakage current and source impedance at the analog input.

Gain error measures the maximum deviation of the last actual transition and the last ideal transition adjusted for offset error. This error appears as a change in slope of the transfer function. The difference in gain error to full scale error is that full scale does not take offset error into account. Gain error can be calibrated out in software.

Linearity error refers to the uniformity of the code changes. Linearity errors cannot be calibrated out of the system. Integral non-linearity error measures the actual code transition versus the ideal code transition adjusted by the gain error for each code.

Differential non-linearity measures the maximum actual code width versus the ideal code width. This measure is unadjusted.

The maximum pin leakage current is specified in the Device Data Sheet electrical specification parameter D060.

In systems where the device frequency is low, use of the A/D RC clock is preferred. At moderate to high frequencies, TAD should be derived from the device oscillator. TAD must not violate the minimum and should be minimized to reduce inaccuracies due to noise and sampling capacitor bleed off.

In systems where the device will enter SLEEP mode after the start of the A/D conversion, the RC clock source selection is required. In this mode, the digital noise from the modules in SLEEP are stopped. This method gives high accuracy.

22.9 Effects of a RESET

A device reset forces all registers to their reset state. This forces the A/D module to be turned off, and any conversion is aborted. The value that is in the ADRES register is not modified for a Power-on Reset. The ADRES register will contain unknown data after a Power-on Reset.

22.10 Connection Considerations

If the input voltage exceeds the rail values (V_{SS} or V_{DD}) by greater than 0.2V, then the accuracy of the conversion is out of specification.

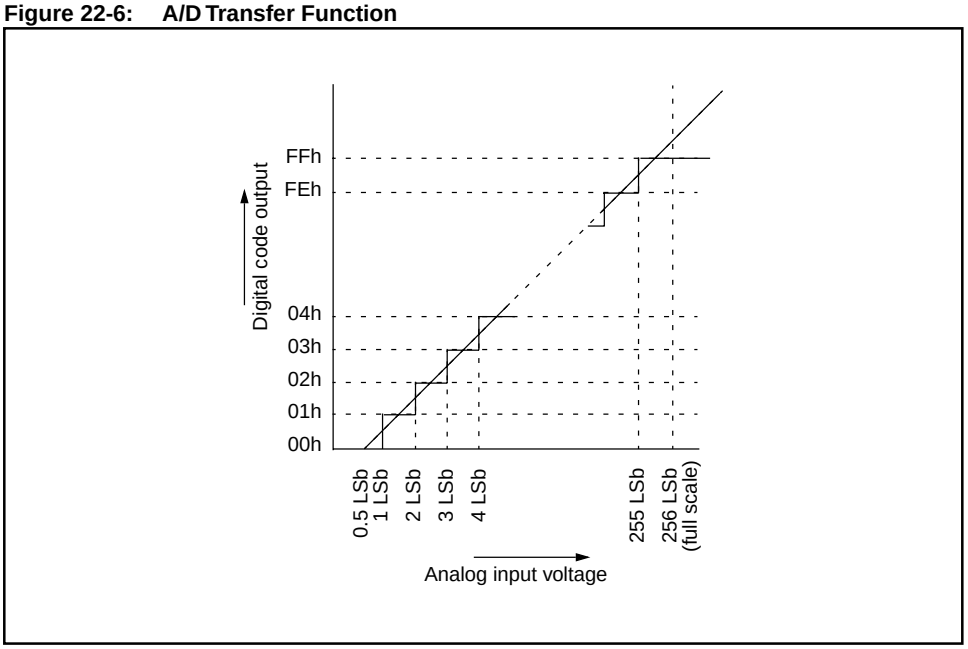
Note:	Care must be taken when using the RA0 pin in A/D conversions due to its proximity to the OSC1 pin.

An external RC filter is sometimes added for anti-aliasing of the input signal. The R component should be selected to ensure that the total source impedance is kept under the 10 kΩ recommended specification. Any external components connected (via hi-impedance) to an analog input pin (capacitor, zener diode, etc.) should have very little leakage current at the pin.

22.11 Transfer Function

The ideal transfer function of the A/D converter is as follows: the first transition occurs when the analog input voltage (V_{AIN}) is 1 LSb (or Analog V_{REF} / 256) (Figure 22-6).

Figure 22-6: A/D Transfer Function



22.12 Initialization

Example 22-4 shows the initialization of the A/D module in the PIC16C711.

Example 22-4: A/D Initialization (for PIC16C711)

```
     BSF     STATUS, RP0    ; Select Bank1
     CLRF    ADCON1         ; Configure A/D inputs
     BCF     STATUS, RP0    ; Select Bank0
     MOVLW   0xC1           ; RC Clock, A/D is on, Channel 0 selected
     MOVWF   ADCON0         ;
     BSF     INTCON, ADIE   ; Enable A/D Interrupt
     BSF     INTCON, GIE    ; Enable all interrupts
;
;  Ensure that the required sampling time for the selected input
;  channel has elapsed. Then the conversion may be started.
;
     BSF     ADCON0, GO     ; Start A/D Conversion
       :                    ; The ADIF bit will be set and the GO/DONE bit
       :                    ;    is cleared upon completion of the
                            ;    A/D Conversion.
```

22.13 Design Tips

Question 1: ***I am using one of your PIC16C7X devices, and I find that the Analog to Digital Converter result is not always accurate. What can I do to improve accuracy?***

Answer 1:

1. Make sure you are meeting all of the timing specifications. If you are turning the ADC off and on, there is a minimum delay you must wait before taking a sample, if you are changing input channels, there is a minimum delay you must wait for this as well, and finally there is TAD, which is the time selected for each bit conversion. This is selected in ADCON0 and should be between 2 and 6 μs. If TAD is too short, the result may not be fully converted before the conversion is terminated, and if Tad is made too long the voltage on the sampling capacitor can droop before the conversion is complete. These timing specifications are provided in the data book in a table or by way of a formula, and should be looked up for your specific part and circumstances.
2. Often the source impedance of the analog signal is high (greater than 1k ohms) so the current drawn from the source to charge the sample capacitor can affect accuracy. If the input signal does not change too quickly, try putting a 0.1 μF capacitor on the analog input. This capacitor will charge to the analog voltage being sampled, and supply the instantaneous current needed to charge the 51.2 pf internal holding capacitor.
3. On the PIC16C71, one of the analog input pins is next to an oscillator pin. Naturally if these traces are next to each other some noise can couple from the oscillator to the analog circuit. This is especially true when the clock source is an external canned oscillator, since its output is a square wave with a high frequency component to its sharp edge, as opposed to a crystal circuit which provides a slower rise sine wave. Again, decoupling the analog pin can help, or if you can spare it, turn the pin into an output and drive it low. This will really help eliminate cross coupling into the analog circuit.
4. Finally, straight from the data book: “In systems where the device frequency is low, use of the A/D clock derived from the device oscillator is preferred...this reduces, to a large extent, the effects of digital switching noise.” and “In systems where the device will enter SLEEP mode after start of A/D conversion, the RC clock source selection is required. This method gives the highest accuracy.”

Question 2: ***After starting an A/D conversion may I change the input channel (for my next conversion)?***

Answer 2:

After the holding capacitor is disconnected from the input channel, one TAD after the GO bit is set, the input channel may be changed.

Question 3: ***Do you know of a good reference on A/D’s?***

Answer 3:

A very good reference for understanding A/D conversions is the “Analog-Digital Conversion Handbook” third edition, published by Prentice Hall (ISBN 0-13-03-2848-0).

22.14 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the Mid-Range MCU family (that is they may be written for the Base-Line, or High-End families), but the concepts are pertinent, and could be used (with modification and possible limitations). The current application notes related to the Basic 8-bit A/D module are:

Title	Application Note #
Using the Analog to Digital Converter	AN546
Four Channel Digital Voltmeter with Display and Keyboard	AN557

22.15 Revision History

Revision A

This is the initial released revision of the Basic 8-bit A/D Converter module description.