

September 1983 Revised February 1999

MM74HC151 8-Channel Digital Multiplexer

General Description

The MM74HC151 high speed Digital multiplexer utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The MM74HC151 selects one of the 8 data sources, depending on the address presented on the A, B, and C inputs. It features both true (Y) and complement (W) outputs. The STROBE input must be at a low logic level to enable this multiplexer. A high logic level at the STROBE forces the W output HIGH and the Y output LOW

The 74HC logic family is functionally as well as pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

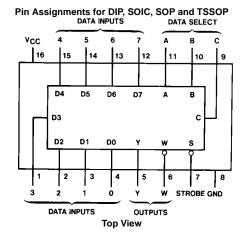
- Typical propagation delay data select to output Y: 26 ns
- Wide operating supply voltage range: 2–6V
- Low input current: 1 µA maximum
- Low quiescent supply current: 80 µA maximum (74HC)
- High output drive current: 4 mA minimum

Ordering Code:

Order Number	Package Number	Package Description
MM74HC151M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC151SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC151MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC151N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Truth Table

	Inputs				Outputs	
	Select	t	Strobe			
С	С В А		s	Υ	W	
Х	Х	Х	Н	L	Н	
L	L	L	L	D0	D0	
L	L	Н	L	D1	D1	
L	Н	L	L	D2	D2	
L	Н	Н	L	D3	D3	
Н	L	L	L	D4	D4	
Н	L	Н	L	D5	D5	
Н	Н	L	L	D6	D6	
Н	Н	Н	L	D7	D7	

H = HIGH Level, L = LOW Level, X = Don't Care D0, D1...D7 = the level of the respective D input

MM74HC151 Logic Diagram STROBE -

Absolute Maximum Ratings(Note 1)

Storage Temperature Range (T_{STG}) Power Dissipation (P_D)

(Note 2)

(Note 3) 600 mW S.O. Package only 500 mW Lead Temperature (T_L) 260°C

-65°C to +150°C

(Soldering 10 seconds)

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})	2	6	V
DC Input or Output Voltage	0	V_{CC}	V
(V_{IN}, V_{OUT})			
Operating Temperature Range (T _A)	-40	+85	°C
Input Rise or Fall Times			
$(t_r, t_f) V_{CC} = 2.0V$		1000	ns
$V_{CC} = 4.5V$		500	ns
$V_{CC} = 6.0V$		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: – 12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units	
Symbol		Conditions	*CC	Тур		Guaranteed L	imits	Units	
V_{IH}	Minimum HIGH Level		2.0V		1.5	1.5	1.5	V	
	Input Voltage		4.5V		3.15	3.15	3.15	V	
			6.0V		4.2	4.2	4.2	V	
V_{IL}	Maximum LOW Level		2.0V		0.5	0.5	0.5	V	
	Input Voltage		4.5V		1.35	1.35	1.35	V	
			6.0V		1.8	1.8	1.8	V	
V _{OH}	Minimum HIGH Level	$V_{IN} = V_{IH}$ or V_{IL}							
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	2.0	1.9	1.9	1.9	V	
			4.5V	4.5	4.4	4.4	4.4	V	
			6.0V	6.0	5.9	5.9	5.9	V	
		$V_{IN} = V_{IH}$ or V_{IL}							
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	4.2	3.98	3.84	3.7	V	
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	5.7	5.48	5.34	5.2	V	
V _{OL}	Maximum LOW Level	$V_{IN} = V_{IH}$ or V_{IL}							
	Output Voltage	$ I_{OUT} \le 20 \ \mu A$	2.0V	0	0.1	0.1	0.1	V	
			4.5V	0	0.1	0.1	0.1	V	
			6.0V	0	0.1	0.1	0.1	V	
		$V_{IN} = V_{IH}$ or V_{IL}							
		$ I_{OUT} \le 4.0 \text{ mA}$	4.5V	0.2	0.26	0.33	0.4	V	
		$ I_{OUT} \le 5.2 \text{ mA}$	6.0V	0.2	0.26	0.33	0.4	V	
I _{IN}	Maximum Input	$V_{IN} = V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μΑ	
	Current								
I _{CC}	Maximum Quiescent	$V_{IN} = V_{CC}$ or GND	6.0V		8.0	80	160	μА	
	Supply Current	$I_{OUT} = 0 \mu A$							

Note 4: For a power supply of 5V \pm 10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{O2}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

 $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 15$ pF, $t_r = t_f = 6$ ns

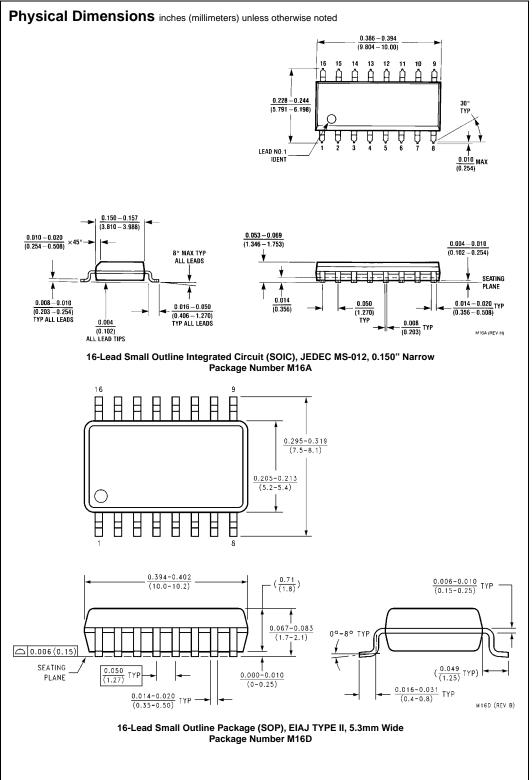
Symbol	Parameter	Conditions	Тур	Guaranteed Limit	Units
t _{PHL} , t _{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay A, B or C to W		27	35	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay Any D to Y		22	29	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay any D to W		24	32	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay Strobe to Y		17	23	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay Strobe to W		16	21	ns

AC Electrical Characteristics

 $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

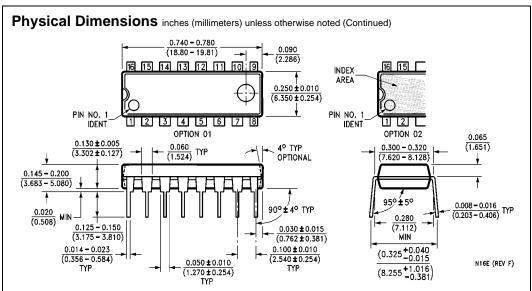
Symbol	Parameter	Conditions	v _{cc}	T _A = 25°C		$T_A = -40$ to $85^{\circ}C$	T _A = -55 to 125°C	Units
Symbol				Тур		Guaranteed Limits		
t _{PHL} , t _{PLH}	Maximum Propagation Delay		2.0V	90	205	256	300	ns
	A, B or C to Y		4.5V	31	41	51	60	ns
			6.0V	26	35	44	51	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay		2.0V	95	205	256	300	ns
	A, B or C to W		4.5V	32	41	51	60	ns
			6.0V	27	35	44	51	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay		2.0V	70	195	244	283	ns
	any D to Y		4.5V	27	39	49	57	ns
			6.0V	23	33	41	48	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay		2.0V	75	185	231	268	ns
	any D to W		4.5V	29	37	46	54	ns
			6.0V	25	32	40	46	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay		2.0V	50	140	175	203	ns
	Strobe to Y		4.5V	21	28	35	41	ns
			6.0V	18	24	30	35	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay		2.0V	45	127	159	185	ns
	Strobe to W		4.5V	20	25	32	37	ns
			6.0V	17	22	28	32	ns
t _{TLH} , t _{THL}	Maximum Output Rise		2.0V	30	75	95	110	ns
	and Fall Time		4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C _{PD}	Power Dissipation	(per package)		110				pF
	Capacitance (Note 5)							
C _{IN}	Maximum Input			5	10	10	10	pF
	Capacitance							

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} \ V_{CC}^2 f + I_{CC} \ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} \ V_{CC} \ f + I_{CC}$.



Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 7.72 TYP. DIMENSIONS METRIC ONLY (1.78 TYP) 0.42 TYP LAND PATTERN RECOMMENDATION GAGE PLANE 6.4 0.25 4.4 ± 0.1 -B-3.2 SEATING PLANE 0.6 ± 0.1 DETAIL A △ 0.2 C B A ALL LEAD TIPS TYPICAL, SCALE: 40X SEE DETAIL A PIN #1 IDENT. (0.90) O.1 C--c-0.10 ± 0.05 TYP 0.09-0.20 TYP 0.65 TYP - 0.30 TYP Φ 0.13 M B (S) Α MTC16 (REV C)

16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC16



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide Package Number N16E

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