Scalable Equivalent Circuit FET Model for MMIC Design Identified Through FW-EM Analyses

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***Abstract*—A scalable approach to the modeling of millimeter-wave field-effect transistors is presented in this paper. This is based on the definition of a lumped extrinsic parasitic network, easily scalable with both the number of fingers and the finger widths. The identification of the extrinsic network parameters is carried out by means of accurate full-wave electromagnetic simulations based on the layout of a single reference device.**

In the paper, the parasitic effects of the gate/drain manifolds and of the source layout are investigated, leading to the definition of realistic linear scaling rules.

The obtained model is experimentally validated by using a family of 0.25-μm millimeter-wave GaAs pseudomorphic HEMTs through the accurate prediction of critical performance indicators, such as the linear maximum power gain or the stability factor.

Despite the simplicity of the proposed model, it proves to be as accurate as typical scalable models provided by foundries.

Straightforward application of the scalable modeling approach to the optimum device geometry selection in a typical design problem is also presented.

***Index Terms*—Electromagnetic (EM) analysis, field-effect transistors (FETs), microwave and millimeter-wave integrated circuits (MMICs), semiconductor device modeling.**

I. Introduction

MICROWAVE AND millimeter-wave integrated circuit (MMIC) design requires empirical models, which accurately describe the linear and nonlinear behavior of electron devices up to extremely high frequencies. When embedded into circuit schematics, accurate device models allow engineers to design and optimize the circuit performance before the actual fabrication.

Optimum device periphery selection in actual design tasks often requires a different model for each particular device layout in a given technological process. In order to avoid this problem, empirical scalable models are available allowing the designer to select the optimum device *geometry* (i.e., number and width of gate fingers) for the specific application through the evaluation of suitably defined figures of merit and design criteria [1], [2]. Scalable models also allow for important time saving during the empirical characterization of foundry processes.

Linear scaling rules are widely adopted for the intrinsic device, providing accurate prediction results [3] up to relatively high frequencies. However, when microwave and millimeter-wave applications are involved, the overall quality of an electron device model also strongly depends on the rules applied to the scaling of the extrinsic network, describing the parasitic phenomena taking part in the physical interconnections of the intrinsic device to the externally accessible terminals.

Simple linear scaling rules [4], [5] applied to conventional lumped parasitic networks do not lead to accurate scalable models at high frequencies. Complex, technology-dependent scaling rules [6]–[9] or quasi-distributed models [10]–[19] have been recently proposed in the literature in order to improve the high-frequency prediction accuracy of scaled device models.

Commercial full-wave electromagnetic (FW-EM) simulators have been also recently exploited (e.g., see [18] and [19]) for the analysis of extrinsic parasitic phenomena and the definition of distributed modeling approaches, where the entire active area is divided into a suitable number of elementary "active slices." Such modeling approaches have been proven very suitable for scaling, providing extremely accurate electrical response predictions. Unfortunately, their exploitation in conjunction with nonlinear models of the active slices leads to relatively poor numerical efficiency in harmonic balance (HB) analyses due to the proliferation in the number of internal nonlinear ports.

In this paper, an almost conventional lumped parasitic network is adopted. However, a new simple parameter identification procedure is proposed on the basis of an FW-EM simulation of the device layout. In addition, suitable rules are provided for improved prediction accuracy of scaled devices. Typical device geometrical parameters, such as the number of fingers and the unit gatewidth, may be used by the designer as swept and even optimization variables by means of the proposed approach. Although this paper deals with linear models, the proposed approach is totally suitable for the application of scalable nonlinear models to the intrinsic device.

This paper is organized as follows. The proposed lumped parasitic network is introduced in Section II-A and the corresponding scaling rules are also discussed. With respect to the somehow similar approach presented in [20], the effects of widening (or shrinking) of the gate and drain manifolds in the presence of a higher (or lower) number of fingers are taken into account here and a new scaling rules are provided for the

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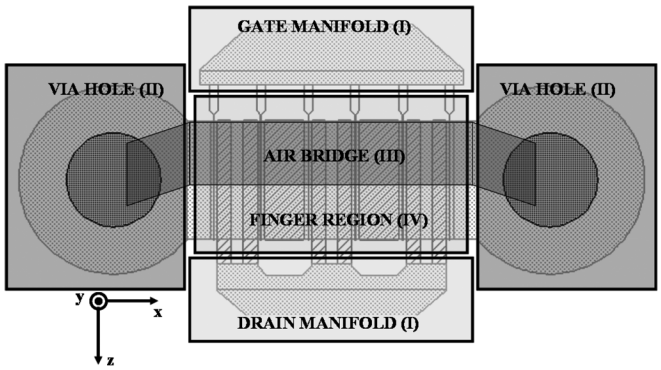

Fig. 1. Device parasitic effects subdivision through device layout considerations. Gate and drain manifolds (I), source via-holes (II), air bridge (III), and finger region (IV) are shown.

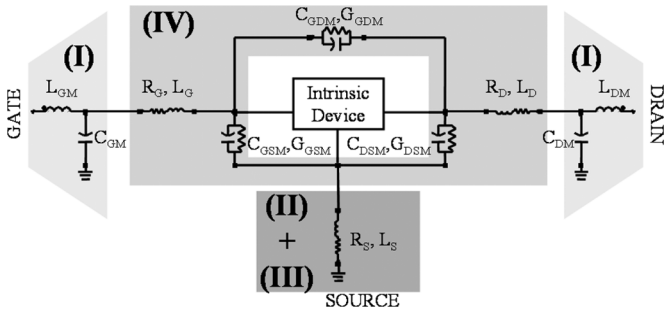

Fig. 2. Lumped component network describing the device extrinsic parasitic phenomena. Schematic regions (I)–(IV) are strictly related to the corresponding layout regions shown in Fig. 1.

manifold and source parasitic components. The new scaling rules lead to critical improvement in the prediction accuracy of scaled devices.

A new procedure for the identification of the lumped components of the parasitic network is then presented in Section II-B. This is based on a three-step process aimed at the separation of the entire equivalent circuit parameter (ECP) set into smaller groups, more easily identifiable through the fitting of simpler FW-EM simulations.

Experimental validation of the model is proposed in Section III. A family of 0.25-μm GaAs pseudomorphic HEMTs (pHEMTs) is fully characterized and scaled models are obtained from a reference device. In order to meet the designer point of view, the evaluation of the prediction accuracy of the scaled models is carried out directly on the basis of critical performance indicators, such as the maximum available gain (MAG), and the stability factor μ [21]. Despite the simplicity of the proposed approach, improvements in accuracy are proven in comparisons with other similar approaches [20] and typical foundry models.

Finally, a practical example of optimum device periphery selection by means of the proposed approach is provided in Section IV. Advantages with respect to other conventional scalable device models are here highlighted by means of a simple application example.

II. Identification of a Lumped Parasitic Network Through FW-EM Analysis

Let us consider the problem of modeling the extrinsic parasitic phenomena associated with the typical device layout shown in Fig. 1 through a scalable lumped component network. The access structures to the device, such as, for instance, coplanar to microstrip line transitions, are considered apart in this context (suitable instrument calibration procedures may be adopted in order to set the device characterization sections at the external edges of the gate and drain manifolds).

In addition, parasitic phenomena associated with doped layers in the semiconductor substrate are not taken into account here (a simple homogeneous substrate is assumed in the EM simulations of the device layout). Thus, additional modeling effort could be required if parasitic phenomena are expected to strongly affect these regions. It is worth noting that, the parasitic phenomena located in the doped layers have been considered fully negligible in the case of the 0.25-μm GaAs pHEMT used in this study. Experimental validation provided in Section III empirically confirms the validity of this assumption.

In order to get proper scaling rules of the model, the device layout in Fig. 1 is separated into four different regions. Region (I) accounts for the parasitic effects due to the gate and drain manifolds, which feed the signals to each finger. Region (II) accounts for the parasitic effects due to the via-holes, which provides source connections to ground. Region (III) accounts for the air bridge, which provide the ground connection to the source fingers through the via-hole pads. Region (IV) accounts for the parasitic effects due to the interactions between the finger metallizations (i.e., ohmic losses along the gate and drain fingers and capacitive-like couplings both between the gate and drain fingers themselves and between the gate/drain fingers and the air bridge).

This somehow intuitive separation leads to the lumped extrinsic parasitic network shown in Fig. 2.

The four elements $L_{\rm GM}$, $C_{\rm GM}$, $L_{\rm DM}$, and $C_{\rm DM}$ (where M denotes manifold) model the parasitic effects of the layout region (I). The elements R_S and L_S model the effects of the via-holes and the air bridge in layout regions (II) and (III). As discussed later, the parasitic effects of the two via-holes in layout region (II) are accounted for separately through a standalone EM simulation of the via structure. This choice is twice useful. In fact, the FW-EM analysis of the remaining layout is strongly simplified and the via-holes may be removed when the specific design application requires floating source electrodes.

The elements R_G, L_G, R_D, and L_D describe the series parasitic effects due to the multigate/drain-finger layout region (IV). The elements $C_{\rm GSM}$, $G_{\rm GSM}$, $C_{\rm GDM}$, $G_{\rm GDM}$, $C_{\rm DSM}$, and $G_{\rm DSM}$ (where M denotes metallization) account for the capacitive-like coupling and dielectric losses both between the metallization structures of the gate and drain fingers and between the gate/drain fingers and the air bridge. It is worth noting that since no doped layers are considered in the substrate definition for the EM simulations, the evaluation of $C_{\rm GSM}$ and $C_{\rm GDM}$ is totally unaffected by the gate–source and gate–drain barrier capacitances associated with the mobile charge depletion beneath the Schottky gate in actual devices.

A. Model Scaling Rules

Let us first define geometry-dependent scaling factors [20] such as

$$\mathrm{SF}_Z = \frac{W_g^{\mathrm{sc}}}{W_g^{\mathrm{ref}}}$$
$$\mathrm{SF}_X = \frac{N_g^{\mathrm{sc}}}{N_g^{\mathrm{ref}}} \tag{1}$$

where W_g^{sc}, W_g^{ref}, N_g^{sc}, and N_g^{ref} are the gatewidth and the number of gate fingers of the scaled and reference device, respectively. According to the axes reference system shown in Fig. 1, the subscript "Z" represents the direction along the gate/drain fingers (z-axis), while "X" denotes the direction along the channel (x-axis), respectively. Thus, the factors SF_Z and SF_X will be applied whenever a scaling of the gatewidth and/or a different number of paralleled fingers are involved.

We first consider the parasitic phenomena associated to the layout region (IV). Simple scaling rules are defined in this case for the lumped components of the corresponding schematic region. These rules state that [20]

$$(R_i, L_i)^{\mathrm{sc}} = (R_i, L_i)^{\mathrm{ref}} \cdot \frac{\mathrm{SF}_Z}{\mathrm{SF}_X}, \qquad i = G, D \tag{2}$$
$$(C_i, G_i)^{\mathrm{sc}} = (C_i, G_i)^{\mathrm{ref}} \cdot \mathrm{SF}_Z \cdot \mathrm{SF}_X, \quad i = \mathrm{GSM}, \mathrm{GDM}, \mathrm{DSM}. \tag{3}$$

More interesting considerations concern layout region (I). The gate and drain manifolds widening (or shrinkage) effects in the presence of a varying number N of fingers are investigated here through simple EM simulations. To this aim, the gate and drain manifold layouts of the generic device are easily drown by modifying the reference device layout on the basis of the minimum distance along the x-axis between two successive gate fingers. The study is carried out for a number of fingers ranging from 4 to 12, which corresponds to the set of electron devices made available in the foundry process considered.

The EM simulation of each gate manifold is carried out by placing $(N+1)$-ports, one for the connection to the external gate line and one for the connection to each internal gate finger [22] (only "gap ports" are used since they are exactly deembedded by the EM solver [23], [24]). Since our goal is the definition of a lumped component scalable description of the parasitic effects associated to the manifold, the internal N ports are then short circuited leading to a two-port EM-based description of the gate manifold. A simple *LC* network, as shown in gate region (I) of Fig. 2 perfectly fits the obtained two-port description up to 100 GHz.

The same procedure is applied also to the drain manifold, with the only difference that $N/2$ internal ports are considered since the drain fingers are half the number of gate fingers.

The extracted values of the *LC* model parameters concerning the gate and drain manifolds are shown in Table I. It is observed that the values of L_{GM} and L_{DM} are nearly constant versus the number of fingers, while the values of C_{GM} and C_{DM} increase almost linearly with N, according to the scaling factor SF_X. This is also clearly seen in Fig. 3, where the extracted inductances and scaled capacitances are plotted versus the number of fingers (SF_X evaluated by considering six gate fingers in the reference device).

TABLE I
LC MODEL OF THE GATE AND DRAIN MANIFOLDS

	4 Finger	6 Finger	8 Finger	10 Finger	12 Finger
C_{GM} [fF]	7.5	10.6	14.4	19.81	25
L_{GM} [pH]	12.5	11.3	10.7	10.7	10.3
C_{DM} [fF]	12.5	14	20.3	25.5	34.4
L_{DM} [pH]	12	10.6	10.2	12.2	11.3

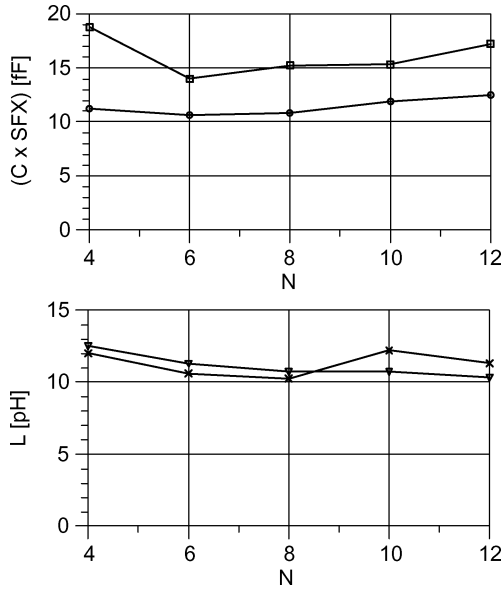

Fig. 3. Variation of the L, C parameters in the gate and drain manifold models with the number of gate fingers: L_{GM} (triangles), L_{DM} (crosses), $C_{\mathrm{GM}}\mathrm{SF}_X$ (circles), $C_{\mathrm{DM}}\mathrm{SF}_X$ (squares). SF_X is evaluated by considering six gate fingers in the reference device.

The obtained results justify the following scaling rules for the parasitic lumped components in schematic region (I)

$$(L_{\mathrm{GM}}, L_{\mathrm{DM}})^{\mathrm{sc}} = (L_{\mathrm{GM}}, L_{\mathrm{DM}})^{\mathrm{ref}}$$
$$(C_{\mathrm{GM}}, C_{\mathrm{DM}})^{\mathrm{sc}} = (C_{\mathrm{GM}}, C_{\mathrm{DM}})^{\mathrm{ref}} \cdot \mathrm{SF}_X. \tag{4}$$

We consider now the parasitic phenomena associated to layout regions (II) and (III). At first glance, R_S and L_S could be considered analogous to the corresponding gate or drain components, but related to the modeling of the parasitic effects associated to the source fingers. According to this view [20], R_S and L_S should be scaled by using the same rules (2) used for the gate and drain series parasitic effects.

However, in this particular case, a more appropriate analysis of the device layout should also take into account the presence of the air bridge, as shown in Fig. 4. In opposition to the previous point of view, this structure suggests that R_S and L_S should not scale with the device periphery. In fact, since the internal source fingers are connected to the ground terminal through the air bridge, which is running along the x-axis, negligible parasitic effects actually take place in the Z-direction (the source finger opposite ends almost correspond to open impedance terminations).

The series parasitic phenomena associated with the air bridge along the x-axis can be considered almost negligible with re-

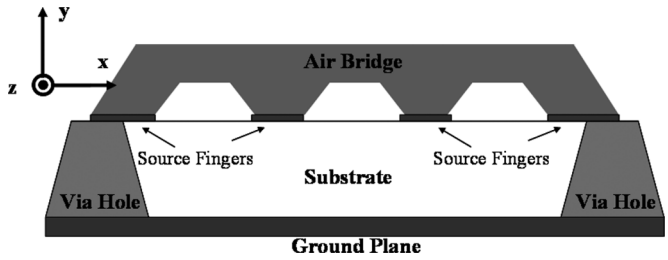

Fig. 4. Cross section of the air bridge providing ground connection to the internal source fingers (six gate finger device). The entire extrinsic structure associated with the source is composed by the via-holes in layout region (II) connected to the air bridge representing layout region (III) (see Fig. 1).

spect to those introduced by the via-holes, as confirmed by a dedicated EM analysis of the air-bridge standalone.

Thus, since the via-holes (actually two vias connected in parallel) are the same for all the device peripheries, the R_S and L_S elements of Fig. 2 may be thought of not requiring any scaling at all, i.e.,

$$(R_S, L_S)^{\mathrm{sc}} = (R_S, L_S)^{\mathrm{ref}}. \tag{5}$$

Particular care must be paid when the source structure is either different than that of Fig. 4 or the air bridge has significant parasitic effects since the source parasitic elements scaling rule (5) might change.

B. Model Identification

The identification of the extrinsic lumped components is based on a few FW-EM simulations of a single reference device structure. Measurements under off-state conditions [or forward-gate cold field-effect transistor (FET)] and characterization of multiple different-in-size devices are not required for the identification of the extrinsic elements using our approach. The FW-EM analyses need of course the knowledge of the substrate physical constants and the geometry of the metal layers of the FET [18], [20]. These data are usually provided with the foundry design kit of any technological process (GDSII files defining the device layout are for instance needed along with information about the thickness of metal layers).

A commercial 3-D planar EM solver [23], providing accurate calibration algorithms for the deembedding of ports discontinuities [24], is adopted and a 6×50 μm pHEMT ($L = 0.25$ μm) is selected as the reference device in this study.

According to the flowchart shown in Fig. 5, the model identification procedure consists of three different steps.

EM simulations of the reference device are performed in step (i). They are: EM1) the FW-EM analysis of the four-port device extrinsic structure (four calibrated ports [24] are used: port-1 for the gate, port-2 for the drain, and ports 3–4 for the two source electrodes); EM2) the FW-EM simulation of the conic via-hole; and EM3) the FW-EM simulations of the gate and drain manifolds.

In step (ii), the simulated data are used in order to extract the extrinsic ECPs. First, RS and LS in region (II) and (III) are extracted by fitting the via-hole simulation EM2, while L_{GM}, C_{GM}, L_{DM}, and C_{DM} in region (I) are extracted by fitting the gate and drain manifold simulations EM3.

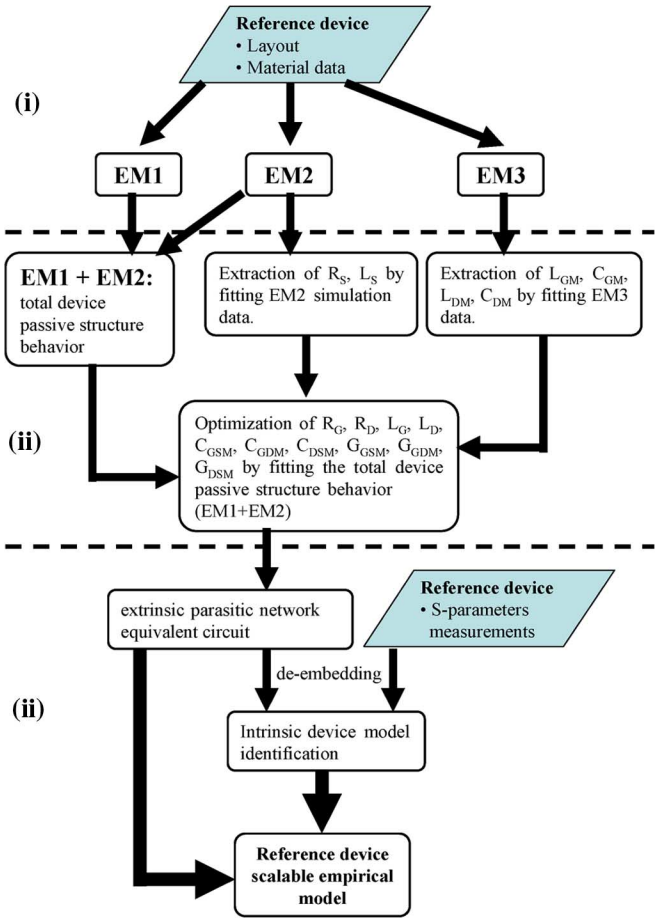

Fig. 5. Flowchart describing the model extraction procedure. The FW-EM simulations EM1, EM2, and EM3 are described in Section II-B.

TABLE II
EXTRACTED PARASITIC PARAMETERS

C_{GSM}	C_{GDM}	C_{DSM}	G_{GSM}	G_{GDM}	G_{DSM}
27.1 fF	25.2 fF	32.2 fF	3.0e-8 S	2.5e-8 S	2.8e-9 S
L_G	L_D	L_S	R_G	R_D	R_S
14.3 pH	13.0 pH	10.63 pH	0.603 Ω	0.085 Ω	0.056 Ω

A distributed two-port description associated to the entire extrinsic layout is then obtained by connecting the source-ports of network EM1 to the description EM2 of the via-holes. This is finally used (by means of a standard optimization routine) for the identification of the remaining extrinsic circuit parameters: R_i, L_i $(i = G, D)$ and C_i, G_i $(i = \mathrm{GSM}, \mathrm{GDM}, \mathrm{DSM})$.

The extraction procedure of the extrinsic elements involves a very well-conditioned optimization problem in ten unknowns. Fast convergence to the same solution is observed by considering very different initial guesses of the parameter values. In some cases, residual parasitic contributions deriving from the source fingers could be effectively considered in the optimization.

Finally, the measured behavior of the reference device is deembedded from the extracted extrinsic equivalent circuit in step (iii). The obtained description is eventually used for the identification of the preferred intrinsic device model.

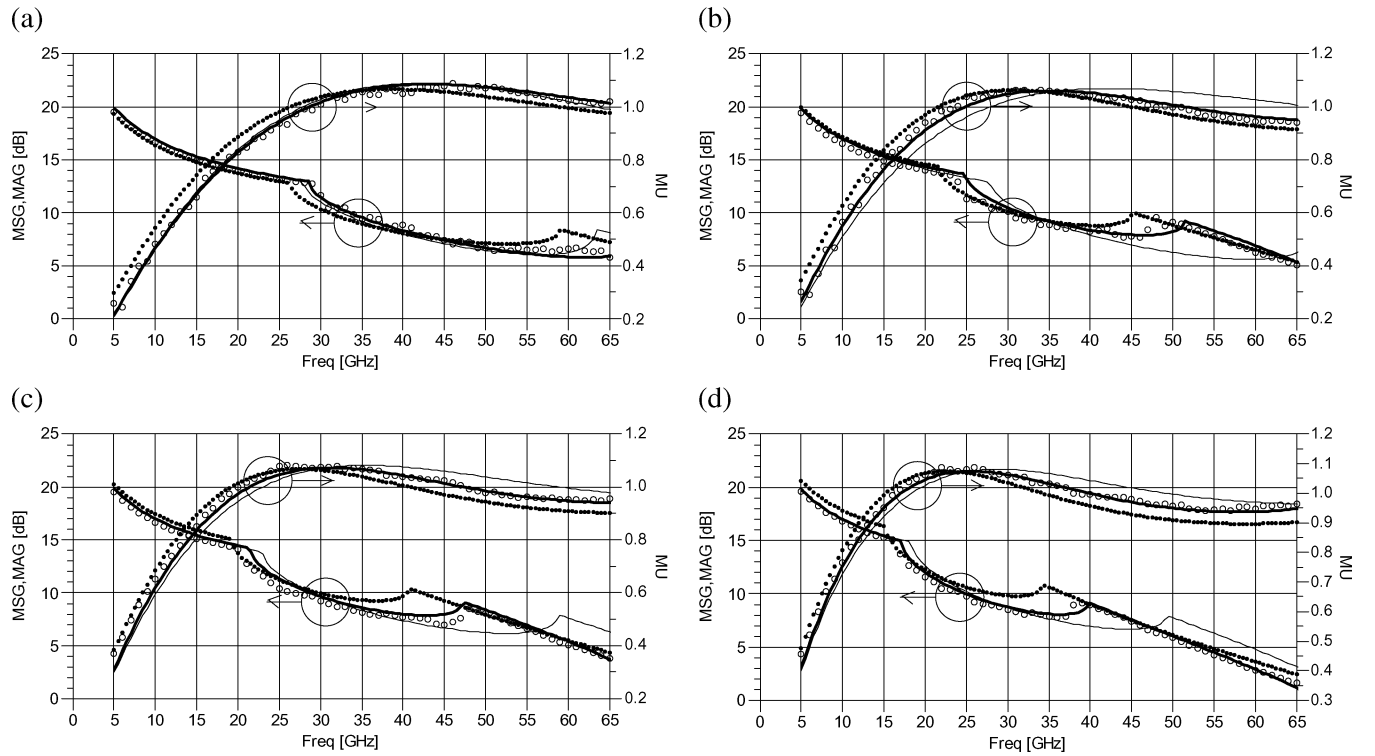

Fig. 6. MAG (or MSG where MAG is undefined) and the stability factor μ versus frequency. (a) 6×50 μm. (b) 10×50 μm. (c) 10×60 μm. (d) 12×75 μm pHEMTs. Measurements (circles) versus predictions obtained through different scalable models: proposed model (bold lines), model presented in [20] (lines), and model provided by the foundry (dots). The results refer to the devices biased in typical class-A operation. Analogous results are obtained in different bias conditions.

Thus, a single set of S-parameter measurements at the operating bias on a single device periphery is only needed for the identification of our linear scalable model.

III. Experimental Validation of the Scalable Model

Experimental validation of the proposed modeling approach is here provided by means of a family of 0.25-μm GaAs pHEMTs. The chosen reference device is a 6×50 μm pHEMT.

FW-EM simulations are performed in the frequency range of 0–100 GHz. The extracted values of the gate and drain manifolds parasitic elements have already been reported in Table I for the six-finger reference device. The optimizations involved in the identification procedure outlined in Section II-B are carried out in order to fit the EM simulation data up to the maximum simulated frequency of 100 GHz. The extracted values of the parasitic elements are listed in Table II.

S-parameter measurements in the frequency range (5–65 GHz) are performed biasing the device at $V_{g0} = -0.5$ V, $V_{d0} = 5$ V ($I_{d0} = 30$ mA), which corresponds to the typical condition for the design of a power amplifier (PA) working in class-A operation.

Following the identification procedure described in Section II-B, the measurements are deembedded from the parasitic elements in order to obtain the intrinsic measured admittance parameters. These data can be used for the identification of any intrinsic linear (or nonlinear) device model. However, since the aim of this study is to investigate the scalability of the proposed extrinsic parasitic modeling approach, we prefer to avoid using any particular model for the intrinsic device. Thus, the linear table-based description of the intrinsic device, in terms of admittance matrix, is used hereinafter in conjunction with simple linear rules for the scaling of the intrinsic device behavior (i.e., $Y_{\rm int}^{\rm sc}(j\omega) = Y_{\rm int}^{\rm ref}(j\omega){\rm SF}_Z{\rm SF}_X$).

The complete linear scalable model is now experimentally validated in terms of prediction capabilities of both S-parameters and global design parameters such as the stability factor μ [21], the MAG or the maximum stable gain (MSG), whenever the MAG is not defined [2]. This represents a rather heavy experimental validation since it also takes into account the way the discrepancies in the prediction of each S-parameter combine within such important global figures of merit.

Four devices are considered, having remarkable differences in number of gate fingers and gatewidth, namely, the 6×50 μm pHEMT reference device plus a 10×50 μm, a 10×60 μm and a 12×75 μm pHEMTs.

Scaled model results are plotted in Figs. 6 and 7. Predictions are compared both to the scalable model described in [20] and the linear scalable foundry model. It must be pointed out that the foundry design kit does not provide a single scalable model, but different linear scalable models, each one extracted for a given number of fingers; thus, the finger width is the only "true" scaling variable available. The foundry models are related to the operating bias condition $V_{d0} = 5$ V and $I_{d0} = 100$ mA/mm (which corresponds to the scaled class-A operating condition of our 6×50 μm reference device).

Accuracy improvements with respect to the model presented in [20] are evident from Figs. 6 and 7. This is due to the modified scaling rules and the improved extraction procedure pro-

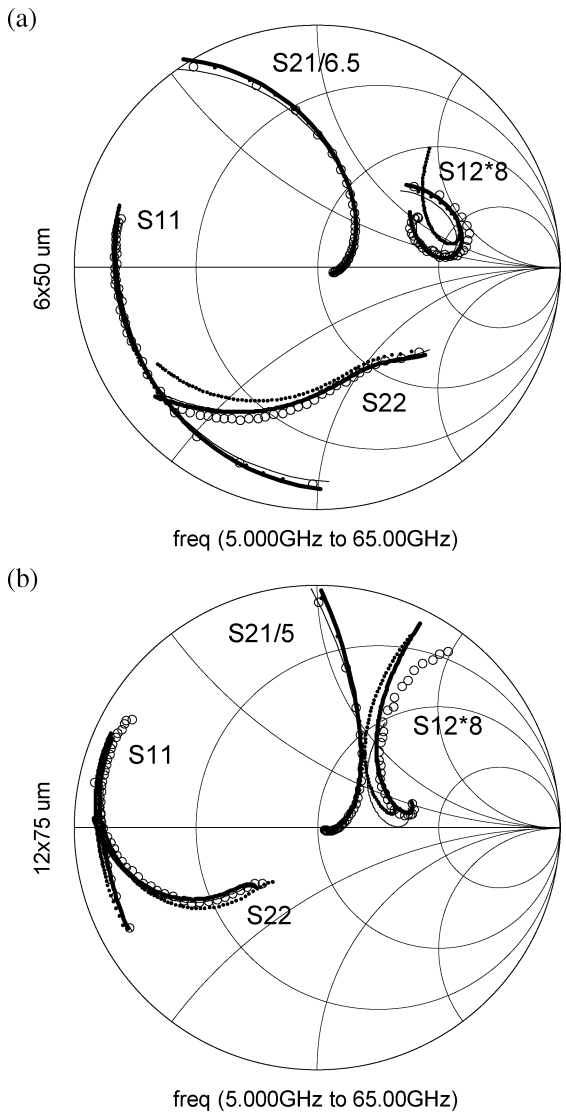

Fig. 7. S-parameters versus frequency for the 6×50 μm: (a) reference device and the largest (12×75 μm) (b) scaled device. Measurements (circles) versus predictions obtained through different scalable models: proposed model (bold lines), model [20] (lines), and foundry model (dots). The results refer to the device biased in typical class-A operation.

posed in this paper. In addition, experimental results in Figs. 6 and 7 point out that the new scalable model is at least as accurate as the most advanced foundry linear scalable models. This is an interesting result considering that the proposed model has been obtained by exploiting the minimum amount of EM simulated data and a single set of S-parameter measurements carried out for a single reference device at the required operating condition. On the contrary, the foundry model is extracted by using both EM simulations, as well as additional measurements performed on different-in-size devices, even considering bias conditions different with respect to the operating one. More precisely, EM-based data matrices are used for the modeling of the access structures, while the additional measurements are used in order to extract the parasitic elements at the finger region reference planes (mixed physical–empirical scaling rules are derived at these reference planes). The foundry model is, therefore,

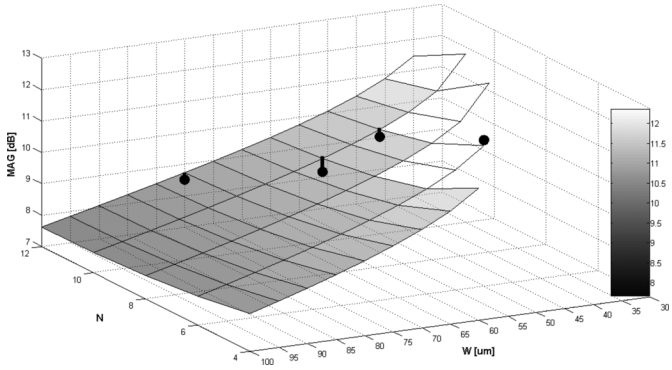

Fig. 8. MAG versus number of gate fingers and finger widths at 30 GHz evaluated through the proposed model. The black dots are the MAG values measured on actual device samples. Bold lines highlight the differences between measured and simulated values.

easily scalable with respect to the unit gatewidth only since data of different EM simulations are required to model the change in the number of fingers. For this reason, the number of fingers cannot be used as swept or optimization variable.

The experimental results in Figs. 6 and 7 highlight the prediction accuracy of the proposed scalable model for a wide set of devices within the technological process under test. This leads the quite interesting opportunity of evaluating the way typical design parameters vary as a function of layout parameters, such as the number N of gate fingers and the gatewidth W. It is important to notice that this task cannot always be accomplished by simply sweeping suitable scaling variables. For example, the provided foundry model necessarily involves a separate simulation for each different number of gate fingers.

The MAG is shown, for instance, in Fig. 8, with N ranging from 4 to 12, and W from 30 to 100 μm. These results, which have been obtained by simply, continuously sweeping the scaling variables, are in good agreement with qualitative expectations [1], i.e., the simulated MAG is nearly constant versus the number of fingers at fixed gatewidth, while it decreases as the device gatewidth increases.

The same experiment has been repeated by using the scalable foundry model involving a separate simulation for each different number of gate fingers. The corresponding results are shown in Fig. 9.

Predicted and actual measured values of the MAG for the available device sizes are reported in Table III. The results quantitatively show that the proposed model accurately predicts (even slightly better than foundry model) the gain variations with respect to the unit gatewidth. Deviations reported in Table III are also graphically highlighted in Figs. 8 and 9.

The results presented in this section show that a lumped representation of the extrinsic parasitic phenomena, identified by means of suitable EM simulations, lead to a an accurate scalable model covering all the possible device sizes actually manufactured by the foundry.

IV. Example of Optimum Periphery Selection

A practical exploitation example of the advantages provided by the proposed scalable modeling approach is provided here.

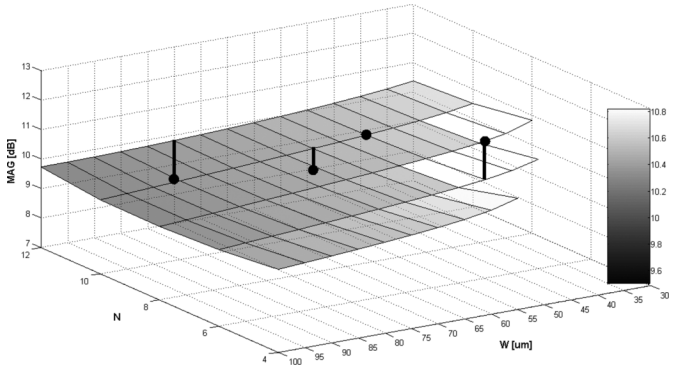

Fig. 9. MAG versus number of gate fingers and finger widths at 30 GHz evaluated through the foundry model. The black dots are the MAG values measured on actual device samples. Bold lines highlight the differences between measured and simulated values.

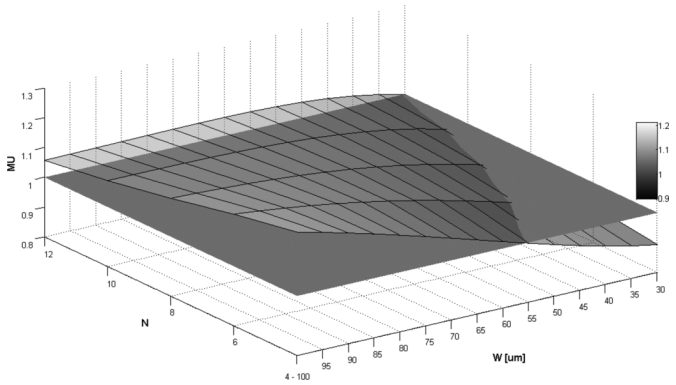

Fig. 10. Stability factor μ versus number of gate fingers and finger widths at 30 GHz evaluated through the proposed model. The gray plane corresponds to the $\mu = 1$ threshold.

TABLE III
MEASURED VERSUS MODELED MAG @ 30 GHz

Perif. [μm]	6x50	10x50	10x60	12x75
Measured [dB]	11.6	10.1	9.2	8.5
Proposed Model [dB]	11.2	10.3	9.5	8.7
Foundry Model [dB]	10.4	10.1	9.9	9.8

Let us consider the goal of selecting the optimum device periphery for the design of a narrowband linear driver amplifier working at 30 GHz.

Different criteria can be adopted for the choice of the elementary device cell to be paralleled in order to achieve the required output power. A first selection could be based on the maximization of MAG, when simultaneous input/output conjugate match (SCM) conditions are satisfied [2]. On the other hand, terminating impedances providing SCM can be only considered if the transistor is unconditionally stable at the desired frequency. In order to test this condition, the stability factor μ is evaluated versus the device periphery by considering $N = 4, 6, 8, 10, 12$ and $W = 30, 35, \ldots, 95, 100$ μm. To this aim, trivial S-parameter simulations are automatically repeated by sweeping the N and W variables. Corresponding results are presented in Fig. 10, showing that most of the investigated peripheries are in this case unconditionally stable at 30 GHz. Analogously, source and load reflection coefficients (Γ_L and Γ_S), providing input/output SCM conditions, are plotted on the Smith Chart versus N and W in Fig. 11. Optimum periphery selection can be easily carried out on the basis of these results, according to suitable design constraints such as gain, sensitivity to parameter variations, physical feasibility of the matching networks, stability margin, and so on.

The results shown in Figs. 8, 10, and 11 are easily and immediately obtained by means of the proposed model. Instead, the same investigation would require separate sets of simulations (one for each different number of gate fingers), when using the foundry model. This limitation could become dramatic if more complex optimization problems involving N and W as unknown parameters were considered.

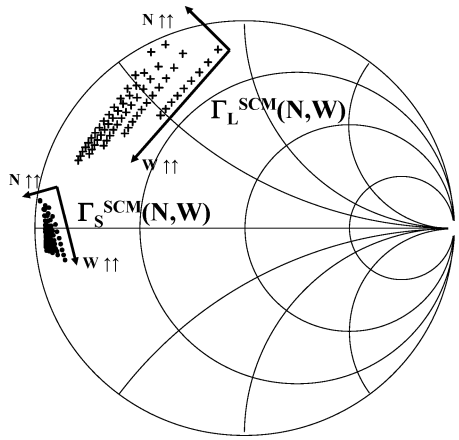

Fig. 11. Load and source reflection coefficients (Γ_L and Γ_S) providing input/output simultaneous conjugate match versus number of gate fingers and finger widths (N and W) at 30 GHz. N varying from 4 to 12 number of fingers (even numbers), W varying from 30 to 100 μm, step 5 μm. The arrows show how the reflection coefficients vary when the independent variables increase.

V. CONCLUSION

A new scalable modeling approach has been presented in this paper. It is based on the definition of a lumped component description of the extrinsic parasitic network, which is proven to be perfectly scalable with the number of gate fingers and the corresponding finger width. The device scalable parasitic elements are identified by using only EM simulation data of just one reference device. This means that neither device measurements in convenient conditions of passivity (i.e., pinched-off or forward-gate cold FET conditions), nor different-in-size device measurements are required for the extrinsic element extraction.

The extrinsic equivalent circuit elements are correctly linked to the device layout, allowing the model to scale with simple linear rules related to geometric-based scaling factors. Such scaling rules are process independent since they are neither completely empirical, nor fitting based. Besides its simple definition and identification procedure, the proposed scalable model provide good accuracy in the prediction of different devices having different peripheries.

Finally, the proposed model allows the designer to use the device geometrical parameters (in this case, the number of fingers and unit gatewidth) as swept and optimization variables.

Although this paper deals with linear descriptions of the intrinsic device, the approach is fully compatible with the application of any nonlinear empirical modeling approach.

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