AMCAD Engineering
Advanced Modeling for Computer-Aided Design

Technical Note

Behavioral Model of High Power GaN HEMTS for RF Doherty Amplifier

Products:

MT930C IVCAD Vector Receiver Load Pull
MT930G IVCAD Time Domain waveforms
MT930R IVCAD Behavioral Model Extraction

Problematic

Doherty Power Amplifier (DPA) architecture is used in modern telecommunication systems to optimize Power Added Efficiency (PAE). DPA is based on a principle of dynamic Load impedance modulation driven by the input level sent to both peak and main amplifier branches. Amplifier designers are using transistor models to create advanced designs with first-pass success. However, the accuracy of the model is a key point in this process.

The problematic of package transistor in the design of DPA is the difficulty to extract an accurate model that will enable a good prediction of the transistor behavior under different conditions of load impedance modulation. One can assume that it is simple for foundries to extract compact models for their transistors; they control their technology and they put the time and effort in it as an added value compared to other suppliers. On the other hand, PA designers don't have the luxury to spend weeks to extract a model before starting their design. AMCAD Engineering developed a behavioral model that will help designer obtain a robust and accurate model to design their DPA in a very short time, using time domain load pull measurements. Designers will then concentrate on designing the best DPA.

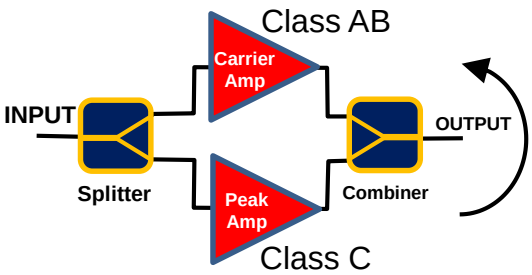


Fig:1 Hybrid Doherty Amplifier Design

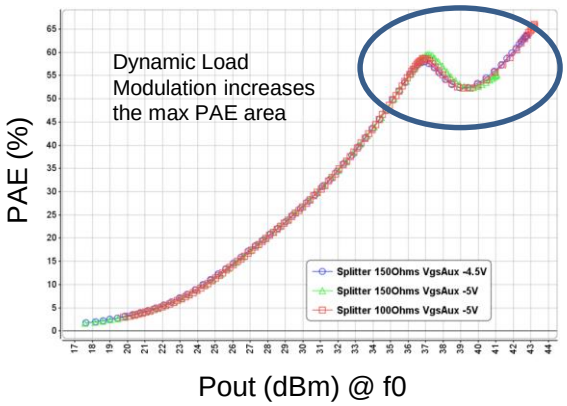


Fig:2 Power Added Efficiency of a DPA

Transistor Models

Three most common types of models are used in the industry today.

Physical Models

Based upon physical phenomena within the transistor, the equation of such a model can be applied to a wide range of operations compared to alternate methods. However, the number of parameters used, the extraction complexity and the nature of the model make it very difficult to use in a simulation environment. Moreover, such a model is practically impossible to extract for a packaged device.

Compact models

Based on an equivalent electrical schematic topology, and extracted from pulsed IV and S-parameters measurements, this model considers complex phenomena such as electro-thermal and trapping effects. Compact Models are ideal for die level applications. The model extraction is straight forward, the procedure is relatively simple and well established in the industry. Compact models are usually extracted by foundries who are in control of their process and can provide their customers with the right tool to start their design. However, compact modeling of a packaged device is more challenging as the dispersive behavior of the package hides the other elements of the transistor. Some foundries succeed to provide good models for their packaged devices but not for all their product lines. When such model is not available from foundries, it is not convenient for a PA designer to start by extracting such a model by himself.

*Behavioral model*s

Based on frequency domain measurements, this model is less flexible than physical or compact model but can easily be extracted for any type of components (bare die and packaged transistor). Behavioral models are considered “black-box” models where only responses of the components to controlled stimuli are known. Up to now, their validity was rather limited to the measured operating conditions. Figure 3 presents a diagram summarizing pros and cons of the three modeling techniques.

Enhanced Poly Harmonic Distortion –EPHD

Classic behavioral models are a good trade-off between modeling complexity and accuracy over a wide dynamic range. Nonetheless, they can suffer from convergence issues as in Doherty designs because of the insufficient isolation between the two DPA branches, which can create a strong dynamic load modulation of the load impedance as a function of the modulated signal envelop, mainly for the C class branch. At low power level, negative load impedances can even be applied. Unfortunately, these operating areas cannot be used for the model extraction, therefore the behavior model of the transistor is not clearly captured using Classical PHD approach.

A novel technique is proposed by AMCAD Engineering with an automatic adaptation order of the model kernel's power expansion. The goal is to take into account the nonlinear influence of the load impedance variations given by the low isolation between the two branches, while keeping a straightforward model extraction methodology. The following hypothesis has been considered: the nonlinear influence of the output port incident wave is observed only at fundamental frequency. Harmonic influences are supposed to be linear. This assumption limits greatly the model complexity and allows an easy extraction process with any Time domain waveforms measurement setups without cumbersome optimization processes.

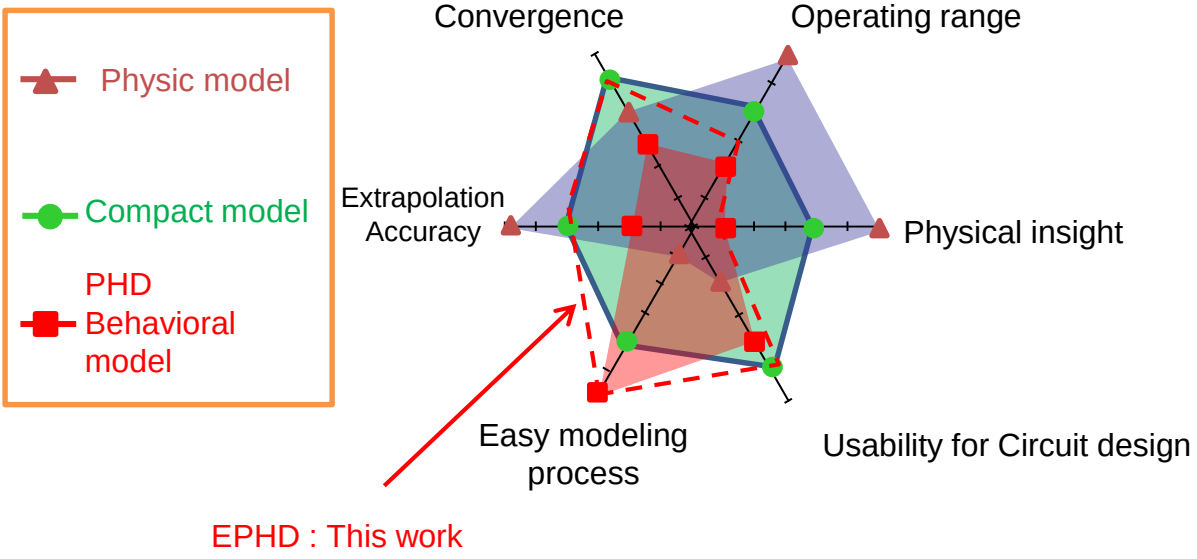
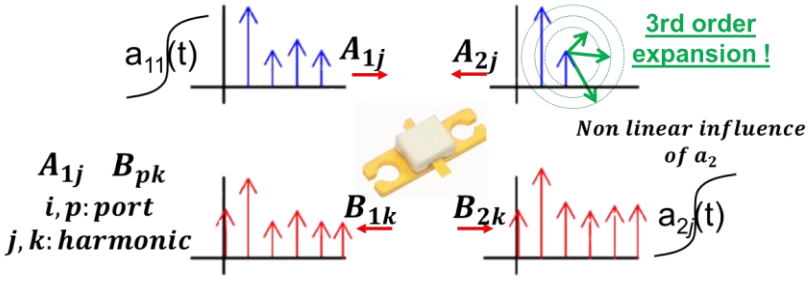


Fig. 3 Large signal Transistor models

EPHD Principle



$$\tilde{\tilde{b}}_{ik,mod}(t) = S_{ik,11,1}(|\tilde{a}_{11}(t)|)\tilde{a}_{11}(t) + S_{ik,21,1}(|\tilde{a}_{11}(t)|)\tilde{a}_{21}(t) + T_{ik,21,1}(|\tilde{a}_{11}(t)|)P^{k+1}\tilde{a}^{*}_{21}(t)$$ ---order1

Traditional PHD

$$+S_{ik,21,2}(|\tilde{a}_{11}(t)|)P^{-1}\tilde{a}^{2}_{21}(t) + T_{ik,21,2}(|\tilde{a}_{11}(t)|)P\tilde{a}_{21}(t)\tilde{a}^{*}_{21}(t) + U_{ik,21,2}(|\tilde{a}_{11}(t)|)P^{3}\tilde{a}^{*}_{21}(t)^{2}$$ ---order2

$$+S_{ik,21,3}(|\tilde{a}_{11}(t)|)P^{-3}\tilde{a}^{3}_{21}(t) + T_{ik,21,3}(|\tilde{a}_{11}(t)|)\tilde{a}^{2}_{21}(t)\tilde{a}^{*}_{21}(t) + U_{ik,21,3}(|\tilde{a}_{11}(t)|)P^{2}\tilde{a}_{21}(t)\tilde{a}^{*}_{21}(t)^{2} + W_{ik,21,3}(|\tilde{a}_{11}(t)|)P^{4}\tilde{a}^{*}_{21}(t)^{3}$$ ---order3

AMCAD Contribution for EPHD

This expression depends on the N order expansion that was chosen. It is linked to the range of load impedances provided at the fundamental frequency. In the linear region, the transistor's behavior is perfectly described with the 4 S-parameters $S_{ik,11}$. When the input power level ($|\tilde{a}_{11}|$) increases, the model validity is given for a reduced load impedance area: $G_{Load} = \tilde{b}_{21}/\tilde{a}_{11}$

The power expansion of a_{21} allows to maximize the validity area of the model if the N order is optimized. During this optimization procedure, for a given frequency, the first step is to determine the optimum load impedance area, centered on Zref which represents the best trade-off between PAE and Output power. Zref is then chosen as the center impedance of the load pull pattern used for the model extraction. Zref is represented in the flowchart sketched in Fig. 5. The second step is then to extract the model using different carrier frequencies and power sweeps during the load pull measurements. For each incident power level, the linear model response is compared to a large set of measurement data using the following function:

$$\tilde{\epsilon}(\tilde{a}_{11}, \tilde{a}_{21}) = \tilde{b}_{ik,mes} - \tilde{b}_{ik,mod}.$$

Once the nonlinear order of the model has been estimated, a specific Zload pattern is applied at the output of the DUT in order to perform an accurate extraction of the model kernels. These empirical specific patterns have been studied from LSQR approximation.

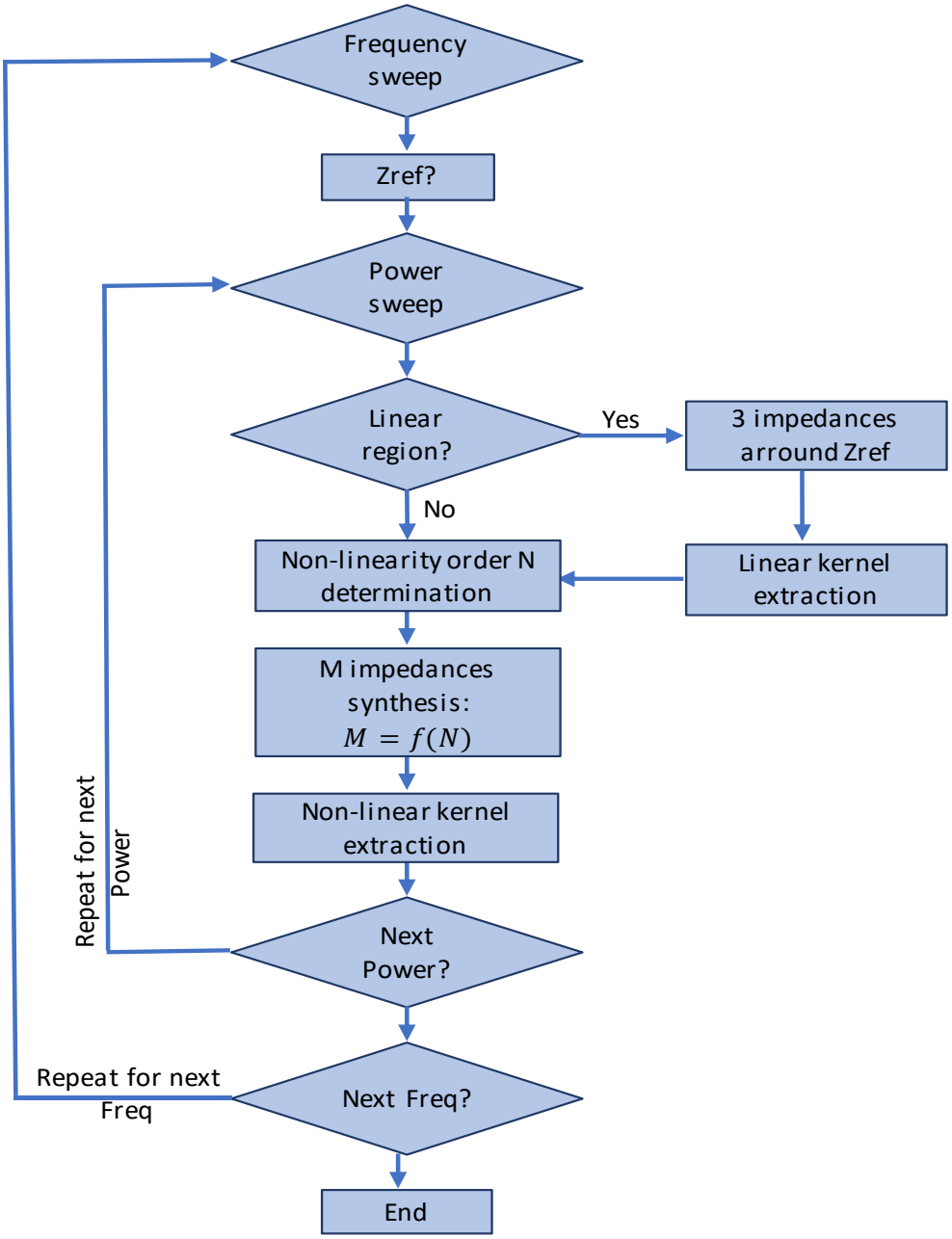


Fig:4 Flowchart for Behavioral model extraction

Measurement Setup for Model extraction

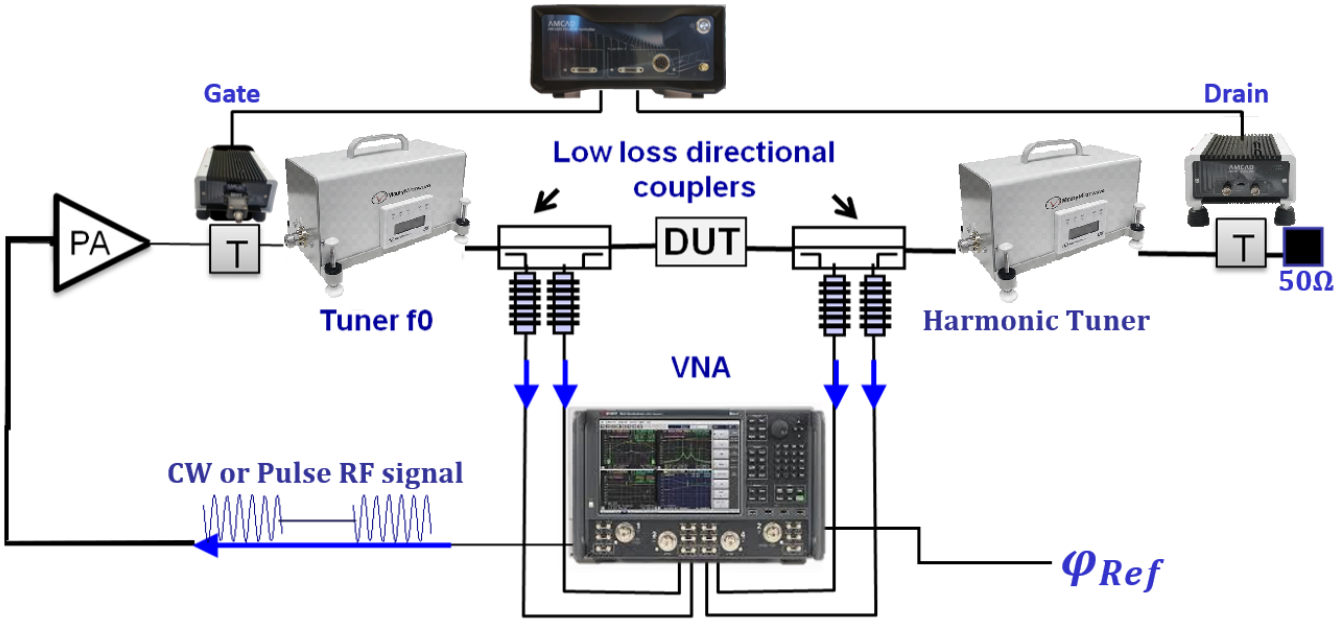


Fig:5 Time domain waveforms measurement setup for EPHD model extraction

In order to extract a model which takes into account the transistor's harmonic behavior, a time domain waveforms measurement setup is used. This one provides absolute phase relationships between fundamental and harmonic tones. The measurement setup for this model extraction is depicted in Fig. 5. a hybrid active or a full active setup can be used as well.

The measurement principle consists of a harmonic load pull control which does not require tickle tone injection, reducing significantly the complexity of the setup and the measurement time. A specific pattern of load impedances is applied for each fundamental frequency.

Experimental and Simulated Results

This section illustrates the behavioral model capabilities for a 10W GaN Packaged Transistor biased in AB and C classes and operating at 3.7 GHz and 3.95 GHz fundamental frequencies.

Class AB Model at 3.7 GHz

On the shelf transistor was chosen for this experiment. Time domain waveform measurements were done using the setup in Fig. 5. The device was biased in Class AB for the main amplifier and an EPHD model was extracted. Figure 6. shows the performance of the transistor (red) and the EPHD model (blue) extracted from Load pull measurements.

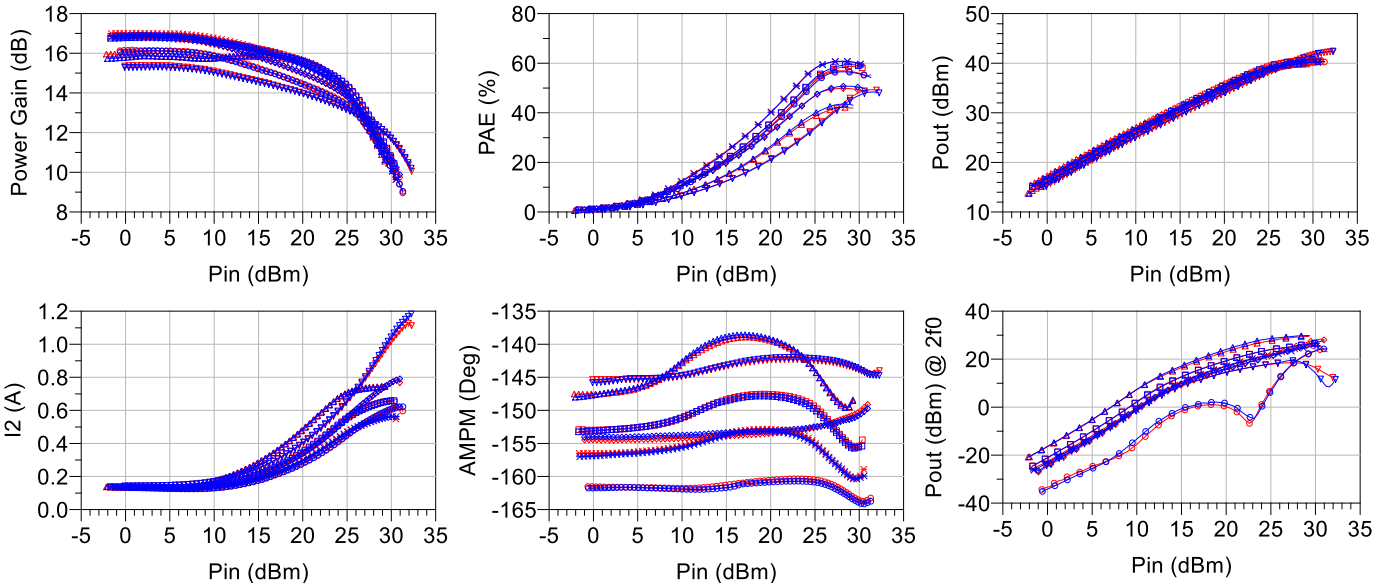


Fig. 6 Measurements vs model results for a package device biased in class AB

One can observe the model ability to predict Power Gain, DC Consumption, Phase shift, Power Added Efficiency, as well as output power generated at harmonic frequencies, for different load impedances.

Class C Model at 3.7 GHz

A second device was used to model the peak amplifier. The device was biased in Class C and an EPHD model was extracted. Figure 7 shows the remarkable performance of the transistor's model , which is able to predict sharp gain expansion , (measurements in red vs EPHD model in blue) for various load impedances.

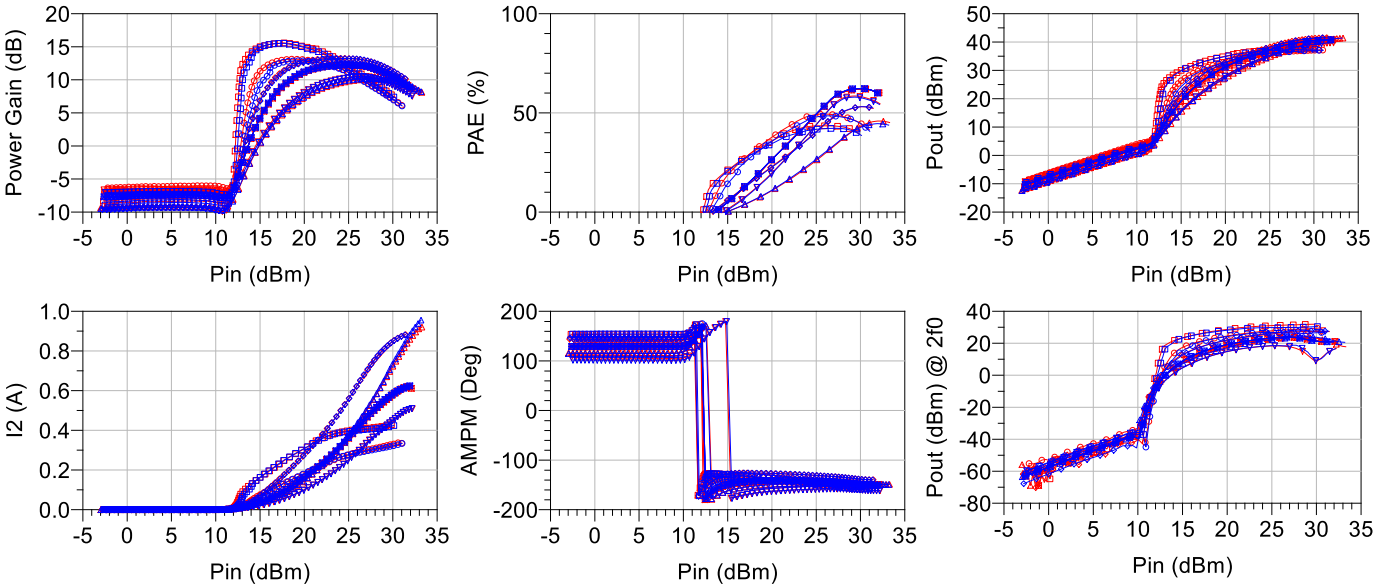


Fig. 7 Measurements vs model results for a package device biased in class C

Doherty Power Amplifier Design

AMCAD Engineering designed a DPA based on simulation using the two models extracted in the previous section. Load pull measurements were done and models were extracted at 3.7 GHz and 3.95 GHz. The EPHD Model should be able to predict the overall Doherty Design performances without any convergences issues across the frequency range.

Fig. 8 represents the simulation results of a DPA at different frequencies. It is clear that the EPHD model was able to predict the frequency interpolation for this design.

A second test is done under extrapolation conditions of load impedances at the frequency band in order to validate the behavioral model for different load modulation paths varying the λ/4 length of the combiner in the design. The results are provided by the behavioral model used in load extrapolation mode. Fig. 9 shows that the model is capable of extrapolating the load impedance modulation even in the worst conditions.

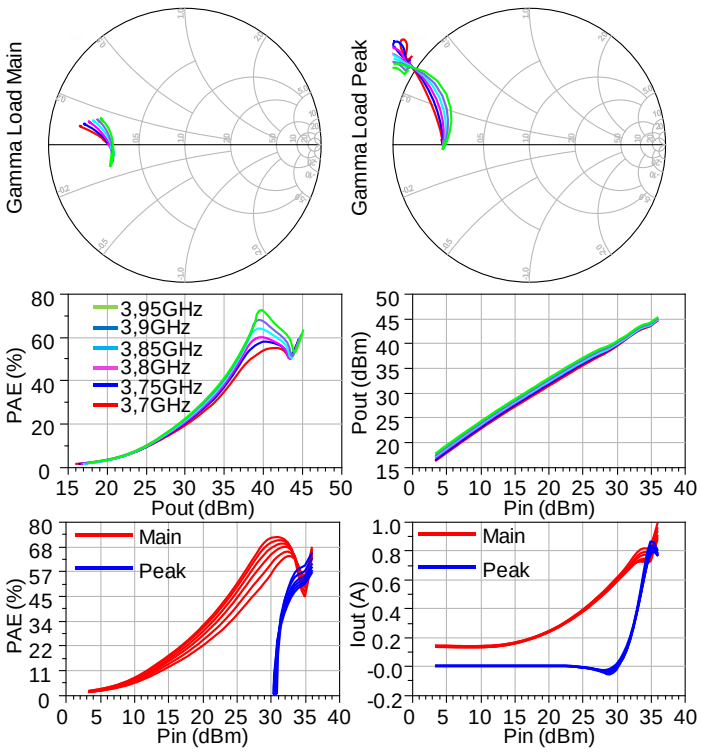


Fig. 8 Behavioral model interpolation capabilities vs frequency

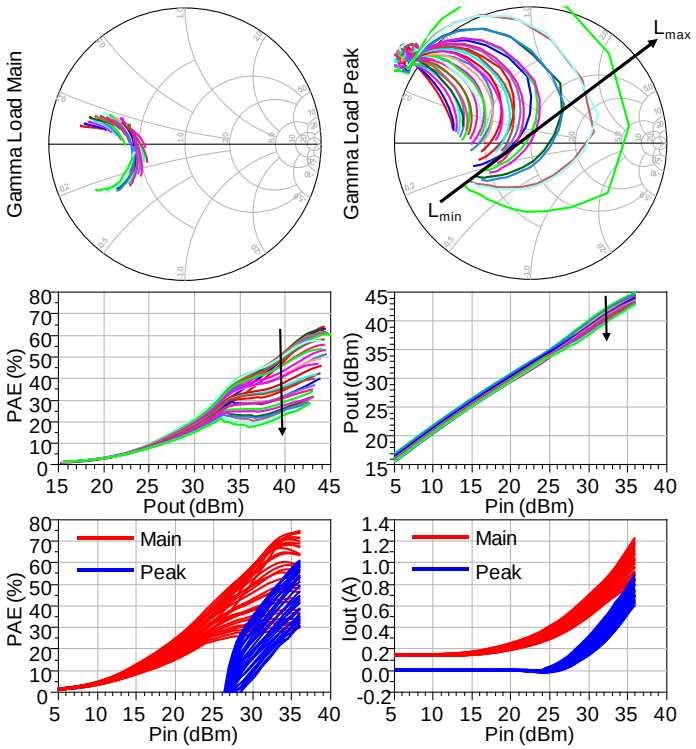


Fig. 9 Behavioral model extrapolation capabilities vs load impedances

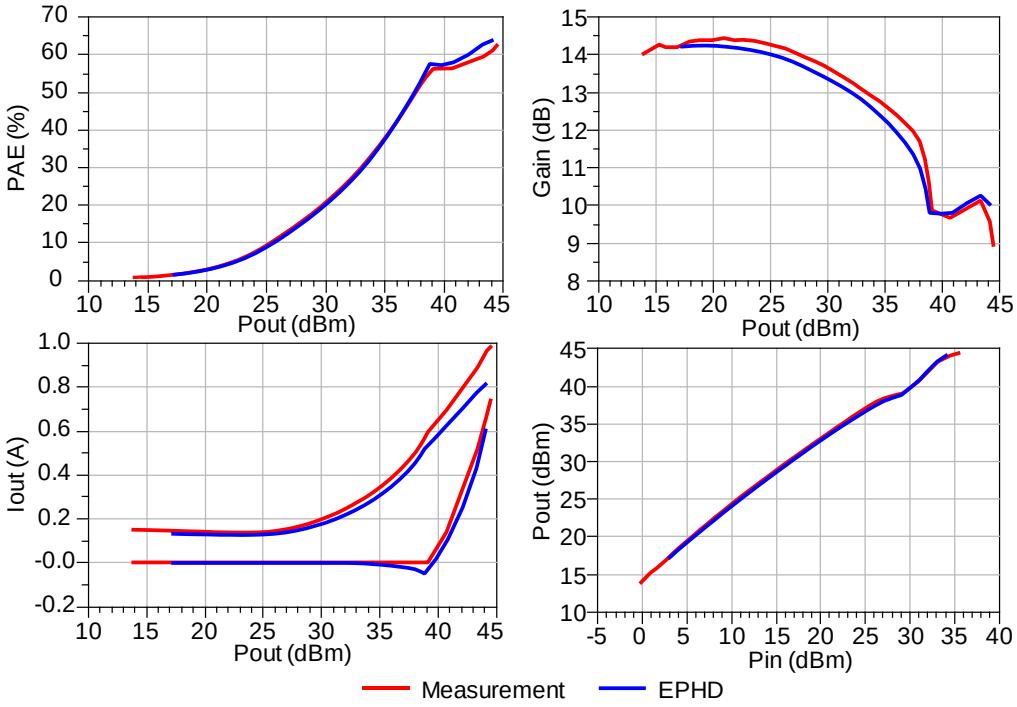


Fig. 10 Overall DPA performances. Measurements vs simulation

Fig. 10 shows an excellent agreement between measurements and simulation results using EPHD models at circuit level. The model was able to accurately predict PAE, Gain, Power and Current.

Conclusion

This new model extraction is a simple methodology that can directly be used with a time domain waveform based Load Pull measurement setup without any further model tuning or optimizations. The good agreement between measured and simulated results confirms the validity of this modeling methodology for the design of high power DPAs. The ability of this model to predict the overall Design performances without any convergence issues has been proved even for extrapolated load conditions, during the simulation, and with the load impedances used during the load pull measurement process. Therefore, this new model is a promising candidate for the design of power amplifiers of future telecommunication systems due to its robustness , flexibility, and reliability.

More references :

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