5G Module Design Rules and Release Procedures

Ver.1.1

1 Document Description

This document is intended to provide an overview about the module design (stackup, layers, routing options…) to give an introduction into the design options in the second chapter.

The design rules (layout rules and formal requirements) are described in the subsequent chapter.

In addition to that the document is provides a description of the procedures and scripts for releasing the design.

2 Module Design Flow Overview

2.1 Software packages

Before starting, you must make sure that all required software packages are installed at your site. The most important are:

- Keysight Advanced Design System ADS 2019 Update 1.1
- Cliosoft SOS Client 7.04.p12
- Modelithics Complete Library for Keysight ADS v19.0
- DownStream Technologies CAM350 v12.1
- Autodesk AutoCAD

2.2 Stackup Description

In Figure 1 Manufacturing Stackup Information Based on MGA36030MK the module stackup and layer thickness based on the first product (MGH36030MK) is described. It shall be noted that the final dielectric thickness of the prepreg materials depends on the copper densities of the design and thus will vary from design to design (the initial sheet thickness will be adopted to achieve the target value). Since the final thickness can only be predicted after the design is finished 50um is used for all layers during the design procedure, as depicted in Figure 2.

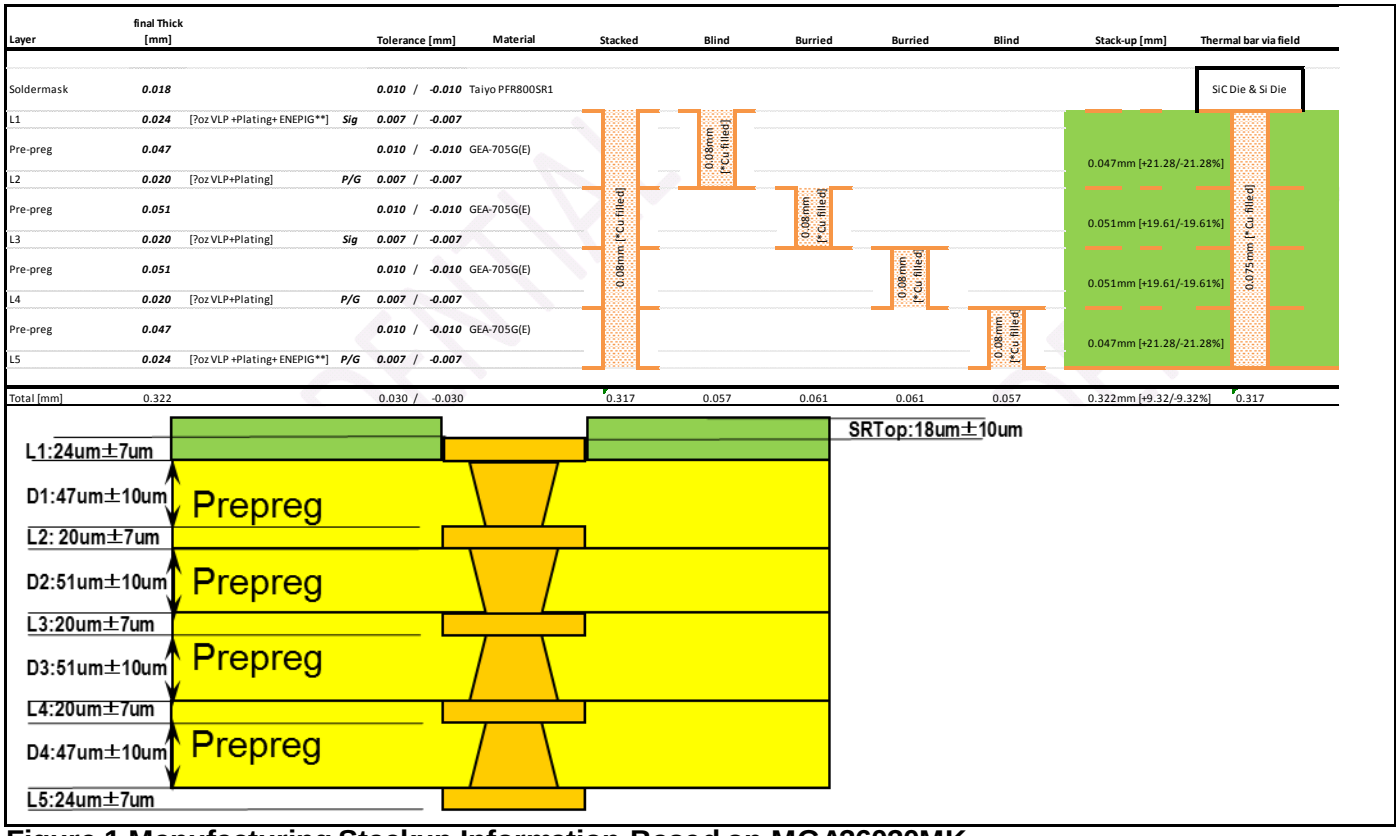
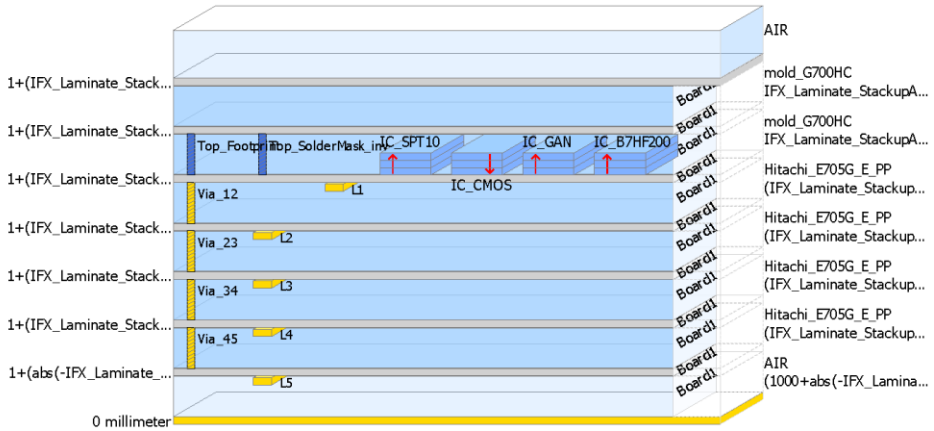


Figure 1 Manufacturing Stackup Information Based on MGA36030MK



L1		24um
Board1	Via_12	50um
L2		20um
Board2	Via_23	50um
L3		20um
Board3	Via_34	50um
L4		20um
Board4	Via_45	50um
L5		24um

Figure 2 Design Stackup Information

2.3 Layer Description

Name	Nr.	Purpose	Description
Ports	11	drawing	Ports Layer, required for compliance with standard ADS layers
PCB_L1	41	drawing	customer/test PCB board metal 1 layer
PCB_L2	42	drawing	customer/test PCB board metal 2 layer
PCB_L3	43	drawing	customer/test PCB board metal 3 layer
PCB_L4	44	drawing	customer/test PCB board metal 4 layer
PCB_VIA12	51	drawing	customer/test PCB board metal 1 to metal 2 via
PCB_VIA23	52	drawing	customer/test PCB board metal 2 to metal 3 via
PCB_VIA34	53	drawing	customer/test PCB board metal 3 to metal 4 via
PCB_board	60	drawing	customer/test PCB board board outline
PCB_top_SM	61	drawing	customer/test PCB board top soldermask
PCB_btm_SM	62	drawing	customer/test PCB board bottom soldermask
PCB_Top_Footprint	63	drawing	customer/test PCB board top footprint layer
PCB_Top_Paste	64	drawing	customer/test PCB board top solderpaste (stencil)
Layout	70	drawing	layer for layout (alignment) purposes, will not be used for any fabrication step
PKG	80	drawing	package outline (overmold) layer
PKG_shield	81	drawing	package top metal shield (sputtered)
PKG_trench_shield	82	drawing	package shielding trench (metal filled)
Bondpad_conn	87	drawing	auxillary bonpad layer needed for establishing proper connectivity (layer binding)
Bondpad	88	drawing	bonpad (ENEPIG plated) layer
Bondwires	89	drawing	Bondwire layer
Top_SilkScreen	90	drawing	Top silkscreen layer
Top_Soldermask	91	drawing	top soldermask (negative) layer
Top_Paste	92	drawing	top solderpaste (stencil) layer
Top_Footprint	93	drawing	top footprint layer
Btm_SolderMask	95	drawing	bottom soldermask (negative) layer

Name	Nr.	Purpose	Description
Btm_SilkScreen	96	drawing	bottom silkscreen layer
Btm_Paste	97	drawing	bottom solderpaste (stencil) layer
L1	101	drawing	routing layer for metal 1 (top)
L1	101	fill	ground/plane layer for metal 1 (top)
L1	101	keepout	indicates ares that need to remain free of metal 1 (top)
L2	102	drawing	routing layer for metal 2
L2	102	fill	ground/plane layer for metal 2
L2	102	keepout	indicates ares that need to remain free of metal 2
L3	103	drawing	routing layer for metal 3
L3	103	fill	ground/plane layer for metal 3
L3	103	keepout	indicates ares that need to remain free of metal 3
L4	104	drawing	routing layer for metal 4
L4	104	fill	ground/plane layer for metal 4
L4	104	keepout	indicates ares that need to remain free of metal 4
L5	105	drawing	routing layer for metal 5 (bottom)
L5	105	fill	ground/plane layer for metal 5 (bottom)
L5	105	keepout	indicates ares that need to remain free of metal 5 (bottom)
Via_12	121	drawing	Via between metal 1 and metal 2
Via_23	122	drawing	Via between metal 2 and metal 3
Via_34	123	drawing	Via between metal 3 and metal 4
Via_45	124	drawing	Via between metal 4 and metal 5
Board1	141	drawing	main board outline
Board2	142	drawing	RFU if lower board layers are different from Board1
Board3	143	drawing	RFU if lower board layers are different from Board1
Board4	144	drawing	RFU if lower board layers are different from Board1
Board5	145	drawing	RFU if lower board layers are different from Board1
Board6	146	drawing	RFU if lower board layers are different from Board1
Text1	190	drawing	RFU unit ID (text) layer for special DRC treatment
IC_SPT10_lib_die	256	drawing	die outline SPT10 nested technology
IC_SPT10_lib_bondpad	257	drawing	bondpads SPT10 nested technology
IC_CMOS_lib_die	258	drawing	die outline CMOS nested technology
IC_CMOS_lib_bondpad	259	drawing	bondpads CMOS nested technology
IC_GaN_lib_die	260	drawing	die outline GaN nested technology
IC_GaN_lib_bondpad	261	drawing	bondpads GaN nested technology
IC_B7HF200_lib_die	262	drawing	die outline B7HF200 nested technology
IC_B7HF200_lib_bondpad	263	drawing	bondpads B7HF200 nested technology
IC_CMOS_lib_bumps	264	drawing	bump pads (flip chip) CMOS nested technology

Table 1 Layer Specification and Description

2.4 Transmission Line Implementation Options

There are 4 main options on how to implement transmission lines on the module substrate, as depicted in Figure 3. Any other combinations are possible, but these 4 combinations are selected as an example as a reference for area efficient implementation. Other options within the design rules are of course possible.

Two Microstrip options **Signal L1/Ground L3** and **Signal L1 and Ground L2**, with different electrical and mechanical properties. Additional two stripline implementation, namely a symmetric stripline with **Signal L4 Ground L3/L5**, as well as an asymmetric stripline (lower loss) with **Signal L3 and Ground L2/L5**, are possible to be implemented. The according electrical properties are given in Figure 4.

L1 Signal	L1	**L1 Signal**
Board1	Via_12	Board1
L2 empty	L2	**L2 Ground**
Board2	Via_23	Board2
L3 Ground	L3	**L3 Signal**
Board3	Via_34	Board3
L4 signal	L4	**L4 empty**
Board4	Via_45	Board4
L5 Ground	L5	**L5 Ground**

Figure 3 Transmission Line Implementation Options

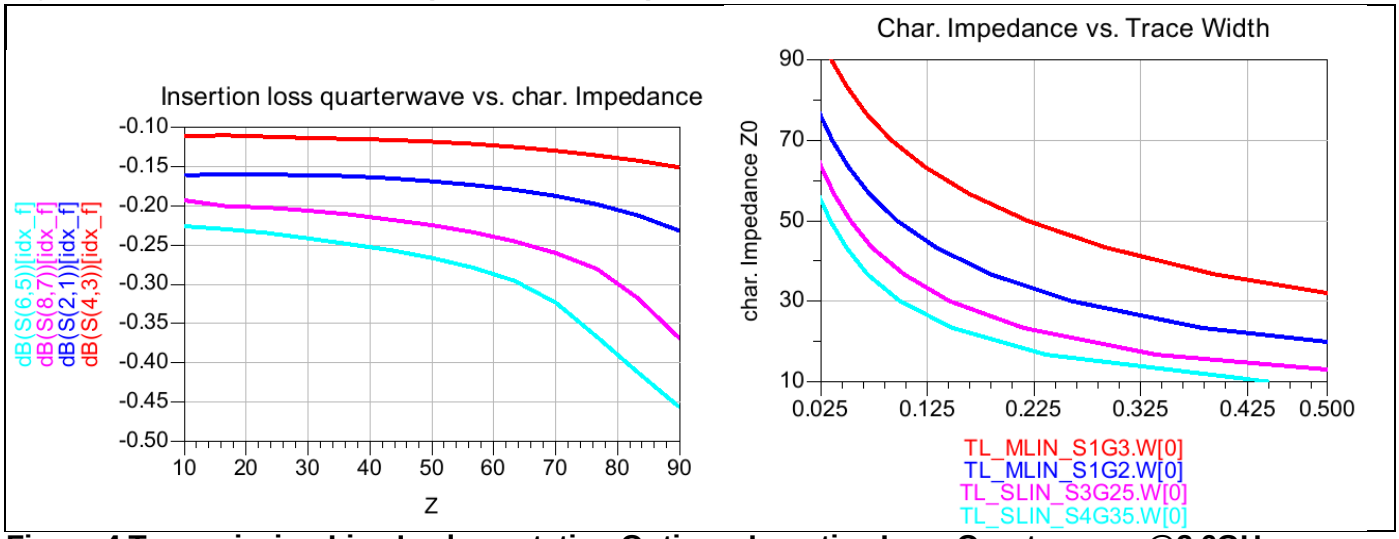


Figure 4 Transmission Line Implementation Options, Insertion Loss Quarterwave @3.6GHz and Characteristic Impedance vs. Width

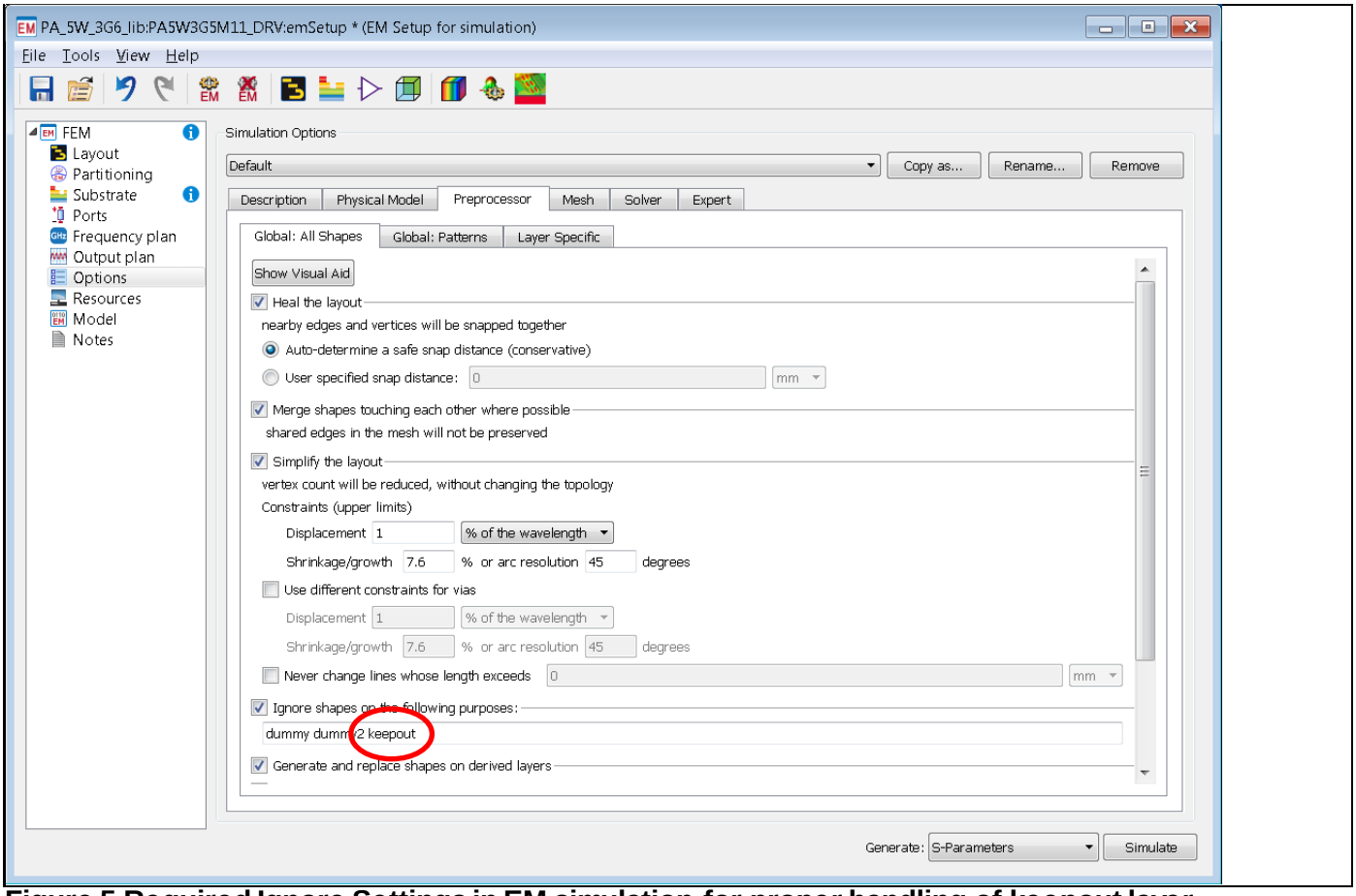


Figure 5 Required Ignore Settings in EM simulation for proper handling of keepout layer

3 ADS custom toolbar

As soon as the IFX laminate PDK is added to an ADS workspace the toolbar will be shown in the schamtic/layout window. Depending on the view (layout/schematic) the toolbar will show different commands.

schematic	
layout	

Table 2 IFX Custom toolbar

Icon	Description	Applies to
	Displays PDK version information	layout / schematic
	Checks the view out of the DataMmgt system (Cliosoft SOS).This command will not check for object dependencies as is done with the SOS integrated command. **Expert use only!**	layout / schematic
	Checks the view into the DataMmgt system (Cliosoft SOS).This command will not check for object dependencies as is done with the SOS integrated command. **Expert use only!**	layout / schematic
	Traverse the design and checks which instances have been tagged with the selected tag name (e.g.: Gold, Silver, DRC_clean etc…)	layout
	Adds the “gold” label/tag(cliosoft SOS) to the view Indicating the level of confidence of the design. Please see sign-off procedure section how labels need to be used.	layout / schematic
	Adds the “silver” label/tag(cliosoft SOS) to the view Indicating the level of confidence of the design. Please see sign-off procedure section how labels need to be used.	layout / schematic
	Adds the “bronze” label/tag(cliosoft SOS) to the view Indicating the level of confidence of the design. Please see sign-off procedure section how labels need to be used.	layout / schematic
	Adds the “layout_done” label/tag(cliosoft SOS) to the view Needs to be applied before DRC results can be added to the Datamanagement system. Please see “How to use DRC” procedure section for details.	layout
	Generates the Bill of Material (BOM) file. Please see BOM export procedure section for details.	layout
	Generates the Bond wire profile (BWP) file for all Bondwires in the selected view. Please see BOM export procedure section for details.	layout

ADS custom toolbar

Icon	Description	Applies to
	Generates the Bond wire profile (BWP) file for predefined Bondwires only.Please see BOM export procedure section for details.	layout
	Generates the gerber and drill (*.ger,*.drl) files. Please see Gerber export procedure section for details.	layout
	Generates the Autocad (DXF) file. Please see Bond wire Diagramm (BWD) generation procedure section for details.	layout
	Calculates the metal densities. Please see Metal Density Check procedure section for details.	layout
	Invoke Design Rule Check (DRC) tool. Please see “How to use DRC” procedure section for details	layout
	View DRC results Please see “How to use DRC” procedure section for details.	layout
	Upload DRC results to the repository Please see “How to use DRC” procedure section and sign-off procedure section for details	layout
	download DRC results from the repository Please see “How to use DRC” procedure section and sign-off procedure section for details	layout
	Create automatically GND return layout pins and construct EM ports	layout

Table 3 IFX Custom toolbar command description

4 ADS Workspace/Library structure and naming convention

4.1 Library structure

To include data files easily in the design flow if required the library structure shown in Figure 6 should apply. The lead designer or library manager is responsible to provide the proper library structure to the designers. Data files need to be stored in the <library_name>\circuit\data subfolder and be under control of the data management system. Therefore these files need not to be stored and referenced to external data locations. During loading of the library the subfolders will be included in the search path such that the data files need only be referenced by name.

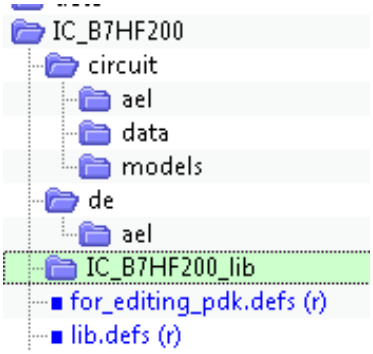


Figure 6 light PDK including OA libraries

4.2 Cellview naming convention

The cellview naming convention as depicted in Figure 7 and described in Table 4 should apply.

A typical cell will include only a subset of the views as shown in Figure 7.

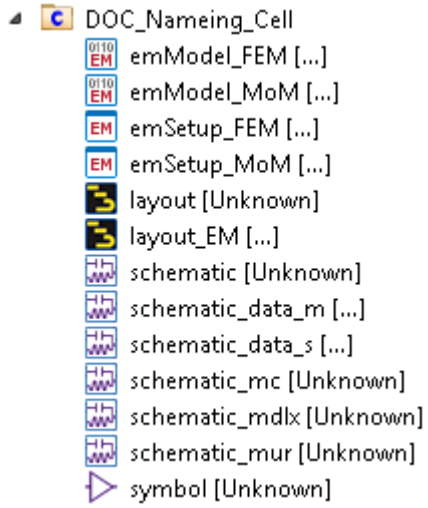


Figure 7 typical cellviews

Cellview name	Description	Status
schematic	Standard schematic view. Holds the nominal schematic design. Will be used in the layout design differences windows.	Required for schematic based design entry
layout	Standard Layout view. Holds the layout design. Will be used in the schematic design differences windows. Does not include planes, pins etc. required for EM simulation	Required for layout based design entry
symbol	The symbol should have only the minimum required number of pins necessary for simulation.	Required for schematic netlisting
schematic_data_m	Schematic referencing to imported measured data files	Optional
schematic_data_s	Schematic referencing to imported data files originating from simulation in external simulators (e.g. Cadence)	Optional
schematic_mc	Holds the schematic design used for statistical analysis (e.g: yield and mote carlo simulations).	Optional
schematic_mdlx schematic_mur e.g.: schematic_<model>	Holds vendor specific device models. Is been used in IFX SMT library.	Optional
layout_EM	Includes a reference to the layout view. Additionally includes objects required only for EM simulation	Optional (Only be used for EM model creation, Not to be used in the hierarchical layout design)
emSetup_MoM emSetup_FEM	Includes necessary configuration settings for running EM simulations.The name should indicate for which simulation engine the settings apply.	Optional
emModel_MoM emModel_FEM	Includes the EM model. The name should indicate for which simulation engine the settings apply.	Optional

Table 4 cellview description

All symbols, circuits, and layouts generated need to have grid snapping enabled. All pins and ports need to be on the grid.
Before you begin drawing a custom symbol, check to see if the current grid spacing is set to something other than the default of 0.125 inch; and if it is, change it back to the default and make sure Enable Snap is turned on. This step ensures that your custom symbol will easily connect to the set of provided symbols. Remember that pins should be located at 0.125-inch intervals so that your custom symbol will connect easily to the set of provided symbols. In addition, pin 1 should be placed at the coordinates (0,0).
The origin for the layout view should be coincident with either the Pin 1 location, the center of the bounding box of the layout or at a corner (e.g.: chip corner, gnd paddle corner etc,). This will be the anchor point for placing the layout in a hierarchical design. Be aware that modifying the origin of a

child layout **after** it has been placed in a parent layout will change the position of the child layout within the parent layout.
The origin for the schematic view should be coincident with Pin 1.

5 Using IFX SMT Library

5.1 Library structure

The IFX SMT library unites the different available simulation models with DRC conform footprint layouts. Additionally it allows easily integrating EM cosimulation capabilities,

The library structure is shown in Figure 8.

Figure 8 IFX SMT library structure

Based on the cell name the following parameters can be derived:

- Component Type:
  - CAP…Capacitor
  - IND…Inductor
  - RES..Resistor
- Component size:
  - 01005(inch): 0.4x0.2 mm
  - 0201(inch): 0.6x0.3 mm
  - 0402(inch): 1.0x0.5 mm
  - 0603(inch): 1.6x0.8 mm
- Vendor:
  - ATC: American Technical Ceramics
  - AVX:
  - MUR: Murata
  - PAN: Panasonic
  - KOA: KOA Speer
  - VIS: Vishay
- Model Family

For each cell/component a few different schematic views (see Figure 9) including different compact models (see Table 5) are available. These can be selected either as simulation view in the cell instance or in a config view to be used during netlisting (dynamic model selection).

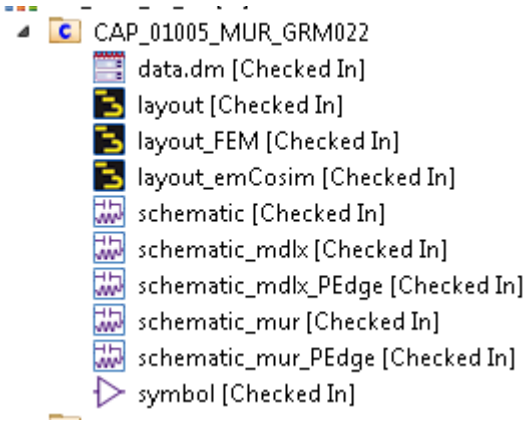


Figure 9 IFX SMT cell structure

Cellview name	Description
schematic	Standard schematic view. Holds the nominal schematic design. Includes a place holder with ideal circuit element.
schematic_mdlx	Holds the modelithics model. The sim model is set to remove pad effects to avoid double accounting with the EM-model of the pad layout
schematic_mdlx_PEdge	Holds the modelithics model. The sim model includes the full parasitic model. The reference planes are coincident with the pad outer edges.
schematic_mur	Holds the murata vendor model. The sim model does not include any substrate or pad effects.
schematic_mur_PEdge	Holds the murata vendor model plus a compact layout model. The sim model does include pad effects.

Table 5 IFX SMT cellview description

For each cell in the library the available cell parameters are listed in Table 6

Cellview design parameter	Description
C/L/R	Component value (real).
Subst	Substrate name (string)
Tolerance	Tolerance (real): Part value tolerance. Nominal value should be 1.0
dW	copper patterning tolerance in um (real)
PartNumber	Partnumber for the component (string)
Comment	Placeholder for additional comments/requirements (string)
Manufacturer	component manufacturer (string)
StockID	Subcon StockID number (read-only) If the entered partnumber is recognized by the system the Subcons "StockID" and the number of items available in the inventory will be shown in the instance parameters. If the partnumber is not found in the system or 0 items are available the StockID parameter will display "not found in stock" resp. "out of stock
StockQuantity	See above
EM_Port1_Ref_plane	EM Port 1 reference plane (EMCosim only) (Drop-down) Reference plane set to Pad center (:0) Reference plane set to Pad edge (:1) Reference plane set to Component body edge (:2) Reference plane set to Pad inside edge (:3)
EM_Port1_GND_reference	EM Port 1 GND reference (EMCosim only) Defines GND return path for EM port (Drop-down) Available layers (need to be mapped in the EM stackup definition) Default-"Implicit"- GND return reference is the closest gnd plane defined in the EM Stackup
Layout_Port1_Ref_plane	Layout pin 1 location (Layout only) (Drop-down) Reference plane set to Pad center (:0) Reference plane set to Pad edge (:1) Reference plane set to Component body edge (:2) Reference plane set to Pad inside edge (:3) For layout connectivity – can be set independent to EM_Portx_Ref_reference
EM_Port2_Ref_plane	EM Port 2 reference plane (EMCosim only) (Drop-down) Reference plane set to Pad center (:0) Reference plane set to Pad edge (:1) Reference plane set to Component body edge (:2) Reference plane set to Pad inside edge (:3)
EM_Port2_GND_reference	EM Port 2 GND reference (EMCosim only) Defines GND return path for EM port (Drop-down) Available layers (need to be mapped in the EM stackup definition) Default-"Implicit"- GND return reference is the closest gnd plane defined in the EM Stackup

Cellview design parameter	Description
Layout_Port2_Ref_plane	Layout pin 2 location (Layout only) (Drop-down) Reference plane set to Pad center (:0) Reference plane set to Pad edge (:1) Reference plane set to Component body edge (:2) Reference plane set to Pad inside edge (:3) For layout connectivity – can be set independent to EM_Portx_Ref_reference
EM_simplifcation	EM simplification (EM only) (Drop-down) ON: simplified layout artwork used in EM sims OFF: full detailed layout artwork used in EM sims
SimulationView	Simulation view Simulation view can be set by parameter or manually using the component drop down menu. **Warning** Expert mode parameter Changes in the cell parameter will override the simulation view set using the manual entry in the component->choose view for simulation drop down menu if you edit the instance parameters (Drop-down) Schematic views available in cell instance "Policy" – follow hierarchy Policies definition

Table 6 IFX SMT cell parameters

5.2 EM Co-simulation

5.2.1 Classical / Manual Methodology

The Classical/Manual Methodology summarizes the steps needed to generate a standalone FEM EM model with the setup Type and EM Simulator settings selected as shown in Figure 10.

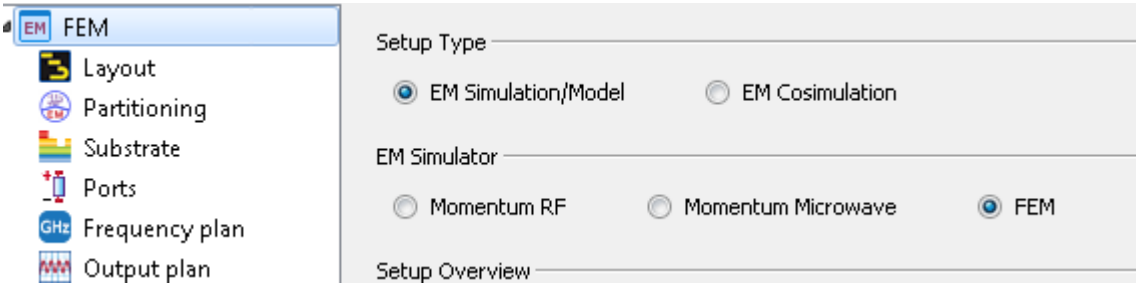


Figure 10 EM setup configuration

For the EM simulation it is important to define the correct location/layer for the ground pin of a port. If the ground is not on the same layer and there are no special requirements/restrictions for the location of the ground reference this shall be done by specifying the ground reference layer in the port editor dialog. The green box in Figure 11 highlights such an example for the port SIG_P, whereas the red box depicts the location where the GND reference needs to be selected. The default setting is "implicit" and it needs to be modified to the desired layer for the ground reference. For special cases, like stripline excitation on lower layers like L3, or if the ground port needs to be on the same layer (eg. L5 external package connections), an explicit ground port assignment is necessary. The orange box

in Figure 11 depicts such an example and the port assignment is done in the same way as it was done for all ports in ADS2016.

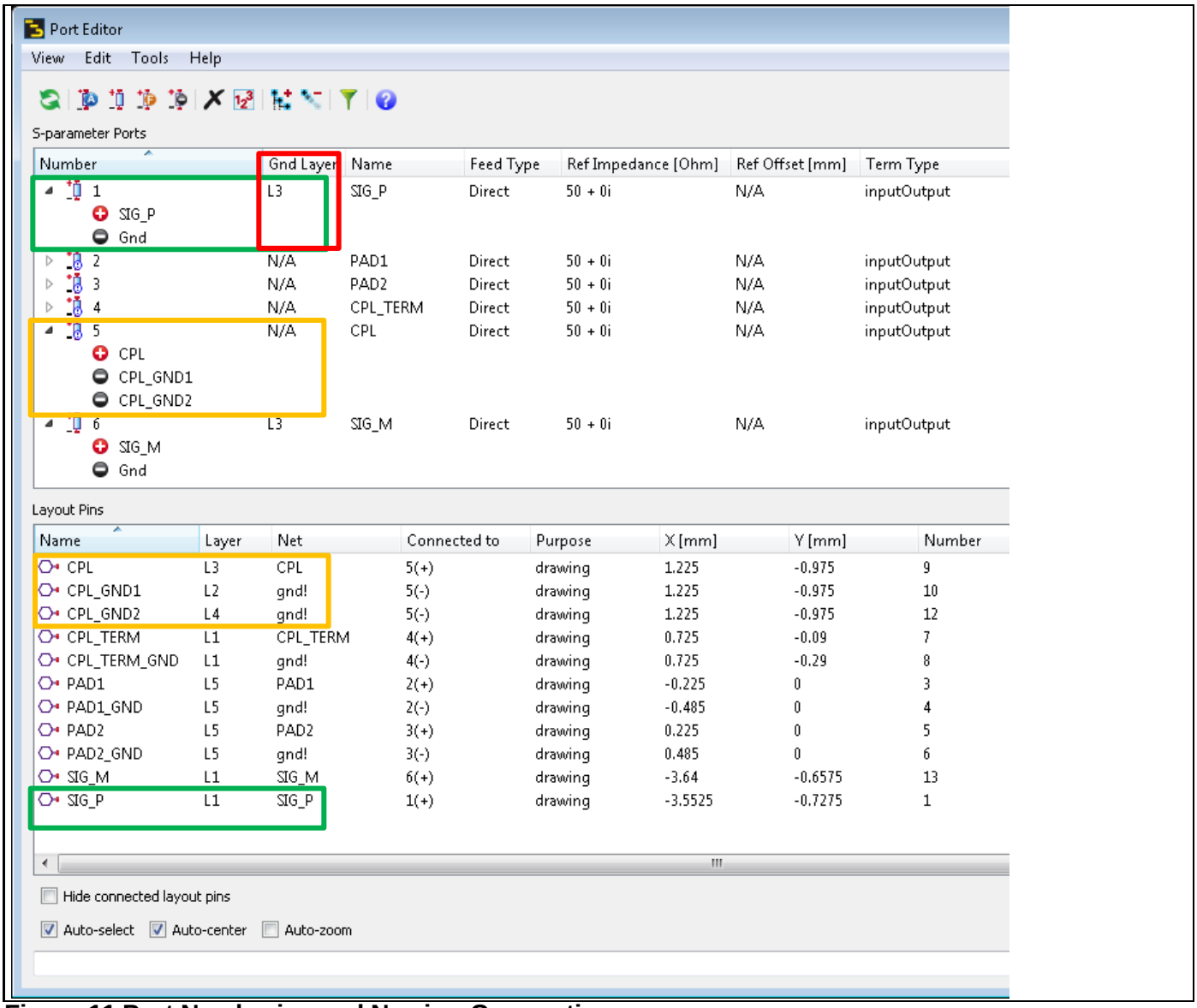


Figure 11 Port Numbering and Naming Convention

The recommended port settings/definition for shunt/series configuration of SMD components are shown in Figure 12. For the shunt components the port must be placed outside the ground via, see Figure 12(a). For series components, as depicted in Figure 12 (b) the ports should be placed at the beginning of the SMD components to reduce the effect of coupling between the ports.

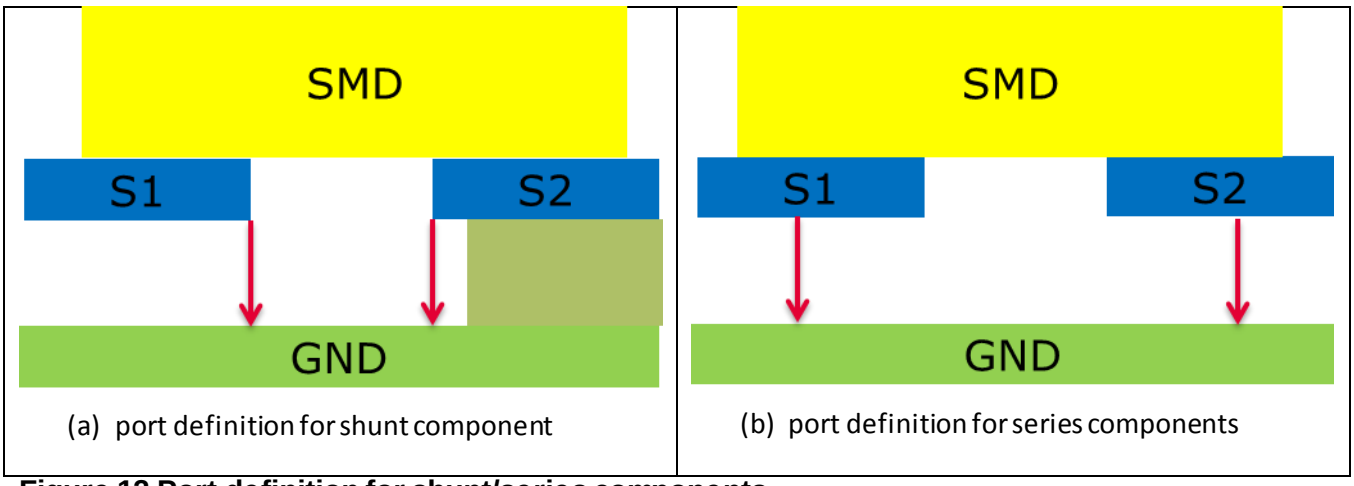


Figure 12 Port definition for shunt/series components

The layout for the landing pad supports both options of pin placement. For the shunt configuration manual placement at the center of the pad gap is required. Figure 13 (a) depicts and according example, the Layout_Portx_Ref_plane should be set to Pad inside edge (:3) For the series port definition the Layout_Portx_Ref_plane option Pad center (:0) shall be used to define the location for the port. Please refer to Figure 13 (b) for an according example.

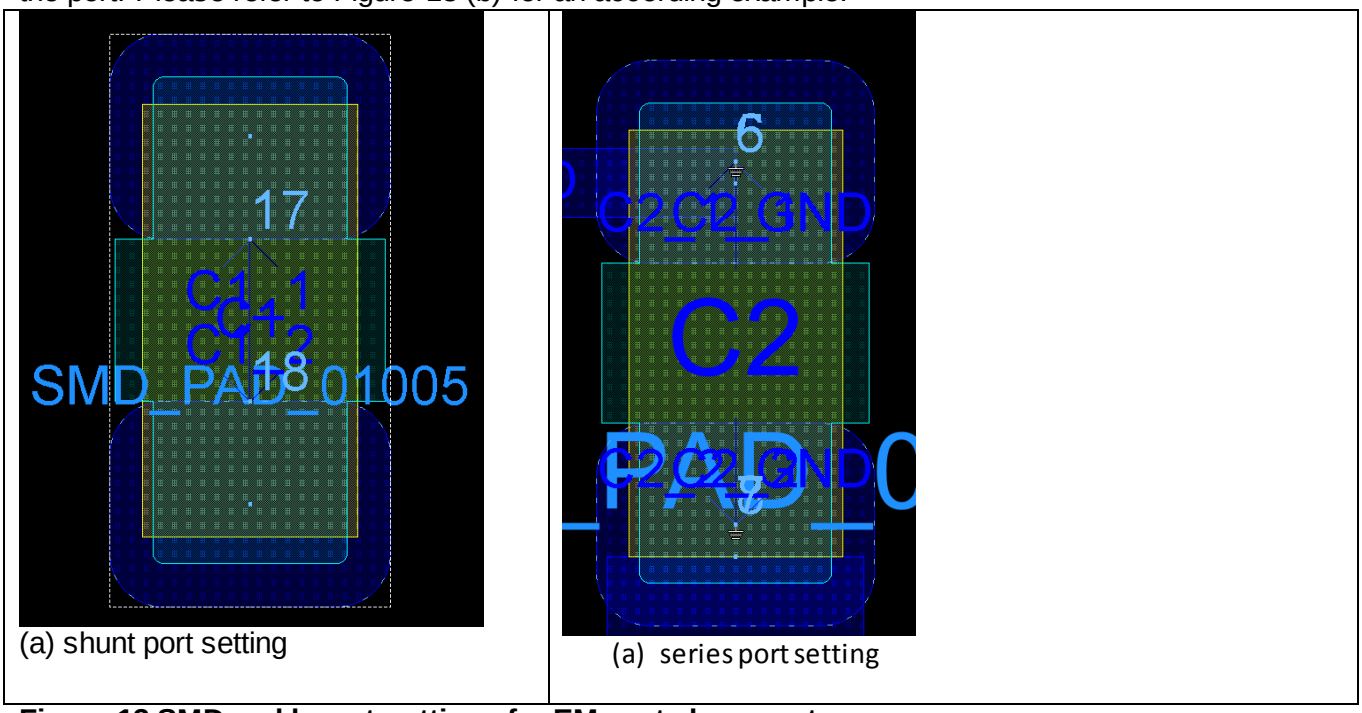
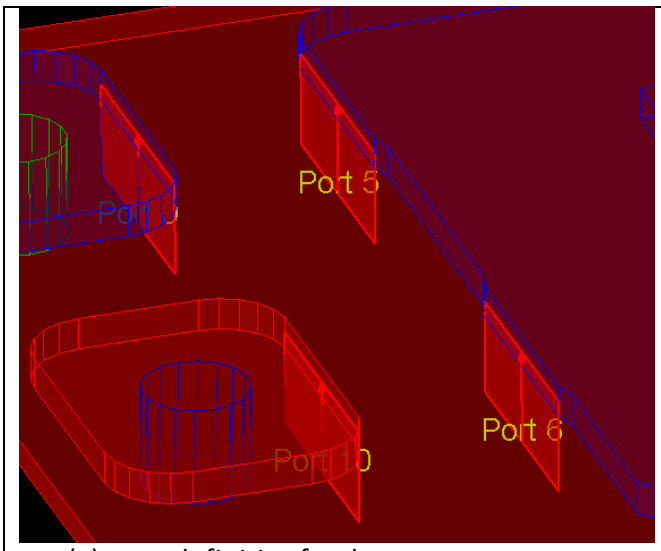
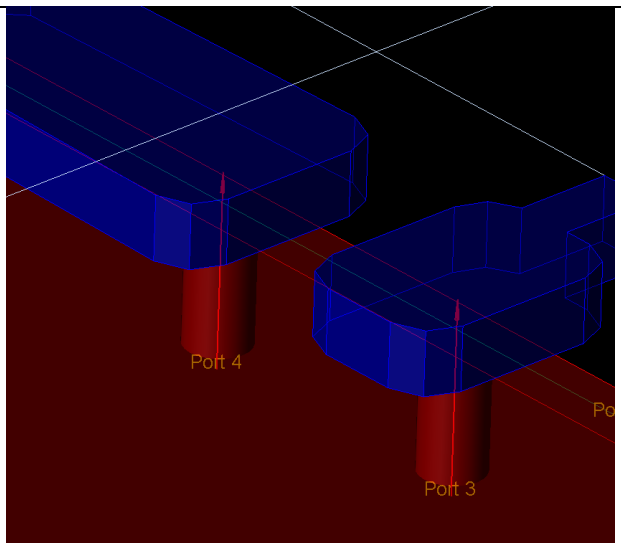


Figure 13 SMD pad layout settings for EM port placement

Figure 14 depicts an example of how the EM-preview should look like for both SMD configurations (shunt and series).



(a) port definition for shunt component



(b) port definition for series components

Figure 14 Example EM preview

For some ports it might be required to add a (poly) line to restrict the width of the port if it is not implicitly defined by the layout itself. Figure 15 shows such an example. In order to define the port width a poly line of the desired with needs to be added and then assigned to the port via: Edit→ Edge/Area Pin, which will open the dialog shown in Figure 15. By assigning the correct pin the port width will be restricted. This will result in well-defined ports, without this restriction the ports would overlap and influence eventually the behavior of the connecting transmission line.

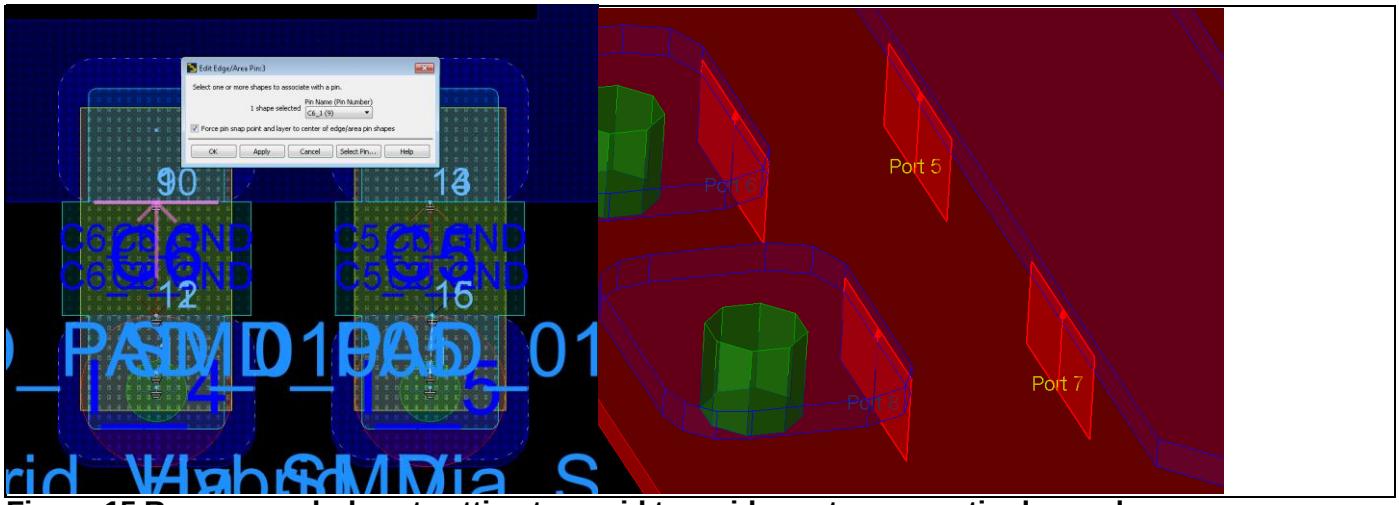
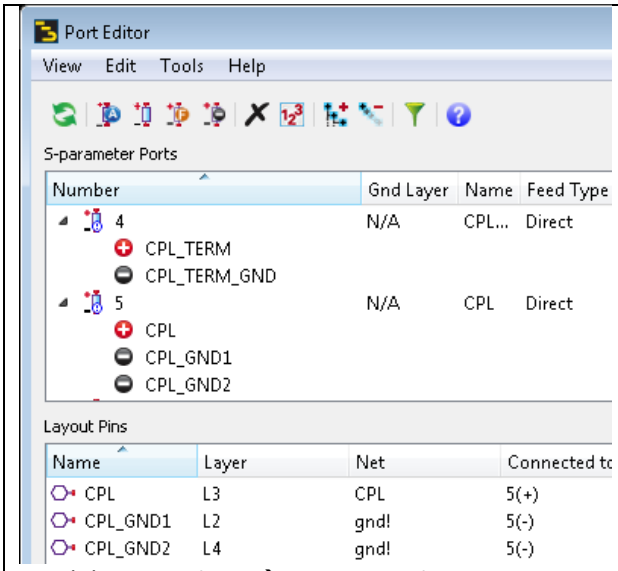
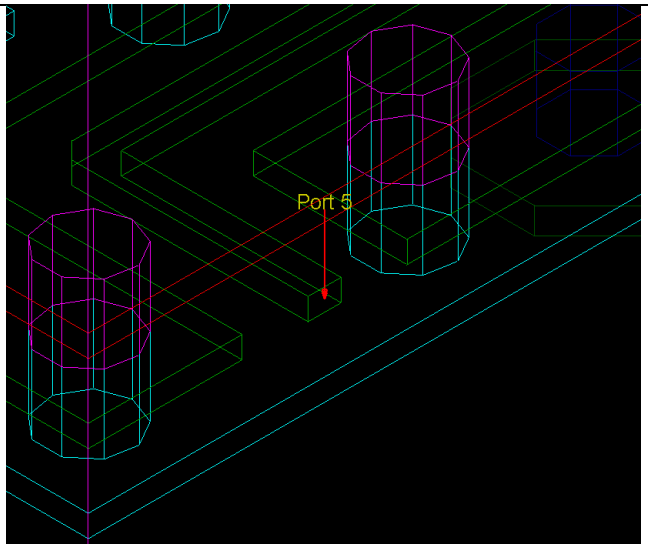


Figure 15 Recommended port setting to avoid too wide ports, respectively overlap

For the case that structure on lower layers (eg. L3) with two ground planes (stripline design) need to be simulated this needs to be accounted for in the port setting by assigning two ground pins to the port to ensure that the structure is excited in the correct way. Figure 16 depicts such an example for the recommended port setup for a structure placed on L3. Also other special cases (such as the GND pin is on the same layer as the port) need this specific gnd pin assignment for the RF port.



(a) port editor → two ground pins are assigned to port CPL



(b) according EM preview

Figure 16 Example L3 Port setting (for port CPL)

- GND pins are not synchronized to schematic

Currently the guideline is not to synchronize the GND pins to the schematic. This is to avoid that the symbol will become too large since all the GND ports would also need to be grounded. Adding the ground ports to the schematic would just deliver another error for the layout differences since the ground ports are assigned to the net "gnd!".

Refer to Figure 17 for an example.

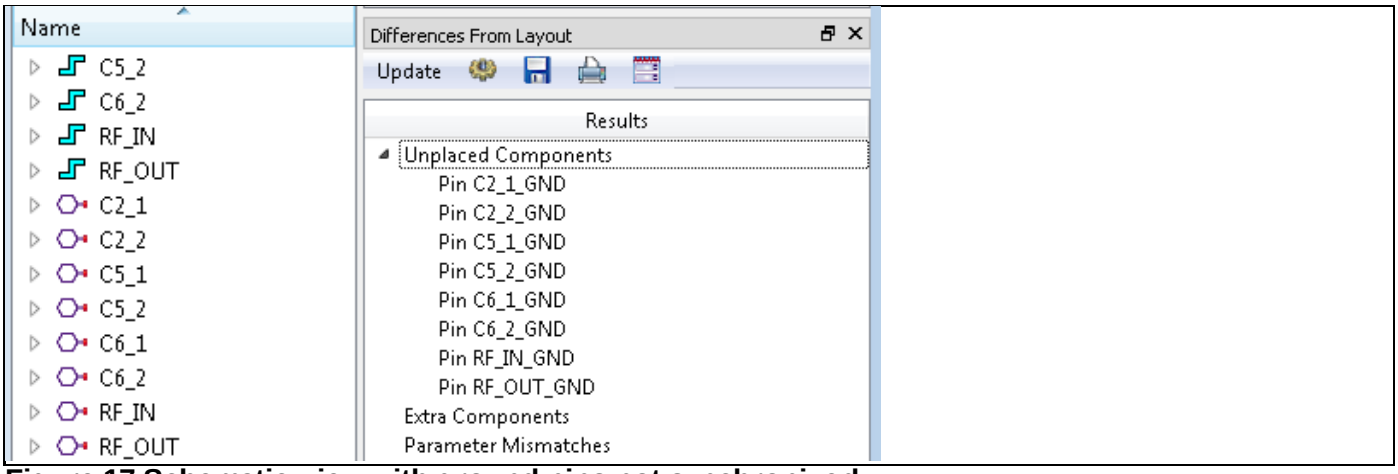


Figure 17 Schematic view with ground pins not synchronized

- Symbols must use the schematic/layout signal pin numbering → do not create symbol based on EM settings with one port → will use the port numbers → causes problem with connectivity

In order to enable the correct connectivity (layout vs. schematic) and support the switching between the EM model and the schematic model the rule above must be kept. Figure 18 depicts such an example.

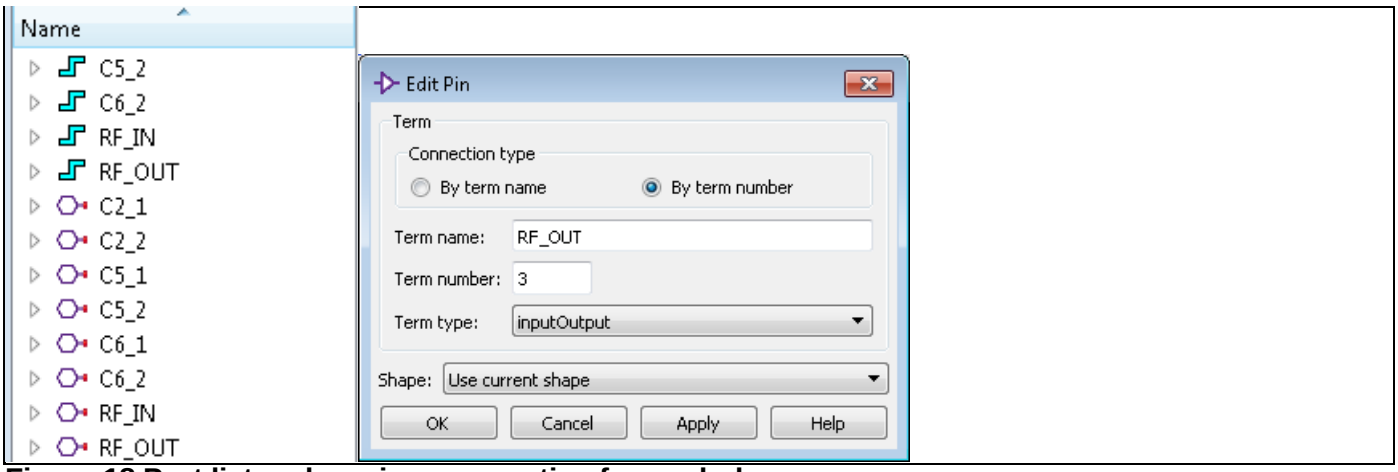


Figure 18 Port list and naming convention for symbol

For the emModel the frequency plan must include DC, the low band, mid band and high band frequency, as well as the according harmonics (up to the 3rd) as explicit frequency points to ensure that this frequencies are simulated. In between an adaptive frequency sweep can be used. The frequency plan shall also include frequencies up to the 7th harmonic (dependent on the harmonic balance setting) to avoid getting active S-parameters due to extrapolation

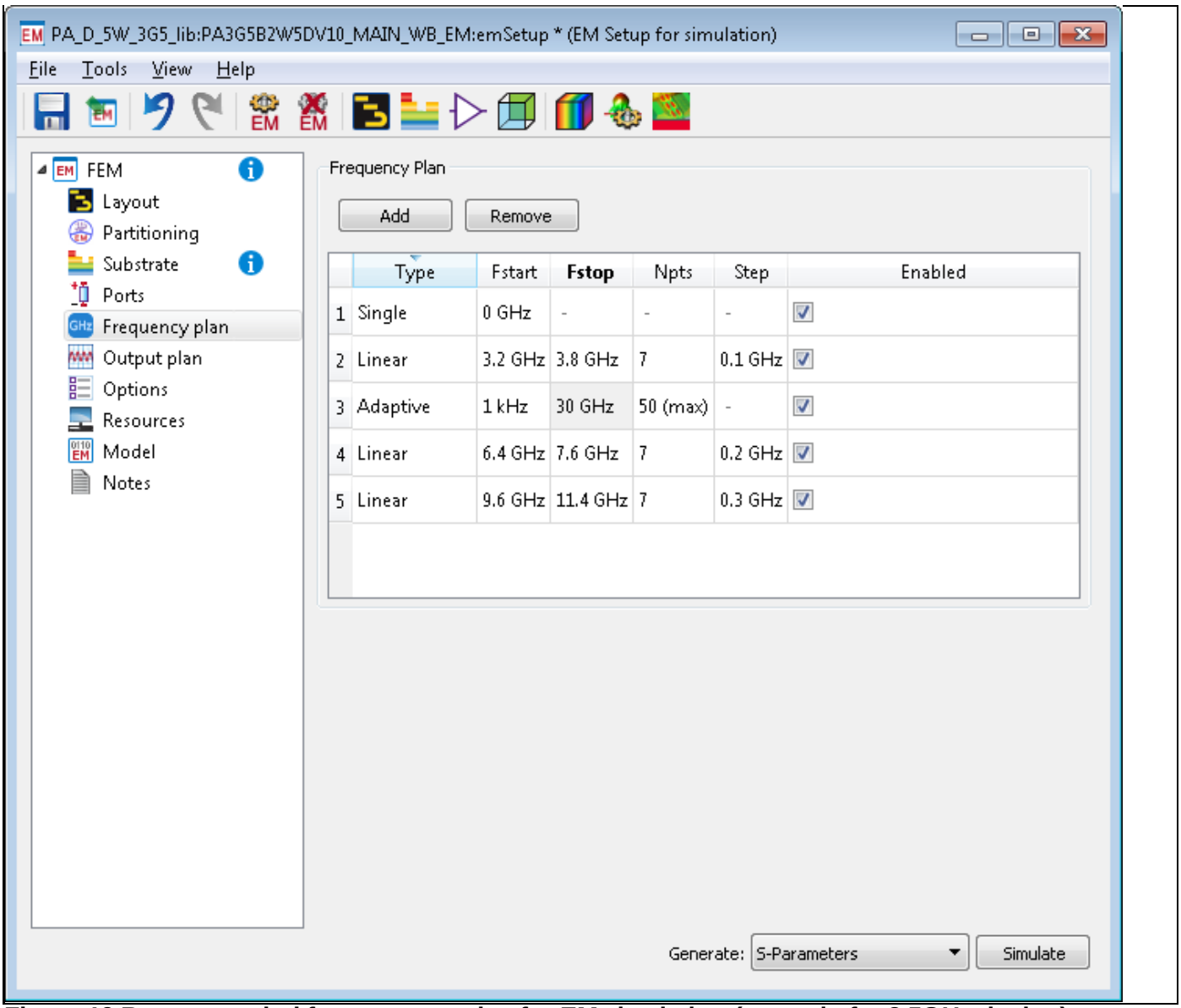


Figure 19 Recommended frequency setting for EM simulation (example for 3.5GHz design)

The selection of the correct substrate is important for the correct simulation results. For the designs in the design library (and planned for all subsequent designs) the substrates are based directly in the library. Thus an appropriate substrate out of the same library as the design needs to be selected. An according example is shown in Figure 20.

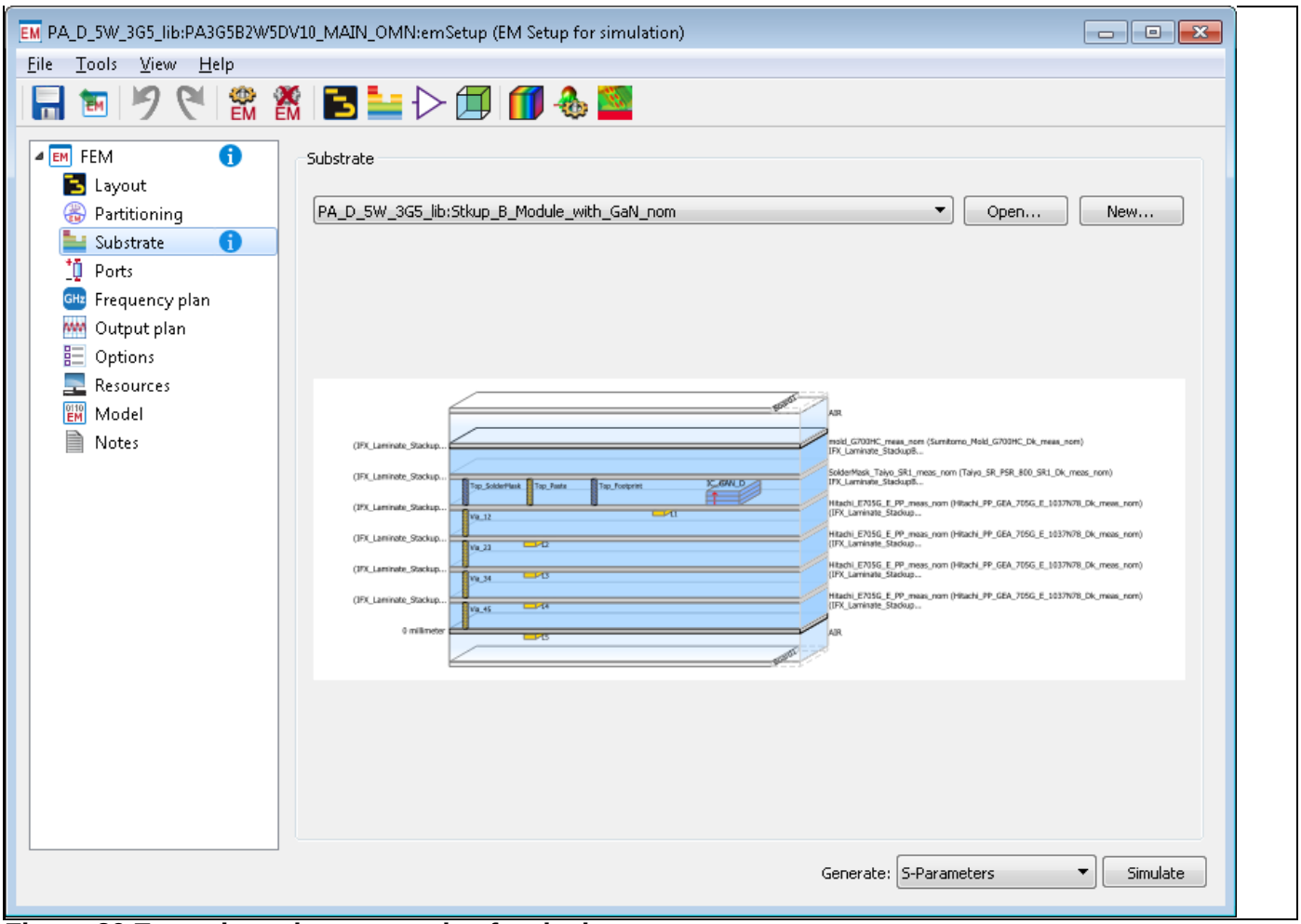


Figure 20 Example substrate setting for designs

5.2.2 Advanced Methodology

In the Advanced Methodology a method is described in which an EM model with the proper port settings (location/gnd return path) is automatically generated based on the SMD component instance settings defined in the layout view. Therefore the setup Type and EM Simulator settings needs to be selected as shown in Figure 21.

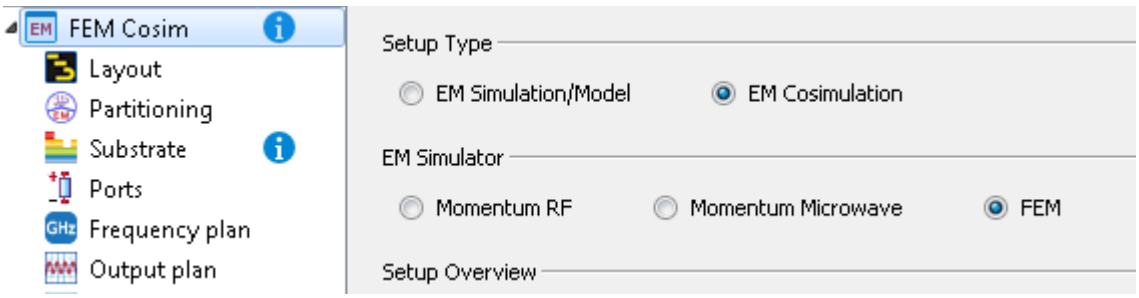


Figure 21 Advanced EM setup configuration

The Methodology will be explained by an example design for a lumped element hybrid.

For the schematic design, components defined in the IFX SMT library have been used as well as elements for the multilayer interconnect pre-defined in ADS.

Figure 22 depicts a subsection of the circuit in which dynamic model selection has been used to choose different models for certain circuit elements.

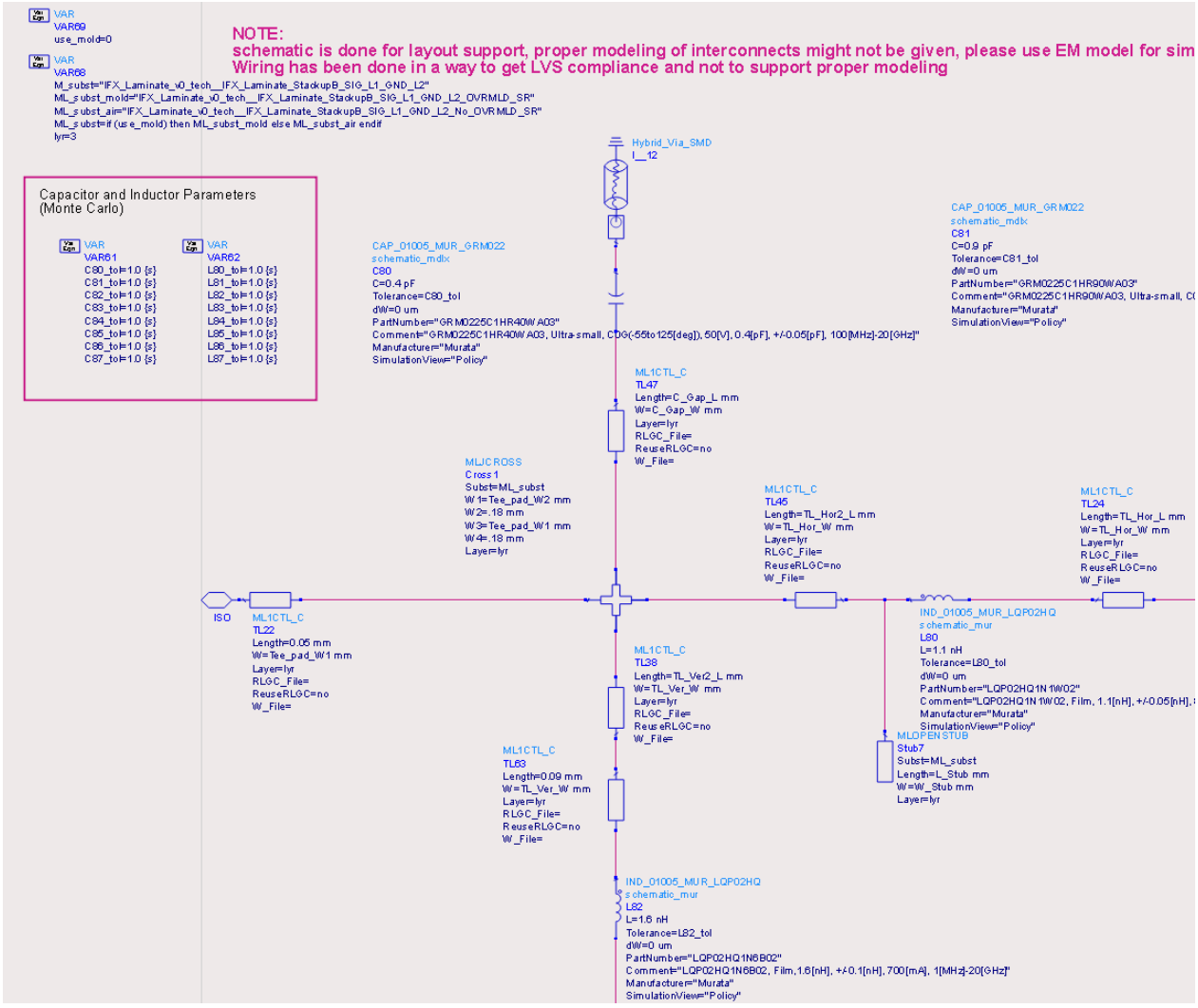


Figure 22 schematic for lumped element hybrid (subsection of the complete circuit)

Essential for this methodology is that the layout view and schematic view are synchronized (see Figure 23).

The Design Differences window (docking window) enables you to manage components between ADS Schematic and Layout. You can select a design and quickly identify differences between the schematic and layout in your design. Upon identifying these differences, the window includes an action-oriented list which enables you to manage:

- Unplaced components
- Extra components
- Parameter mismatches
- Nodal mismatches
- Net name mismatches
- Incomplete Net connections
- Overlapping Nets

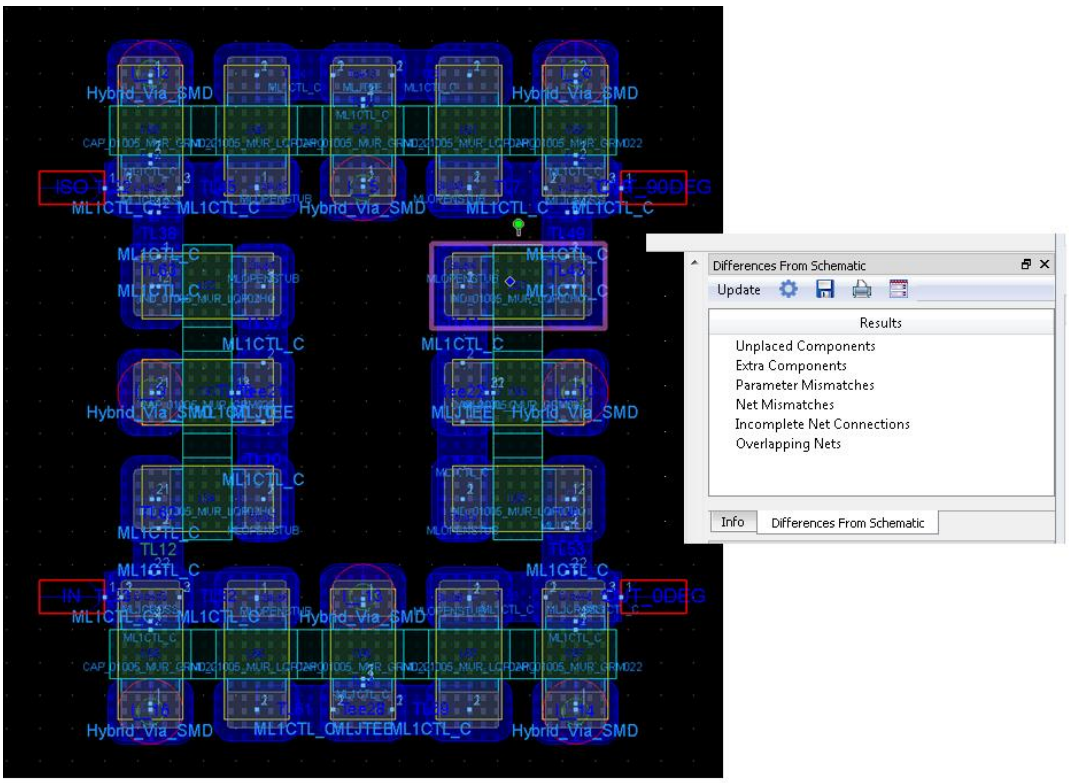


Figure 23 layout view for the lumped element hybrid showing no differences from schematic – Design Difference window

Since the EM/circuit Partitioning and the hierarchical netlisting for circuit simulation is derived from the layout view, any changes in the circuit view like parameters etc. must be synchronized with the layout view.

5.2.2.1 EM/circuit Partitioning

The Partitioning tab of an EM Setup controls whether individual instances are EM simulated or circuit simulated. For proper partitioning for all SMD components the “emCosim” partitioning rule need to be selected as shown in Figure 24. Please make sure that you refresh the list to get an updated view on the elements which will generate EM ports in the EM model. Depending on the instance settings given in Table 7 one can define the EM port location and GND reference layer. A 3D view shown in Figure 25 after the generation of the model shows the user selected EM/circuit Partitioning and Port configuration. Other EM setup parameters like substrate/Frequency plan etc. needs to be provided similar to the generation of a standard EM model described in 5.2.1. If the layout isn’t parameterized the user needs to select the “layout” mode of operation in the Cosimulation tab of the EM setup and provide a view name as depicted in Figure 26. Afterwards by pressing the go button the corresponding new cell “x_emCosim_FEM” is generated and can be inspected.

Instance parameter	Description
EM_Port1_Ref_plane	EM Port 1 reference plane (EMCosim only) (Drop-down) Reference plane set to Pad center (:0) Reference plane set to Pad edge (:1) Reference plane set to Component body edge (:2) Reference plane set to Pad inside edge (:3)

Instance parameter	Description
EM_Port1_GND_reference	EM Port 1 GND reference (EMCosim only) Defines GND return path for EM port (Drop-down) Available layers (need to be mapped in the EM stackup definition) Default-“Implicit”- GND return reference is the closest gnd plane defined in the EM Stackup
EM_Port2_Ref_plane	EM Port 2 reference plane (EMCosim only) (Drop-down) Reference plane set to Pad center (:0) Reference plane set to Pad edge (:1) Reference plane set to Component body edge (:2) Reference plane set to Pad inside edge (:3)
EM_Port2_GND_reference	EM Port 2 GND reference (EMCosim only) Defines GND return path for EM port (Drop-down) Available layers (need to be mapped in the EM stackup definition) Default-“Implicit”- GND return reference is the closest gnd plane defined in the EM Stackup
EM_simplifcation	EM simplification (EM only) (Drop-down) ON: simplified layout artwork used in EM sims OFF: full detailed layout artwork used in EM sims

Table 7 IFX SMT instance parameter used for EM port generation

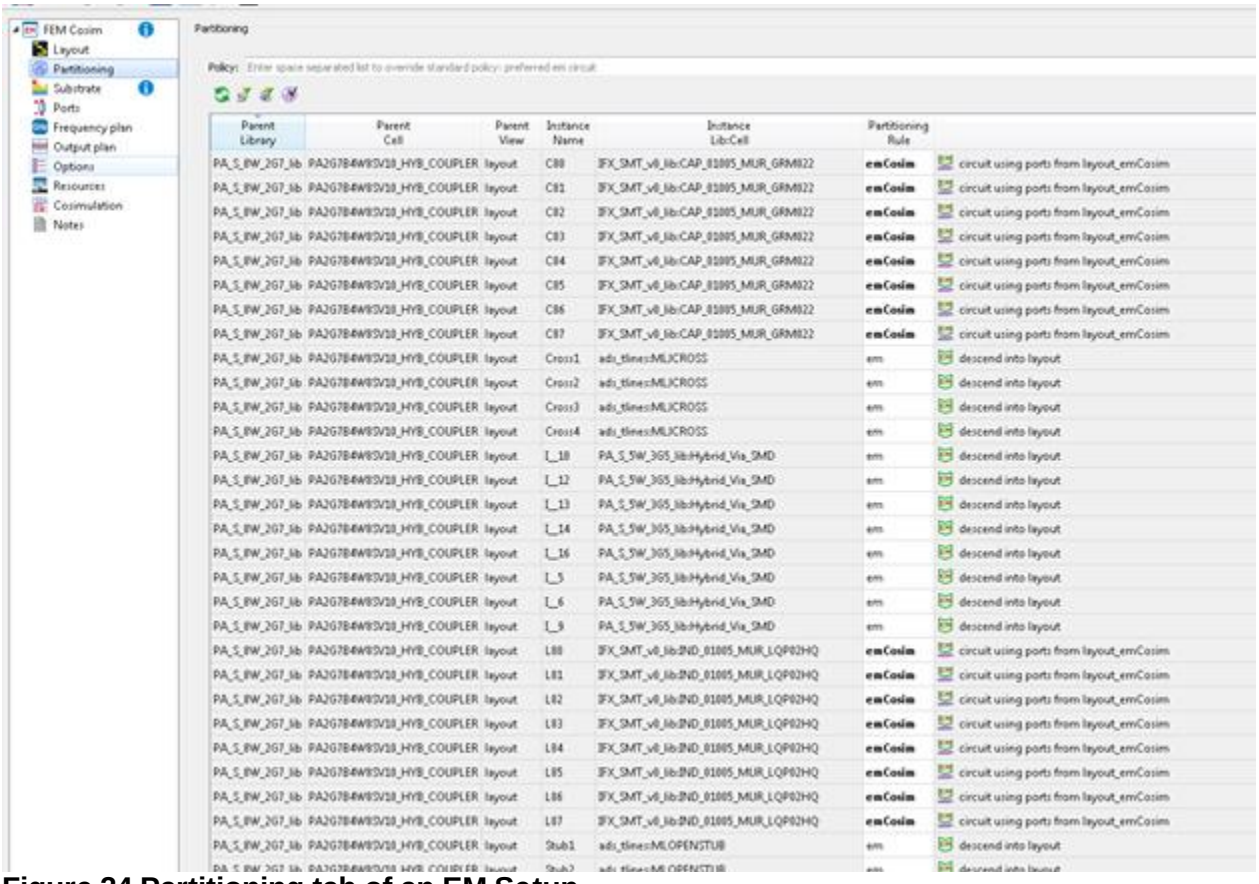


Figure 24 Partitioning tab of an EM Setup

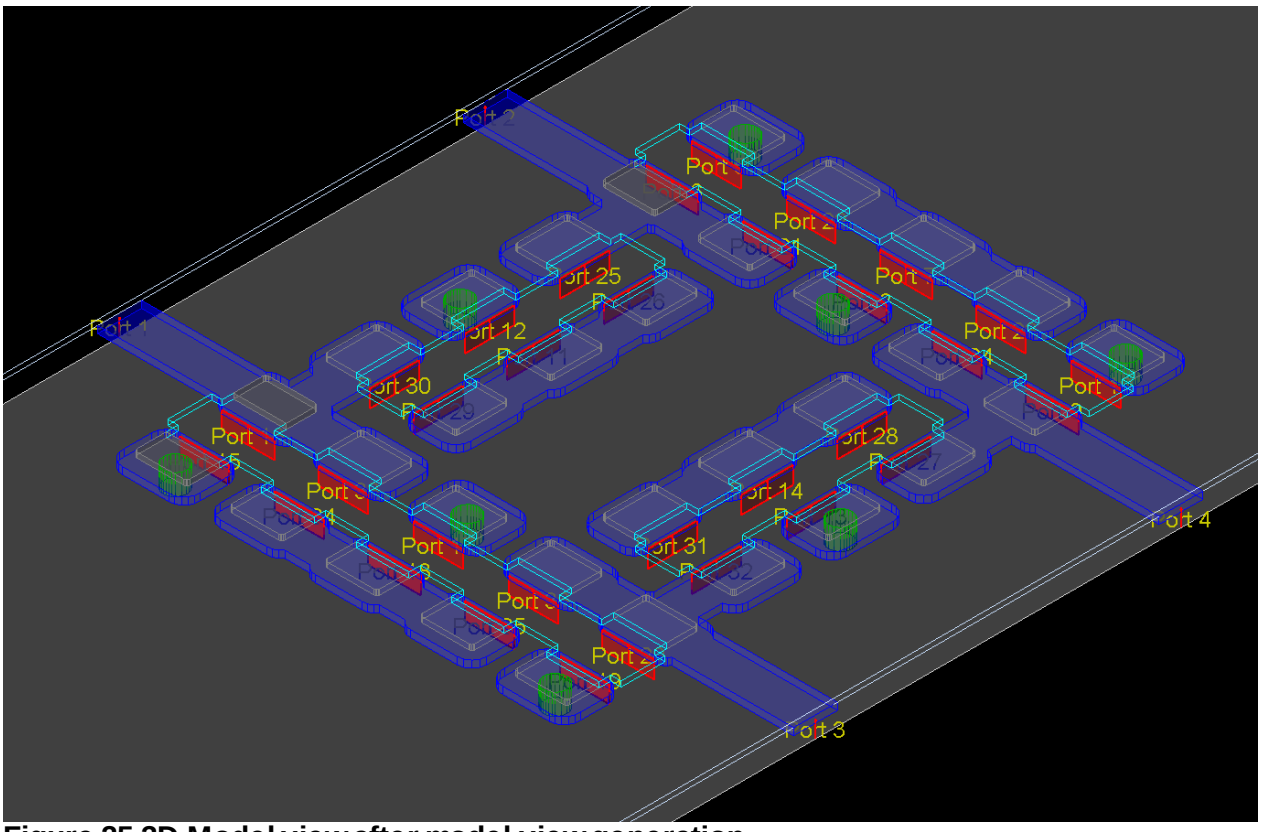


Figure 25 3D Model view after model view generation

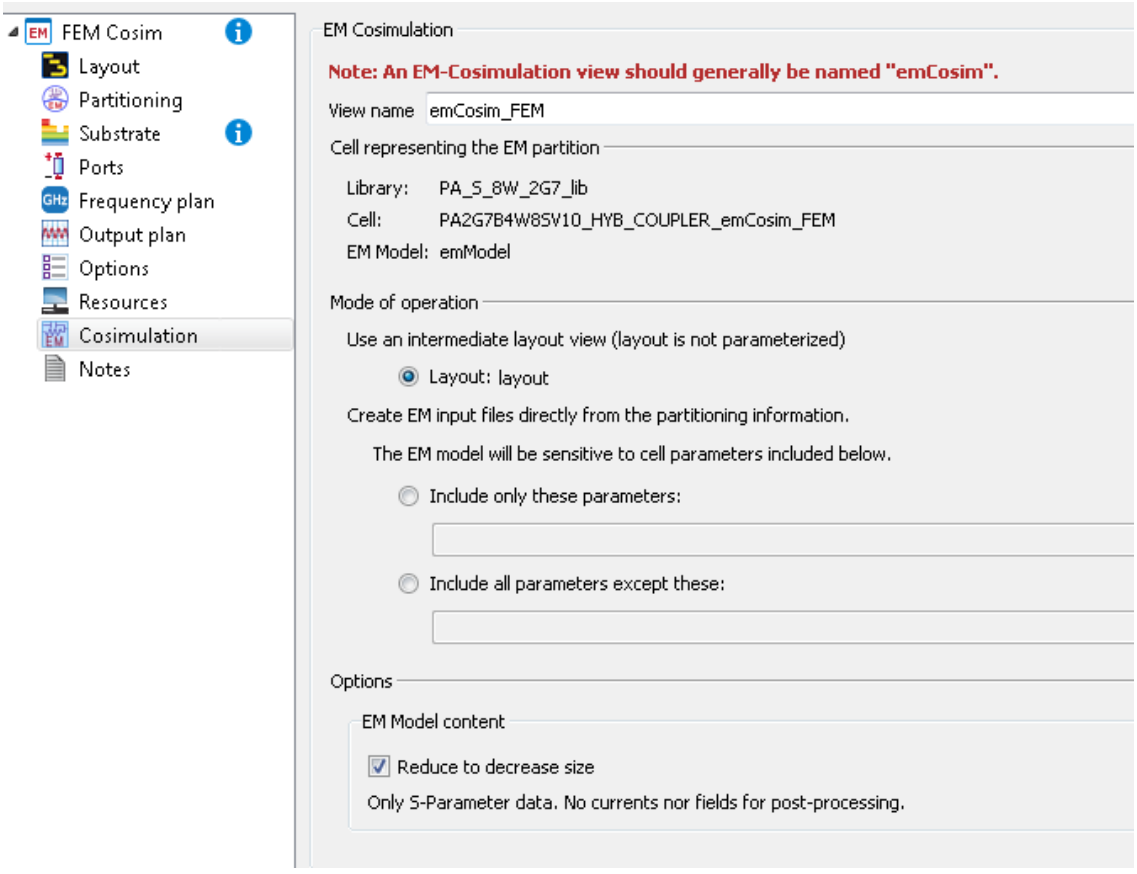
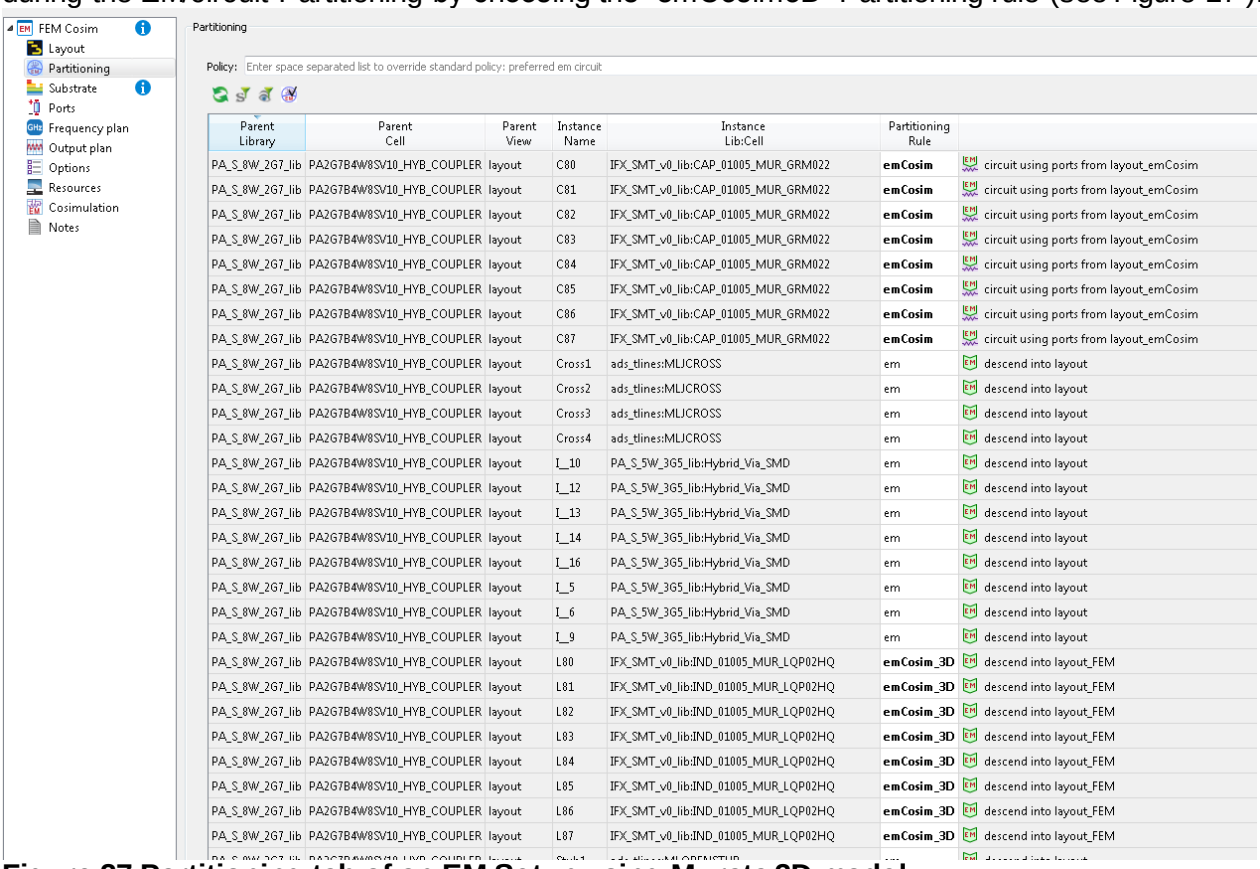


Figure 26 Cosimulation Mode of Operation

For murata inductor SMD components a complete 3D EM model is available, which can be selected during the EM/circuit Partitioning by choosing the “emCosim3D” Partitioning rule (see Figure 27).



Parent Library	Parent Cell	Parent View	Instance Name	Instance Lib:Cell	Partitioning Rule	
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	C80	IFX_SMT_v0_lib:CAP_01005_MUR_GRM022	emCosim	circuit using ports from layout_emCosim
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	C81	IFX_SMT_v0_lib:CAP_01005_MUR_GRM022	emCosim	circuit using ports from layout_emCosim
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	C82	IFX_SMT_v0_lib:CAP_01005_MUR_GRM022	emCosim	circuit using ports from layout_emCosim
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	C83	IFX_SMT_v0_lib:CAP_01005_MUR_GRM022	emCosim	circuit using ports from layout_emCosim
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	C84	IFX_SMT_v0_lib:CAP_01005_MUR_GRM022	emCosim	circuit using ports from layout_emCosim
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	C85	IFX_SMT_v0_lib:CAP_01005_MUR_GRM022	emCosim	circuit using ports from layout_emCosim
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	C86	IFX_SMT_v0_lib:CAP_01005_MUR_GRM022	emCosim	circuit using ports from layout_emCosim
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	C87	IFX_SMT_v0_lib:CAP_01005_MUR_GRM022	emCosim	circuit using ports from layout_emCosim
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	Cross1	ads_tlines:MLICROSS	em	descend into layout
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	Cross2	ads_tlines:MLICROSS	em	descend into layout
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	Cross3	ads_tlines:MLICROSS	em	descend into layout
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	Cross4	ads_tlines:MLICROSS	em	descend into layout
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	I__10	PA_S_5W_3G5_lib:Hybrid_Via_SMD	em	descend into layout
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	I__12	PA_S_5W_3G5_lib:Hybrid_Via_SMD	em	descend into layout
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	I__13	PA_S_5W_3G5_lib:Hybrid_Via_SMD	em	descend into layout
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	I__14	PA_S_5W_3G5_lib:Hybrid_Via_SMD	em	descend into layout
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	I__16	PA_S_5W_3G5_lib:Hybrid_Via_SMD	em	descend into layout
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	I__5	PA_S_5W_3G5_lib:Hybrid_Via_SMD	em	descend into layout
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	I__6	PA_S_5W_3G5_lib:Hybrid_Via_SMD	em	descend into layout
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	I__9	PA_S_5W_3G5_lib:Hybrid_Via_SMD	em	descend into layout
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	L80	IFX_SMT_v0_lib:IND_01005_MUR_LQP02HQ	emCosim_3D	descend into layout_FEM
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	L81	IFX_SMT_v0_lib:IND_01005_MUR_LQP02HQ	emCosim_3D	descend into layout_FEM
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	L82	IFX_SMT_v0_lib:IND_01005_MUR_LQP02HQ	emCosim_3D	descend into layout_FEM
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	L83	IFX_SMT_v0_lib:IND_01005_MUR_LQP02HQ	emCosim_3D	descend into layout_FEM
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	L84	IFX_SMT_v0_lib:IND_01005_MUR_LQP02HQ	emCosim_3D	descend into layout_FEM
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	L85	IFX_SMT_v0_lib:IND_01005_MUR_LQP02HQ	emCosim_3D	descend into layout_FEM
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	L86	IFX_SMT_v0_lib:IND_01005_MUR_LQP02HQ	emCosim_3D	descend into layout_FEM
PA_S_8W_2G7_lib	PA2G7B4W8SV10_HYB_COUPLER	layout	L87	IFX_SMT_v0_lib:IND_01005_MUR_LQP02HQ	emCosim_3D	descend into layout_FEM

Figure 27 Partitioning tab of an EM Setup using Murata 3D model

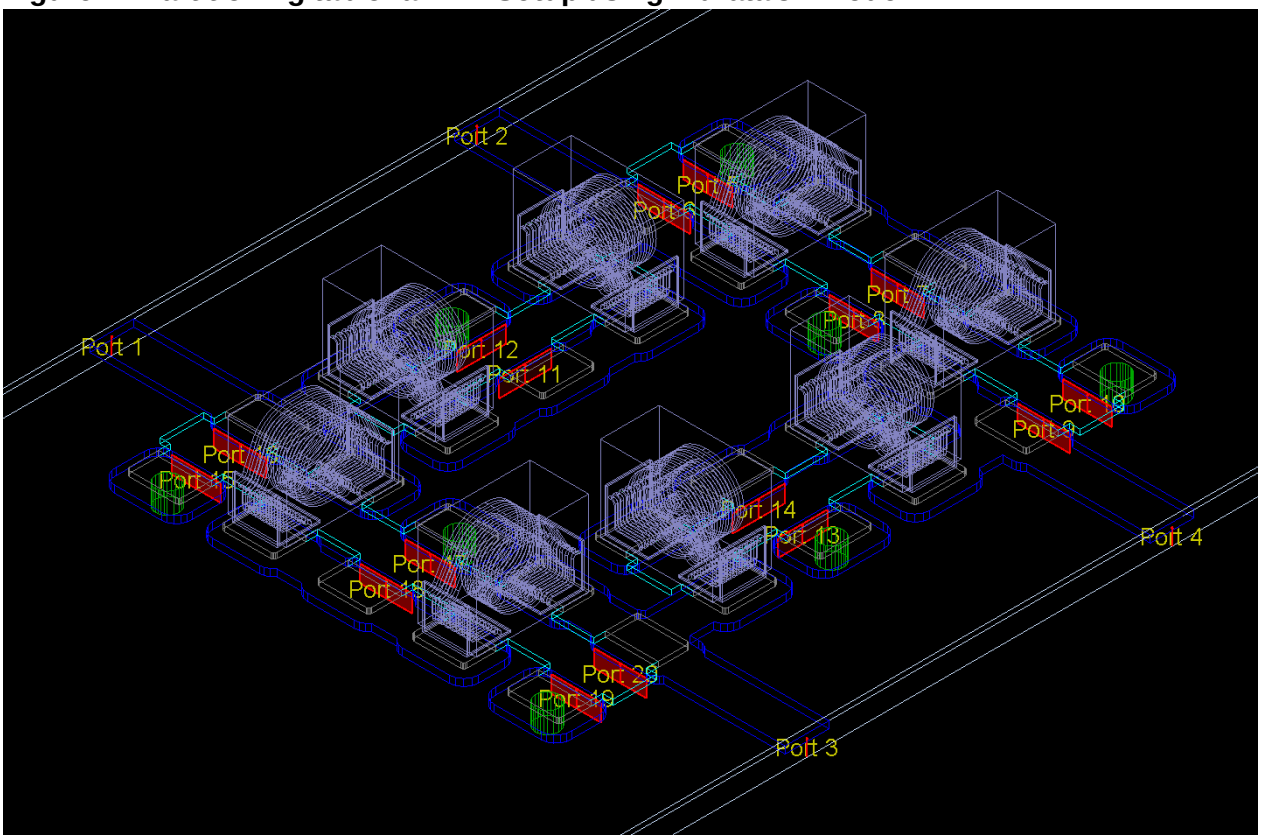


Figure 28 3D Model view after model view generation using Murata 3D inductor models

5.2.2.2 Using the EMCosim model in a circuit simulation

Standard method:

As described in 5.2.2.1 for generating a nonparametric EMCosim view only changes to the circuit elements instance parameters (e.g.: Component value) are allowed. Any changes to the layout require a new generation of the emCosim view. Since the hierarchical netlisting for the cosimulation is done through the layout view any component value change needs to be done in the layout view or forced by design synchronization from the schematic to the layout!
To choose the EMCosim view for simulation, the in the previous section generated model view needs to be selected in the schematic view of your test bench as shown in Figure 31.
To choose specialized instances for the circuit elements of the Cosimulation the “view for simulation” needs to be selected in the layout view and **not** in the schematic view as shown in Figure 31.

Additionally the proper Hierarchy policy needs to be selected in the simulation settings window for the simulation testbench schematic (Simulate→Simulation settings→Output Setup→Choose Hierachy Policy). Here you should select “standard_ic_em”. By using the Hierarchy policy editor “simulate→ Hierarchy editor” the selection for netlist generation can be verified. If you haven’t select the proper policy all SMD circuit elements will show the “layout” as selected for simulation view (see Figure 29), which will result in an error when you start the simulation. For correctly running a simulation either schematic_mur, schemactic_mdlx or a similar schematic model view needs to show up.

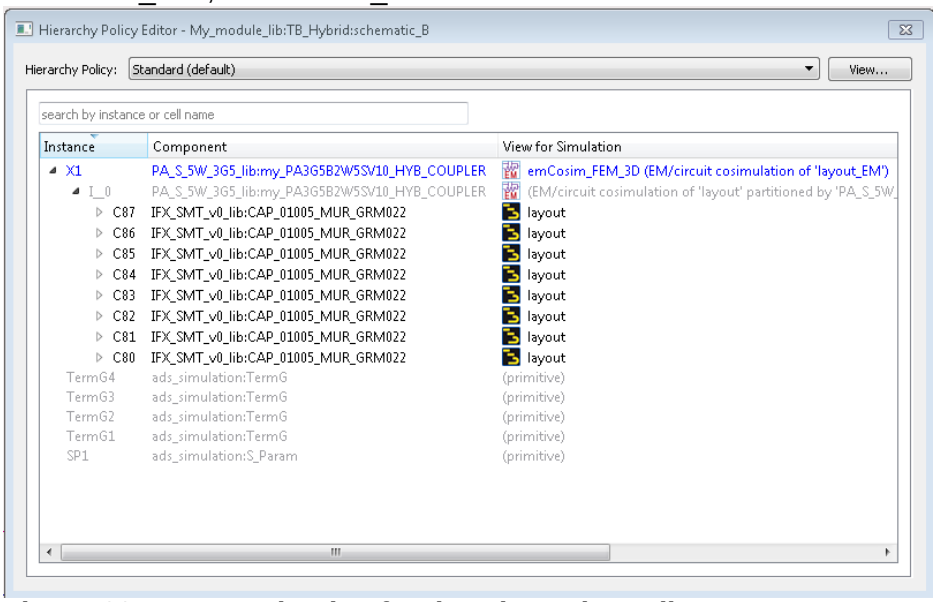


Figure 29 Wrong selection for the Hierarchy Policy

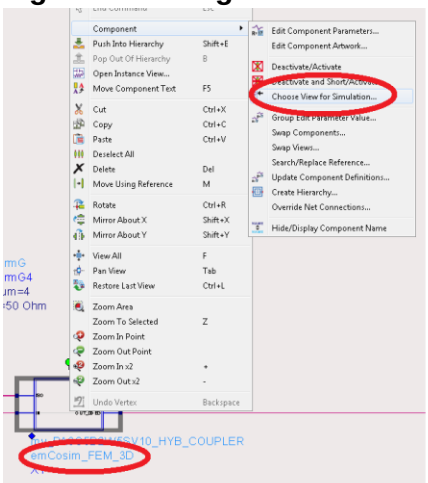


Figure 30 Choose emCosim view for simulation

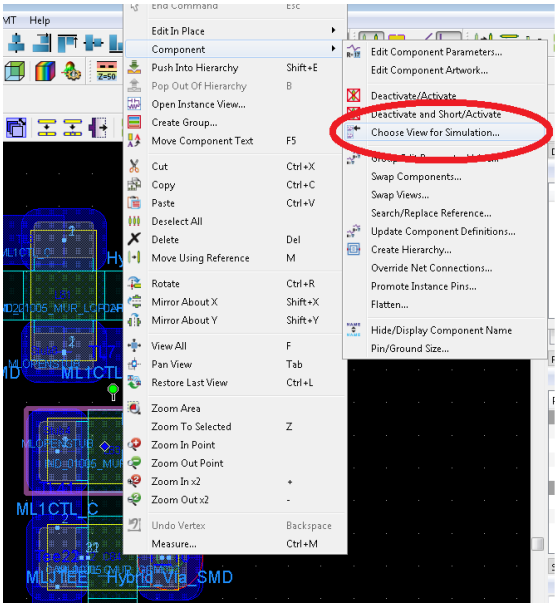


Figure 31 Choose instance view for simulation

Method Using a Config view

Another Dynamic Model Selection method how to determine which model of a cell is used during circuit simulation is to create a config view for your testbench cell.

Config view controls the expansion of design hierarchy for simulating or netlisting your designs. You can perform this by creating and editing rules that define a design configuration.

A config view includes a top cell view that it points to. All other information regarding Switch Views and Stop Views is then created based on the top cell view that is being pointed to. It also provides a way for you to set the view bindings for cell, instances, and occurrence at any level of the hierarchy **without** modifying the design.

This is a clear advantage compared to the standard method manually changing the simulation view for each instances within the design hierarchy, which requires modifying the design. In a data management system for a multiuser environment this modification will be present for each user which makes it difficult to use all the capabilities provided from polymorphism.

Details how to create and configure a config view can be found in the ADS documentation.

An example using instance bindings in a config view is shown in Figure 32.

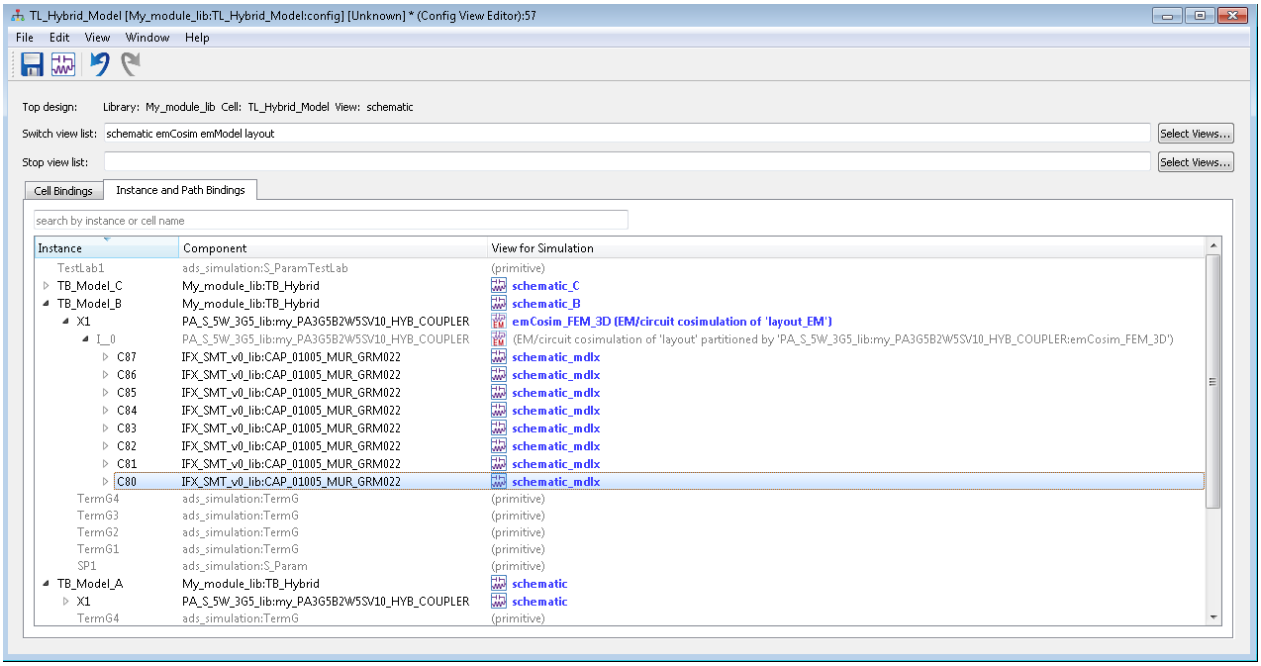


Figure 32 Example: Config view editor

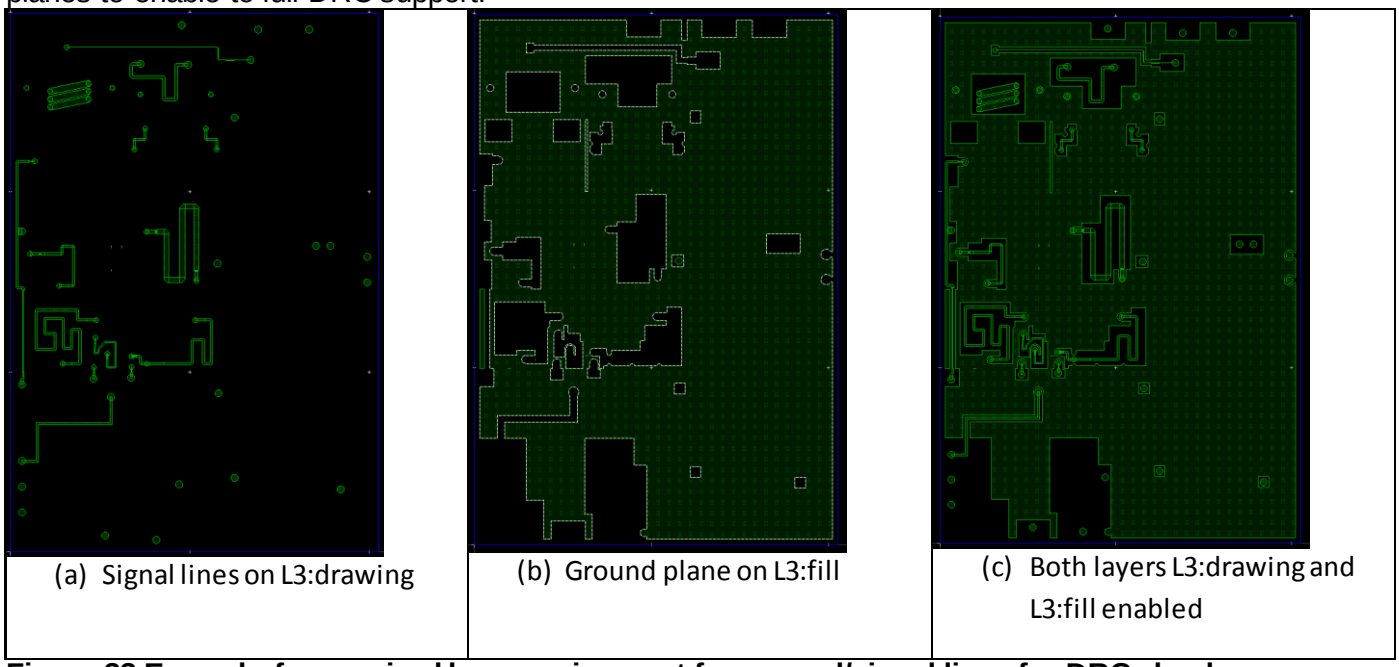
6 Module Design Rules

This chapter is split into two main sections. The first will briefly describe how to use the DRC and the most important rules (but not all of them). The second section will cover all additional rules that are not covered by the DRC and that need to be checked manually.

6.1 DRC covered rules

6.1.1 DRC requirements

All ground planes need to be drawn on layer fill in order to enable full DRC rule checking. Figure 33 depicts an example on how the layout needs to be done with respect to signal lines and ground planes to enable to full DRC support.



(a) Signal lines on L3:drawing

(b) Ground plane on L3:fill

(c) Both layers L3:drawing and L3:fill enabled

Figure 33 Example for required layer assignment for ground/signal lines for DRC checks

6.1.2 DRC rules

Refer to the DRC feedback for details on each error.

6.1.3 How to use DRC

The DRC can be run by selecting the layout to check Menu Tools→DRC or by clicking on the corresponding icon in the IFX laminate toolbar  .

Note that for running the DRC the layout needs to be checked out since the DRC writes on the layer ads_drc_error to highlight the errors and thus needs write access.

Then a window like in Figure 34 should pop up. Please select ADS as the DRC engine and make sure to enable the run in background option. It is important to select Library:IFX_Laminate_v0 for the Rule location and the High Volume Manufacturing (HVM) rule set for the rule folder. Afterwards select the option for the DRC check. For a complete check use drc_all_AMKOR_LGIT.ael. See Table 8 for detail rule selection options. Additionally you can specifically select a reduced rule set in the categories section. Please note that for read only access clients the selection from the main window does not

work automatically and the according *.atf files need to be selected manually from the folder (Browse button).

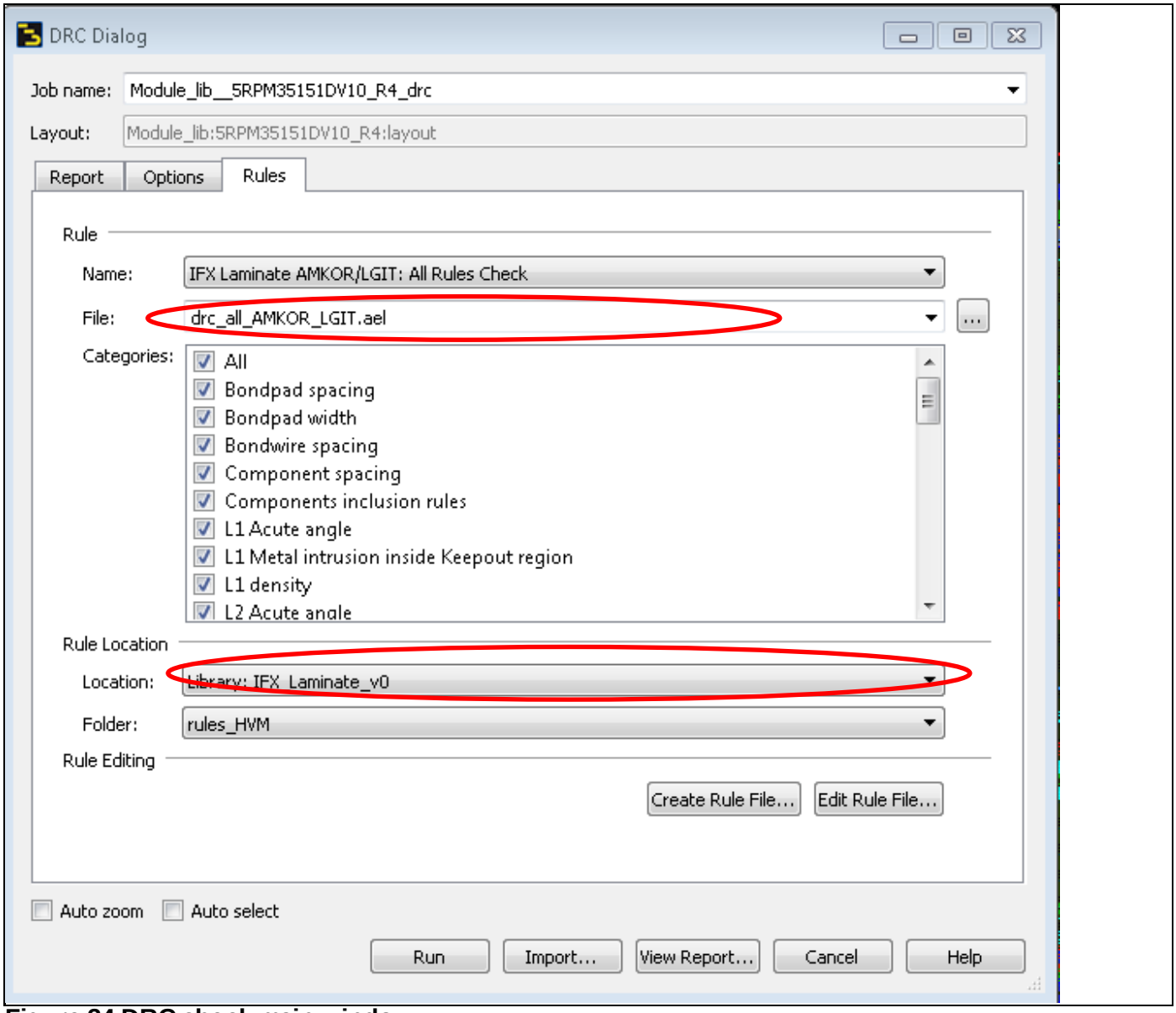


Figure 34 DRC check main window

Rule set	Description
drc_all_AMKOR_LGIT.atf (.ael)	Runs a complete DRC check
drc_width_AMKOR_LGIT.atf (.ael)	Runs width rule DRC checks only
drc_spacing_AMKOR_LGIT.atf (.ael)	Runs spacing rule DRC checks only
drc_inclusion_AMKOR_LGIT.atf (.ael)	Runs inclusion rule DRC checks only
drc_intrusion_AMKOR_LGIT.atf (.ael)	Runs intrusion rule DRC checks only
drc_density_AMKOR_LGIT.atf (.ael)	Runs metal density rule DRC checks only
drc_angles_AMKOR_LGIT.atf (.ael)	Runs trace angle rule DRC checks only
drc_calc_densities_AMKOR_LGIT.atf (.ael)	Calculates metal densities (**Expert use only!**). Not included in the complete DRC check.
drc_double_vias_AMKOR_LGIT.atf (.ael)	Check for double vias (**Expert use only!**). Not included in the complete DRC check.

Table 8 IFX Laminate PDK DRC rules

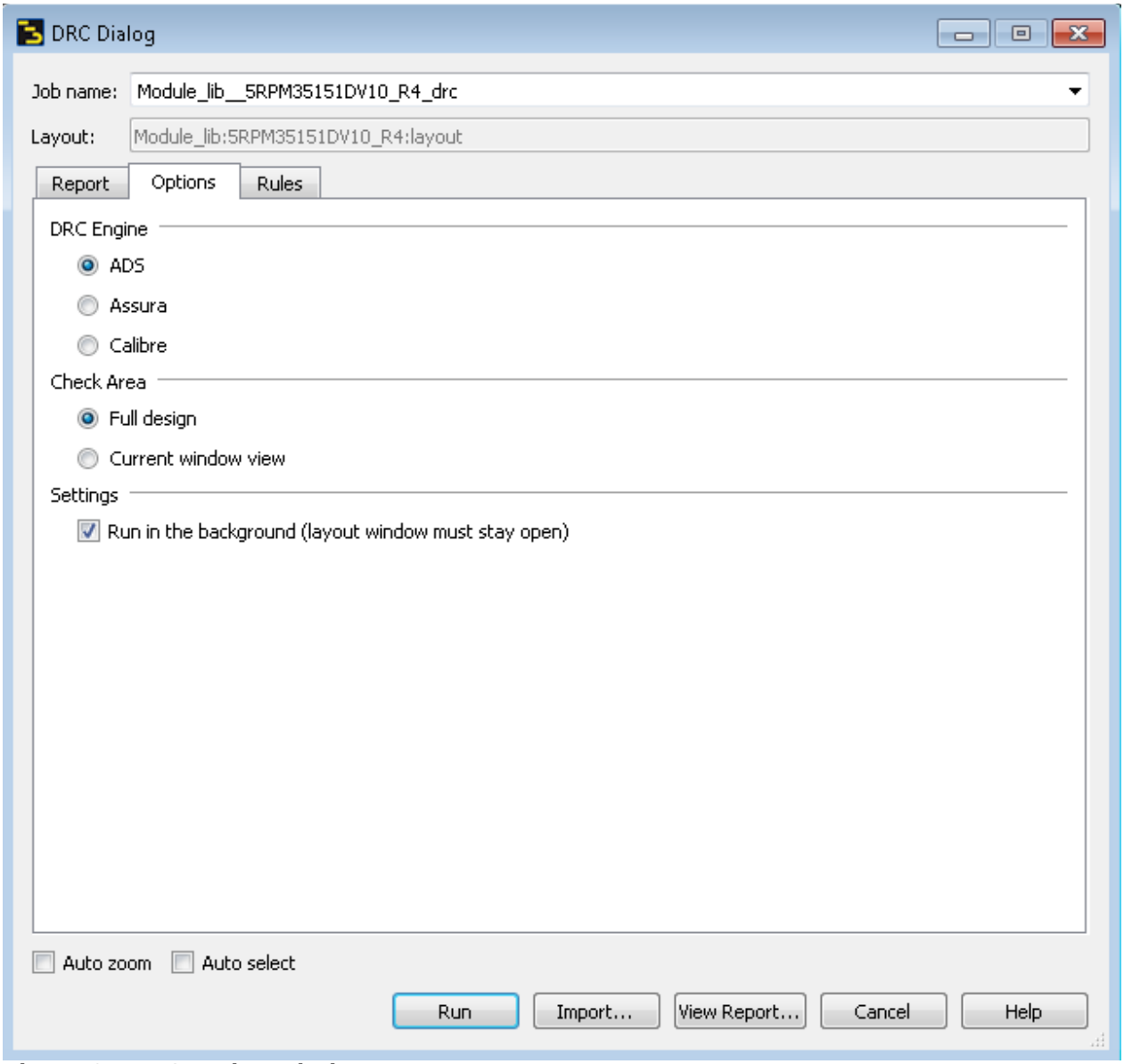


Figure 35 DRC option window

After the DRC has been run the results pane will show design rule violations which needs to be fixed or in case of false positves to be waived in alignment with the design lead or verification engineer. Errors can be waived by selecting the specific error or the whole group and pressing the right mouse button. Waived errors will show up below the “fixed” section.

The procedure outlined in Table 9 should be followed in general for each layout cell in the design hierarchy. Please use the “check tag” functionally to verify that subcells have been already marked as “drc_clean”. In alignment with the design lead or verification engineer a subset of the design hierarchy can be defined.

Step (sequence)	Description
1. 	Check the status of the design hierarchy: displays all cells for which the selected tag has been set. Check for “layout_done” and/or “drc_clean”
2. 	Check out layout view
3. 	Select rule set and run the DRC
4. 	Review DRC results. Fix DRC errors. Waive false positive DRC errors in alignment with the lead designer or verification engineer.
5. 	Check in “DRC clean” layout view
6. 	Add “layout_done” tag/label to the layout view
7. 	Upload/checkin DRC results.

Table 9 DRC check off procedure

6.2 Non DRC covered rules

6.2.1 Bonding rules

Die pads and bondpads are ENEPIG surface finish. This needs to be indicated using the layer bondpad at the according locations

	Description	Die size	Value
A	die to top metal (epoxy die attach)	<1.5mm	125um
		<3.0mm	150um
		>=3.0mm	225um
B	Copper to SM (SRR?)		50um
C	min SM width		125um
D	Bondpad to SM (SRR?)		55um
E	Die to bondpad	<1.5mm	355um
		<3.0mm	380um
		>=3.0mm	455um
F	Bondpad length		175um

ASE rule

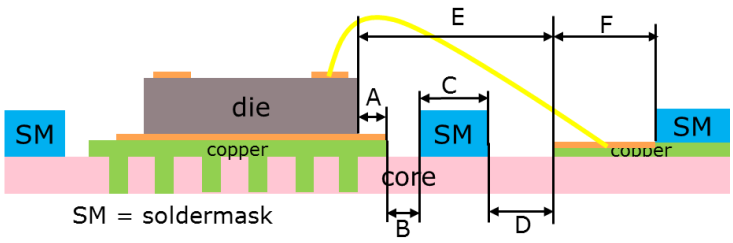


Figure 36 Die/Bonding Rules Non Soldermask defined (NSMD), preferred option

	Description	Die size	Value
A	die to SM (epoxy die attach)	<1.5mm	125um
		<3.0mm	150um
		>=3.0mm	225um
B	SM Overlap (SRR?)		50um
C	min SM width		125um
D	Bondpad to SM (SRR?)		55um
E	Die to bondpad	<1.5mm	305um
		1.5<x<2.54mm	330um
		2.54<x<3.0mm	355um
		3.0<x<10.16mm	405um
F	Bondpad length		175um

ASE rule

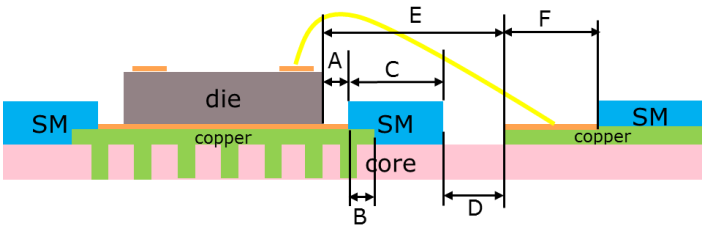


Figure 37 Die/Bonding Rules Soldermask defined (SMD)

	Description	value
DW	Bondpad design width	> 90um
DL	Bondpad design length	> 175um
DS	Bondpad design spacing	> 30um
R	Bondpad design angle	+-15°
SRRB	Soldermask registration bondpad	>40um

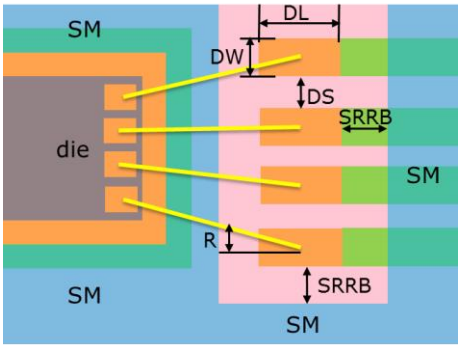


Figure 38 Bondpad/finger design rules (NSMD), preferred option

- Bondpad is not allowed to touch the via and also the according annular ring (AR) spacing around the via. An example that violates this design rule is depicted in Figure 39.

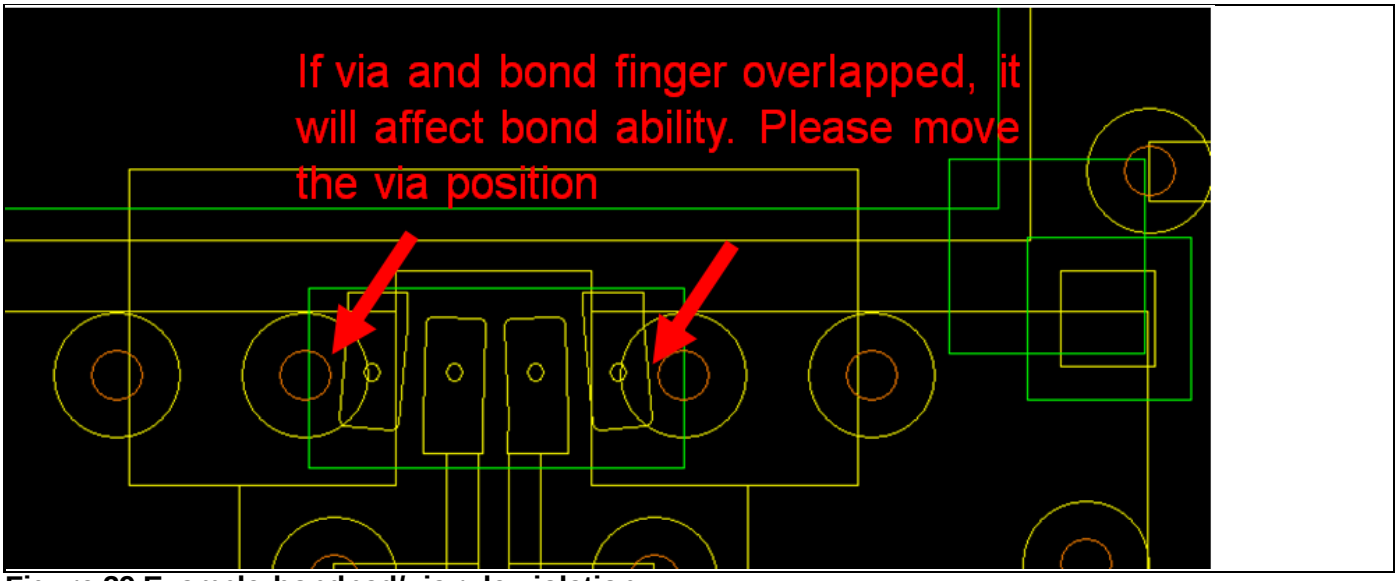
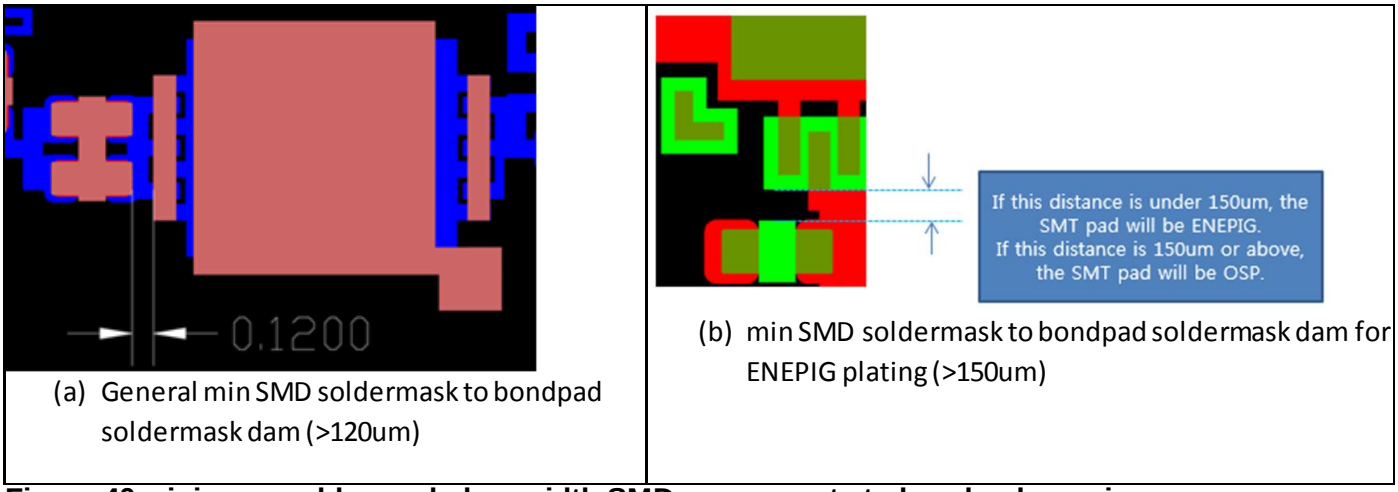


Figure 39 Example bondpad/via rule violation

- The minimum width of the soldermask dam for SMD components to bondpad soldermask opening is described in Figure 40. There are two rules applicable a general rule that defines the minimum spacing (>120um) in Figure 40(a) and a rule regarding the plating. If for manufacturing reasons (eg. reliability) no ENEPIG plating on the SMD pads is allowed the minimum distance increase to 150um, as depicted

in Figure 40(b). If condition (a) or (b) apply needs to be clarified and aligned with the DFM (Design for Manufacturing) responsible person.



(a) General min SMD soldermask to bondpad soldermask dam (>120um)

(b) min SMD soldermask to bondpad soldermask dam for ENEPIG plating (>150um)

Figure 40 minimum soldermask dam width SMD components to bondpad openings

6.2.2 Die to Die Clearance rules

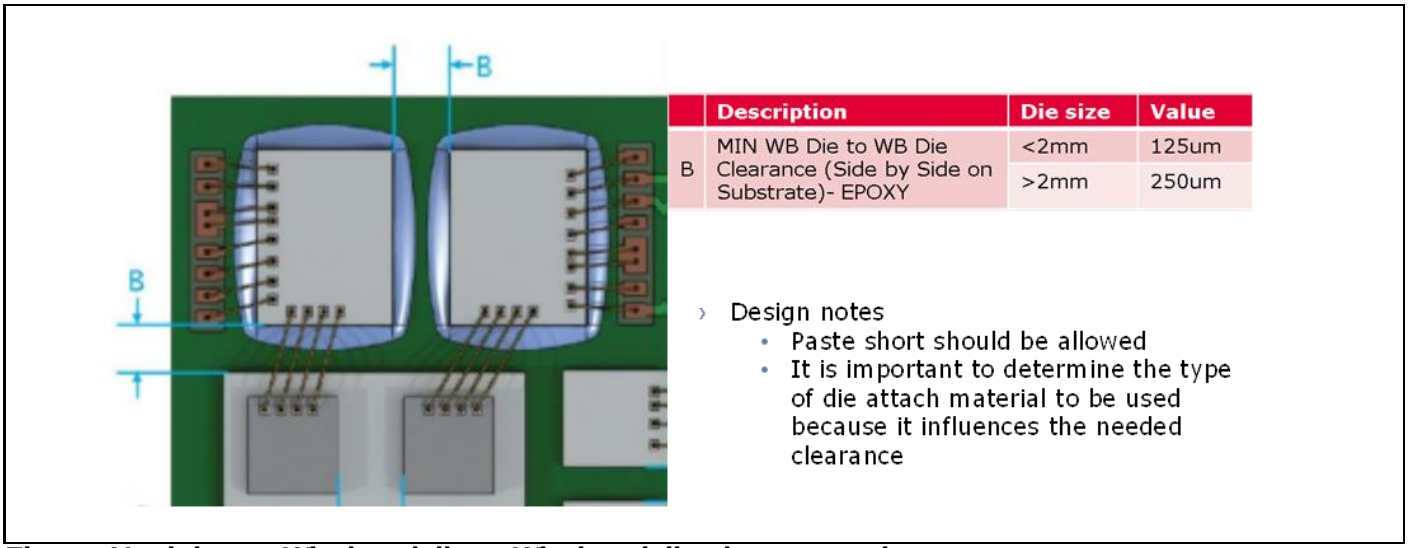


Figure 41 minimum Wirebond die to Wirebond die clearance rules

6.2.3 Other Design Rules

- All bar vias must be exactly 76um width. In Figure 42 an example of a bar via array for thermal cooling is depicted.

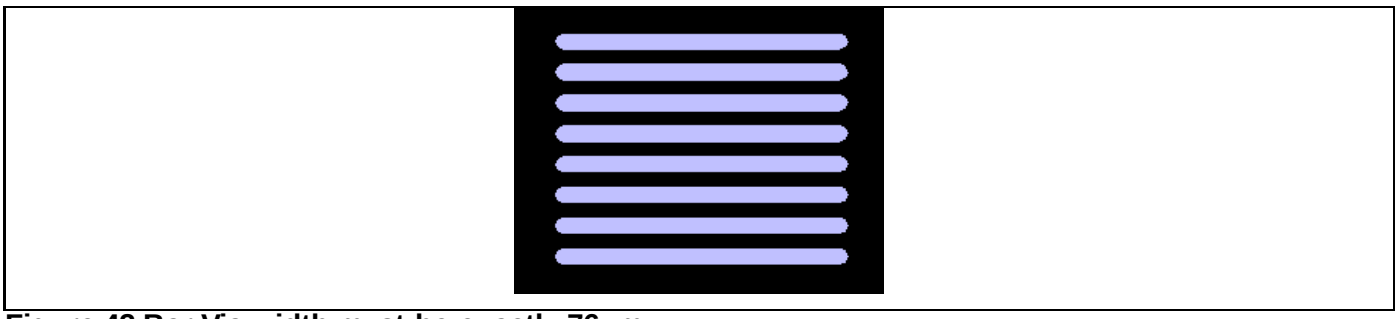


Figure 42 Bar Via width must be exactly 76um

- All fiducials must not touch any other metal. Figure 43 shows an example violating this rule.

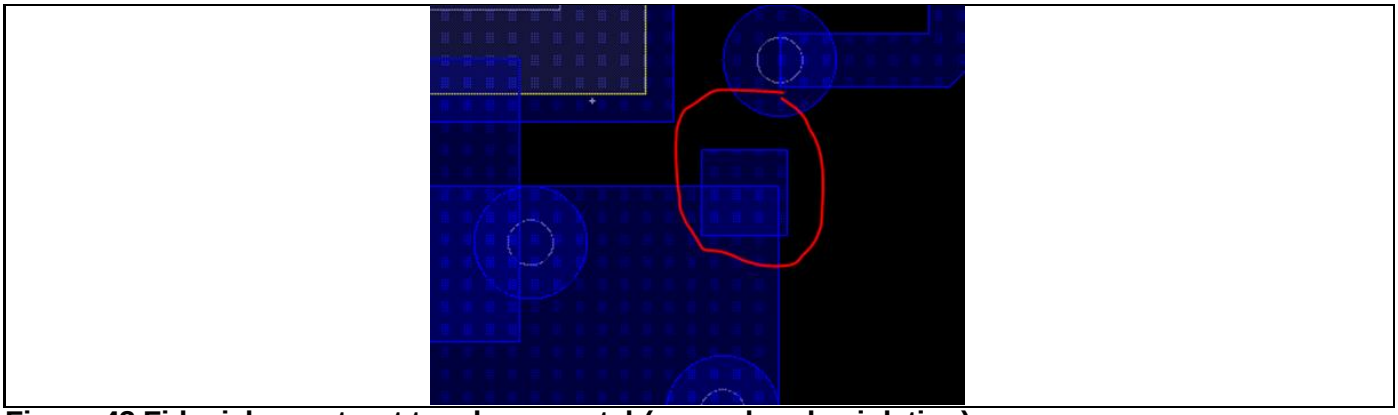


Figure 43 Fiducials must not touch any metal (example rule violation)

6.3 Module Integration and Formal Requirements

- No objects/shapes on any non-design layer are allowed. This can be checked during the export, as can be seen in Figure 44. Common errors that occurred were the use the layer Top_SolderMask_inv, which is supposed to be only a derived layer for EM simulations (but no design layer), or the occurrence of _layer0, which indicates that objects (that could be a desired part of the design) are placed on an unknown layer. Figure 45(a) depicts an example that can cause the occurrence of _layer0, whereas Figure 45(b) shows the correct settings for this example. These occurrences need to be resolved prior releasing the design.

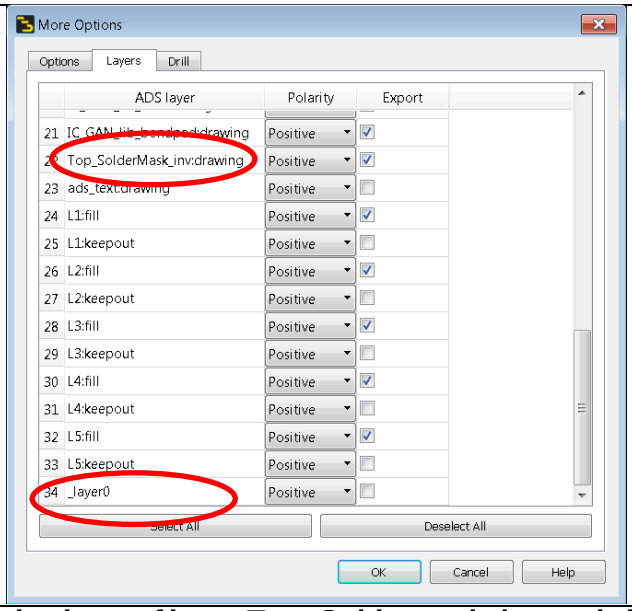
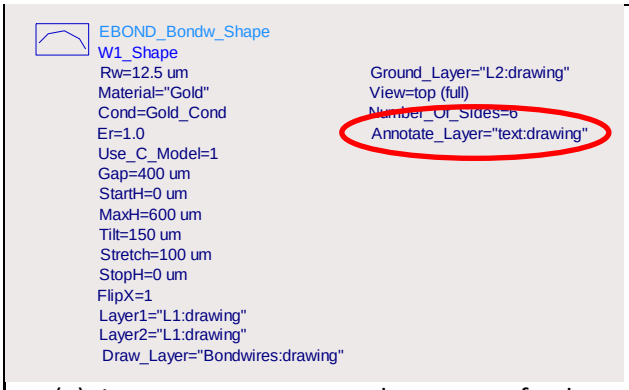
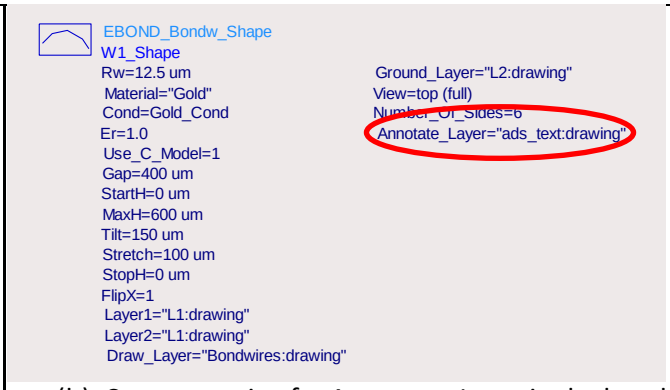


Figure 44 Example of undesired use of layer Top_Soldermask_inv and _layer0



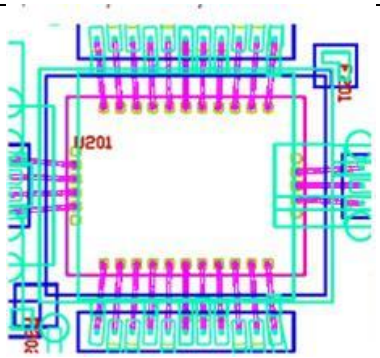
(a) Layer zero occurrence due to use of unknown layer "text:drawing" for the Annotate_Layer in the bondprofile definition



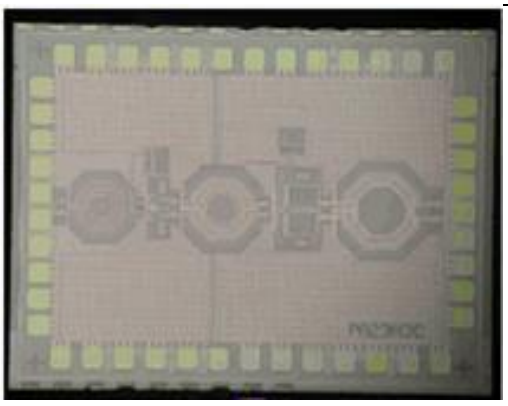
(b) Correct setting for Annotate_Layer in the bondprofile definition

Figure 45 Example that can cause the occurrence of _layer0

- Die bondpads must include all bondpads (not only the ones used), as well as all relevant features that are required to avoid misunderstanding (die name, die fiducials, other unique features that allow recognize/confirm orientation eg. coils). Figure 46 shows a non-optimum example of module design data vs. final delivered chip.



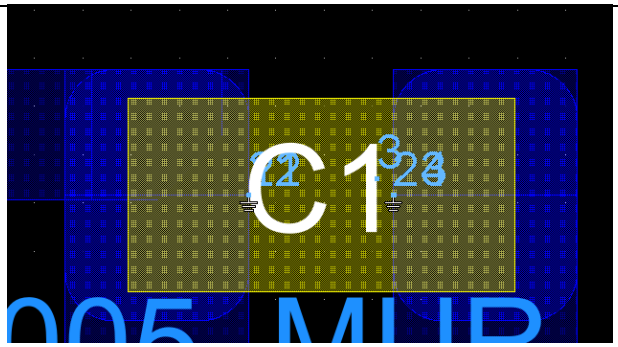
(a) Non-optimum example of design data not showing all bondpads, die fiducials or die name



(b) Corresponding picture of final delivered chip showing more bondpads than in the design data

Figure 46 Non-optimum example for chip design data vs. actually delivered design

- All component texts on layer Top_SilkScreen (needs to be aligned with BOM and also includes the Bondwire profiles). Figure 47 depicts the required setting for SMD components. It shall be noted that this also applies to bondwire components. Only BOM and bondwire items shall have their instance name on the layer Top_SilkScreen This is required to provide a component placement drawing



(a) Component layout View

Property	Value
Component Text	
Font	Arial For CAE
Size	0.127
Component name layer	ads_devicerads_annotate
Instance name layer	Top_SilkScreen:drawing
Component Pin Net Name	
C1 P1	N_49
C1 P2	N_53

(b) Component Properties setting: Instance name layer needs to be on Top_SilkScreen:drawing

Figure 47 Required SMD/bondwire component settings for component placement drawing

- All ground planes/layout elements need to be on the net gnd! to allow for the use of ground planes in the top cells. (required for all subcells). This needs to be checked (proper ground plane connectivity). Figure 48 shows an example based on layer on how to check to proper support the use of ground planes on top level layouts. The red circle in Figure 48 shows an example of an error the via annular ring in this case is not properly on the net ground in this case causing a problem in the ground plane connection adjacent to the via. This would need to be resolved prior releasing the layout.

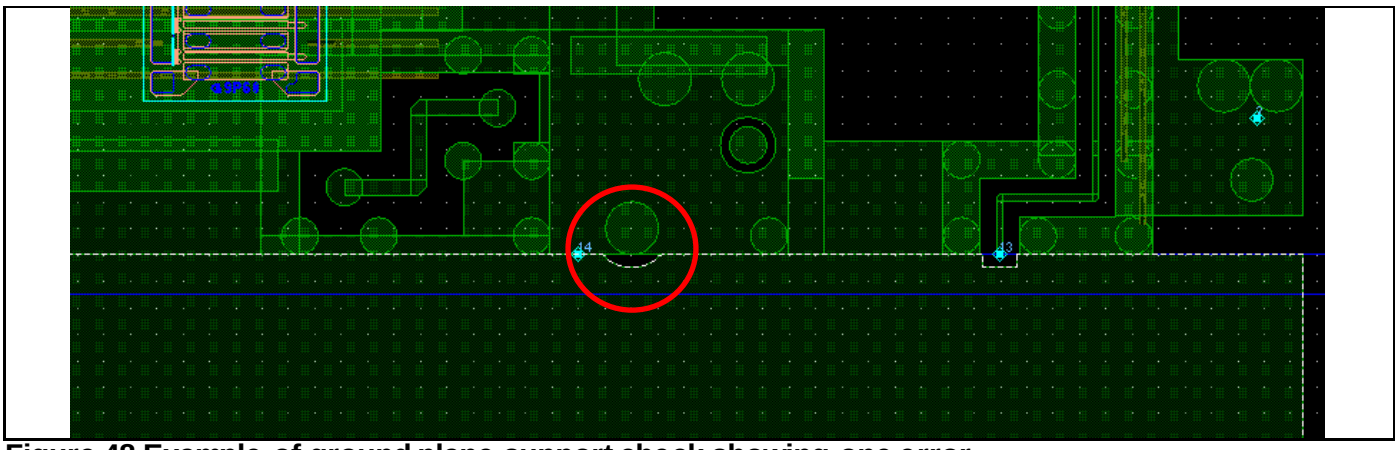


Figure 48 Example of ground plane support check showing one error

- BOM checked and verified (part numbers, value comment must match, tolerance needs to properly selected…, relationship to different variants must be checked…..).
  All BOM values used need to be verified for availability and correct partnumber → partnumber needs fully match to what will be sent to AMKOR (part number might also depends on packaging type eg. tape and reel). If the entered partnumber is recognized by the system the Subcons "StockID" and the number of items available in the inventory will be shown in the instance parameters. If the partnumber is not found in the system or 0 items are available the StockID parameter will display "not found in stock" resp. "out of stock".
  Figure 49 depicts an typo error in the part number as example for BOM errors.

ReferenceID	Manufacturer	Part Number	Value	Package	Position (mm)	Orientation	Comment
C87	Murata	GRM0225C1HR690WA03	0.6 pF	01005	(+9.5500 +0.2750)	R 90.00	GRM0225C1HR60WA03, Ultra-small, C0G(-55to125[deg]), 50[V], 0.6[pF], +/-0.05[pF], 100[MHz]-20[GHz]

Figure 49 Example of part number error in BOM

BOM numbering/items must be unique (eg. no C1 in multiple subcells). In order to avoid that the numbering scheme shown in Figure 50 must be followed. It shall be noted that this rule applies to all BOM items (U/R/L/C/BW….).

cell	#1	X2 (RFU)
PA	C1-C99	C101-C199
Predriver	C201-C299	C301-C399
LNA/switch	C401-C499	C501-C599
Bias Controller	C601-C699	

Figure 50 BOM numbering rules

The user can customize the numbering during the BOM generation by adding custom instance properties to cell instances.

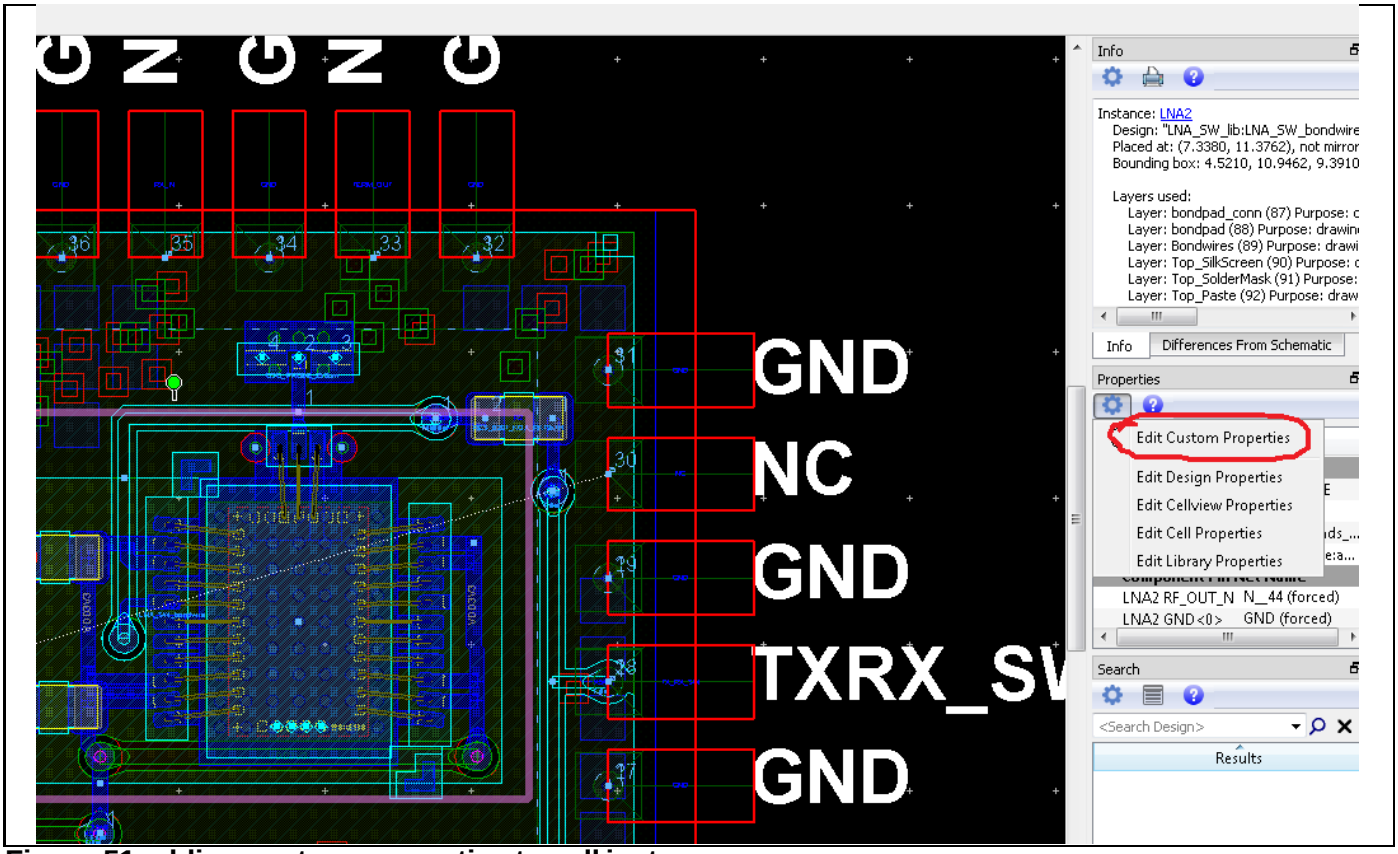


Figure 51 adding custom properties to cell instances

Property name	Type	Description
IFX_BOM_OFFSET_U	integer	Adds a cumulative offset to all instances in subcells named “U”
IFX_BOM_OFFSET_R	integer	Adds a cumulative offset to all instances in subcells named “R”
IFX_BOM_OFFSET_L	integer	Adds a cumulative offset to all instances in subcells named “L”
IFX_BOM_OFFSET_C	integer	Adds a cumulative offset to all instances in subcells named “C”
IFX_BOM_OFFSET_F	integer	Adds a cumulative offset to all instances in subcells named “F”

Table 10 supported custom instance properties

7 Module Design Release Procedures

- All design rules given in section 5 have to be fulfilled
- DRC run clean (exceptions need to be clarified and documented)
- All Non DRC design rules checked and compliant
- Define all bondwires that need to be loop controlled (shape specified)
- no cells/subcells in private workspaces (eg. wrk_name)
- verify connectivity of the top layout cell/and or generated artwork cell (→ generate Artwork)

7.1 Export Procedure/Scripts

Order	Procedure	Reference
1	Metal Density Check Transfer results in Excel sheet “Copper_density_revX.xlsx” (found in the root of the tape out (TO) folder on the project share) Check strip design compliance.	7.1.1
2	Export BOM Transfer the file in the corresponding design variant folder <productname_variant> (e.g.: 5RPM35151DV10_R0) under the TO folder. Rename file to <productname_variant_pick_and_place_report_revN.txt>	7.1.2
3	Export BWP a) all bondwire shapes Transfer the file in the corresponding design variant folder <productname_variant> (e.g.: 5RPM35151DV10_R0) under the TO folder. Rename file to <productname_variant_Bondwire_coordinates_revN.txt> b) loop controlled BW shapes Transfer the file in the corresponding design variant folder <productname_variant> (e.g.: 5RPM35151DV10_R0) under the TO folder. Rename file to <productname_variant_Bondwire_coordinates_shape_revN.txt>	7.1.3
4	Export Gerber Transfer the gerber folder in the corresponding design variant folder <productname_variant> (e.g.: 5RPM35151DV10_R0) under the TO folder. Rename folder to <gerber_revN> Note down the via number count as stored in the *.drl files and transfer the number into the Fab Document	7.1.4
5	Import Gerber in CAM350 Export screenshots according to the Fab Document requirements	7.1.6
6	Import DXF file in Autocad	7.1.7

	Generate Bond wire Diagram	
7	Create a .zip archive (see Figure 52) named “productName_revX” Including Subfolder with the gerbers **gerber_revX** Bondwire coordinates all-shapes ***productName*_Bondiwre_coordinates_revX** Bondwire coordinates to be controlled ***productName*_Bondiwre_coordinates_shapes_revX** BOM of components ***productName*_pick_and_place_report_revX** Fab spec document summary **AFE_Module-Fab Spec_*ProductName*_PG-LFLGA62-1-A_revX** Bonding diagram .dwg **Bonding_diagram_*ProductName*_revX.dwg** Bonding diagram .pdf **Bonding_diagram_*ProductName*_revX.pdf**	
8	in Fab Spec document: verify consistency of **PRODUCT NAME** and **REV** verify consistency in the **tables containing the list of gerbers** and the **list of documents** (name **MUST** be identical) verify **metal density** table consistency verify **via count** tables consistency in the .zip folder: all the files listed before must be included (no other files) no other files should be included	

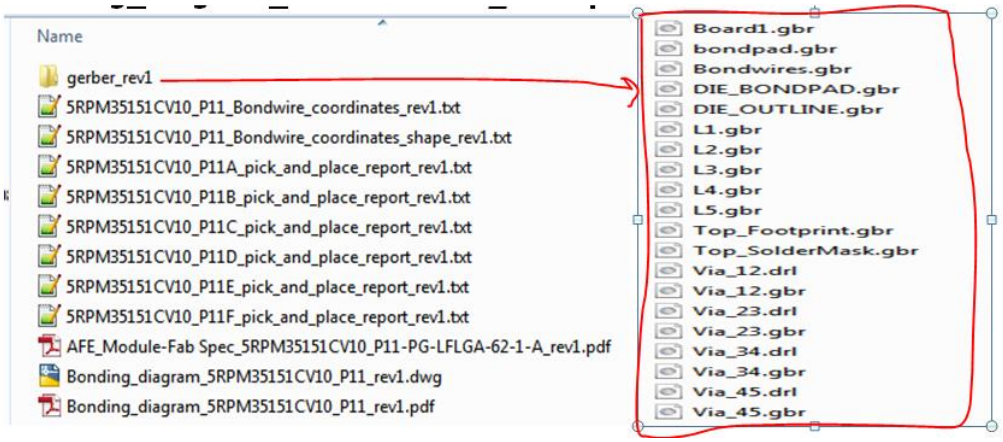


Figure 52 Zip archive file content

7.1.1 Metal Density Check

7.1.1.1 Using the IFX Laminate toolbar

1. Press  to view the Metal densities of the actively opened layout view.
2. The calculated Metal area and densities of L1 to L5 will be displayed (see Figure 53).

7.1.1.2 Using the Command line (Expert mode only!)

How to use the script:

1. open the command line: ADS Main Window→Tools→Command Line
2. -select/open design you want to check
3. run "IFX_VIH_AreaCalc_schubec(1);"
4. A window will pop that looks like in Figure 53

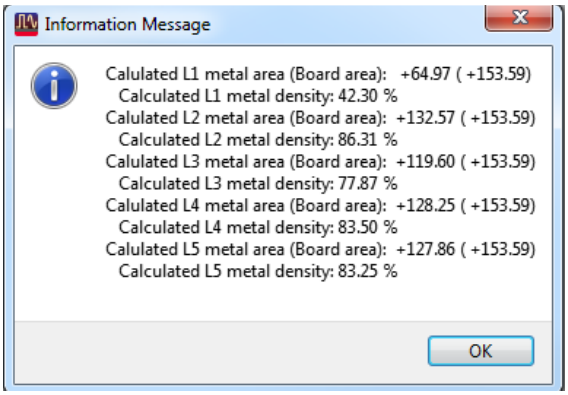


Figure 53 Metal Density Calculation Summary Window

The metal densities need to fulfill the following rules provided in Figure 54.

All Layers Metal Density >30% Variant to Variant difference <20% L2 to L4 difference <15% (symmetry)

Figure 54 Metal densities requirement

7.1.2 BOM Export

7.1.2.1 Using the IFX Laminate toolbar

1. Press  to create the Bill of Material (BOM) of the actively opened layout view.
2. The sorted BOM will show up in a text editor to be reviewed.

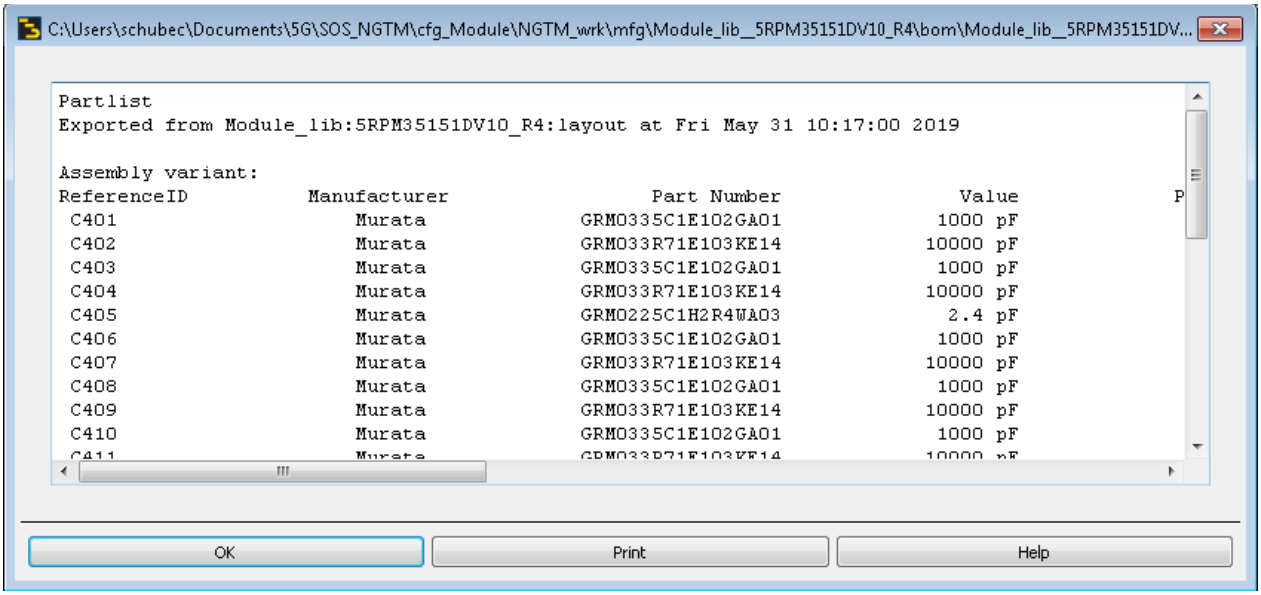


Figure 55 BOM Text Editor Window

3. The BOM will be automatically saved in the following location:
   <ADS_workspace>/mfg/*<libName__cellName>/bom/libName__cellName.bom*

The “StockID” column will indicate if the Part Number was found in the subcon inventory database. If the part number was not found in the database (exact string match) “NFIS” (Not Found In Stock) is displayed. If the item count number is 0 “OoS” (Out of Stock) is displayed

If the file already exists the file will be overwritten.

7.1.2.2 Using the Command line (Expert mode only!)

1. open the command line ADS Main Window→Tools→Command Line…
2. -select/open design you want to check
3. IFX_VIH_BOM_schubec("filename.txt",1,1);
   a. IFX_VIH_BOM_schubec(file,sort,showui);

Input parameters	Description	Type
File	file location to store the BOM ads workspace folder will be the default storeage location if no full path is specified	String
Sort	BOM list will be sorted based on the Reference designator in descending order (Sort=1)	Integer (0/1)
Showui	The BOM will be shown in the ADS integrated Text editor (showui=1)	Integer (0/1)

4. Will deliver a file (filename.txt) in the specified folder

7.1.3 Bondwire Definition Export

7.1.3.1 Using the IFX Laminate toolbar

Export all wires:

1. Press  to create the Bond wire profile (BWP) report of the actively opened layout view.
2. Select the Substrate definition to be used for the BWP generation.
3. The BWP will show up in a text editor to be reviewed.

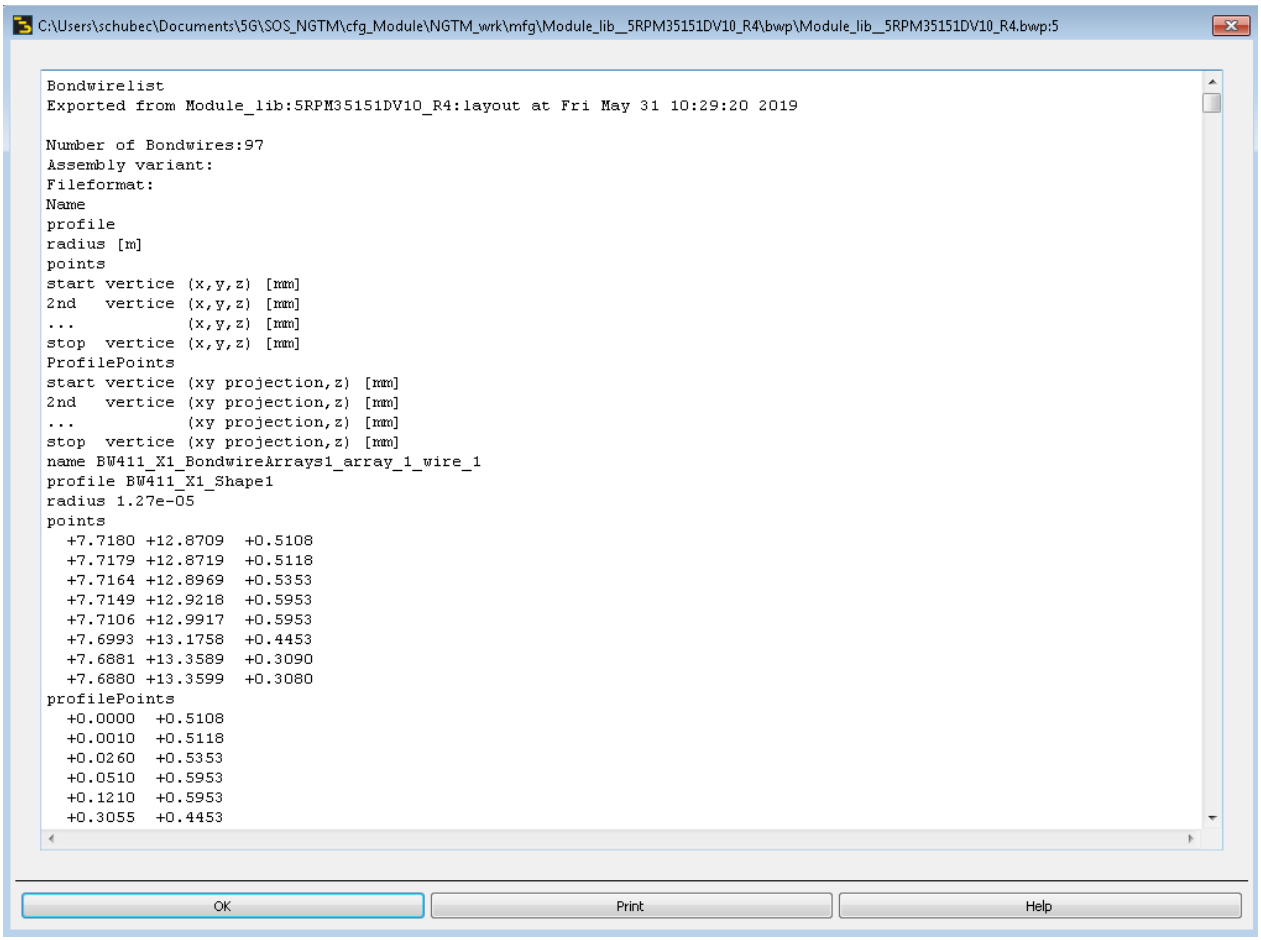


Figure 56 BWP Text Editor Window

4. The BOM will be automatically saved in the following location:
   <ADS_workspace>/mfg/*<libName__cellName>/bwp/libName__cellName.bwp*

If the file already exists the file will be overwritten

Export predefined “RF” wires:

1. Press  to create the Bond wire profile (BWP) report of the actively opened layout view for predefined bondwires only.
   Only Bondwire cell instances with the custom instance property “IFX_BW_INCLUDE” set to 1 will be included in the BWP report.
2. Select the Substrate definition to be used for the BWP generation.
3. The BWP will show up in a text editor to be reviewed.

4. The BOM will be automatically saved in the following location:
   <ADS_workspace>/mfg/<*libName__cellName>/bwp/libName__cellName_shape.bwp*

If the file already exists the file will be overwritten

7.1.3.2 Using the Command line (Expert mode only!)

1. open the command line ADS Main Window→Tools→Command Line…
2. -select/open design you want to check
3. Export command for controlled shapes:
   IFX_VIH_BWD_schubec("filename","substate_name",0,list("BW1","BW2"));
4. Export command for controlled shapes: for all shapes
   IFX_VIH_BWD_schubec("filename","substate_name",0,NULL);
5. This will deliver a file (filename) in your workspace folder

IFX_VIH_BWD_schubec(file, stackup, showUI, BWIncludeList);

Input parameters	Description	Type
File	file location to store the BWP ads workspace folder will be the default storage location if no full path is specified	String
stackup	EM stackup "libraryname:stackupname" e.g.: "IFX_Laminate_v0_tech:Module_with_dies_assembly"	string
Showui	The BOM will be shown in the ADS integrated Text editor (showui=1)	Integer (0/1)
BWIncludeList	Reduce to BWP generation to the Bondwires included in the list e.g.: list(“BW1”, “BW2”, “BW3”, “BW203”, “BW204”, “BW503”, “BW404”)	List of strings

7.1.3.3 Bond wire profile definition format

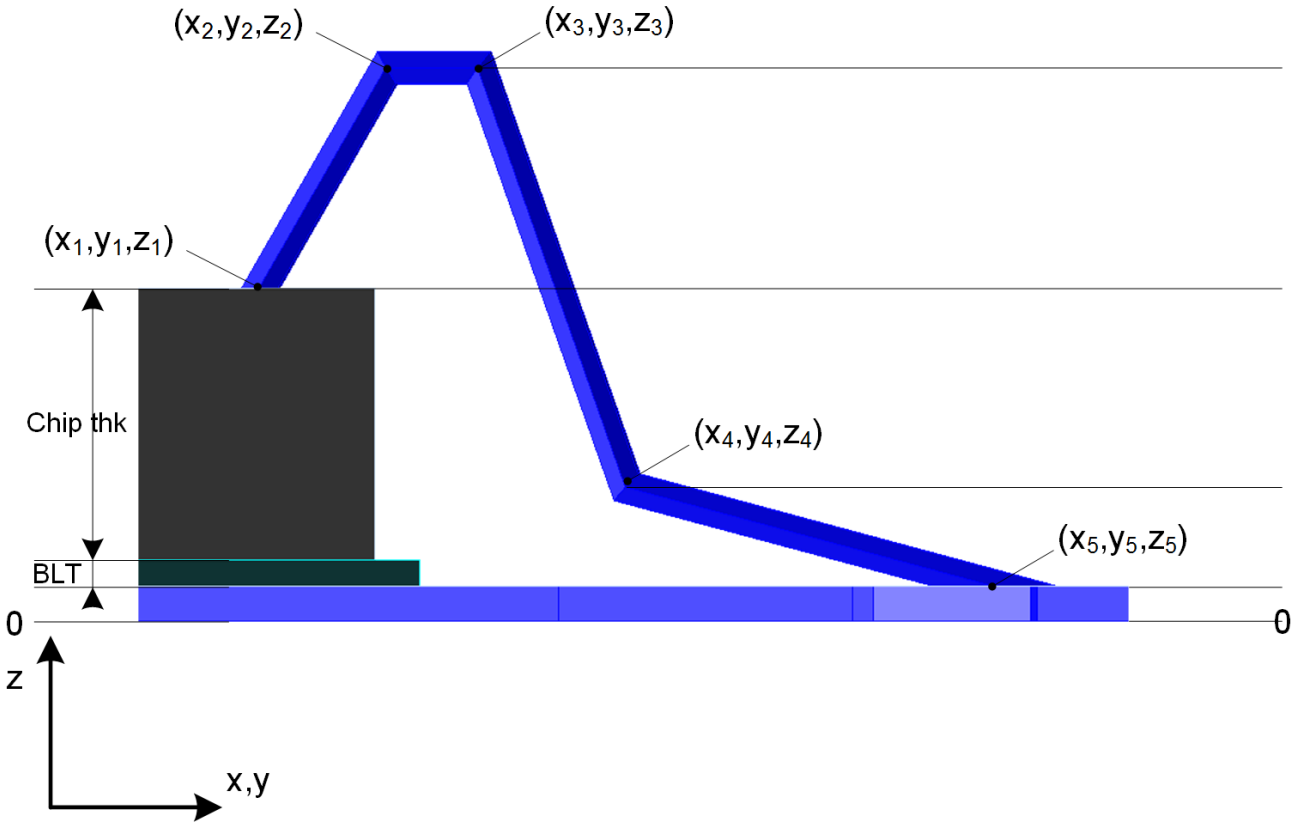


Figure 57 Bondwire vertices points

The text file “Bondwire_coordinates.txt” contains the bondwire vertice location. The (x,y) is referenced to the package origin (see Package outline). The z coordinate is referenced as shown in the above figure.
The above picture represents the standard 5 point JEDEC shape.

File format description:

For each bondwire the following information is included:

name “Reference Designator”
profile “profile name”
radius [m] 12.5e-6
points
start vertice (x,y,z) [mm]
2nd vertice (x,y,z) [mm]
... (x,y,z) [mm]
stop vertice (x,y,z) [mm]
ProfilePoints
start vertice (xy projection,z) [mm]
2nd vertice (xy projection,z) [mm]
... (xy projection,z) [mm]
stop vertice (xy projection,z) [mm]

7.1.4 Gerber file Export

7.1.4.1 Using the IFX Laminate toolbar

1. Please make sure that all layers are visible and selectable before starting the export.
2. Press 

to create the gerber and drill files of the actively opened layout view.
3. The gerber (*.ger) and drill files (*.drl) will be automatically saved in the following location: <ADS_workspace>/mfg/<*libName__cellName>/gerber/*

If the files already exist the files will be overwritten

7.1.4.2 Using the ADS GUI (Expert mode only!)

Export the gerber files:

-pay attention to include layers drawing and fill, but not keepout (for the metal layers)
-select all other design relevant layers
-export without polylines (set to 0) eg. to avoid lines exported used for port definition (which will increase the trace width unintentionally)

1. From ADS export the gerber files from the top cell by using the setting in the “more options” window as shown in Figure 58. (after the first time you do it, ADS should set this as default for the next extraction)
2. in the same window go to “layers” to check the list of layers to be exported. Normally the layers are the ones specified in Figure 59. If there are other layers that should not be in the list, then this must be verified (if a layer is in the list it means that there is one shape drawn in that layer).
3. the “drill” table (see Figure 60) provides a list of the layers where there are circular shapes. This must be checked to select ONLY the vias. Note that in this table there is also the count of the vias that must be included then in the documentation. This count may be not correct in case two or more holes are overlapping

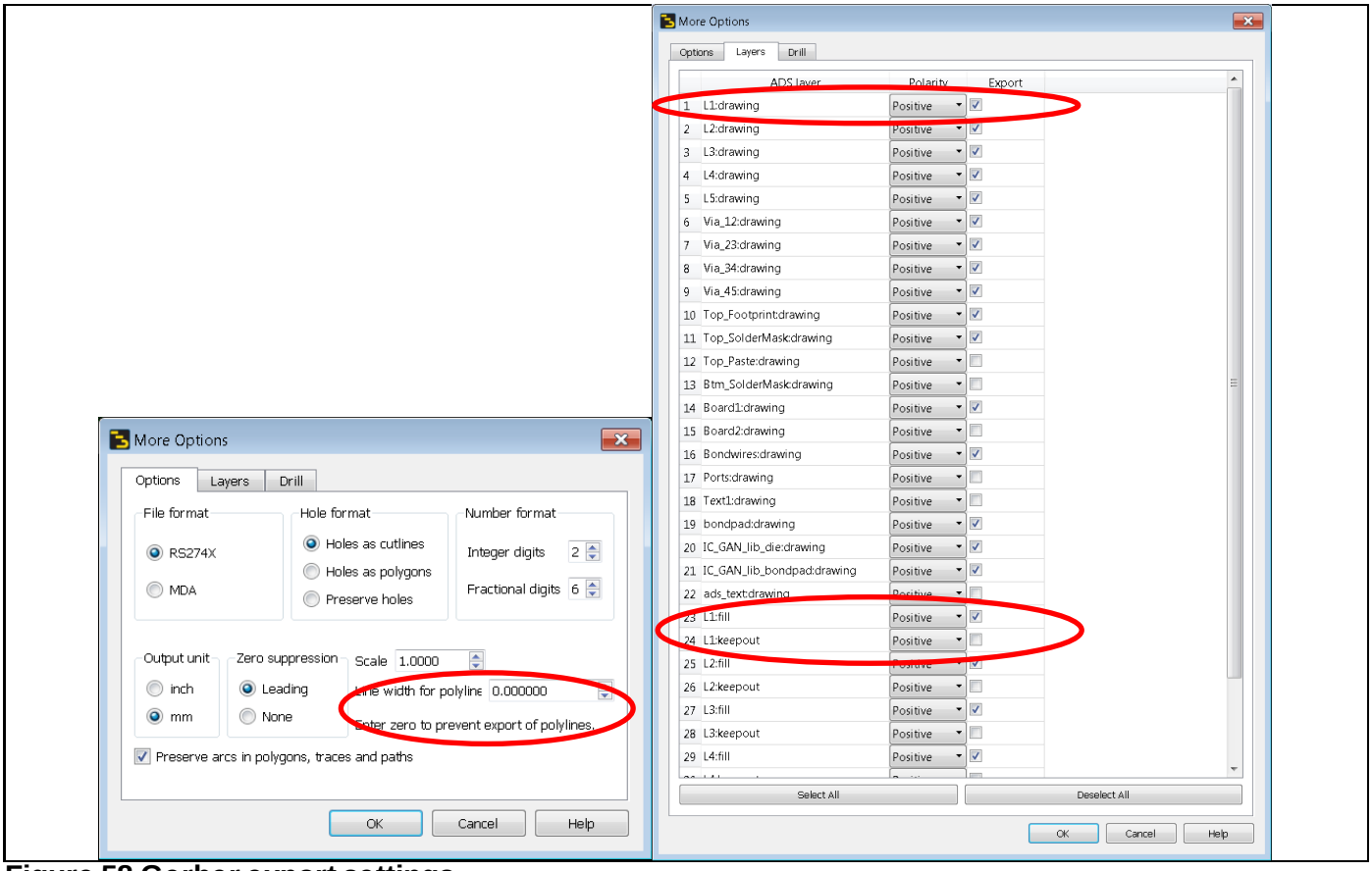


Figure 58 Gerber export settings

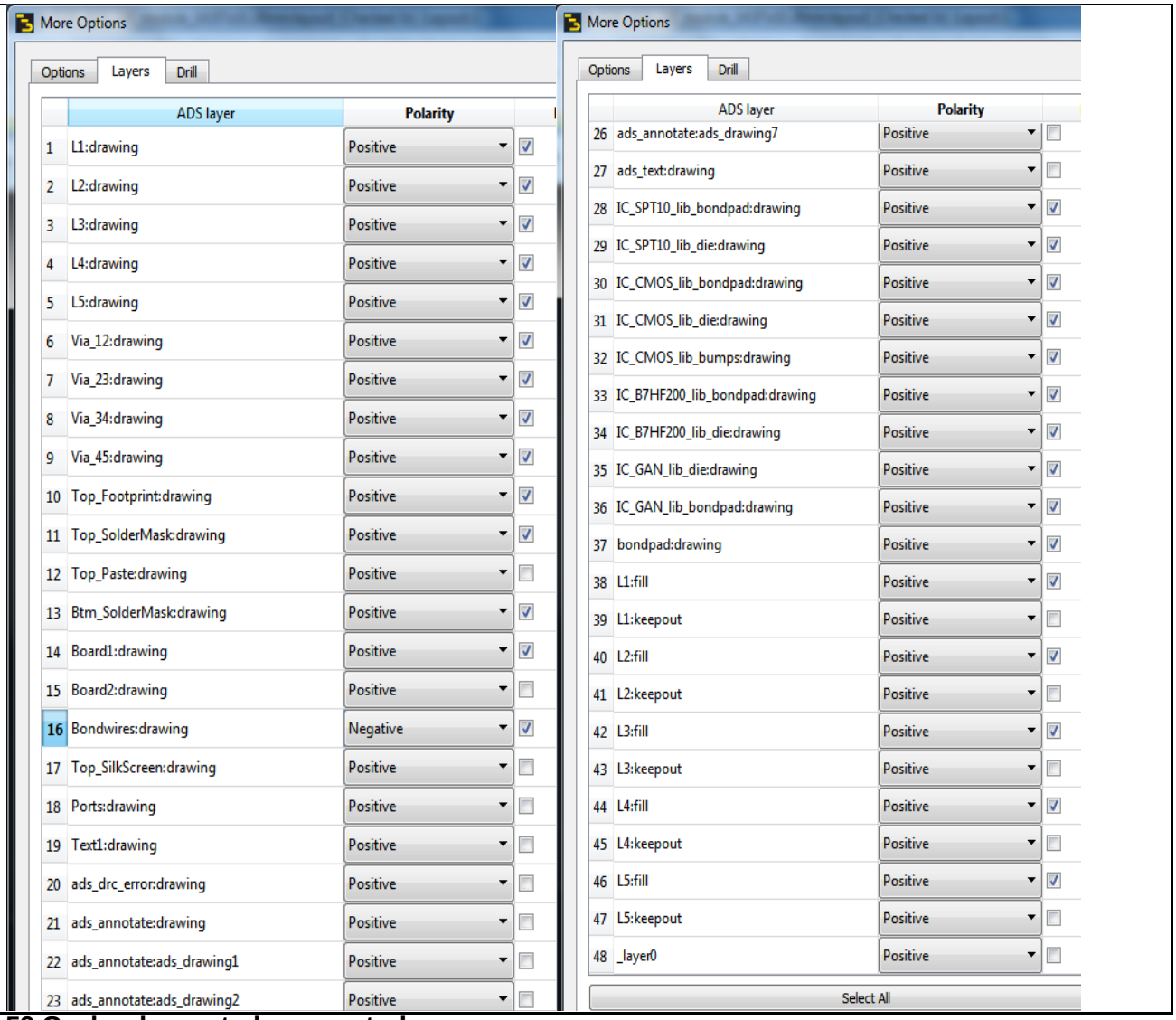
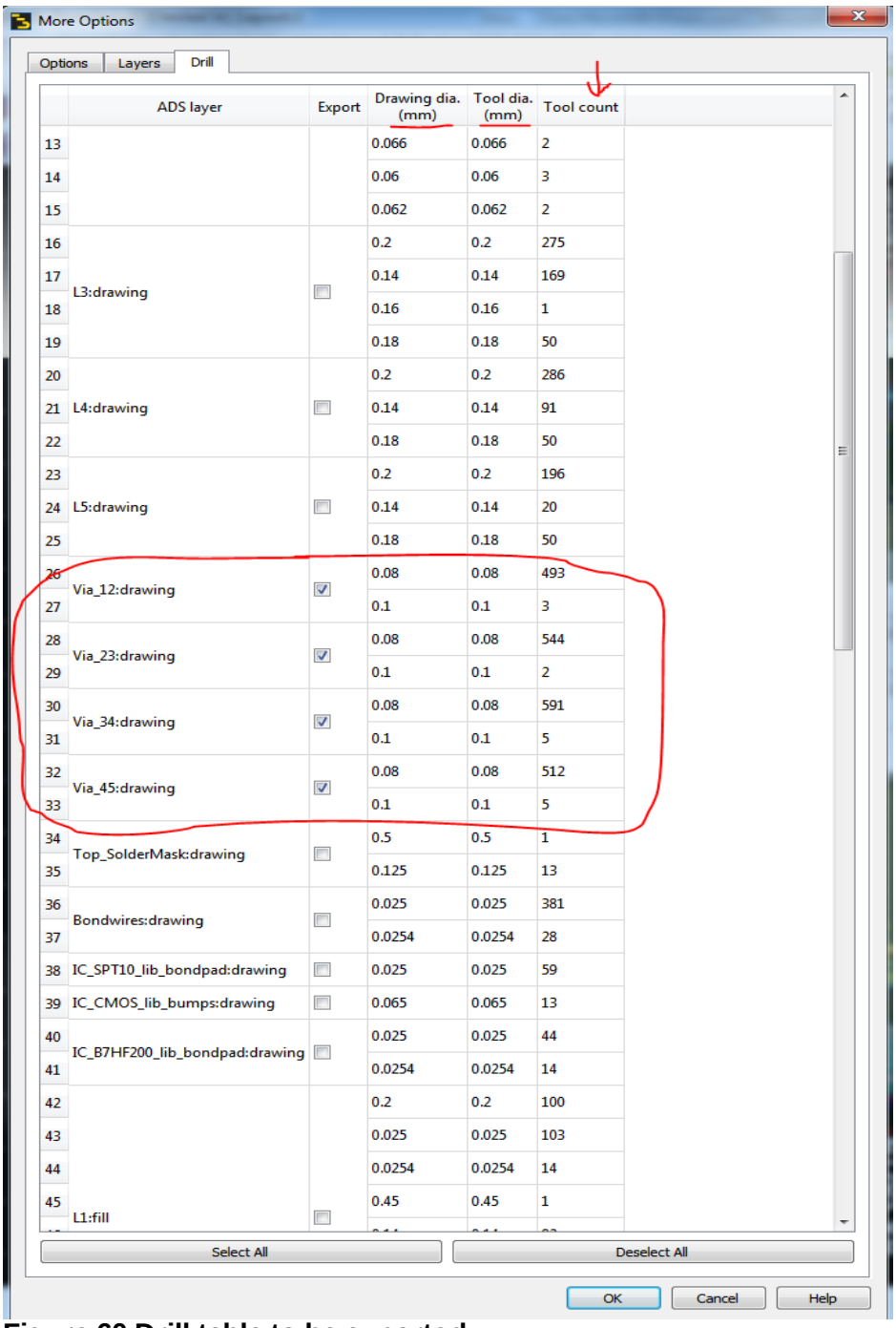


Figure 59 Gerber layers to be exported



	ADS layer	Export	Drawing dia. (mm)	Tool dia. (mm)	Tool count
13			0.066	0.066	2
14			0.06	0.06	3
15			0.062	0.062	2
16	L3:drawing	☐	0.2	0.2	275
17			0.14	0.14	169
18			0.16	0.16	1
19			0.18	0.18	50
20	L4:drawing	☐	0.2	0.2	286
21			0.14	0.14	91
22			0.18	0.18	50
23	L5:drawing	☐	0.2	0.2	196
24			0.14	0.14	20
25			0.18	0.18	50
26	Via_12:drawing	☑	0.08	0.08	493
27			0.1	0.1	3
28	Via_23:drawing	☑	0.08	0.08	544
29			0.1	0.1	2
30	Via_34:drawing	☑	0.08	0.08	591
31			0.1	0.1	5
32	Via_45:drawing	☑	0.08	0.08	512
33			0.1	0.1	5
34	Top_SolderMask:drawing	☐	0.5	0.5	1
35			0.125	0.125	13
36	Bondwires:drawing	☐	0.025	0.025	381
37			0.0254	0.0254	28
38	IC_SPT10_lib_bondpad:drawing	☐	0.025	0.025	59
39	IC_CMOS_lib_bumps:drawing	☐	0.065	0.065	13
40	IC_B7HF200_lib_bondpad:drawing	☐	0.025	0.025	44
41			0.0254	0.0254	14
42			0.2	0.2	100
43			0.025	0.025	103
44			0.0254	0.0254	14
45	L1:fill	☐	0.45	0.45	1

Figure 60 Drill table to be exported

7.1.5 Autocad file Export

7.1.5.1 Using the IFX Laminate toolbar

1. Please make sure that all layers are visible and selectable before starting the export.
2. Press 

to create autocad (*.dxf) file of the actively opened layout view.
3. The autocad (*.dxf) file will be automatically saved in the following location: <ADS_workspace>/mfg/<*libName__cellName>/dxf/ libName__cellName.dxf*

If the file already exists the file will be overwritten

Only the following layers will be exported / merged:

ADS_layer	DXF Layer
Bondwires:drawing	BONDWIRES
Top_SolderMask:drawing	TOP_SOLDERMASK
Board1:drawing	BOARD1
bondpad:drawing	BONDPAD
IC_GAN_lib_bondpad:drawing IC_B7HF200_lib_bondpad:drawing IC_CMOS_lib_bondpad:drawing IC_SPT10_lib_bondpad:drawing	DIE_BONDPAD
IC_GAN_lib_die:drawing IC_B7HF200_lib_die:drawing IC_CMOS_lib_die:drawing IC_SPT10_lib_die:drawing	DIE_OUTLINE
Top_Footprint:drawing	TOP_FOOTPRINT
L1:drawing L1:fill	L1
L5:drawing L5:fill	L5

Table 11 DXF export layers

During the export all shapes on the same ads layer will be merged (union).

7.1.6 CAM350 file import

1. Import the gerber files using the settings and color legend depicted in Figure 61

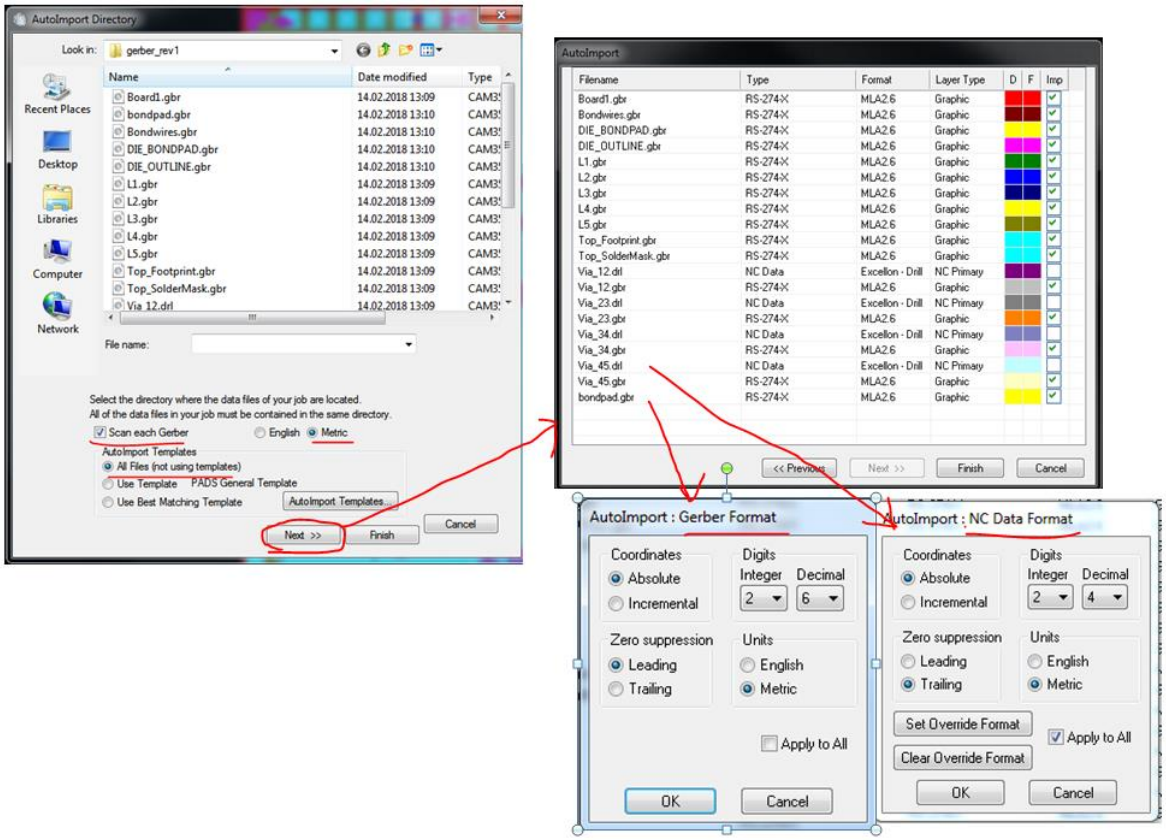


Figure 61 Cam350 gerber auto import settings

7.1.7 Autocad dxf import

1. Open the DXF file in Autocad Mechanical 2014
2. run the command: NETLOAD and load the dll library CDM_AutoCAD_AddOn.dll
3. run the command: **INITDRAWING** and select the proper .bom and .bwp files and template for autocad as shown in Figure 62.

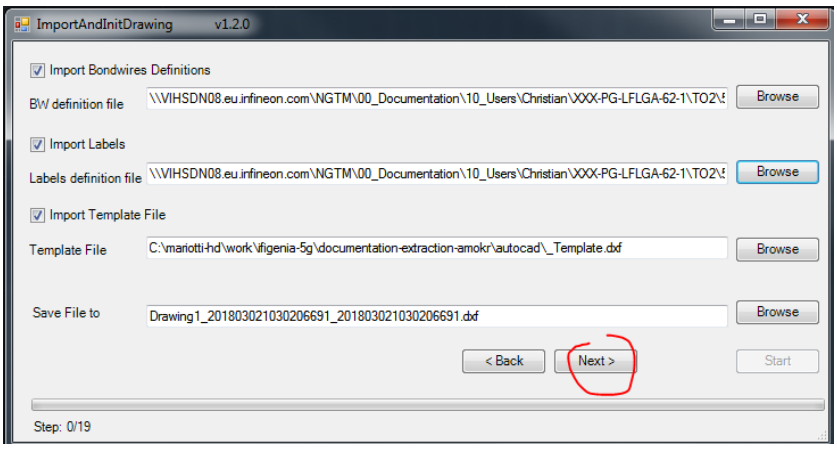


Figure 62 AutoCAD addon import dialog

4. Save the file in both .dxf and .dwg format with the name: “Bonding_Diagram_productName_revX”

5. Views available:

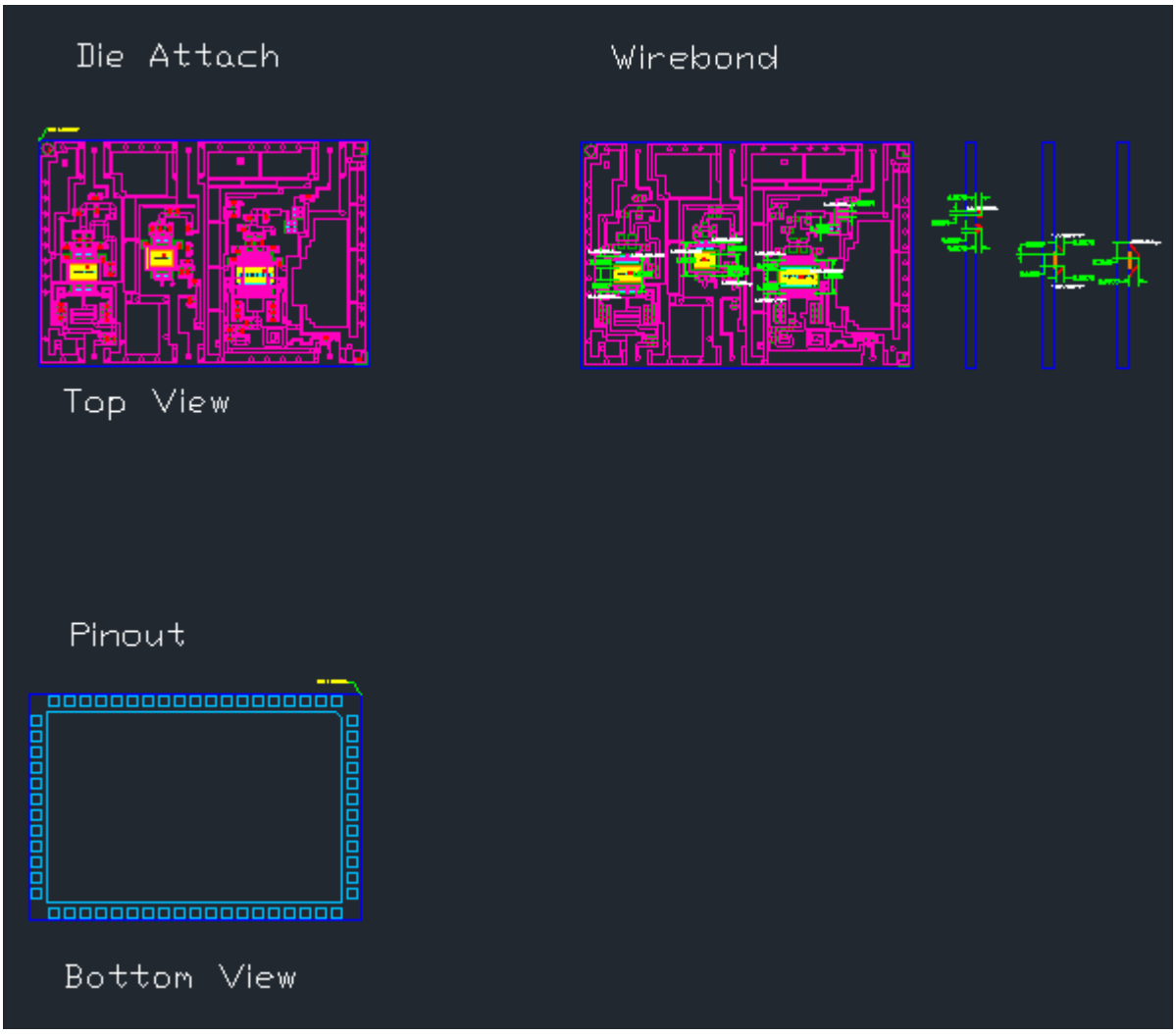


Figure 63 AutoCAD model space view

6. Adjust the wirebond projection (use construction lines, anchor points, power dimension).
7. Place the table with the BW in each page
8. Generate the output .pdf file with the name given to the .dxf and.dwg

7.1.8 ADS Export Macro Example

By using a ADS macro file the export procedures can be done efficiently for multiple cells.

Figure 64 shows an example macro file to export the BOM and bondwire data for two designs (the rest of the script is not shown for simplicity).

It can be called from the main ADS window Tools→Playback Macro…

```
/* Begin */
de_bring_view_to_top_or_open_new_window("PA_5W_3G6_lib", "5RPM35151CV10_P11", "layout", 3);
IFX_VIH_BOM_schubec("5RPM35151CV10_P11_bom", 0);
IFX_VIH_BWD_schubec("5RPM35151CV10_P11_Bondwire_coordinates_shape_rev1",
"IFX_Laminate_v0_tech:Module_with_dies",0,list("BW1","BW2","BW3","BW4","BW5","BW6","BW10",
"BW11","BW12","BW13","BW14","BW15","BW16","BW17", "BW18", "BW19","BW20",
```

```
"BW21","BW22","BW23","BW24","BW25","BW26","BW27", "BW28", "BW29","BW30"));
IFX_VIH_BWD_schubec("5RPM35151CV10_P11_Bondwire_coordinates_rev1",
"IFX_Laminate_v0_tech:Module_with_dies",0,NULL);
de_close_window();

de_bring_view_to_top_or_open_new_window("PA_5W_3G6_lib",  "5RPM35151CV10_P13",  "layout", 3);
IFX_VIH_BOM_schubec("5RPM35151CV10_P13_bom",  0);
IFX_VIH_BWD_schubec("5RPM35151CV10_P13_Bondwire_coordinates_shape_rev1",
"IFX_Laminate_v0_tech:Module_with_dies",0,list("BW1","BW2","BW3","BW4","BW5","BW6","BW10",
"BW11","BW12","BW13","BW14","BW15","BW16","BW17", "BW18", "BW19","BW20",
"BW21","BW22","BW23","BW24","BW25","BW26","BW27", "BW28", "BW29","BW30"));
IFX_VIH_BWD_schubec("5RPM35151CV10_P13_Bondwire_coordinates_rev1",
"IFX_Laminate_v0_tech:Module_with_dies",0,NULL);
de_close_window();

….

/* End */
```

Figure 64 Example of ADS macro to do BOM and bondwire export for multiple cells (example.dem)

8 Appendix

8.1 Installation procedure for Windows 10 VDIs

8.1.1 General stuff

- Software folder path: \\VIHSDN08.eu.infineon.com\NGTM\00_Documentation\10_Users\Christian\flow_tools
- Useful software from *IFX App Store*: *UltraEdit* (text editor), *PathCopy* (shortcut to copy file's path).
-

8.1.2 Backup

- Go to your SOS workarea and compress directly the folder as .zip file.
- Since all the old simulation results are always stored by ADS and use a lot of space (especially EM), it is better to delete all the relative files before the backup (path: *<ADS_workarea>/<simulation>/..*).
-

8.1.3 Environment Variables

Add the following Environment Variables:

- AGILEESOFD_LICENSE_FILE 3009@vihlal21.vih.infineon.com,3009@vihlal22.vih.infineon.com,3009@vihlal23.vih.infineon.com
- ADS_LICENSE_FILE 3009@vihlal21.vih.infineon.com,3009@vihlal22.vih.infineon.com,3009@vihlal23.vih.infineon.com
- MODELITHIC_LICENSE 3800@vihlal04.vih.infineon.com
- HOOPS_PICTURE dx11/window0

8.1.4 VDI shortcut

When running *Remote Desktop Connection* click on *Show Options* and use *Connection settings* > *Save As* to create a shortcut for the VDI.

8.1.5 Virtual machine login

Login with username with small letters for SOS working properly. Consider to restart the virtual machine and the Windows remote desktop connection and login with small letters.

8.1.6 ADS

1) Run *ads_2019_update1.0_win_x64* as Administrator and install ADS:
   a. Choose Install Set: Complete.
   b. Where would you like to install? Specify *C:\Keysight*. Better to avoid *C:\Program Files*.
   c. Choose your home folder as preferred.
   d. Install.
2) Completed the ADS installation with the update: run *ads_2019_update1.1_win_x64* installation as Administrator.
3) With the environment variables set up ADS should not request the license, otherwise: enter 3009@vihlal21.vih.infineon.com,3009@vihlal22.vih.infineon.com,3009@vihlal23.vih.infineon.com as license servers.

4) To import the configuration variables (as defined hotkeys and templates) from another ADS it is possible to copy-paste the folders *circuit* and *config* from *ADS_HOME*.

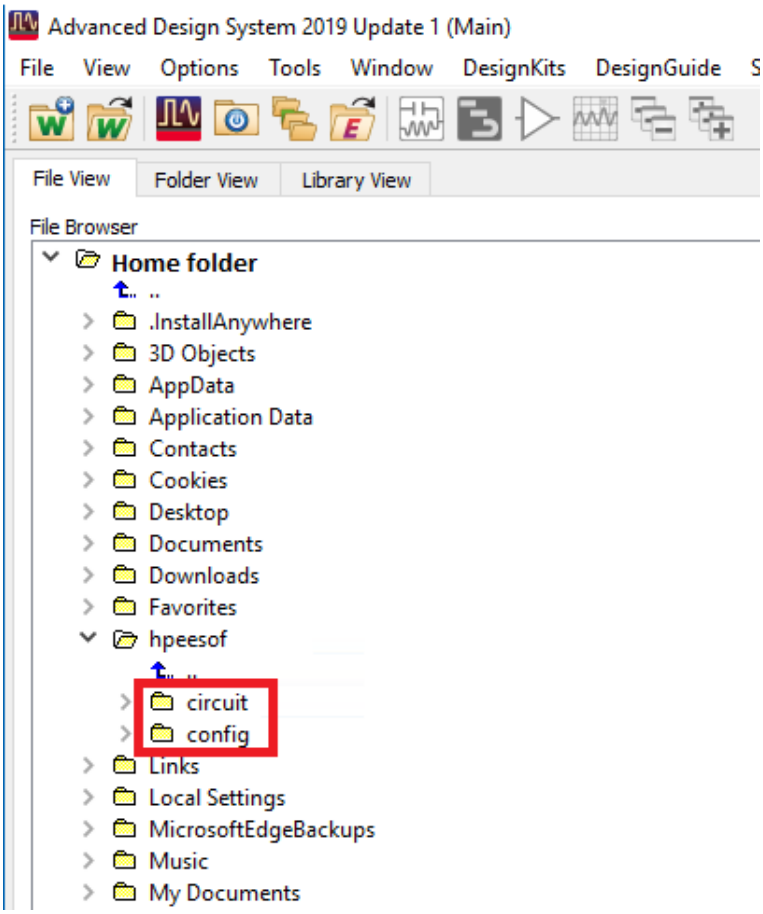
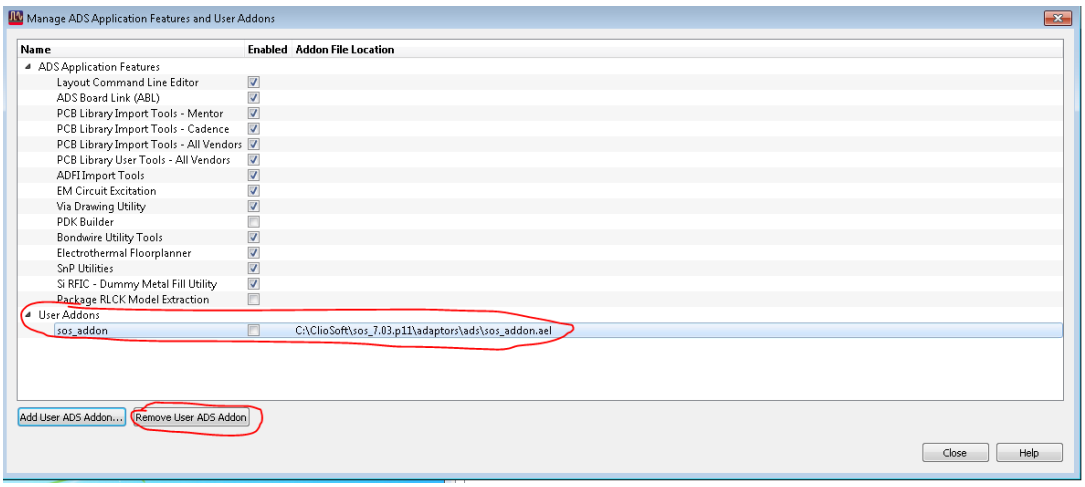


Figure 65 ADS main window

8.1.7 SOS

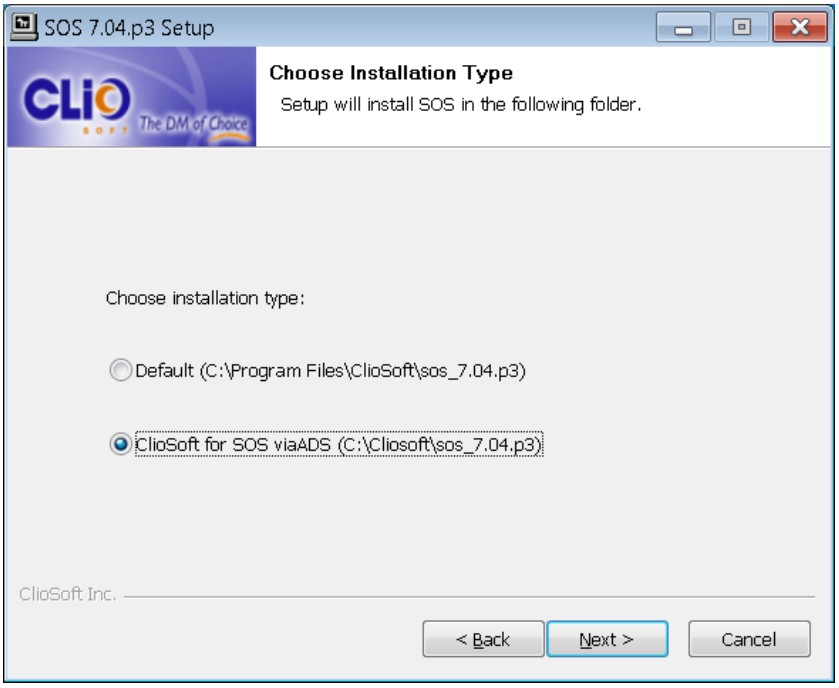
1) Get administrator privileges (iARM tool).
2) Close ADS workspace (if open).
3) As a safety precaution if not already done please make a backup of your local workarea.
4) If present an old SOS version:
    a. Remove Cliosoft ADS Addon: →Tools →App Manager…



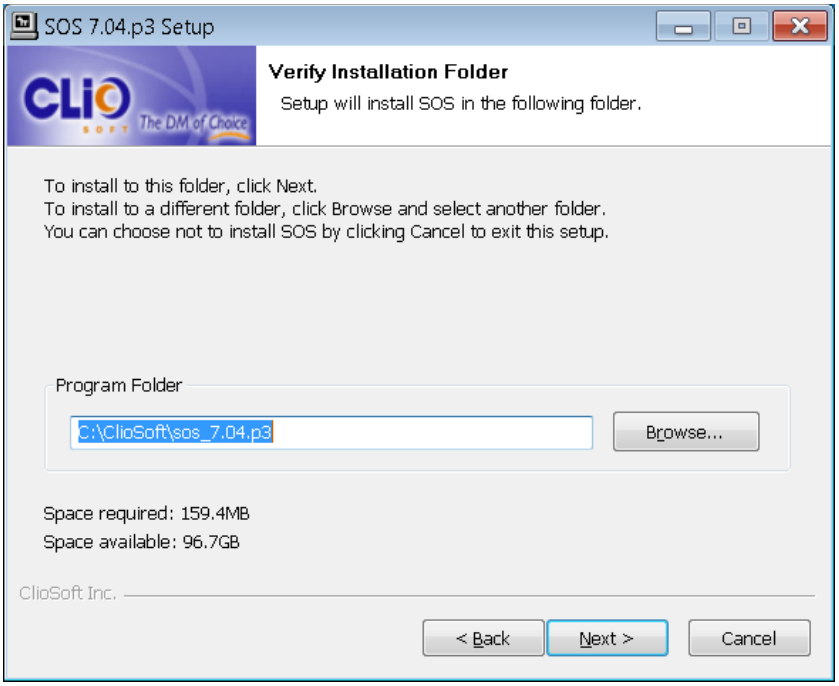
b. Uninstall cliosoft client (Settings → App → Unistall).

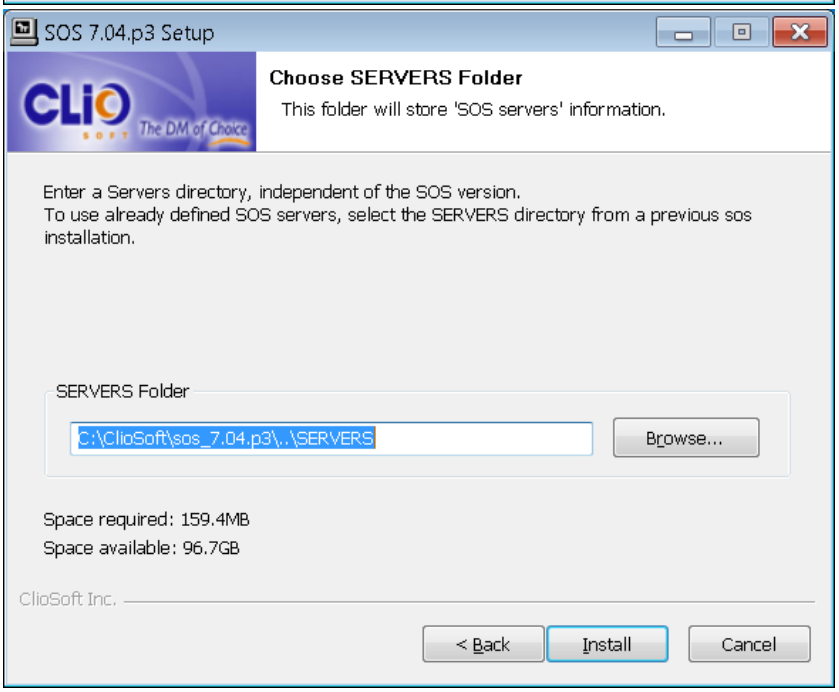
5) Run *sos_7.0x.px_win_x64* as Administrator and install:

a. Choose installation type *ClioSoft for SOS viaADS*.



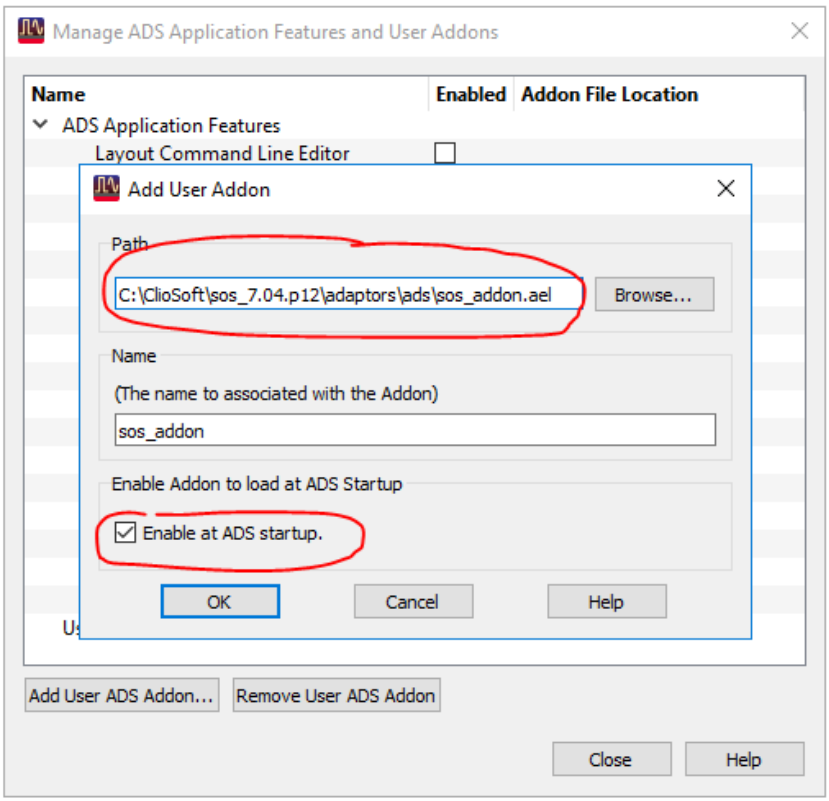
b. Use *C:* as Program Folder



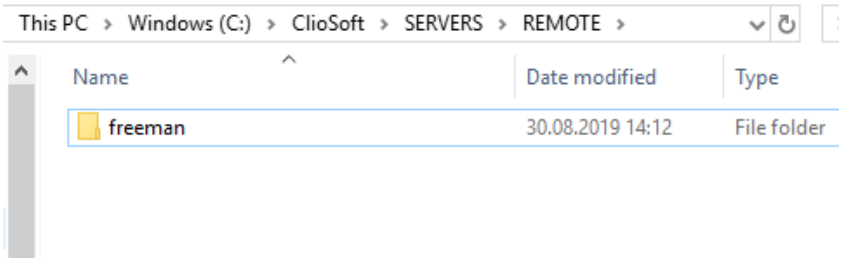


6) After installation check that the following environmental variables exists (if not, please add the variable):
   a. CLIOLMD_LICENSE_FILE 3800@vihlal01.vih.infineon.com,3800@vihlal02.vih.infineon.com,3800@vihlal03.vih.infineon.com
   b. CLIOSOFT_DIR C:\ClioSoft\sos_7.04.p12
   c. SOS_SERVERS_DIR C:\ClioSoft\SERVERS
7) Start ADS.
8) Install User Addon:
   a. →Tools→App Manager… Add User ADS Addon
   b. Path: *C:\ClioSoft\sos_7.04.p12\adaptors\ads\sos_addon.ael*

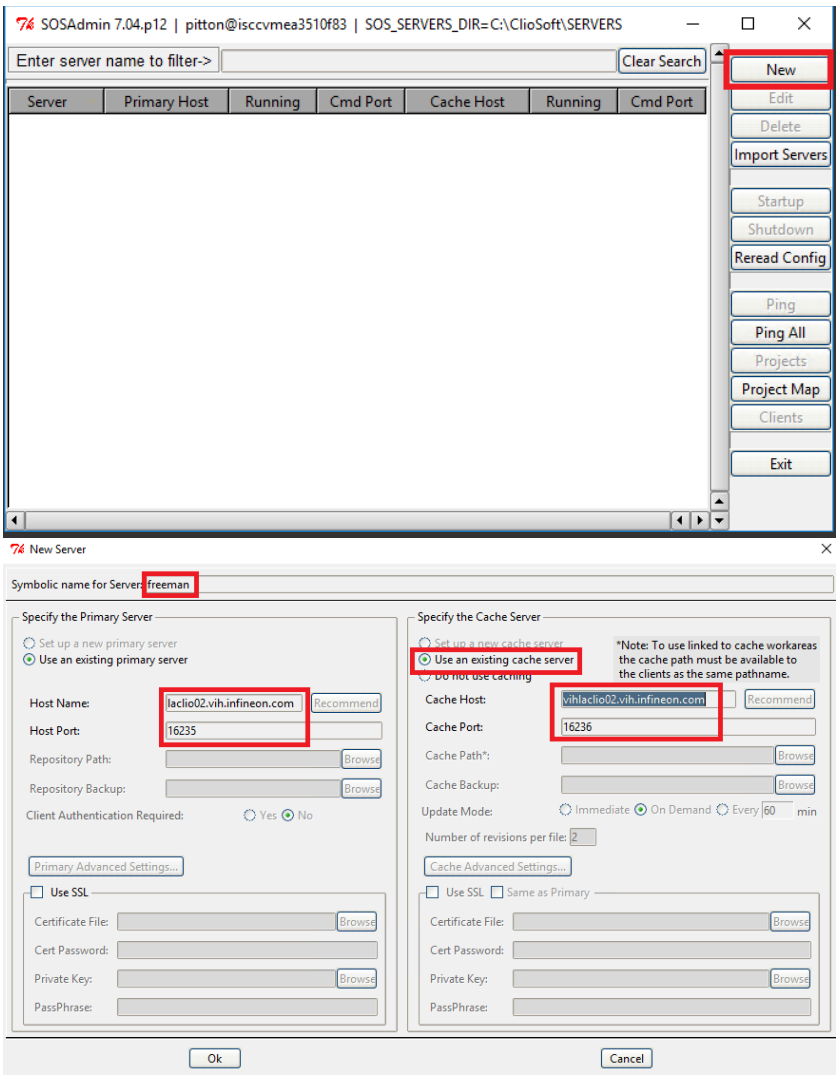
c. Check Enable at ADS startup.



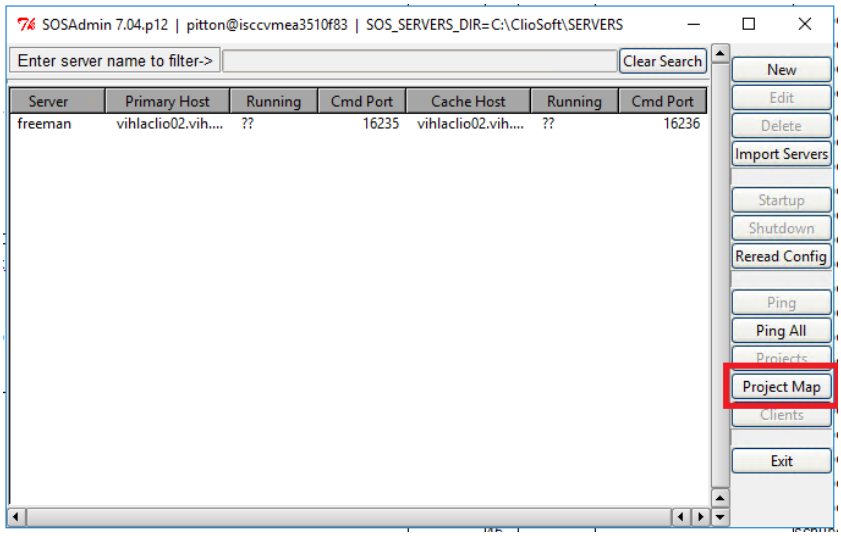
9) Close ADS.
10) If is the first installation of SOS you should create the server:
    a. The easier way is to copy-paste the freeman folder (which you can find here in the ClioSoft installation folder) to *C:\ClioSoft\SERVERS\REMOTE\..*



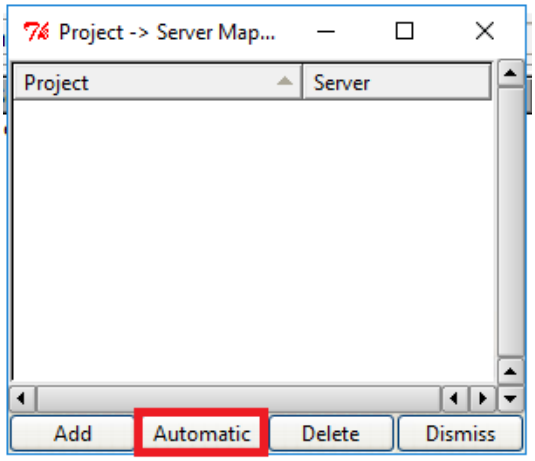
    b. Otherwise go to *sosadmin* and set the server:
        i. Create new server



11) Go to *sosadmin* and add the *Project Map*:
    a. Select the Server.
    b. Press *Project Map*.

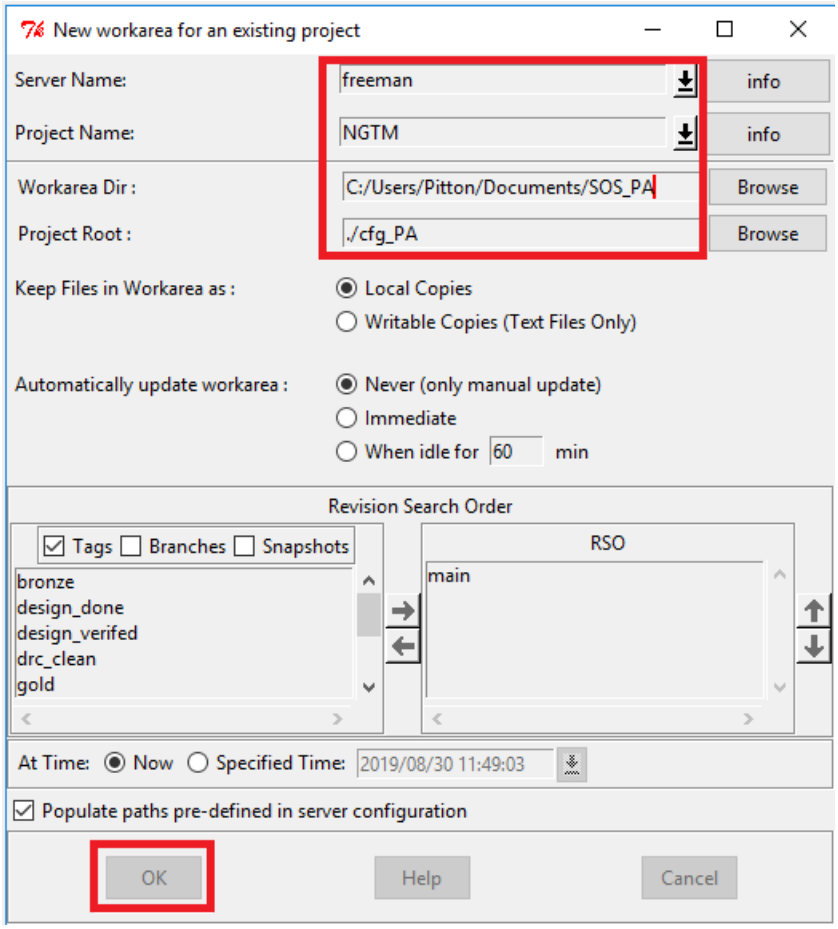


c. Press *Automatic*.



d. Then *Yes* to the next window.
e. Exit with *Dismiss* and *Exit*.

12) After the setup of the server it is possible to create a new workarea for SOS:
    a. If have an old backup: copy-paste.
    b. Otherwise create a new one selecting: server name, project name, workarea directory and project root.



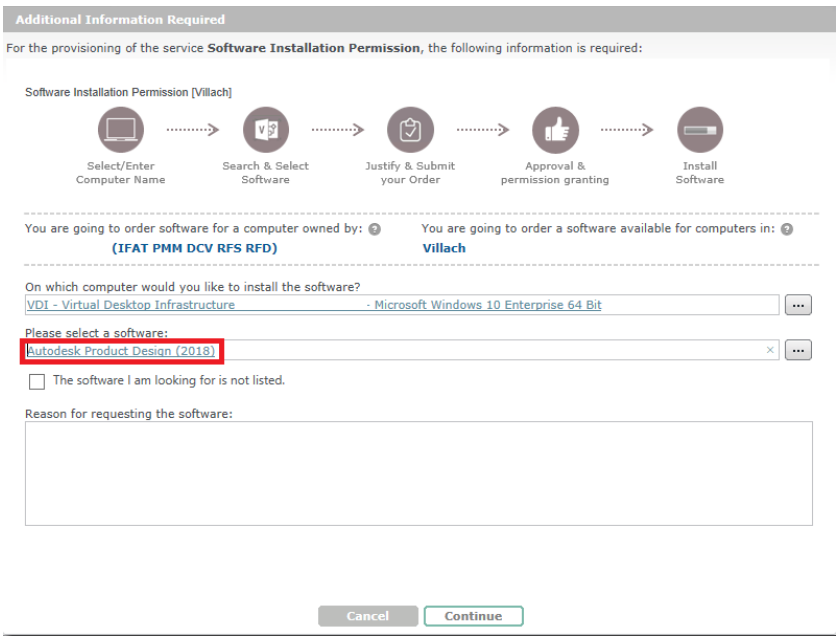
13) Update your SOS workarea using the new cliosoft client. (Please check mark the "check entire workarea consistency").
    This may take some time.
14) Done.

8.1.8 Modelithics

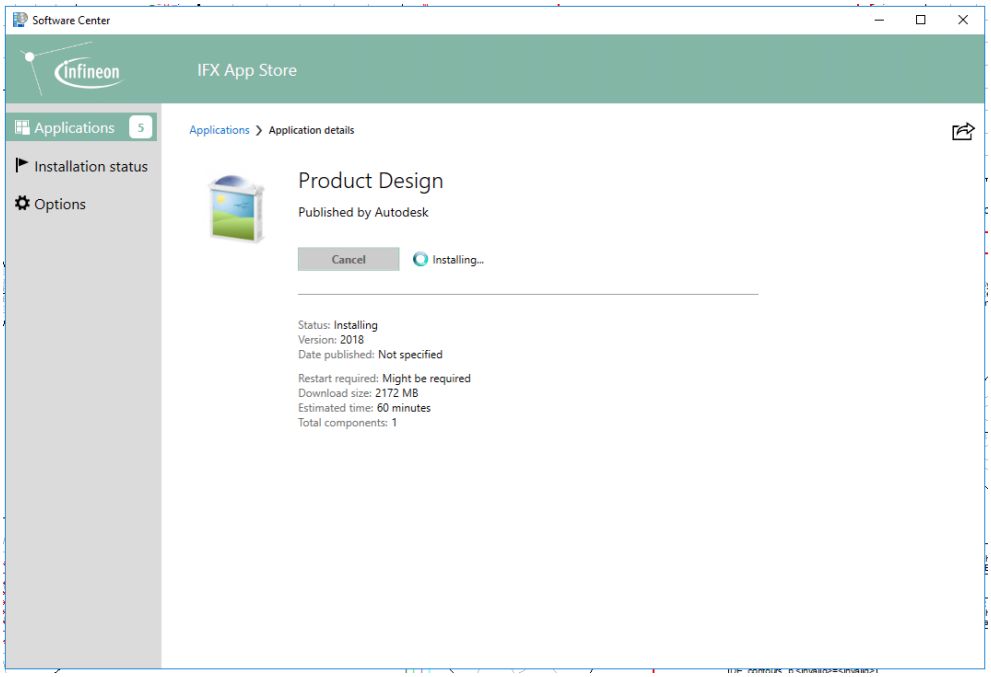
1) Run *Setup_COMPLETEv19.0_ADS* as Administrator and install:
    a. Choose Installation Directory "*C:\Modelithics*".
    b. Select "Complete" as installation type.
2) Setup Modelithics:
    a. Set 0 days for license expiration warning
3) Done.

8.1.9 AutoCAD

1) Request the permission through the IT Shop for *Autodesk Product Design (2018)*.



2) Once approved can be installed from *IFX App Store*.



9 Revision History

Rev.	Date	Name	Comment
1.0	1.3.2018	Schuberth/Seebacher	Converted Design Rules from power point and added lessons learned from AMKOR tapeouts
1.0.1	21.11.2018	Schuberth	Modified layer description
1.0.2	29.05.2018	Schuberth	Added IFX toolbar section reworked “How to use DRC” section
1.0.3	31.05.2018	Schuberth	Reworked Module Design Release Procedures section and ADS Workspace/Library structure and naming convention
1.04	04.07.2018	Schuberth	Reworked ADS custom toolbar section , Module DRC Section, and Module Design Release Procedures
1.05	26.07.2018	Schuberth	Added software package section
1.06	18.11.2019	Pitton	Added installation procedure to appendix section
1.07	12.03.2020	Schuberth	Added die to die clearance rules
1.1	08.10.2020	Schuberth	Added Section “Using IFX SMT Library”

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG