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Requirements for Highly Integrated TX Frontend ICs for FR1 4G/5G TDD mMIMO systems “PAM 2.0+”

PRELIMINARY, subject to change

Otto Koch, Tilman Felgentreff, Janne Peltotupa

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Version 2.1

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Scope

- This is RFI stage.
- Nokia seeks for the long term (year 2020 onwards) cost and power optimized solution and partitioning for TX and RX frontend functions needed in 4G/5G TDD mMIMO systems.
- If several iterations are needed to get to the final functionality and integration level please indicate the timeline you need to fulfill complete functionality.
- This specification covers the version 2.0+ of the PAM (Power Amplifier Module).
- The PAM 3.0 specification from Sept 2019 will be updated and covered in a separate specification.
- Nokia would like to receive feedback from the vendor to the proposed partitioning, functionalities and requirements. Especially proposals related to power consumption reduction or cost optimization.
- Nokia would like to receive a price indication from the vendor.
- The Rx part is described in a separate specification, only shown in this presentation for completeness

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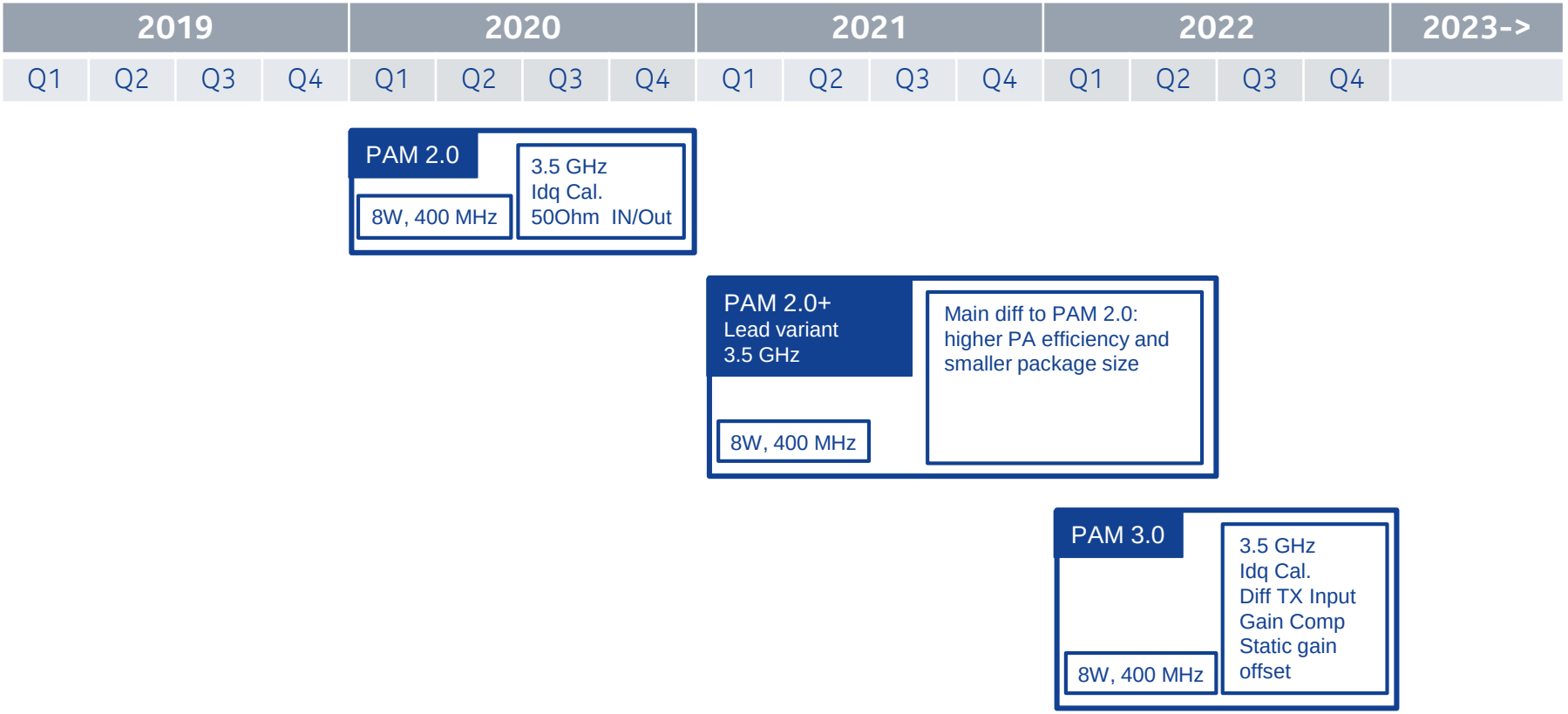
Nokia mMIMO PA module Roadmap

Left edge = First Sample
Right edge = Volume production



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Overview

- Highly integrated TX Frontend ICs for 4G/5G TDD mMIMO Systems
- Separate TX and RX Frontend ICs
  - Single Channel TX Frontend IC with 6W to 10W RMS output power (PAR 7.5dB)
- This concept is of interest for the frequency range from 2.3GHz to 5GHz
- Initial frequency bands of interest: 3.6GHz (Bands n77, n78). Priority Bands and Power Levels:

Frequency and iBW/oBW	Band	Pout	R&D Priority	Time line
3.4 GHz to 3.8GHz, 400MHz/200MHz iBW/oBW	includes B42/B43/B48/n77/ n48 partly n77	39dBm	RFI, Priority 1 (lead variant)	see slide 3
		40dBm	Priority 3	tbd.
		37.7dBm	Priority 3	tbd.
3.3 GHz to 3.6 GHz, 300MHz/200MHz iBW/oBW	sub-band n77/n78 includes B42/B52	39dBm	Priority 3	tbd.
2.3GHz to 2.690 GHz, 390MHz/200 iBW/oBW	includes B40/n40/n41/ n90/n38	39dBm	Priority 2	3 month later than lead variant
3.7 GHz to 4.2 GHz, 500MHz/200MHz iBW/oBW	sub-band n77	38dBm	Priority 2	3 month later than lead variant
4.4 GHz to 5.0 GHz, tbd/tdb iBW/oBW	band n79	39dBm	Priority 3	tbd.

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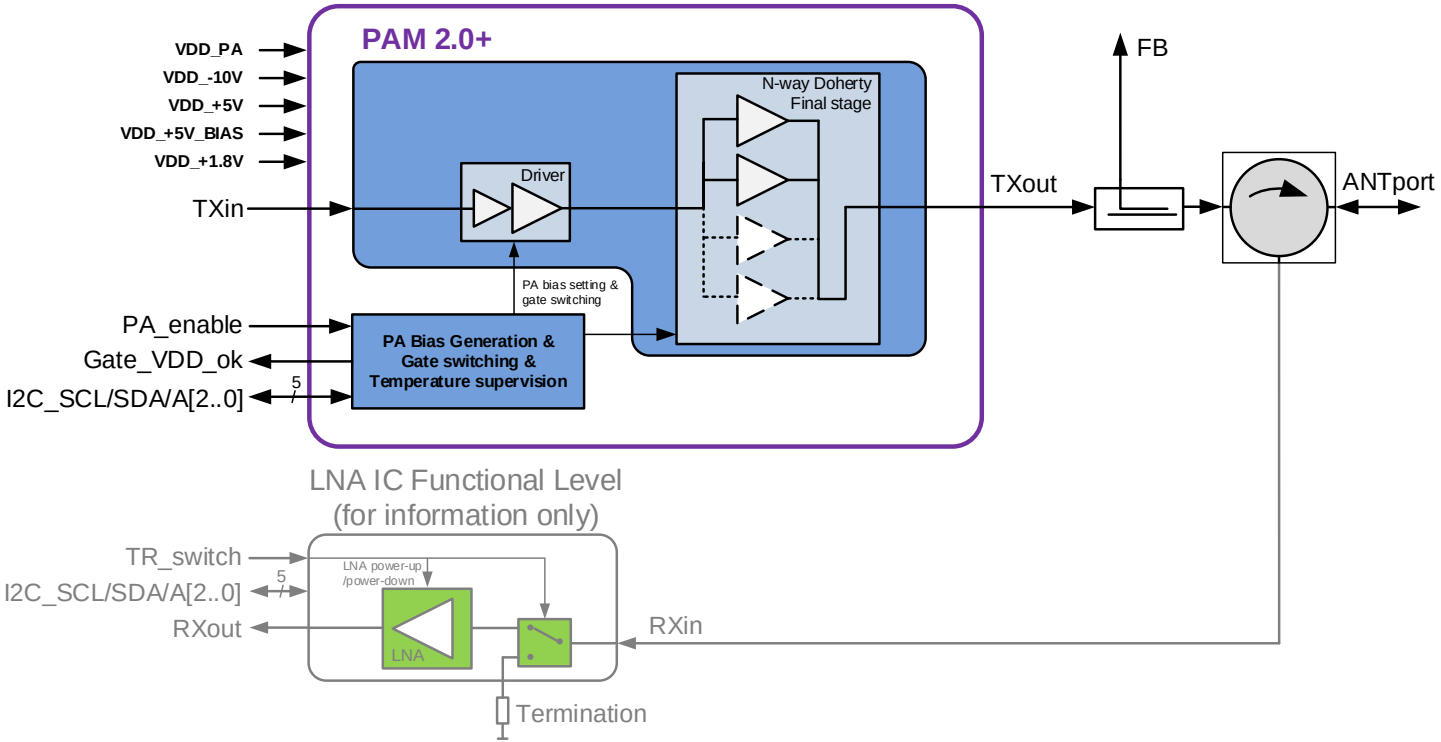
Block diagram of the proposed solution



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General requirements

- Optimized cost and power consumption for TDD mMIMO TX and RX frontend functionality
- IC or Multi-Chip Module (MCM)
- Surface-Mounted Technology (SMT) packages
- Digital control interface
- Integrated temperature sensor
- ICs are delivered fully adjusted and fully tested. Adjustment settings shall be stored inside the IC and shall be taken into use automatically after power-up.
- PAM simulation model (ADS preferred) should be provided by vendor.

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High-level TX Frontend IC requirements (1/2)

- Single channel TX Frontend IC with lineup gain of 29.5dB
- Integrated bias controller with digital control interface
  - Proposed control interface: I2C.
- Vendor calibrated quiescent currents (Idq):
  - Temperature Compensated Idq values.
  - Possibility to define temperature compensation by Nokia.
  - Possibility to set offsets to the calibration values via I2C
  - Possibility to read out temperature via I2C bus
- Possibility to turn on/off Idq of drivers and final stages within 1µs (µDTX) via dedicated control pin
- Gate Bias feedback pin for Gate Voltage which is supplied to Gate of the PA (GaN) transistor. Gate Voltage good signal, HIGH = ok, LOW = not ok. See also page “Interface signals”
- Vendor calibrated nominal gain
- Input and Output matched to 50 Ohm

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High-level TX Frontend IC requirements (2/2)

- Packaging concept prepared for up to 10W output power
  - Maximum Temperature 110°C at cooling interface
  - Vendor to report thermal resistance junction to case

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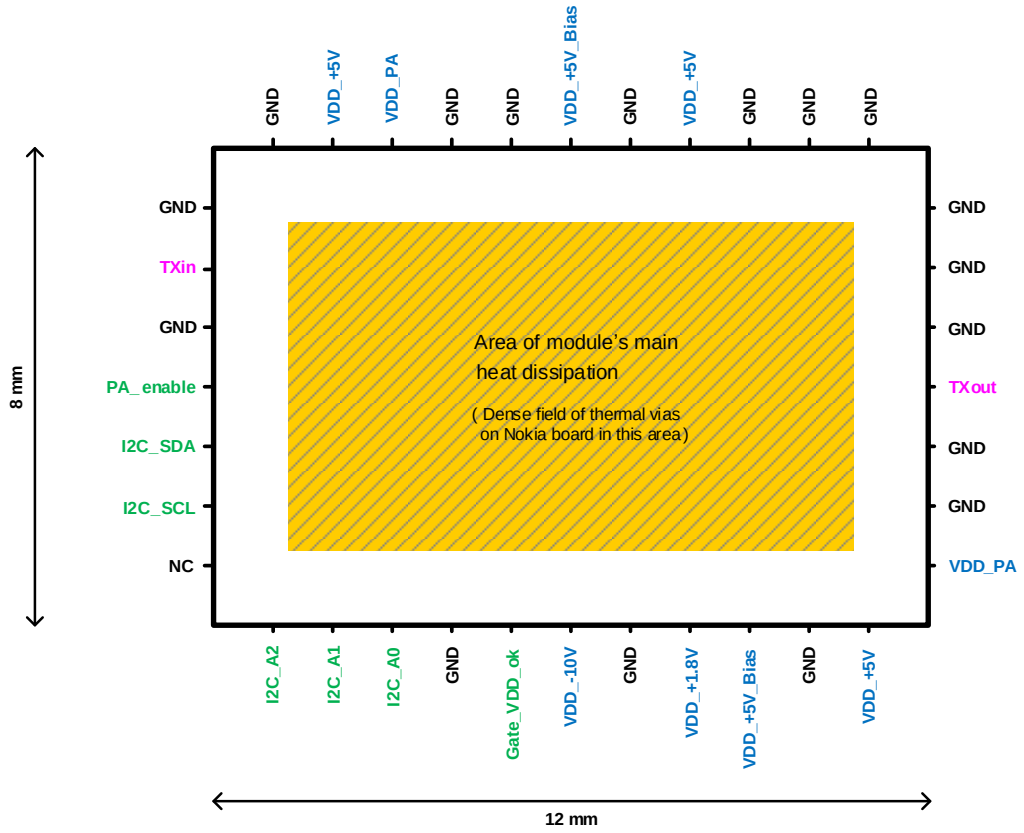
Pinning Geometry for PAM 2.0+ module



Drawing shows top view
All dimensions are in mm
Pins are on a 1 mm raster
Pad dimensions are not yet fixed

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PA module common requirements

Parameter	req.No.	Min	Max	Notes
Radio Application		4G/5G TDD mMIMO		with up to 100% DL dutycycle
Number of TRX in AAS system		16	64	information of use case
Operating temperature range	C 1.1.1	-10 °C	110 °C	Temperature at flange. All specifications must be fulfilled
Operable temperature range	C 1.1.2	-40 °C	120 °C	Temperature at flange. RF performance degradation is accepted @120°C 1dB back off from nominal Pout
	C 1.1.3		200 FITS	Failure rate at highest expected temperature. Assumes constant failure rate model
Supply voltages	C 1.2.1	1.8 V ± 0.15V		Permanently on, only for I2C
	C 1.2.2	5.0 V ± 5%		Permanently on
	C 1.2.3	5.0 V ± 5%		Permanently on. Only for biasing
	C 1.2.4	-10 V ± 5%		Permanently on.
	C 1.2.5	20V	50V	nominal (includes DVM), turned on for PA operation Device must be stable from 0 to Vdd max
Module length and width	C 1.3.1	10x8mm		Target
PA Module height	C 1.3.2		2 mm	
PA Module weight	C 1.3.3		25 g	
Package warpage	C 1.3.4		0.1 mm	JEDEC publication 95, Design Guide 4.25 (August 2016, Issue B)

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PA line up 3.6 GHz main requirements (1/2)

Parameter	req.No.	Min	Max	Notes
Frequency Range / Band	TX 1.0	3400 MHz	3800 MHz	RFBW (Radio Frequency bandwidth)
PAR	TX 1.1			7.5dB
Maximum Instantaneous BW	TX 1.2.1		400 MHz	
Maximum Occupied BW	TX 1.2.2		200MHz	
Pavg at TXout	TX 1.3.1	39dBm		TXout load impedance 50 Ohm RL ≥ 18 dB
P3dB at TXout (LTE or pulsed condition) referred to Pavg	TX 1.3.2	47.4 dBm		test signal modulated unclipped LTE signal
Gain @Pavg (39dBm)	TX 1.4.1	27.0 dB	32.0 dB	29.5 dB typical for ambient temperature Min/Max applies vs operating temperature and device to device variation. Note: In case of other output power or frequency variants for further future PAM, all PAM shall have the same nominal gain as well as same min/max gain.
Dynamic gain variation over 800MHz band	TX 1.4.2		2.0dB	@Pavg to -30dB back off Measured with LTE5, 10dB PAR
			3.0dB	Dynamic gain including gain expansion
Gain Flatness in 3400 - 3800 MHz	TX 1.4.3		1.5 dB	max. 1 dB within any 200MHz
Gain Flatness in 3200 - 4000 MHz	TX 1.4.4		3.0 dB	
raw ACLR	TX 1.5	-25 dB		LTE 20MHz 1C E-TM1.1, 7.5dB PAR @Pavg
ACLR with DPD	TX 1.6.1	-60dB		LTE 5MHz 1C E-TM1.1, 7.5dB PAR @Pavg
ACLR with DPD	TX 1.6.2	-50dB		2x100MHz blocks NR-FR1-TM1.1, 7.5dB PAR @Pavg 10xLTE20 carrier E-TM1.1 , 7.5dB PAR @Pavg
Module Efficiency @Pavg, 7.5dB PAR	TX 1.7	48%		Module efficiency will be measured by 100% TX phase. One LTE carrier 20MHz, E-TM1.1, 7.5dB PAR @Pavg

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PA line up 3.6 GHz main requirements (2/2)

Parameter	req.No.	Min	Max	Notes
Return Loss (TXin)	TX 1.9	16 dB		
VBW	TX 1.10	800 MHz		tested with Nokia DPD, no resonance in IM3 characteristic
AM-PM max @Pavg + PAR	TX 1.11		≤ 25 °	
max phase deviation inband @Pavg + PAR within iBW	TX 1.12		≤ 8°	
PA_enable, ON switching time, PA gain deviation from final value after 1 μs from trigger	TX 1.19.1		0.2 dB	1 µs after enabled the PA, reference level@2ms; @Pavg
PA_enable, OFF switching time, PA gain drop after 1 μs from trigger	TX 1.19.2	40 dB		gain drop 1 µs after disabled the PA
140μs PA_enable on/off cycle, PA gain variation	TX 1.19.3		+/- 0.25 dB	7kHz on/off switching frequency. Test signal single tone @Pavg Max gain variation 70μs after PA_enable_on vs. constant switched on gain
Idle Mode power consumption, TX mode, PA disabled	TX 1.20		20 mW	PA_enable = LOW => PA quiescent current off

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Interface signals

Name	Description	Specification	
TXin	TX signal from TX RF Driver stage.	Impedance 50Ω	
PA_enable	All PA related (=final stage, driver and pre-driver) power-up/down functionalities are derived from this signal. HIGH = PA quiescent current nominal, LOW = PA quiescent current off	1.8V LVCMOS acc. JESD8-7A normal range, 1.8V ± 0.15V. No pull-up/pull-down resistors inside PAM allowed. Input capacitance max. 5pF	
Gate_VDD_ok	Gate Voltage good signal, HIGH = ok, LOW = not ok	1.8V LVCMOS acc. JESD8-7A normal range, 1.8V ± 0.15V. No pull-up/pull-down resistors inside PAM allowed.	
I2C_SDA/I2C_SCL	I2C bus SDA signal (Data) / I2C bus SCL signal (Clock 400kHz)	1.8V LVCMOS acc. JESD8-7A normal range, 1.8V ± 0.15V. No pull-up/pull-down resistors inside PAM allowed.	
I2C_A[2..0]	I2C bus address pins	1.8V LVCMOS acc. JESD8-7A normal range, 1.8V ± 0.15V. Pull up required, except in case of I2C controller using n.c. for address coding like LMP92066	
TXout	TX to antenna	Impedance 50Ω	
VDD_PA	PA final (+driver) stage power supply. Turned on for PA operation, VDD_PA is switched on after all other VDD's.	Supported range is 20V ...50V	
VDD_-10V	-10V power supply. Permanently on.	± 5%	Note: PAM shall operate with any power-up sequence of VDD_-10V, VDD_+5V, VDD_+5V_BIAS, VDD_+1.8V
VDD_+5V_BIAS	5V power supply. Permanently on. Imax = 10mA	± 5%	
VDD_+5V	5V power supply. Permanently on. Imax = 250mA	± 5%	
VDD_+1.8V	1.8V power supply. Permanently on.	± 0.15V	

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Control Interface requirements: Basic

Name	req.No.	
Type		**I2C**
Speed		SCL: **400kHz**
Electrical Level		**1.8V** LVCMOS acc. JESD8-7A normal range, i.e 1.8V ± 0.15V
Input Capacitance		max. **10pF** per SCL, SDA,
Slave Base Address		**40h** decoding of 8 devices per bus via I2C address lines
VERSION Register (low level interface identification)	CI1.0	**1Fh** Value: high nibble=Vendor; low nibble=version For using LMP92066 value A1h and for AMC7904 value A3h is defined. For using other solutions following vendor coding has to be used: Vendor A : 2xh Vendor E : 6xh Vendor I : Bxh Vendor B : 3xh Vendor F : 7xh Vendor J : Cxh Vendor C : 4xh Vendor G : 8xh Vendor K : Dxh Vendor D : 5xh Vendor H : 9xh Vendor L : Exh

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Control Interface requirements: functional

Name	req.No.	
Module Type identification	CI1.1	**20 Byte of vendor pre programmed nonvolatile memory** Byte Address Offset 00h: Vendor Code: 1Byte (will be defined later) 01h: Unique module type number: 2Byte (for unique SW identification) 03h: Power: 1Byte (binary value in 1/10 Watt → 0.1 .. 25.5W) 04h: DL Frequency Range LOW edge 2Byte (binary in MHz: lower Address LSB – little endian) 06h: DL Frequency Range HIGH edge 2Byte (binary in MHz: lower Address LSB – little endian) 08h: Date Code: YEAR 1Byte (binary: year - 2000) 09h: Date Code: WEEK 1Byte (binary: week) 0Ah: Module Name 10Byte (ASCII Module name or/and serial Number)
Temperature sensor	CI1.2	-40°C .. 120°C, ±3.2°C error
Thermal compensation	CI1.3	Thermal compensation Iqd table (resolution, steps) will be agreed with Nokia. Vendor storing it to nonvolatile memory

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EVB requirements

Name	req.No.	
Max PCB area for PAM incl. Bias Controller and passives		10 mm x 22 mm (= module length and width requirements C 1.3.1 +2mm length and +10mm width); connectors can be placed outside this area
Bias Controller		If not already integrated then own bias controller or TI AMC7904
Mechanics		PCB mounted on a metal base plate (no cooling fins)
Power supply interface		Banana plug or jack (4 mm)
Control interface		Pin header, male, 2*5 pins, contact pitch: 2.54 mm. Mounted on EVB or as adapter Pin 1: PA_enable Pin 2: GND Pin 3: I2C_A0 Pin 4: I2C_SCL Pin 5: I2C_A1 Pin 6: I2C_SDA Pin 7: I2C_A2 Pin 8: GND Pin 9: GND Pin 10: Gate_VDD_ok
RF connectors		SMA or N
De-embedding data		PCB insertion loss from PAM TXout pin to EVB TX output connector

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Version history

Version	Content	Author	Date
2.0	First Version	Nokia	7th April 2020
2.1	Slide 4: - For band 2.3GHz to 2.690 GHz missing oBW value of 200MHz added, "*2.3GHz to 2.690 GHz, 390MHz/200MHz iBW/oBW*" - For For band 2.3GHz to 2.690 GHz "B40" was listed two times. Now corrected: "*includes B40/n40/~~B40~~/n41/n90/n38*" Slide 9: - Package size changed from "8mm x 10mm" to "8mm x 12mm" - Pinning updated Slide 11: - Parameter naming for TX1.2.1 and TX1.2.2 "Maximum Instantaneous BW /Occupied BW" corrected - Parameter naming "Module Efficiency" PAR corrected from 8dB to 7.5dB and notes "*LTE 20MHz 1C*" modified to "*one LTE carrier 20MHz*" Slide 13: - Parameter description for "TXin" updated to *"..from TX RF Driver stage...."*. Slide 16: - Max PCB area for PAM, width updated from 20mm to 22mm "*10 mm x 22 mm (= module length and width requirements C 1.3.1 +2mm length and +10mm width)*"	Nokia	23rd June 2020

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