A Load–Pull Characterization Technique Accounting for Harmonic Tuning

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***Abstract*—A novel methodology for the characterization of the nonlinear dynamic behavior of electron devices (EDs) is presented. It is based on a complete and accurate ED characterization that is provided by large-signal low-frequency *I/V* measurements, performed by means of a low-cost setup, in conjunction with any model-based description of the nonlinear reactive effects related to ED capacitances. The unique feature of the proposed technique is that a fully harmonic control of waveforms at the current generator plane is achieved, and as a consequence, high-efficiency operation can be simply investigated. Different experimental data are presented on GaAs and GaN transistors, and to definitely verify the capability of the new approach, the design of a class-F GaN power amplifier is deeply investigated as a case study.**

***Index Terms*—Field-effect transistor (FET), harmonic tuning, integrated circuit measurements, microwave amplifier, nonlinear modeling, semiconductor device measurements.**

I. Introduction

OVER THE last years, the theory on high-efficiency power amplifier (PA) operating classes has been widely dealt with and detailed, definitely demonstrating that harmonic tuning is needed to correctly design high-efficiency PAs [1]–[4]. Therefore, harmonic tuning strategies have been widely used by PA designers for this purpose (e.g., [5]–[10]). Accordingly with the theoretical formulation of harmonically tuned PA classes, well-defined current and voltage waveforms have to be synthesized at the current generator plane (CGP) [1], [2], [11]. As an example, for class-F PAs, short- and open-circuit harmonic terminations are required at the device CGP in order to obtain the square-shaped voltage and half-rectified current waveforms, which lead to high-efficiency operation.

From a practical point of view, designers can exploit two different approaches to PA design: computer-aided design (CAD) simulations or load–pull measurements. Obviously, both present strong and weak points.

In particular, when simulation-based approaches are used, the waveforms are available both at the CGP and extrinsic plane (EP) at the design frequency. The drawback is that an accurate prediction of these variables requires an accurate electron-device (ED) nonlinear model. However, due to the presence of low-frequency (LF) dispersive phenomena related to charge trapping and thermal effects [12]–[15], the identification of an accurate and global ED model is still an open research issue. Limits in model accuracy may lead to underestimation/overestimation of PA performance.

On the other hand, experimental characterization using high-frequency (HF) measurement setups [16], [17] allows to know the ED response under actual operating condition at the design frequency, in terms of source and load impedances, but no information on the CGP waveforms is provided. In fact, load–pull measurements carried out at microwave frequencies [8], [18], [19] are not able to settle the desired impedance termination at the CGP. The only way to obtain information on CGP operation, starting from HF measurements, is to exploit a time-domain load–pull setup and then perform a nonlinear de-embedding of the experimental EP data [20], [21]. Moreover, when harmonic tuning has to be applied, several measurement iterations are needed to obtain optimal conditions at fundamental frequency and harmonics [8], [18]. Finally, the cost and complexity of such a kind of setup become critical, especially when frequency and power levels increase.

The aim of this paper is to discuss a novel alternative characterization technique for high-efficiency PA design that allows to achieve a tradeoff between the previously described approaches combining the qualities of both. Starting from the preliminary results in [22] and [23] for single-tone excitation, in this paper the theoretical background is fully detailed considering also the extension to the multi-tone excitation case. In particular, for the first time the proposed approach is exploited to draw load–pull contours at microwave frequencies controlling harmonic terminations at the CGP.

This paper is organized as follows. In Section II, commonly adopted strategies for the characterization of EDs are briefly recalled and the proposed characterization method is introduced. In Section III, some modeling concepts are presented to better understand how the proposed approach supplies the information required for the design phase. Finally, in Section IV, experimental results are provided both for 0.15-μm GaAs pseudomorphic HEMT (pHEMT) and 0.25-μm GaN HEMT devices. The design of a class-F PA, realized in GaN technology, will be also discussed as further validation.

II. Transistor Characterization for High-Efficiency PA Design (Harmonic Tuning)

In the context of nonlinear transistor characterization, different HF passive/active load–pull setups have been developed and successfully exploited for PA design [8], [16]–[19]. All

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these systems are able to characterize an ED at the design frequency in terms of output power, efficiency, and other indicators commonly adopted to evaluate transistor performance. Time-domain setups [(e.g., large signal network analyzer (LSNA)] give also additional information about the current and voltage waveforms at the EP of the ED. Nevertheless, none of these systems is actually able to force the desired loading condition at the CGP because of the contribution of nonlinear dynamic effects appearing with the increase of frequency. Moreover, when harmonic control is needed and high power levels have to be managed, these systems can become complex and expensive. As an example, when considering class-F/F^{-1}/J operation, an active load–pull setup [24] needs to control at least three harmonic terminations, which implies a number of active loops equal to four! Moreover, the research of the optimum impedance has to be carried out not only at the fundamental frequency, but also at harmonics. This means, as reported in the literature [3], [18], that it takes many measurements and long and tedious iterations since, at microwave frequencies, it is not possible to directly set the impedance at the CGP. If it would be possible, the theoretical formulation of the different PA classes of operation [1]–[3] clearly indicates the impedance values to be synthesized at the harmonics (e.g., short and open for class-F) and only load–pull at the fundamental frequency would be needed (i.e., the same measurement effort required for class-A amplifier design).

In this paper, a novel transistor characterization strategy is presented for high-efficiency PA design based on a harmonic time-domain load–pull measurement system working at LF. The proposed approach provides direct information on waveforms at the CGP by forcing arbitrary terminations at fundamental and harmonics. The "trick" is to carry out large-signal measurements at LF where parasitic and nonlinear dynamic phenomena are negligible [11]. As will be shown in the following, this characterization, jointly with a model-based description of transistor nonlinear dynamic effects, provides complete and accurate information on large-signal performance at the required operating frequency.

The accuracy of the HF prediction is strictly related to the quality of the capacitive-core model, whose identification techniques are furthermore widely exploited in the literature and usually accurate enough. It must be highlighted that any reasonable capacitive core model (e.g., look-up table, analytic- or foundry-based models) can be used for that purpose.

The adoption of LF large-signal measurements allows to easily manage the instrumentation setup since, at LF, power management and cost are not an issue. The block diagram of the exploited setup is shown in Fig. 1.

It is based on multi-harmonic excitations [25]: a 2-MHz fundamental frequency is conveniently adopted in order to operate above the cutoff of the LF dispersive effects [12]–[15] and to completely neglect the reactive phenomena of ED. Such a setup, composed of general-purpose and commercial low-cost instrumentation, operates as a LF multi-harmonic active load–pull system: by controlling gate and drain incident waveforms and their relative phase, different load terminations can be arbitrary synthesized at the fundamental frequency and its harmonics for given bias conditions. In particular, the function generator has two 50-Ω channels that can independently provide arbitrary

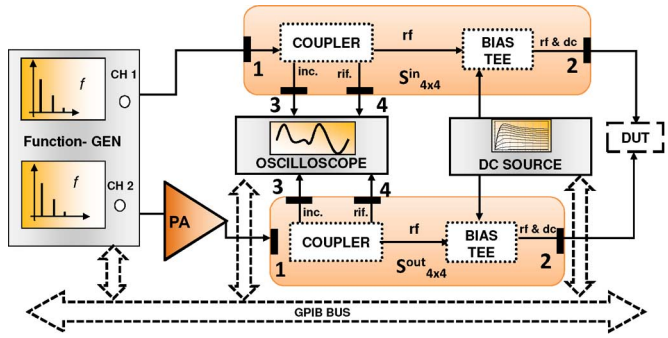

Fig. 1. Block diagram of the adopted measurement system. From [25].

waveforms in the frequency range (1 mHz–120 MHz). To overcome power limitation, a 30-W PA is cascaded to the device output port excitation. Two wideband (10 kHz–400 MHz) dual directional couplers monitor the DUT incident and reflected waves, which are acquired by means of a four-channel digital oscilloscope (4 GSa/s). A high-resolution (4 μV; 20 fA) and accurate (V: 0.05%, I: 0.2%) dc source provides the bias for the device-under-test (DUT). To ensure dc and RF path isolation, two wideband (200 kHz–12 GHz) bias-tees are used. In the selected frequency range, all the measurement setup components satisfy linear nondistortion conditions. This greatly simplifies the setup calibration procedure, which practically consists in the experimental characterization of the two four-port networks ($S^{\rm in}_{4\times4}$ and $S^{\rm out}_{4\times4}$) shown in Fig. 1. The characterization can be carried out by simply exploiting an LF VNA.

The measurement setup is fully controlled via an IEEE488 standard interface by means of a commercial instrument automation software running on a PC (i.e., NI LabVIEW). The user can set a grid of impedances at the fundamental frequency, and after setting the harmonic terminations, carry out measurements for different input power levels. To guarantee safe operating conditions, the control software allows to set *compliances* both on average values and instantaneous values. The former are maximum gate and drain average currents in dc and ac operation. The latter are maximum incident gate and drain signals and maximum gate–drain dynamic voltage. This setting is very useful when high-field reliability constraints have to be accounted for [26], [27].

The control software has been improved with respect to preliminary works [22], [23] published by the authors where only the fundamental control was implemented. Fig. 2 shows the impedance grid measured for a 600-μm periphery 0.15-μm GaAs pHEMT device biased under class AB at $V_{d0} = 6$ V, $I_{d0} = 20$ mA. The impedance grid is set out with the condition that for each impedance synthesized at the fundamental frequency, represented by empty squares in Fig. 2, short and open loading conditions are synthesized, respectively, at the second and third harmonics. It must be emphasized that the condition of Fig. 2 is obtained at the CGP: impedances at harmonics are fixed by the theoretical analysis of the specific class of operation considered [1]–[3], and load–pull has to be carried out only at the fundamental frequency. Moreover, for all the synthesized impedances, current and voltage waveforms (i.e., $[i(t)]^r$ and $[v(t)]^i$) at the input and output ports are acquired,

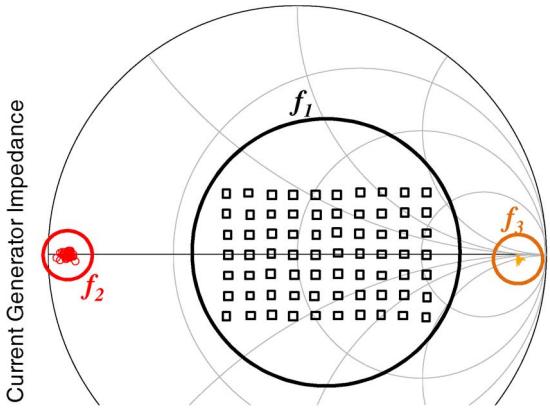

Fig. 2. Grid of impedances measured at 2 MHz for 600-μm periphery 0.15-μm GaAs pHEMT biased at $V_{d0} = 6$ V, $I_{d0} = 20$ mA. For each impedance synthesized at the fundamental frequency f_1 (squares), the second harmonic f_2 is a short circuit (circles) and the third (f_3) is an open circuit (dots).

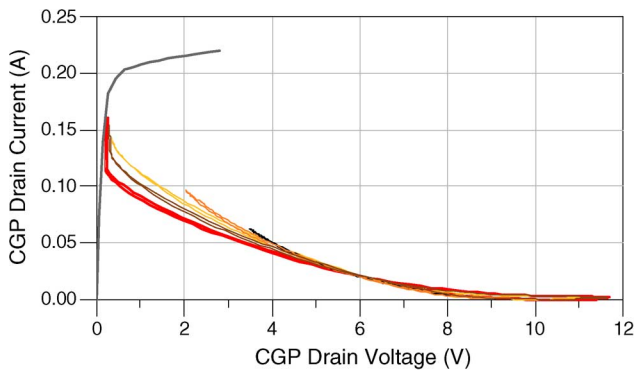

Fig. 3. Measurements at the CGP for the fundamental load impedance $Z = 83.5\ \Omega$ as a function of increasing input power performed on 600-μm periphery 0.15-μm GaAs pHEMT biased at $V_{d0} = 6$ V, $I_{d0} = 20$ mA. The load-lines are superimposed to dc characteristic at $V_{\rm gs} = 0$ V.

and consequently, load-lines at the CGP are directly available. In this way, the optimal *I/V* load-line satisfying the theoretical requirements associated to the selected amplifier class of operation can be simply identified.

As an example, Fig. 3 shows the load-lines synthesized for one impedance of the grid in Fig. 2.

As can be seen, it is a typical class-F shaped load-line. Once the characterization phase is concluded, the measurements can be elaborated in order to obtain the information at the EP needed for drawing load–pull contours at the design frequency. This step is fully detailed in Section III.

III. From "Intrinsic" to "Extrinsic"

In order to fully understand how the LF characterization (i.e., ED current generator electrical variables) leads to the HF information (i.e., ED extrinsic electrical variables) some modeling concepts have to be recalled. The nonlinear model of a field-effect transistor (FET) device can be considered composed of three parts: the linear extrinsic parasitic network and the intrinsic *capacitive* and *resistive cores*, [11], as shown in Fig. 4.

The linear extrinsic parasitic network describes the access passive structure to the device active area and accounts for metallization and dielectric losses as well as for associated inductive and capacitive effects. Its correct modeling is fundamental

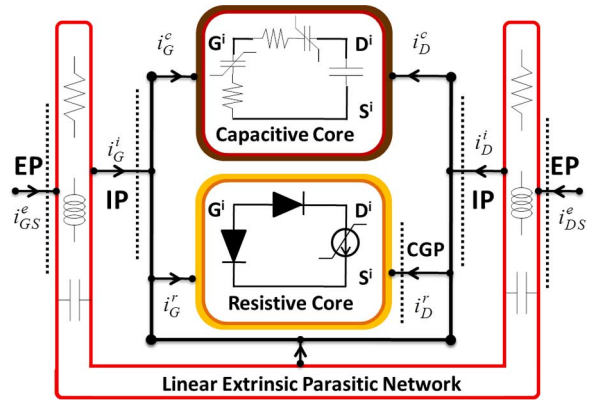

Fig. 4. FET model topology.

to obtain accurate model predictions. Parasitic elements can be identified by exploiting well-assessed techniques based on conventional lumped descriptions [28], [29], or alternatively, by adopting electromagnetic simulations of the device layout [30]. The "intrinsic device" is divided in two parts connected in parallel: a *capacitive core*, describing the nonlinear dynamic phenomena and a *resistive core*, accounting for the dc and LF *I/V* device characteristics. The latter ones differ from the dc response due to surface state densities, deep-level traps, and thermal phenomena [12]–[15].

Due to such phenomena and important nonlinear effects, obtaining an accurate and global ED model for the resistive core is a hard task and limited model accuracy may lead to underestimated/overestimated PA performance. The aim of our procedure is to avoid the modeling of the resistive core and to exploit its direct characterization, thus improving accuracy.

Once all the load impedances have been synthesized under LF operation, the vectors of the measured currents at input and output ports $[i(k\omega_{\rm LF})]^r$ (where k represents the harmonic index) completely describe the device *resistive-core currents* in the frequency domain. Through the de-embedding of resistive parasitic elements, the vector $[v(k\omega_{\rm LF})]^i$ of the *intrinsic voltages* at input and output port can be easily obtained. It is worth noticing that the resistive-core contribution is actually frequency independent. As a consequence, considering at the design frequency the vector of the voltage phasors $[v(k\omega_{\rm RF})]^i = [v(k\omega_{\rm LF})]^i$, the phasors of the resistive-core currents are identical to the ones measured under LF operation (i.e., $[i(k\omega_{\rm RF})]^r = [i(k\omega_{\rm LF})]^r$).

The *capacitive-core* elements can be identified by means of bias-dependent S-parameter measurements [31], [32]. In practice, the ED nonlinear capacitances are less affected by thermal and LF dispersion phenomena and their identification on the basis of small-signal, bias-, and frequency-dependent S-parameters is usually accurate enough. A π-model of capacitors (usually assuming $C_{\rm gs}$ and $C_{\rm gd}$ nonlinearly dependent on the intrinsic device voltages, and $C_{\rm ds}$ constant) is often adopted. Better prediction can be obtained at higher frequencies by introducing gate–source and gate–drain *RC* series, as shown in Fig. 4, to describe nonquasi-static effects, which accounts for a finite device memory time. Other nonquasi-static phenomena can be described in terms of trans-capacitances or delay times.

Nevertheless, the procedures described in the following can be applied whichever approach is adopted for the capacitive-core description. Alternatively, a model of device capacitances provided by the foundry can be adopted. It must be outlined that, as far as the capacitance model is considered, our approach provides the same accuracy of nonlinear modeling approaches, but a major advantage derives from the direct measurement of the resistive-core behavior.

Once the characterization of device capacitances is done, given the amplifier design frequency, the vector $[v(k\omega_{\rm RF})]^i$ of the intrinsic voltages can be applied to the capacitive-part description in order to achieve the device *capacitive-core currents* $[i(k\omega_{\rm RF})]^c$. To this end, the current contributions related to the ED capacitive core have to be evaluated according to the following explicit equations:

$$[i(t)]^c = \left[\sum_{k=-M}^{M} [i(k\omega_{\rm RF})]^c\, e^{jk\omega_{\rm RF}t}\right] = \sum_{k=-M}^{M} jk\omega_{\rm RF}\underline{C}\left([v(t)]^i\right)[v(k\omega_{\rm RF})]^i\, e^{jk\omega_{\rm RF}t} \quad (1)$$

where the time-domain intrinsic voltage vector can be expressed by

$$[v(t)]^i = \sum_{k=-M}^{M} [v(k\omega_{\rm RF})]^i\, e^{jk\omega_{\rm RF}t}. \quad (2)$$

The capacitance matrix $\underline{C}$ in (1) can be identified on the basis of frequency- and bias-dependent S-parameter measurements. Alternatively, the capacitive core of a suitable already available (e.g., by foundry) nonlinear model can be used. It must be outlined that when HF nonquasi-static effects are not negligible, the displacement currents cannot be explicitly evaluated in terms of a capacitance matrix only as in (1), but nonlinear circuit analysis is required. To this end, any frequency- or time-domain available CAD environment can be easily exploited.

The vector $[i(k\omega_{\rm RF})]^i$ of the total intrinsic currents (*resistive-core currents* plus *capacitive-core currents*) can be simply calculated by

$$[i(k\omega_{\rm RF})]^i = [i(k\omega_{\rm RF})]^r + [i(k\omega_{\rm RF})]^c, \qquad k = -M, \ldots, M \quad (3)$$

and, since all the electrical variables at the intrinsic device are known, the extrinsic electrical variables $[v(k\omega_{\rm RF})]^e$ and $[i(k\omega_{\rm RF})]^e$ can be obtained exploiting the four-port parasitic network description $H(\omega)$

$$\begin{Bmatrix} [v(k\omega_{\rm RF})]^e \\ [i(k\omega_{\rm RF})]^e \end{Bmatrix} = \underline{H}(k\omega_{\rm RF}) \begin{Bmatrix} [v(k\omega_{\rm RF})]^i \\ [i(k\omega_{\rm RF})]^i \end{Bmatrix}, \qquad k = -M, \ldots, M. \quad (4)$$

Once the extrinsic electrical variables are known, the load impedance at the fundamental and harmonic frequencies can be obtained,

$$Z_l(k\omega_{\rm RF}) = -\frac{v^e_{\rm DS}(k\omega_{\rm RF})}{i^e_{\rm DS}(k\omega_{\rm RF})}. \quad (5)$$

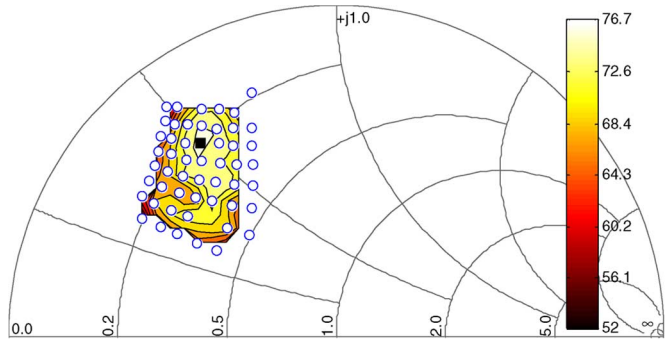

Fig. 5. Grid of impedances at the fundamental frequency of 20 GHz (circles) and constant efficiency contours at constant maximum gate–drain voltage $V_{\rm GD} = -13.5$ V, obtained from the LF measurement grid in Fig. 2 for a 600-μm periphery 0.15-μm GaAs pHEMT device biased at $V_{d0} = 6$ V, $I_{d0} = 20$ mA.

In addition, the device input "large-signal impedance" can also be easily computed,

$$Z_{\rm in}(k\omega_{\rm RF}) = \frac{v^e_{\rm GS}(k\omega_{\rm RF})}{i^e_{\rm GS}(k\omega_{\rm RF})} \quad (6)$$

which, for instance, can be used to synthesize the optimum source impedance (e.g., $Z_s = {\rm conj}(Z_{\rm in})$) providing a matching condition under large-signal operation.

The direct control of time-domain voltage and current waveforms, referred to the ED CGP, represents one of the most effective approaches for maximizing the efficiency of a PA. The data obtained by means of the proposed approach provide information on output power, efficiency, gain, etc., and can be exploited to draw contour plots and find the optimum condition. Fig. 5 shows, as an example, the grid of impedances resulting at the fundamental frequency of 20 GHz from the exploitation of the LF measurements in Fig. 2. Constant efficiency contour at constant maximum gate–drain voltage $V_{\rm GD} = -13.5$ V are also reported.

Fig. 6 shows the 20-GHz EP load-lines corresponding to the CGP load impedance in Fig. 3. As can be seen, the EP loci are very different from the CGP ones, and as a consequence, it is not immediate to understand that they correspond to high-efficiency operation.

An important capability of the proposed method is that, once the LF characterization is carried out, variables can be computed at any frequency of interest by simply reapplying the computational procedure that takes from the intrinsic to EP, without any additional measurement. In fact, only the computations related to the capacitive-core and parasitic-network models are required since, by definition, the intrinsic resistive core response is frequency independent. This is a useful feature for example when designing wideband PAs. In particular, broadband fundamental and harmonic terminations that guarantee the same measured intrinsic resistive-core *I/V* load-line can be gathered by reapplying, in the band of interest, the procedure previously described.

IV. Experimental Results

The proposed approach has been initially validated through the comparison with 20-GHz measurements carried out on a

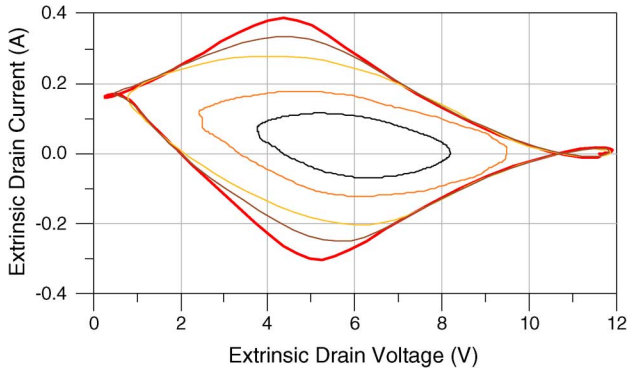

Fig. 6. EP load-lines at the design frequency of 20 GHz, corresponding to the CGP load lines reported in Fig. 3 for a 600-μm periphery 0.15-μm GaAs pHEMT device biased at $V_{d0} = 6$ V, $I_{d0} = 20$ mA.

GaAs pHEMT by means of a passive load–pull system [16]. Such a comparison is carried out only at the fundamental frequency since harmonic load–pull systems are not able to set the desired harmonic terminations at the CGP so it is not possible to rigorously compare the results between the two methods. Finally, the described technique has been successively exploited to design and prototype a 2.4-GHz GaN Class-F PA.

The first validation is presented on a 600-μm periphery 0.15-μm GaAs pHEMT biased under class AB ($V_{g0} = -0.6$ V, $V_{d0} = 6$ V, $I_{d0} = 74$ mA). LF load–pull characterization has been carried out on a grid of 63 loads in order to find the maximum output power at 20 GHz. Fig. 7 shows 1-dB gain compression output power contours predicted on the basis of LF measurements and the ones measured by means of a 4–26.5-GHz passive load–pull system [16]. The optimal output impedance at 20 GHz, found through the proposed approach, is $Z_l = 29.5 + j^*18\ \Omega$, which corresponds to 347-mW (25.4 dBm) output power and 55% drain efficiency. The corresponding values obtained by means of HF load–pull measurements are $Z_l = 29.2 + j^*18.4\ \Omega$, maximum output power 363 mW (25.6 dBm) and drain efficiency 51%.

The fair agreement confirms the validity of the proposed characterization strategy.

The second validation concerns the design of a class-F PA based on a discrete 1.25-mm periphery 0.25-μm GaN on SiC HEMT, whose main foundry specifications are summarized in Table I.

The GaN HEMT was biased under class-AB condition ($V_{g0} = -3.9$ V, $V_{d0} = 32$ V, $I_{d0} = 10$ mA), and accordingly with the proposed approach, an LF load–pull characterization of the device intrinsic resistive core was carried out. To this end, by exploiting the harmonic active load–pull setup of Fig. 1, the 2-MHz impedances shown in Fig. 8 were synthesized. For each of the 30 impedances synthesized at the fundamental frequency, the second harmonic impedance was settled to be a short circuit and the third one to be a high-impedance termination. All the experimentally synthesized impedances perfectly match with class-F theoretical formulation [1]–[3].

Once the LF characterization phase was concluded, all information in terms of output power, drain efficiency, maximum gate–drain voltage, etc., was available and LF load–pull contours were drawn to evaluate the device performance. The

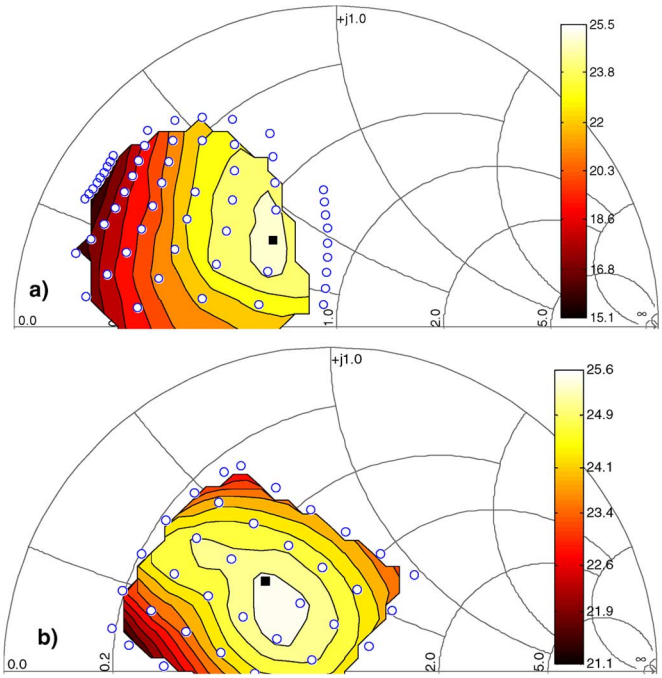

Fig. 7. Constant output power contours at 1-dB transducer power gain compression predicted by (a) exploiting the proposed approach and by (b) load–pull measurements at 20 GHz for a 600-μm periphery 0.15-μm GaAs pHEMT device biased at $V_{d0} = 6$ V, $I_{d0} = 74$ mA.

TABLE I
0.25-μm GaN HEMT TECHNOLOGY SPECIFICATIONS

Quantity	*Value*
Breakdown Voltage	-70 V
Pinch-off Voltage	-4 V
I_{dss}	1 A/mm
Saturated Output Power	5 W/mm

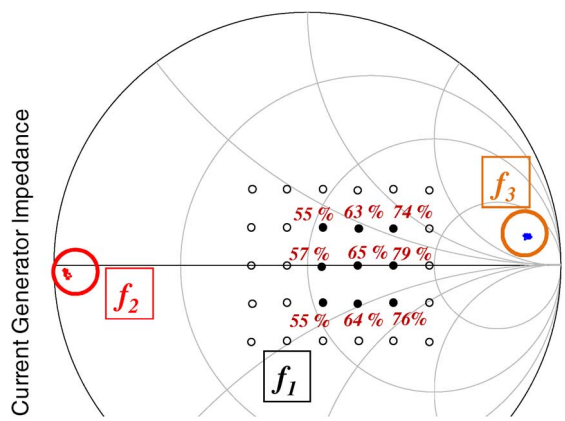

Fig. 8. Grid of impedances measured at fundamental frequency of 2 MHz (circles) for 1.25-mm periphery 0.25-μm GaN HEMT biased at $V_{d0} = 32$ V, $I_{d0} = 10$ mA. Impedances corresponding to an output power level of at least 5 W (filled circles) and corresponding efficiency values.

design target was to obtain the maximum power for the selected device (1.25-mm periphery) with the maximum efficiency achievable: 5 W (~37 dBm) has been considered a reasonable target for the output power. Efficiency values for the selected output power level are shown in Fig. 8.

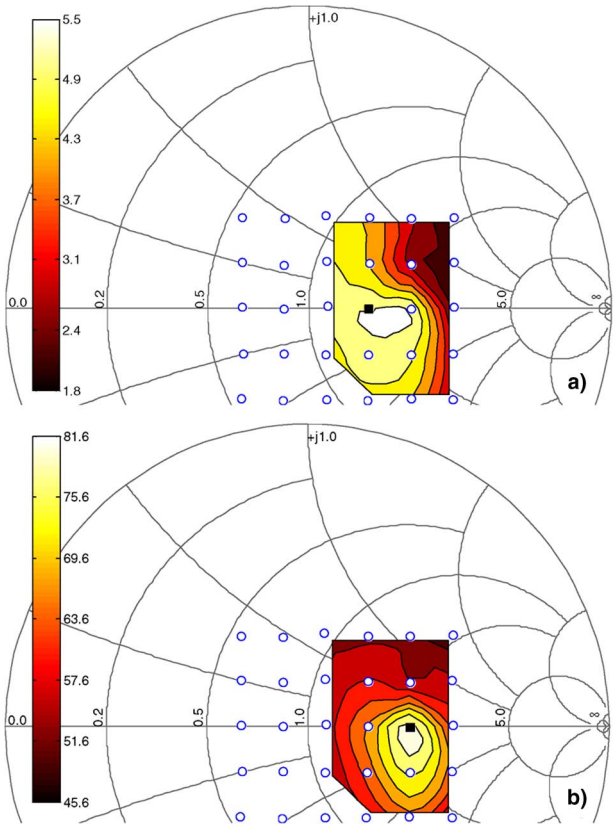

Fig. 9. (a) Constant output power and (b) efficiency contours at constant maximum gate–drain voltage $V_{\rm GD} = -69$ V. Measurements carried out at 2 MHz for 1.25-mm periphery 0.25-μm GaN HEMT biased at $V_{d0} = 32$ V, $I_{d0} = 10$ mA.

TABLE II
MEASURED LF DRAIN IMPEDANCES

Frequency [MHz]	*CGP load impedance [Ω]*
2	103 - j 0.4
4	0.3 + j 0.1
6	344 + j 515

It should be pointed out that only nine impedances get the target. The reason is essentially related to reliability constraints since, for the remaining impedances, the compliances related to the maximum gate–source or gate–drain voltage are reached. In order to clarify this important aspect, Fig. 9 shows the output power and efficiency contours for the fixed maximum $V_{\rm GD}$ value of -69 V (value close to the breakdown voltage in Table I). In Fig. 9(a), it can be noticed that the maximum 5.5-W output power, corresponding to a 68.4% drain efficiency, is achieved at $Z^P_{l,\rm CGP} = 75\ \Omega$, whereas from Fig. 9(b), the optimal efficiency condition (81.6%) is found at $Z^E_{l,\rm CGP} = 103 - j0.4\ \Omega$, which corresponds to 5.4-W output power. Since the target is to maximize the efficiency obtaining as much power as possible, $Z^E_{l,\rm CGP}$ has been chosen for the design phase. The optimum impedances at the fundamental and harmonics are reported in Table II. As can be seen, short and open circuits are synthesized at the second and third harmonic, respectively.

Fig. 10 shows the trajectories of the load-line synthesized at the ED intrinsic resistive core as a function of the input power

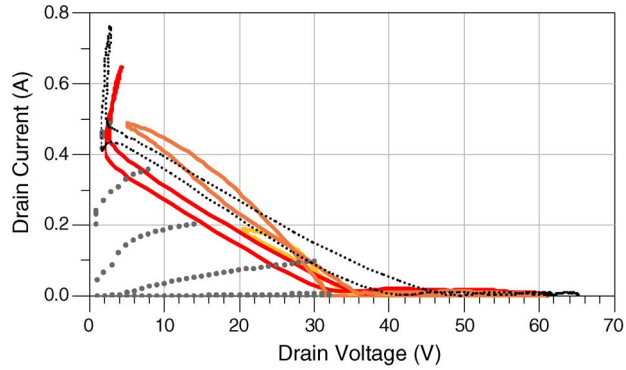

Fig. 10. LF measurements (solid line) for the load impedance $Z_l = 103 - j^*0.4\ \Omega$ as a function of increasing input power under class-F operation performed on a 1.25-mm periphery 0.25-μm GaN HEMT biased at $V_{d0} = 32$ V, $I_{d0} = 10$ mA. The load-lines are superimposed to dc characteristics ($V_{\rm gs}$ swept from -5- to 0-V step 0.5 V). The simulated load-line provided by the foundry model, which overestimates device performance, is also drawn (dotted line).

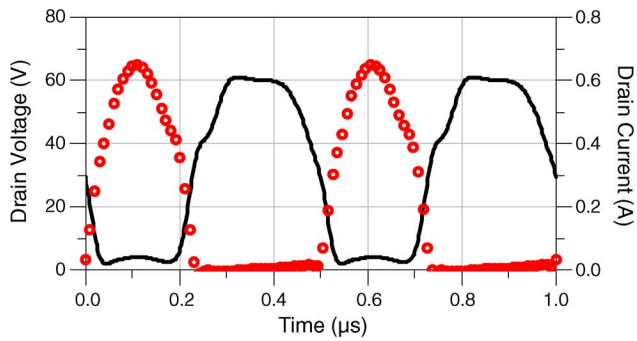

Fig. 11. LF time-domain voltage (solid line) and current (symbols) waveforms at the device CGP for the highest value of input power, corresponding to the synthesized class-F operating mode (loading condition of Table II) performed on 1.25-mm periphery 0.25-μm GaN HEMT biased at $V_{d0} = 32$ V, $I_{d0} = 10$ mA.

sweep. The measured load-line for the highest value of input power was compared with the one obtained by exploiting the foundry model, which predicts 6.9-W output power with a drain efficiency of 90% (dotted line in Fig. 10). This simulation was performed under the same condition of the LF measurement. It is very evident the poor predictive capability of the foundry resistive-core model, which is usually tailored for class-A or class-AB design. As previously said, thermal and trapping phenomena make the identification of a global and accurate model for the current generator [12]–[15] very difficult. Fig. 11 shows the measured LF time-domain voltage and current waveforms referred to the CGP: it is very evident that such electrical variables satisfy the minimal-overlapping condition imposed by class-F operation.

It is worth outlining that the resistive core performance in terms of output power and drain efficiency also determines the performance at microwave frequency. Therefore, in accordance with the proposed design methodology, the obtained LF electrical variables corresponding to each termination of the grid in Fig. 8 were elaborated in order to obtain the behavior of the selected class-F operating mode at the design frequency of 2.4 GHz. More precisely, the foundry model (EE_FET3 [33]) has been exploited for both the capacitive core and the linear extrinsic parasitic network behavior.

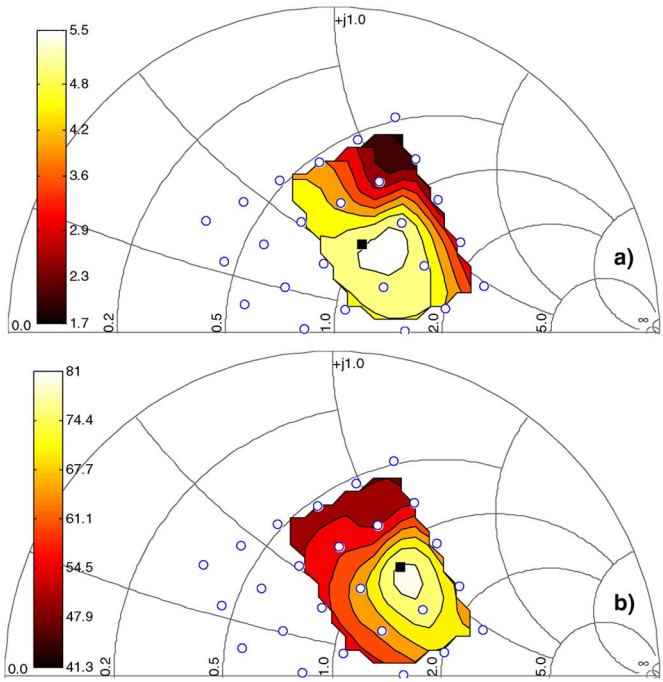

Fig. 12. Grid of impedances at the fundamental frequency of 2.4 GHz obtained from the measurement grid in Fig. 8 for a 1.25-mm periphery 0.25-μm GaN HEMT (circles) biased at $V_{d0} = 32$ V, $I_{d0} = 10$ mA. (a) Constant efficiency contours for 5-W output power. (b) Constant efficiency contours for the maximum gate–drain voltage $V_{\rm GD} = -69$ V.

Fig. 12 shows the grid of impedances at the fundamental frequency of 2.4 GHz, resulting from the computation of the LF grid reported in Fig. 8.

At this point, all the information in terms of output power, efficiency, PAE, gain, etc. is available at the design frequency of 2.4 GHz and can be conveniently exploited to find the optimal impedance.

As shown for the CGP measurements ($f_1 = 2$ MHz), Fig. 12 also reports output power and drain efficiency contours for the fixed $V_{\rm GD}$ value of -69 V. In Fig. 12(a), a maximum output power of 5.5 W and a corresponding 68% drain efficiency are achieved at $Z^P_{l,\rm EP} = 50.6 + j^*29.9\ \Omega$, whereas from Fig. 12(b), the optimal efficiency condition is found at $Z^E_{l,\rm EP} = 57 + j^*45.4\ \Omega$, which corresponds to 81% drain efficiency and 5.4-W output power. It is evident that the impedance providing the best efficiency for this application is represented by the value $Z^E_{l,\rm EP}$, which will be synthesized with the PA output matching network (OMN). It should be pointed out that the optimal impedance $Z^E_{l,\rm EP}$ found at the design frequency is the $Z^E_{l,\rm CGP}$ after elaboration from "intrinsic" to "extrinsic" (Section III). The procedure is applied to the whole impedance grid in order to draw Class-F contours at 2.4 GHz.

Table III shows the optimum extrinsic load terminations at the frequency of 2.4 GHz compared to the CGP terminations. It must be outlined that information on the CGP impedance values is not directly deducible from the extrinsic data. As an example, the obtained third harmonic high-impedance condition at the intrinsic device, typical of class-F operating mode, is not easily evincible from its extrinsic value. This is the reason why large-signal measurements carried out at the design frequency cannot give useful information at the CGP, unless a rigorous nonlinear de-embedding procedure is adopted [20], [21].

Moreover, as clearly shown in Fig. 13, by observing extrinsic voltage and current time-domain waveforms at the design frequency of 2.4 GHz, it is very difficult to assert that the GaN HEMT is working in class-F operation, whereas this is very evident by looking at the same electrical variables referred to the CGP (Fig. 11).

Successively, the electrical variables corresponding to the optimum loading condition at the CGP have been computed in the frequency range of 2.3–2.5 GHz. Fig. 14 shows the trajectories of the fundamental, second, and third harmonic input (a) and output (b) impedances in this frequency range. Fig. 14 also shows the value of terminations to be synthesized at the extremes of the considered bandwidth corresponding to fundamental frequencies of 2.3 and 2.5 GHz. In particular, the source impedance has been chosen equal to the conjugate of the large-signal ED input impedance over the whole bandwidth.

TABLE III
COMPARISON BETWEEN SELECTED CURRENT GENERATOR LOAD IMPEDANCE AND EXTRINSIC ONE AS A FUNCTION OF FREQUENCY

CGP load impedance [Ω]	*Frequency [GHz]*	*Extrinsic load impedance [Ω]*
103 - j 0.4	2.4	57 + j 45.4
0.3 + j 0.1	4.8	1.4 – j 11
344 + j 515	7.2	2.3 + j 29.7

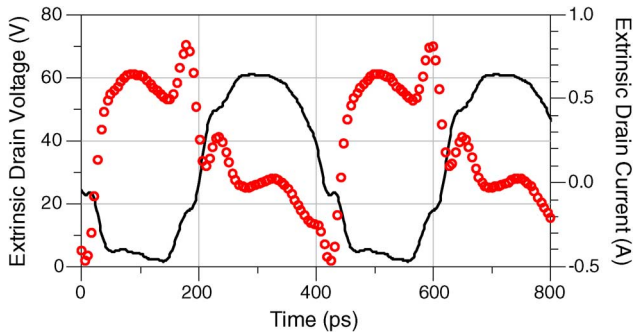

Fig. 13. Extrinsic time-domain voltage (continuous line) and current (circles) waveforms at the device drain extrinsic terminal for the highest value of input power, at the design frequency of 2.4 GHz (loading condition of Table III) obtained for a 1.25-mm periphery 0.25-μm GaN HEMT biased at $V_{d0} = 32$ V, $I_{d0} = 10$ mA.

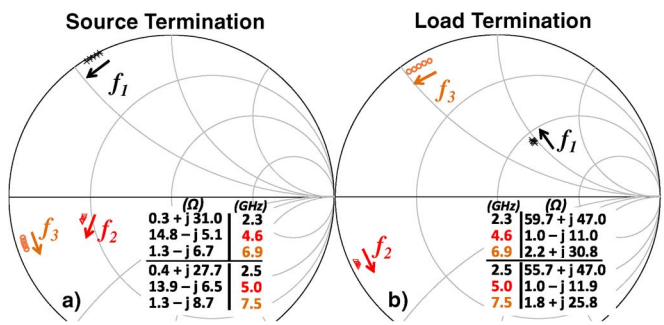

Fig. 14. (a) Source and (b) load impedances evaluated in the frequency range of 2.3–2.5 GHz: fundamental f_1 (stars), second f_2 (triangles), and third f_3 (circles) harmonic termination trajectories for a 1.25-mm periphery 0.25-μm GaN HEMT biased at $V_{d0} = 32$ V, $I_{d0} = 10$ mA.

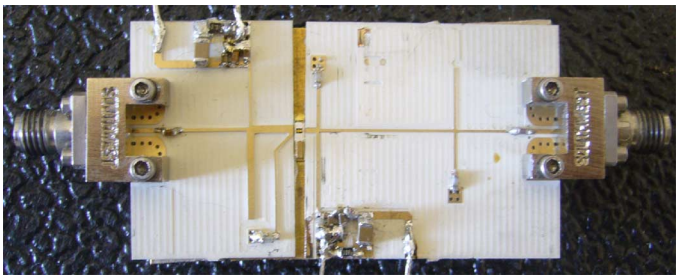

Fig. 15. Realized GaN class-F hybrid PA.

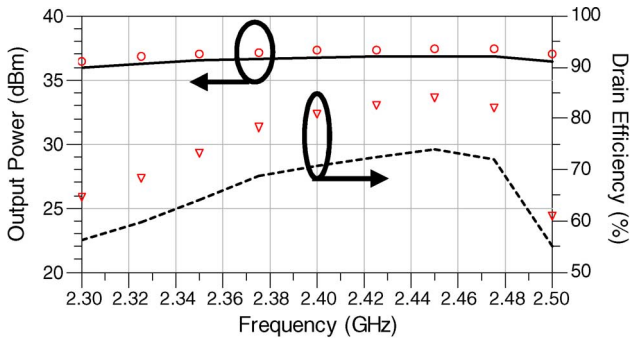

Fig. 16. Measured output power and drain efficiency of the realized PA across the bandwidth 2.3–2.5 GHz at PA plane (bold and dotted lines, respectively) and ED plane (circles and triangles, respectively).

The designed GaN class-F PA was manufactured on an HF laminate. Fundamental and harmonic target impedances have been synthesized in the frequency range of 2.3–2.5 GHz by means of simple topologies for both the input matching network (IMN) and OMN. It must be observed that, once the trajectories over the frequency of fundamental and harmonic impedances have been computed by exploiting the proposed approach, an arbitrarily large bandwidth could be obtained by increasing the topological complexity of the IMN and OMN. Nevertheless, since the aim of this work is to demonstrate the effectiveness of the proposed technique, we privileged the use of simple topologies for the IMN and OMN.

A photograph of the realized class-F PA is shown in Fig. 15. The PA delivers an output power greater than 36 dBm (∼4 W) with a drain efficiency greater than 55% over the frequency range of 2.3–2.5 GHz with a maximum of 4.9 W (36.9 dBm) and 74% at 2.45 GHz. Moreover, if the PA bandwidth is considered in the frequency range of 2.375–2.475 GHz, the measured efficiency is always greater than 70%, while the output power is never lower than 4.9 W (36.9 dBm).

With the aim of comparing the experimental performance of the PA with the predicted ones, which are referred to the ED ports, both measured output power and drain efficiency were de-embedded from the losses of the OMN. Fig. 16 shows the comparison between the performance of the PA with and without considering the matching networks. As a matter of fact, an output power greater than 4.4 W (36.4 dBm) with a drain efficiency greater than 61% were registered over the frequency range of 2.3–2.5 GHz at the PA plane. On the other hand, the peak value of the output power and drain efficiency

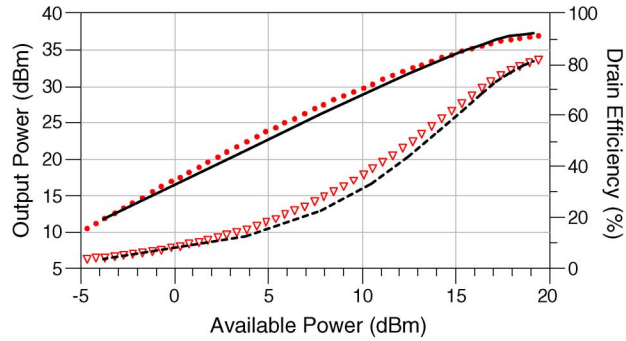

Fig. 17. Measured output power and drain efficiency of the realized class-F PA at ED plane (dots and triangles respectively) compared to the one predicted by the proposed technique (solid line and dashed line, respectively).

at the ED plane were, in this case, 5.5 W (37.4 dBm) and 84%, respectively. Besides, in a smaller range of frequencies (2.375–2.475 GHz), efficiency is always greater than 80% and output power is never smaller than 5.4 W (37.3 dBm). Experimental performance at the ED reference plane are in very good agreement with the predicted ones (37.3 dBm and 81%), based on the LF load-line characterization.

Finally, Fig. 17 shows the comparison between measured and predicted output power and drain efficiency sweeps at 2.45 GHz, frequency where the impedance values reported in Fig. 14 have been more accurately synthesized since the best performance is reached. The excellent agreement between data confirms the validity of the proposed load–pull technique.

V. Conclusion

In this paper, a novel load–pull characterization technique for high-efficiency PA design has been presented. Such a technique, which has the unique capability of performing waveform engineering at the ED CGP, has been validated by comparing results obtained at 20 GHz with conventional load–pull measurements and by designing a 2.3–2.5-GHz class-F PA in GaN technology. Experimental results are in fair agreement with the predicted ones, thus demonstrating that the proposed approach can guarantee the same level of accuracy achievable by time- or frequency-domain large-signal setups operating at microwave frequency.

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