PAM2.0 Steering

2022-09-29

Agenda

- Open Action Items Aug Steering / all
- Customer feedback / Ismail
- PAM2.0 Project Update / Mohamed, Andrea
- Tx Baseline Project Update -- Dual Driver / Andrea
- RF Prototyping line MAL / Bernd
- Status of mini-pac activity to support device selection for optimum module design / Bhagath

Action Items August Steering

- **AI: some more molded samples/EVB’s needed for sampling customers beyond Nokia / Alessio**
  - No samples needed as performance target not met

- Voltages: PAM-B @ 30V, PAM-A @ 32V → **AI: check ppm rate expectation of RF GaN-C1 at 32V drain voltage with TD / GerhardL**
  - Increase of ppm rate by 30% expected with 2V operation voltage increase acc to calculation from John Twynam
  - According to E/ feedback (60k modules in field operation since Jan‘22 w/o fail notification) the current IFX model is much too conservative and needs tb revised

PAM Customer Update

Ismail Nasr

Customer feedback / Ismail

- Nokia communicated new Radio schedule, due to changes from product marketing :
  - AVQR (PAM A 8W 3.4-3.8 GHz) Oulu
    - Ramp in Q4 2023
    - Nokia sees chance our design can meet the schedule → updated Information in next biweekly call
  - AVHA (PAM B 10 W 2.5-2.7 GHz) Oulu
    - Samples in August 2023
    - Ramp in Q4 2024
  - AVQA (10 W 3.45-3.98 GHz)
    - Nokia requested PAM A samples for initial testing
    - Ramp up in Q4 2023
    - Nokia can accept Efficiency >40% → main target US customers
    - Alignment meeting with Nokia done → we cannot meet timeline
  - Nokia Volume forecast in clarification: new indication seem too low/unrealistic

PAM-A
Project Update

M. Hamouda & Team

PAM2.0+ PAM-A, Milestone status: M4 (FE: RFGaN-C1, LD8C, B11HFC, SPT10 BE: PG-VFLGA-34-1)
Budget: Actual 12.6 M€, Forecast 19.7 M€, Last Approved 9.4 M€

Started and progress as planned | At risk/delayed, but not critical | At risk/delayed, mgmt. support needed

Status: Sep. 28, 2022

Executive summary & Customer update

- **Budget** Forecast **reduced** from **22.3 M€** to**19.7 M€** → **156 MM** reduced from Jan. '23 onwards; **300 k€** less material
  - **Assumption:** Design/CV **overhead** shifts to new **project** at **Jan. '23**
  - **Budget till Dec. '22: 2.5 M€ | Jan. '23-Sep. '24: 4.5 M€**

Traffic light

Red

Status of key customer deliverables and milestones/deliverables

Topic		End date	Comment
AVQR Sampling	Green	30.04.23	New **time line** shown to **Nokia** and **approved** Laminate **TO** pushed by **3 weeks**→ **no** impact on **schedule**
Module linearity (EVM)	Red	31.12.22	**B&C Tapeout done** → **Fab-out** end of **Oct.** Correlation bet. TDD EVM & gate lag IDQ recovery found **Plan** for production implementation **not clear**
Package concept	Yellow	30.09.22	New package potential → 0.4% higher efficiency **Unknown risks** → Package Price & Reliability
Ni. Thickness	Yellow	30.01.23	First measurements show ~0.4% higher efficiency for thin Ni. → Delayed due to priority topics Next Step: **Reliability** stress test
Test program	Yellow	15.10.22	Enabling high power measurement is ongoing. **Next Step: Correlation with CV lab** **Difficulties** on **correlation** due to **burn-in effects**
Pre-qualification	Yellow	15.01.23	HTSL 175C,1000h | HTSL 200C ✓ | TC ✓ | ESD,LU ✓ HAST, DC-HTOL **delayed** due to **mishandling** at RPT; **8D requested**

Achievements since last report

- New **mold compound** approved**;** more **reliable**
- Test **structures released** for **new material** characterization
- **Quotation** of new less lossy **material received**: same price but **expensive** thick **Ni**.
- **2000** PAM-A **PD3B** samples successfully tested at **ATK**
- **Test load board** can support **32V**

Critical issues to watch

- **PAM-A** product **costs** (laminate, SMDs)
- **PAM-A PD4 performance (>43% EFF.)**
- **EVM** performance **control** during **production** at **FE**
- RFGaN **Reliability at 32V** drain voltage

Next steps

- PAM2.0+ **CR** at **RFS Board** on 12th Oct. '22
- **PD4 design review on 15th Nov.**
- **Testing-CV** correlation
- **Data Analysis of 2k tested samples; select samples for lab correlation**
- **Quotation** update from **Amkor**

PAM-B
Steering

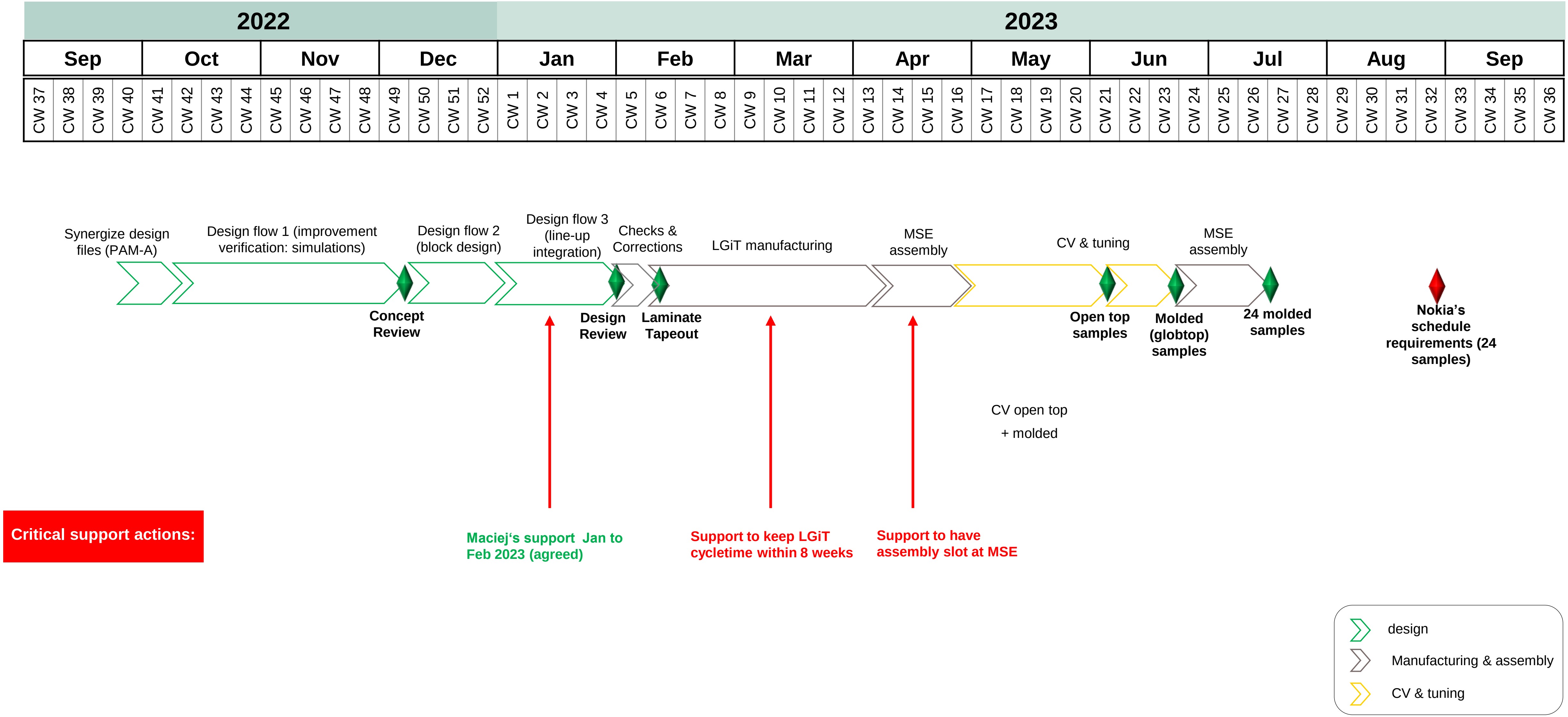
A. Scarpa & PAM-B team

PAM-B improvement strategy

		Expected performances						
Improvement	**Target**	**ACLR**	**gain**	**PAE**	**Reliability**	**Check measure**	**Check date**	**Result**
Current design (@32V)		-44dBc	29.6dB	45%	Lifetime risk			
MOSCAPs	2nd harmonic termination: Reduce input sensitivity & improve wideband linearity (AM/PM)	↑	↓	=	=	Simulations on main device with and without MOSCAP	10.09.22	AM/PM sprad reduced with MOSCAP
						Modulated measurements end stage Doherty and main device only	16.09.22	AM/PM similar main and end-stage: Higher confidence on the root cause
Use dies without gate resistor	Improve PAE and gain	=	↑	↑	=	Simulations	CW49_22	
Change Driver die	Improve PAE and gain	=	↑	↑	=	Simulation	CW49_22	
Bias network improvement: Low impedance feed (*) (including output combiner optimization)	Improve VBW → Improve ACLR	↑	=	=	=	Simulation	CW49_22	
Change of main & peak dies	• Improve PAE and linearity • Improve reliability (@28V)	↑	=	↑	↑	Simulation	CW49_22	
Wilkinson	Reduce imput sensitivity	=	=	=	=	Simulation	CW49_22	

(*) Re-use from PAM-A

PAM-B Timeline (Stretched) – Up to sample delivery



Copyright © Infineon Technologies AG 2022. All rights reserved.

PAM-B, Milestone status: M4 (**FE:** RFGaN-C1, SPT10 **BE:** PG-VFLGA-34-1)
PAM-B Budget: Actual 236k€

Progress as planned | At risk/delayed, but not critical | At risk/delayed, mgmt. support needed

Status: Aug 26, 2022

Executive summary & Customer update

- Performance improvement strategy defined and peer reviewed: Re-use of PAM-A experience and design
- Planning defined and agreed by Nokia
- Support actions identified

Traffic light

Red

Status of key customer deliverables and milestones/deliverables

Topic		End date	Comment
Design flow 1 (improvement verification)	Green	09.12.22	
Design flow 2 (block design)	Green	23.12.22	
Design flow 3 (integration)	Green	10.02.23	Module integration and layout: Agreed Maciej to support to pull-in schedule
Laminate manufacturing	Red	05.04.23	Management support needed to get priority at LGiT and keep cycletime ≤ 8 wks
Laminate assembly	Red	20.04.23	Management support needed to get assembly slot at MSE
CV & tuning	Green	30.06.23	Molded (globtop) samples

Achievements since last report

- Design flow and approach defined and peer reviewed
- Stretched planning defined and consolidated: Support actions identified
- Work space available (including MOSCaps)
- AM PM measurements on PAM-B Main test chip in line with line-up measurements: Higher confidence on root cause of poor linearization.

Critical issues to watch

- Laminate and assembly cycle time

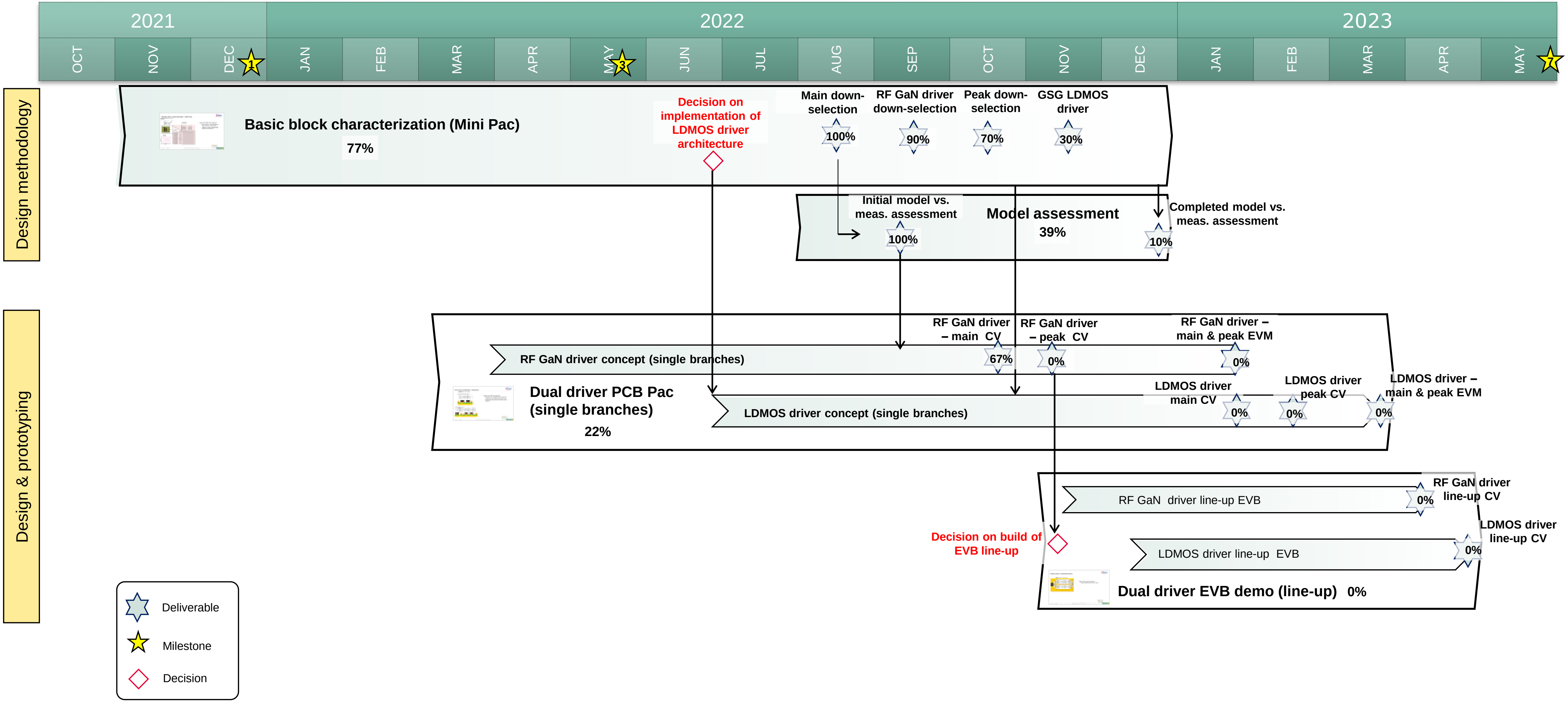
Next steps

- Project task breakdown
- Alignment on Mini Pac simulations: Filippo, Bhagath, Salih, Paul
- Start Design flow 1 tasks
- Task execution control (2x weekly stand-up meetings besides existing JFs)
- Weekly management report on progress

Study TX baseline Update

Andrea Scarpa, Talluri Bhagath
29.09.2022

Tx baseline project OKRs – 29.09.2022



Tx baseline, Milestone status: I3 (**FE:** RFGaN-C1, LD8C, **BE:** tbd)
Budget: Actual 2.2 M€, Forecast 4.0M€, Last Approved 4.0 M€

Started and progress as planned | At risk/delayed, but not critical | At risk/delayed, mgmt. support needed

Status: Jul 16, 2021

Executive summary & Customer update

- Mini Pac execution progressing, though still in pipe cleaning mode
- Design of first dual driver branch (PCB Pac) started
- Good progress on model assessment

Traffic light

Yellow

Status of key customer deliverables and milestones/deliverables

Topic		End date	Comment
Mini Pac execution (dual driver dies)	Yellow	18.11.22	• Several weeks delay on measurement of peak Mini Pac due to tool calibration and meas. issues • 5 wks dealy of LDMOS GSG dicing, delaying the build of PCB Pacs
Model assessment	Green	29.07.22	Initial model assessment done
PCB Pacs RF GaN driver – Main branch	Green	21.10.22	First dual driver branch (RG GaN driver)
PCB Pacs RF GaN driver – Peak branch	Yellow	01.11.22	Dealy of Mini Pac with Peak die causes slip from Oct to Nov
PCB Pac LDMOS driver	Yellow	12.08.22	Dealy of Mini Pac with GSG driver die causes slip from Oct to Dec

Achievements since last report

- Mini Pac measurement in progress. Load-pull measuremetns planned at Anteverta in CW40-42 to speed up and recover (part of) delay
- Good progress on model assessment: Workshop in CW37
- First dual driver branch (main) assembled
- EVM measurement strategy defined and design of PCB for EVM test in progress

Critical issues to watch

- Dicing of LDMOS GSGs
- Mini Pac execution is still in pipe cleaning mode, with long time to solve issues and deliver results (pre-assembly, assembly, CV)
- Allocation at assembly for last Mini Pac (LDMOS) and at suppliers (Astron, Cibel) for PCB builds

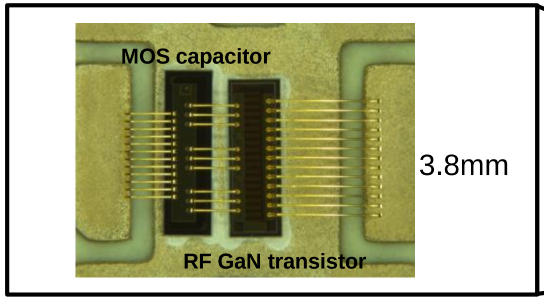
Next steps

- Proceed with Mini Pac DoE execution (LDMOS GSG assembly and measurement, buld 3 measurement)
- Proceed with PCB Pac measurement (RF GaN driver – main) and build (EVM PCB Pac, other PCB Pacs)
- Proceed with model tuning

Tx baseline mini-pac status

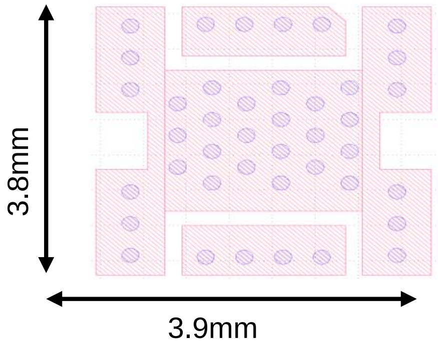
Minipac	Geometry [mm (µm)]	 DOE	 Design	 Assembly	 Measurement	 Model	Immediate application	Future application
1	5.76 (24 x 240)	DOE_1			CW44 (ANT)			1. Different specfication/trade-off 2. Different architecture/Topology 3. Model improvement 4. Module tuning 5. Sensitivity analysis 6. Stability analysis 7. Inputs for next tech. evaluation/bench-marking
	5.76 (30 x 160)	DOE_2			CW44 (ANT)			
2	4.80 (30 x 160)	DOE_3			CW44 (ANT)			
	5.12 (16 x 320)	DOE_4				CW 46	Dual driver main / PAM-A	
2b	Passives only					CW 46		
3	10.1 (42 x 240)	DOE_5			CW44 (ANT)			
	12.0 (30 x 400)	DOE_6			CW43	CW51	Dual driver peak	
4	2.4 (6 x 400)	DOE_7			CW44 (ANT)			
	1.92 (8 x 240)	DOE_8			CW 40	CW 49	GaN driver	
5	11.52 (36 x 320)	DOE_9			CW44 (ANT)			
	10.24 (32 x 320)	DOE_10			CW44 (ANT)			
6	3.84 (12 x 320)	DOE_11		CW41	CW44 (ANT)			
	3.84 (1 x 240)	DOE_12		CW41	CW44 (ANT)			
7	6.4 (20 x 320)	DOE_13			CW44 (ANT)			
	4.8 (12 x 400)	DOE_14			CW44 (ANT)			
8	LDMOS-A GSG 2.40 (6 x 400)	DOE_15		CW 44	CW50		LDMOS driver	
	LDMOS-B GSG 3.20 (8 x 400)	DOE_16		CW 44	CW52		LDMOS driver	
9	2.4 (10 x 240)	DOE_17						

Mini-pac build matrix



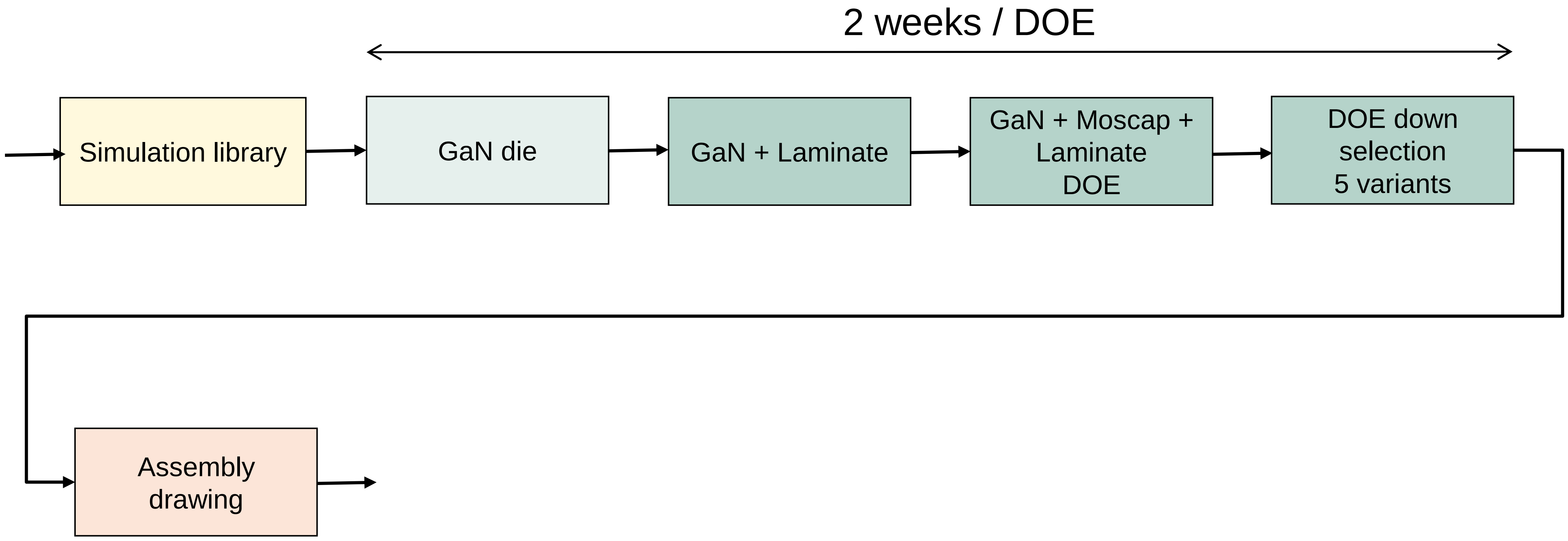
RF GaN transistor	MOS Capacitor	N9500B_V6	N9500B_V6	N9500B_V5	N9500B_V5	-	N9501B_V1	N9501B_V1	N9501B_V4	N9501B_V4	-	…	…
5.76 (24x240µm)	P19	•	•	•	•	•							
5.76 (36x160µm)	P6						•	•	•	•	•		
4.8 (30x160µm)	P3											⋮	⋮
5.12 (16x320µm)	P14												
10.1 (42x240µm)	P76												
12 (30x400µm)	P53												
11.52 (36x320µm)	P39												
10.24 (32x320µm)	P35												
2.4 (6x400µm)	T9507B_2												
1.92 (8x240µm)	2P4												
3.84 (12x320µm)	P13												
3.84 (16x240µm)	P10												
6.40 (20x320µm)	P15												
4.8 (12x400µm)	P55												

Mini Pac

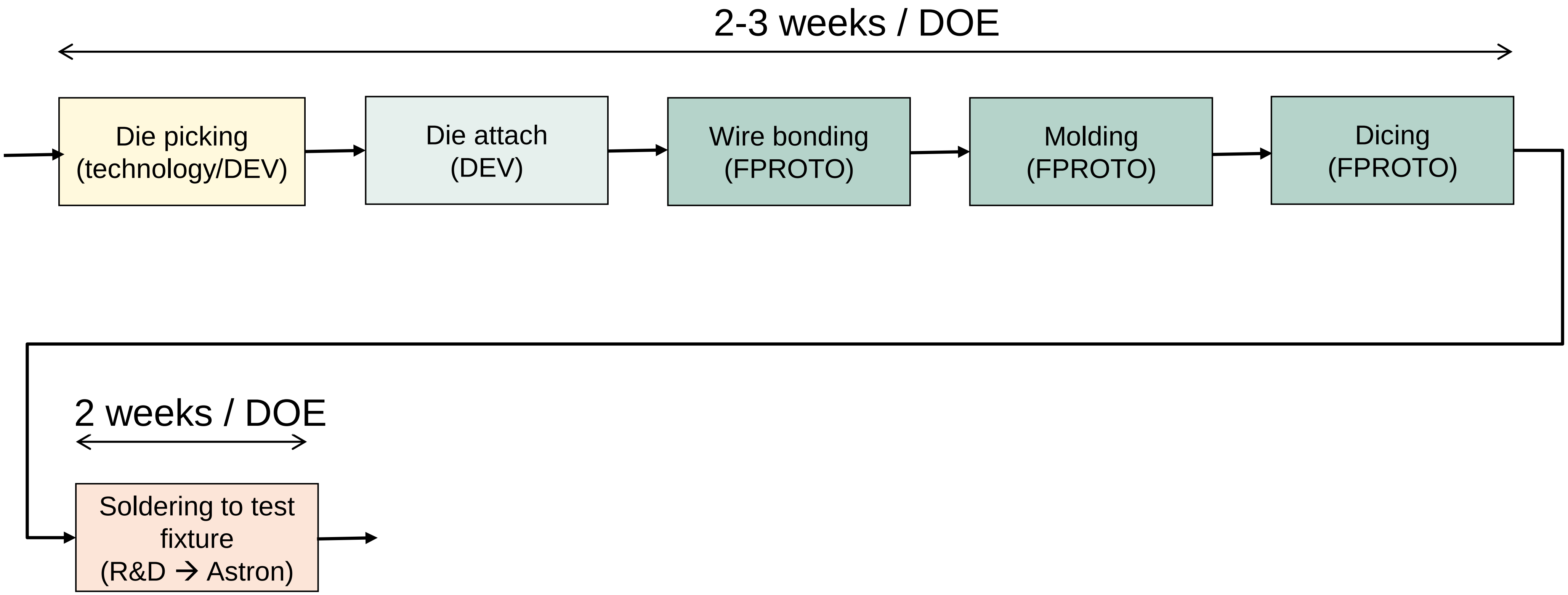


› Goal of Mini Pac matrix
- Down-selection of dies for dual driver
- Enabling of active + passive model
- Database for future designs

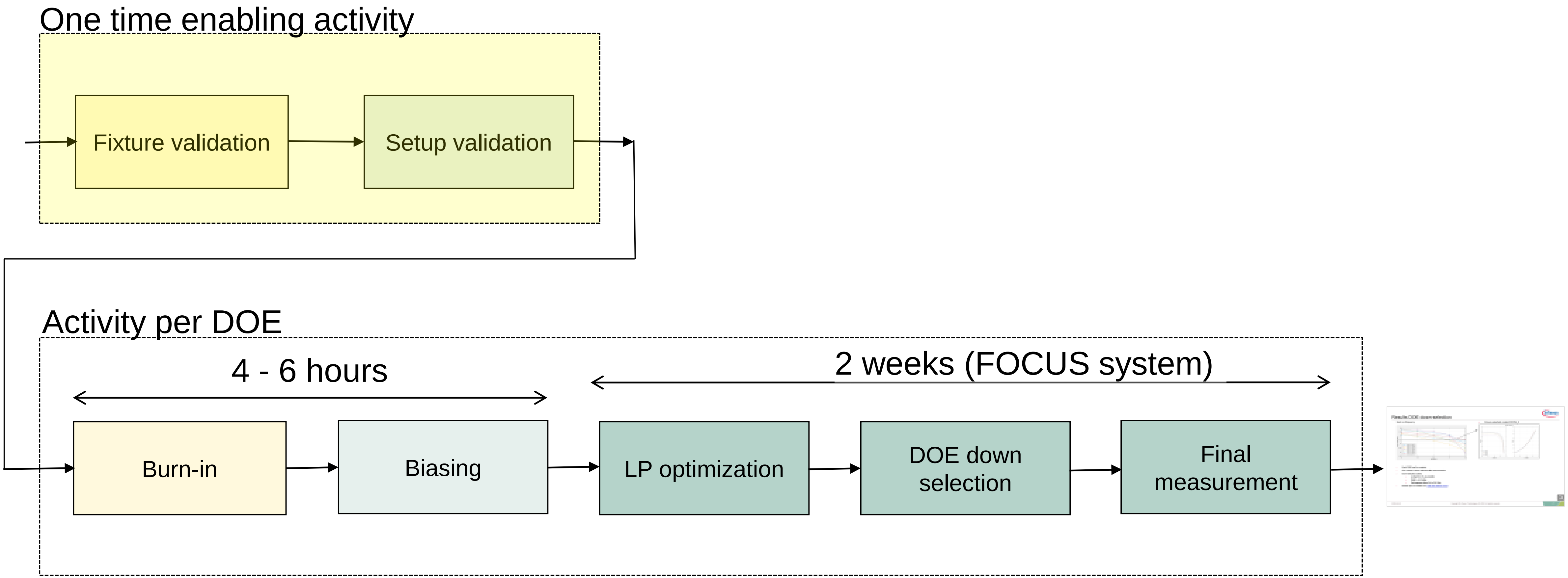
Mini-pac design flow (simulation)



Mini-pac assembly flow

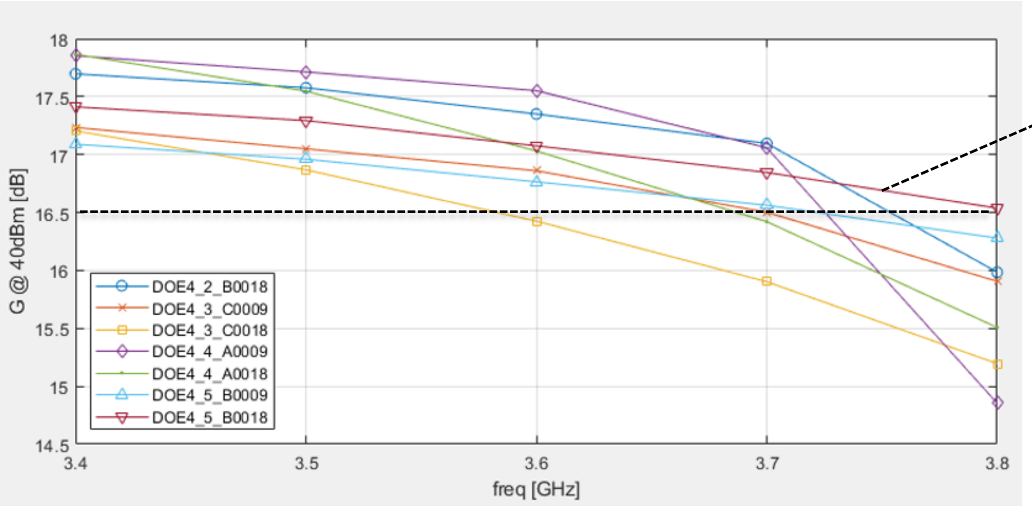


Mini-pac LP measurement flow

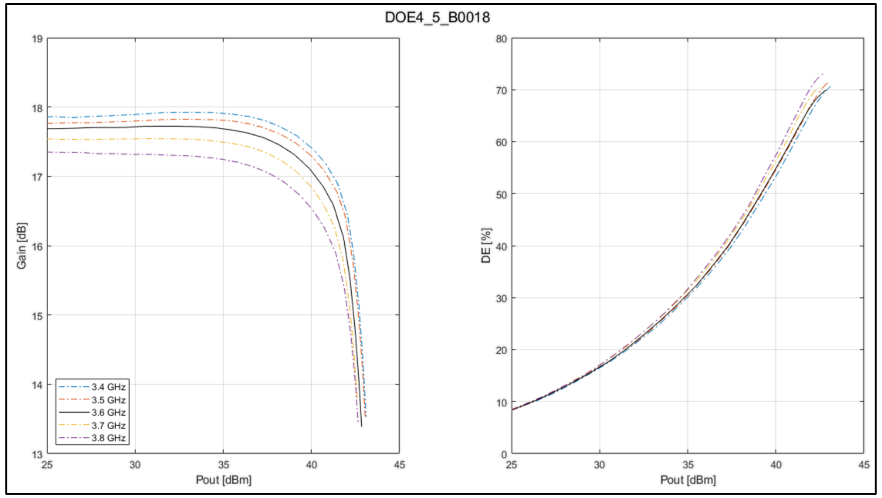


Results DOE down-selection

Gain vs frequecy



- Down-selected variant DOE4_5

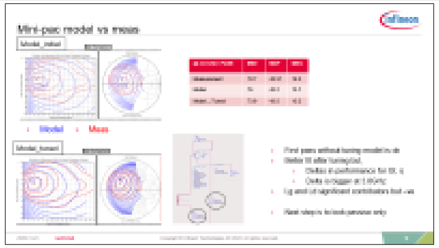


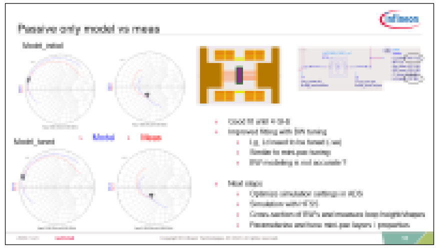
- Each DOE has five variants
- One variant is down selected after measurements
- Down-selection criteria
  - As high Gt, η% as possible
  - P3dB > 43.2 dBm
  - Flat response from 3.4 to 3.8 GHz
- Detailed report is available here: [DOE down-selection report]

Model flow

One time enabling activity

ADS templates → Tuning flow (active + passive) → Passive modeling





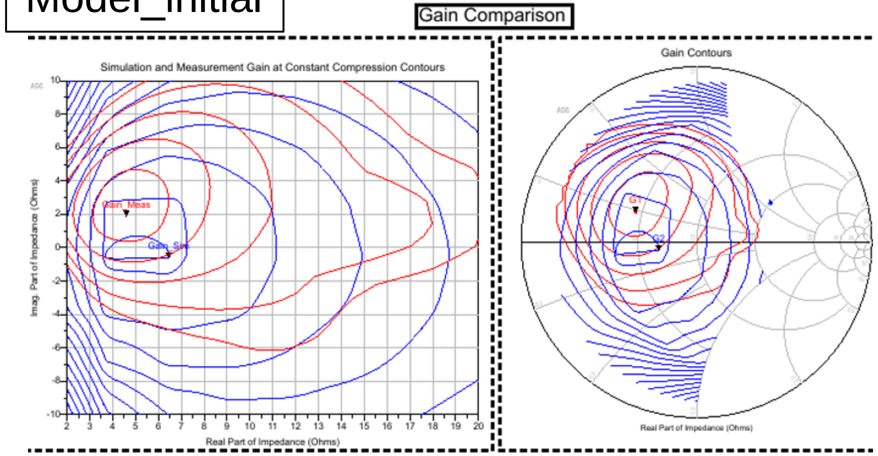
Activity per DOE

1- 2 weeks

Mini-pac EM simulation → S-par. tune Sim vs Meas → LP tune Sim vs Meas → Model report & benchmarking → Qualified model

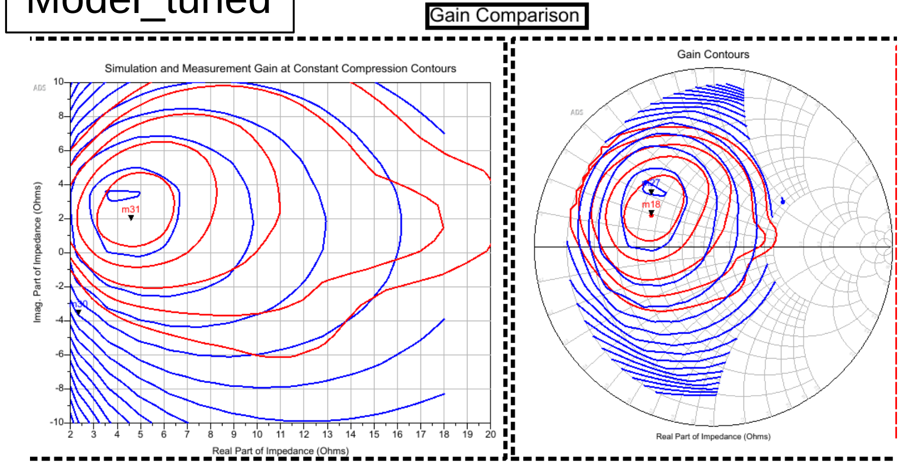
Mini-pac model vs meas

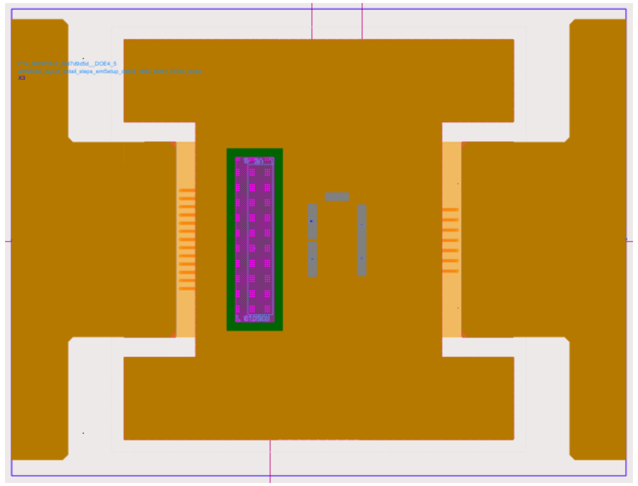
Model_initial



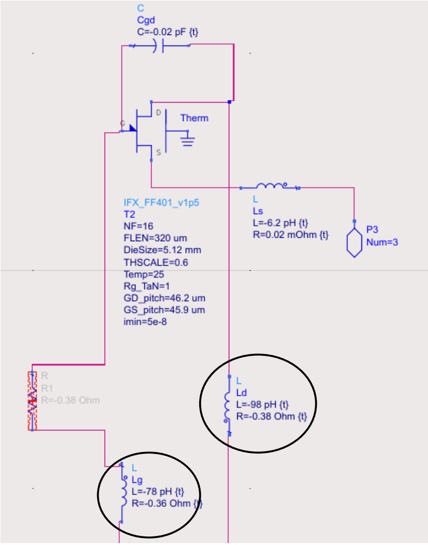
- Model
- Meas

Model_tuned





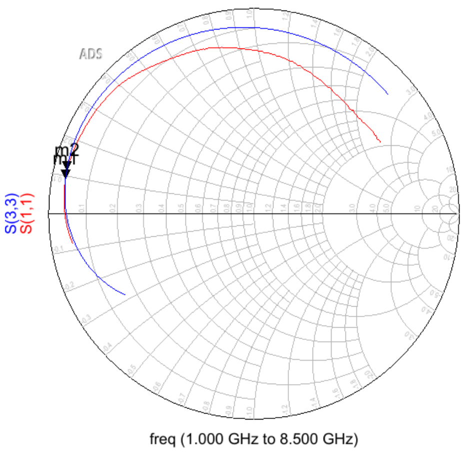
@ 3.6 GHz / P2dB	MXE	MXP	MXG
Measurement	70.7	43.57	16.3
Model	76	43.2	15.1
Model _ Tuned	73.9	43.5	15.2

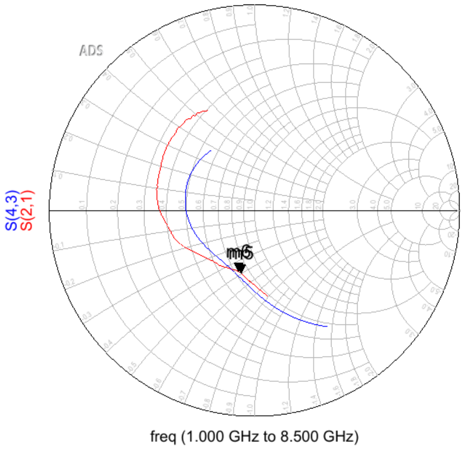


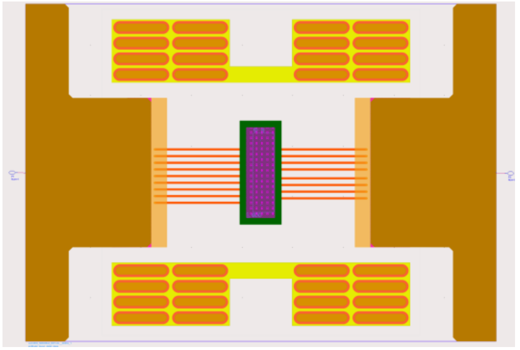
- First pass without tuning model is ok
- Better fit after tuning but,
  - Deltas in performance for Gt, η
  - Delta is bigger at 3.8GHz
- Lg and Ld significant contributors but –ve
- Next step is to look passive only

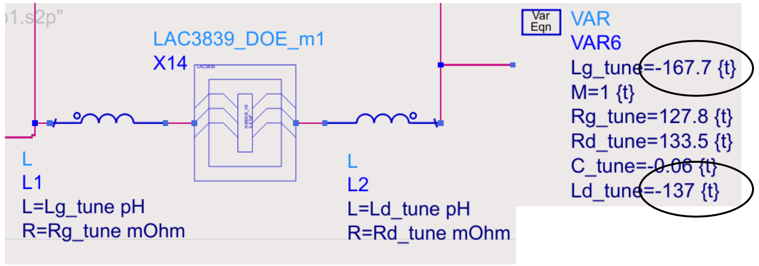
Passive only model vs meas

Model_initial



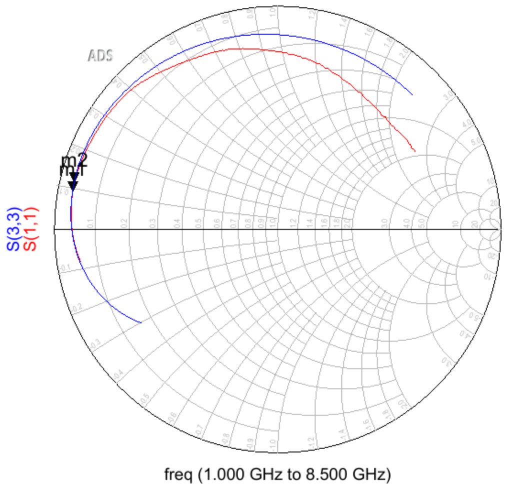


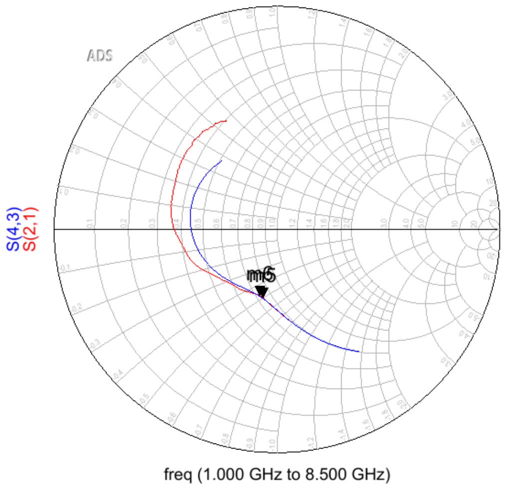




Model_tuned

- Model
- Meas



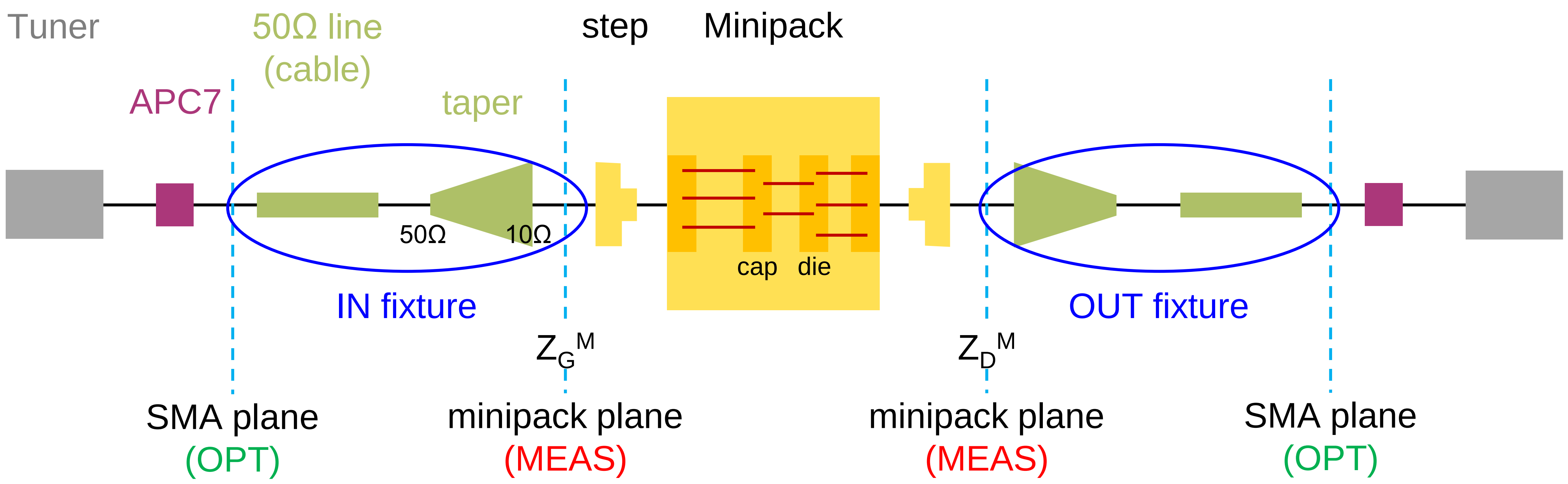


- Good fit until 4 GHz
- Improved fitting with BW tuning
  - Lg, Ld need to be tuned (-ve)
  - Similar to mini-pac tuning
  - BW modeling is not accurate ?

- Next steps
  - Optimize simulation settings in ADS
  - Simulation with HFSS
  - Cross-section of BW's and measure loop height/shapes
  - Parameterize and tune mini-pac layers / properties

Part of your life. Part of tomorrow.

Measurement strategy and de-embedding plane



- Optimization performed @SMA plane for higher accuracy (long fixture).
- Measurements @minipack plane for direct down-selection w\o need for de-embedding. To evaluate performance over frequency (3.4-3.8GHz) impedances Z_G^M and Z_D^M are kept constant over bandwidth.

- What are the differences between SMA and minipack reference plane?
  - Difference can be summarized in approximately 2dB of IL:
    - 0.4dB coming from resistive losses on output fixture → Z_D^M is close to 10Ω and therefore fixture is matched;
    - 1.6dB coming from IL (S21) on input fixture → Z_G^M is far from 10Ω and therefore losses due to reflection are significant.