International Journal of Microwave and Wireless Technologies

cambridge.org/mrf

Fully integrated three-way LDMOS Doherty PAs for 1.8–2.2 GHz dual-band and 2.6 GHz m-MIMO 5G applications

Marc Vigneau, Mariano Ercoli and Stephan Maroldt

AMPLEON, 5 Boulevard Jean-Auguste Ingres, 31770 Colomiers, Toulouse, France

Industrial and Engineering Paper

Cite this article: Vigneau M, Ercoli M, Maroldt S (2021). Fully integrated three-way LDMOS Doherty PAs for 1.8–2.2 GHz dual-band and 2.6 GHz m-MIMO 5G applications. *International Journal of Microwave and Wireless Technologies* 1–18. https://doi.org/10.1017/S1759078721000131

Received: 30 October 2020
Revised: 21 January 2021
Accepted: 22 January 2021

Keywords:
Power Amplifier; Doherty; MMIC; LDMOS; 3-way; 5G; Dual band; Digital Pre-Distortion

Author for correspondence:
Marc Vigneau,
E-mail: marcvigneau47@yahoo.fr

Abstract

This paper presents a fully integrated three-way Doherty architecture to address the challenges of 5G applications using laterally-diffused metal-oxide semiconductor (LDMOS) technology. By using the so-called C_{DS} cancelation method for the Doherty combiner design, a wideband impedance transformation is achieved, that combined with the three-way Doherty power amplifier (DPA) architecture allows for high efficiency in deep back-off, with a reduced load modulation for high bandwidth. Throughout this paper, the design approach and realization are described, while multiple critical design challenges will be addressed such as low frequency drain resonance optimization, impact of in-package coupling effects, and linearity versus efficiency tradeoff. Two state-of-the-art three-way fully integrated LDMOS DPA monolithic microwave integrated circuit (MMICs) are presented to demonstrate how these measures have been successfully applied to different power amplifier (PA) line-up components for 5G base station systems. First, a 60 W 1.8–2.2 GHz multi-stage device for driver application in true dual-band operation is presented. The circuit design pays special attention to extended PA video bandwidth thanks to integrated passive device. After digital pre-distortion (DPD) in dual-band operation, this highly linear device achieves an outstanding adjacent channel leakage ratio (ACLR) of −56 dBc for a 2cLTE 20 MHz 8 dB peak-to-average ratio signal spaced by 345 MHz, thus 385 MHz instantaneous bandwidth (IBW), with 29% efficiency at 35 dBm, 12 dB output back-off (OBO). Second, the simulation and measurement results of a 55 W 2.6 GHz multi-stage DPA for massive-MIMO final stage application are presented, which yields an excellent linearized efficiency of 49% using a 200 MHz 10cLTE signal with an ACLR lower than −47.5 dBc. For 8cLTE 20 MHz (160 MHz IBW), the device yields 50% efficiency with −50.7 dBc ACLR linearized after DPD. The achieved efficiency is well comparable to published GaN DPAs. These results were achieved by improved simulation techniques to minimize frequency dispersion and thus allow high efficiency operation over wide bandwidth. Both devices show that LDMOS is not only a mature technology which allows those PAs to be reliable and low-cost for mass production in very compact packages, but also provide best-in-class RF performance according to the needs of 5G base station systems.

Introduction

With the roll out of the fifth generation (5G) active antenna unit (AAU), telecommunication industry requires ever higher efficiency and linearity of RF power amplifiers (PAs) to support wideband signals for high data-rate transmission in low cost and compact solutions. Now typical 5G massive-MIMO base stations have 32–64 transceivers. To avoid excessive energy consumption and thermal management issues, the efficiency of PAs must significantly improve compared to previous generations. On the other hand, as discussed in [1] 5G New Radio requires wider bandwidth (400 MHz instantaneous bandwidth (IBW) for macro base stations and 200 MHz for m-MIMO base stations) with stringent linearity requirement fixed by 3GPP and Federal Communications Commissions (FCC). This involves more complexity to linearize PAs with digital pre-distortion (DPD) whereas on the other hand DPD power consumption needs to be lowered. Achieving high efficiency over wide IBW remains the most challenging issue for the design of RF PAs, especially based on silicon LDMOS technology. Indeed, 5G breakthrough is synonym to GaN High Electron Mobility Transistor (HEMT) technology introduction for the telecommunication base station industry. As compared in [2, 3], GaN has multiple advantages over LDMOS for PA design, namely higher power density, higher output impedance, lower C_{DS}, therefore more wideband, and higher efficiency at the device level. However, GaN has still some undesirable effects such as self-heating, trapping effects, and reliability affecting the reproducibility for mass production [3]. Moreover, as demonstrated in [4] LDMOS still yields good performance until 5 GHz. The combination of a mature technology and good RF performance for sub 6 GHz band makes LDMOS technology still very interesting for 5G if the bandwidth and efficiency limitations at the transistor level can be compensated by design improvements.

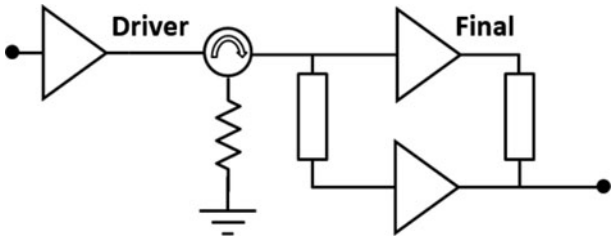

Fig. 1. Transceiver PAs line-up.

Conventional Doherty power amplifiers (DPAs), which utilize the concept of active load modulation, have been used for decades in base stations due to their advantages in efficiency when used with high peak-to-average ratio (PAR) modulated signals [5, 6]. However, when using silicon LDMOS technology, the efficiency of the classical two-way symmetric DPA is far from sufficient, while the two-way asymmetric DPA has intrinsically more limitations in bandwidth and wideband DPD linearizability (raw linearity is not a reliable parameter to judge DPD linearizability). Many studies have been conducted to push the bandwidth limitations of two-way DPAs [7–11] with excellent results. However, although those approaches are suitable for discrete PAs on large printed circuit board (PCB) areas, they are less suitable for a fully integrated solution due to compactness constraint required by base station manufacturers [12]. Some architectures such as outphasing or envelope tracking are quite interesting to increase efficiency. However, those architectures are not suitable for base station requirements such as linearity and bandwidth, and furthermore require fundamental change in base station architecture level [13]. At the end as described in [12–14] DPAs are still the trend in 5G industry, especially integrated circuits for compactness reason. In summary, the challenge to design 5G RF PAs can be formulated by this question, what is the Doherty architecture which can be integrated in one single compact package and small PCB area (in total less than a few cm^2), while achieving highest linearized efficiency in deep back-off (8–10 dB), respecting 3GPP and FCC constraints for wideband modulated signals of 200 MHz and more. Moreover, the solution must be low cost. We also would like to emphasize the necessity of evaluating efficiency as a line-up efficiency, including the power consumption of driver stages, which heavily depends on the achieved gain of the final stage. In many cases, this does have a non-negligible influence (even for an optimized line-up, one can typically count at least 5–6% efficiency reduction due to the drivers). This study will show how the possibility of high integration in LDMOS MMICs allows us to implement more complex three-way DPAs, breaking the boundaries of classic Doherty topologies in industry field. This comprises the use of the C_{DS} cancellation technique [15] to realize the combiner circuit, allowing for wideband PA impedance transformation and full integration in a single compact package which reduces the size of the device.

As displayed in Fig. 1, a transceiver PA line-up of a base station (BTS) typically consists of at least two or more amplifier components. To achieve the required total line-up gain, typically 50–60 dB, some amplifiers are using several gain stages (multi-stage PAs) to increase the gain per component. Although often more focus is given to the final stage, also the driver stage plays a significant role when it comes to linearity, line-up efficiency and last but not least miniaturization and integration of the BTS. Compared to a final stage, the drivers require equally complex and challenging DPA architectures, especially as they typically operate even further in power back-off (for higher linearity margin). Key advantage of multi-stage integrated LDMOS MMICs for drivers is to have high gain in one single package which implies significant cost reduction (same power supply, remove circulator, less manufacturing operation, etc.).

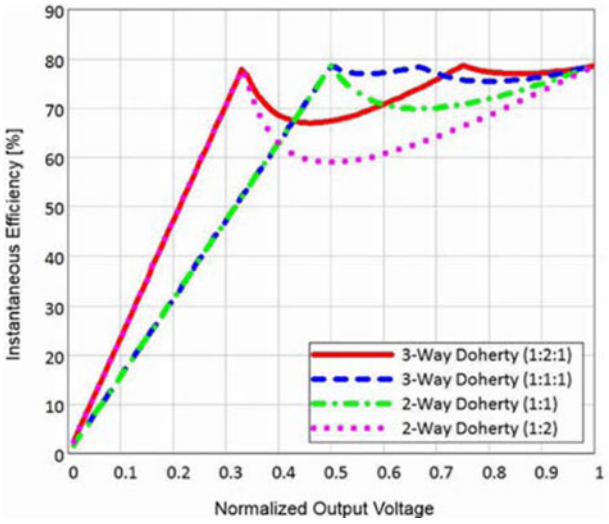

Fig. 2. Theoretical efficiency for *N*-way Doherty [15].

In this paper, multiple critical design challenges in industry will be addressed for driver and final stage DPAs in silicon LDMOS technology, such as low frequency drain resonance optimization, in-package coupling effect mitigation, linearity improvement, and prediction in simulation, all based on the architecture and design of three-way DPAs. Applying these methods, two fully integrated Doherty LDMOS MMIC PAs were realized, and obtained results will be shown and discussed. First, a 60 W 1.8–2.2 GHz multi-stage device for driver application in true dual-band operation, and second, a 55 W 2.6 GHz DPA for massive-MIMO final stage applications are designed. Both devices are designed for high gain between 27 and 30 dB, thus based on integrated multi-stage amplifiers.

Broadband-integrated LDMOS Doherty

Choice of Doherty architecture

Although GaN offers better performance at the transistor level when compared to LDMOS, the advantage of LDMOS lies in the feasibility (technical and cost-wise) of more complex Doherty architectures. The optimum compromise to satisfy the requirements of low-cost circuit, compact architecture, and broadband is to exploit LDMOS technology with a strong effort on Doherty architecture optimization with higher complexity.

The theoretical demonstration of different Doherty structures is widely treated in [15]. Figure 2 clearly shows the comparison of theoretical efficiency of various Doherty structures. It is important to keep in mind that any two-way Doherty allows us to place a single efficiency peak in back-off, given by the *k*2 parameter. One must change the power ratio of the two amplifiers to change *k*2 (1:1 versus 1:2), which at the same time affects bandwidth in the opposite way, more back-off causes reduced bandwidth. In contrast, a three-way Doherty allows not only to place a second efficiency peak at intermediate back-off level (impact

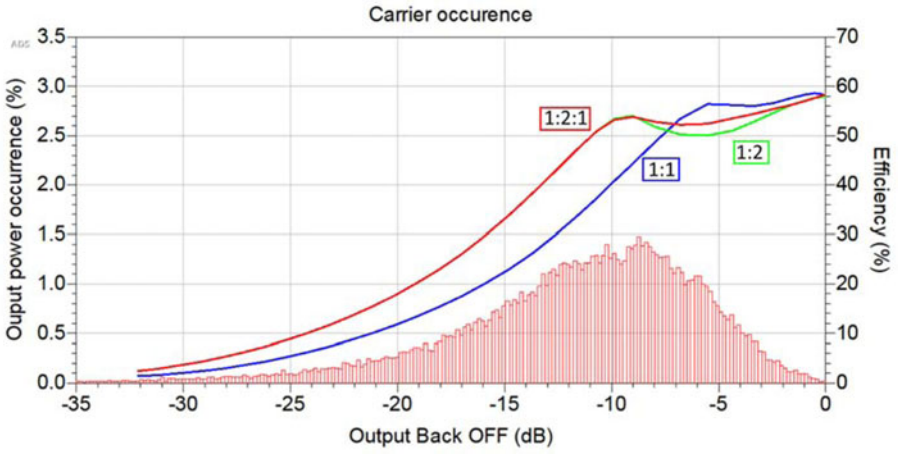

Fig. 3. Simulated response of *N*-way Doherty with LTE signal distribution.

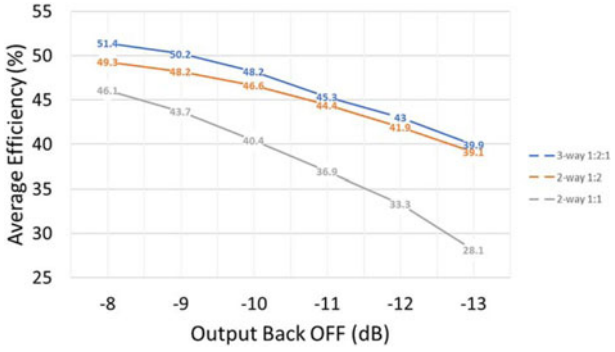

Fig. 4. Simulated response of the average efficiency for *N*-way Doherty with 1cLTE signal distribution at various output back-off.

Table 1. DPA architecture comparison back-off ($k1$, $k2$), load modulation (VSWR), and fractional bandwidth ($\Delta f/f$) of a quarter wavelength transformer for the required VSWR

Doherty architecture	$k1$ (dB)	$k2$ (dB)	VSWR	$\Delta f/f$ (%)
2-way 1:1	0.00	−6.02	2.00	16.3
2-way 1:2	0.00	−9.54	3.00	9.9
3-way 1:2:1	−2.50	−9.54	2.25	13.8

will be further discussed below), but it also offers a multitude of different power ratios, which completely overcomes the fundamental trade-off limitation between bandwidth and back-off (efficiency) of the two-way Doherty.

As discussed in the previous section, many possibilities have been published to improve the bandwidth of the two-way combiner, which in a matter of fact results in an up-shift of the bandwidth–efficiency trade-off to a higher bandwidth. But the fundamental trade-off limitation remains. Moreover, the area requirement of such combiner networks is rarely taken into account but is an equally crucial parameter for real use in 5G m-MIMO systems than efficiency itself. Last but not least, one also has to keep in mind that most structural improvements of the two-way combiner found in the literature can in principle be applied also to a three-way combiner. However, once all factors for 5G m-MIMO are achieved, such as efficiency, linearity, bandwidth, compactness, cost, and practical reliability, the three-way architecture is clearly key for LDMOS technology, as will be discussed step by step later on.

Latest LTE modulations exploit 256QAM that is translated with a 9–9.5 dB of output back-off for final stage applications. At the same time, this involves for the driver amplifier to operate at a power back-off close to 13 dB, in order to preserve the linearizability of the full line-up. To analyze the impact of a high back-off efficiency, a study is performed under three different versions of Doherty amplifier to verify how the theoretical efficiency behavior translates into a more realistic circuit. All the circuits are simulated using LDMOS technology [4] and exploiting the same design approach, based on two-stage amplifiers. Two-stage means that each branch of the Doherty is composed of a small driver and a final stage transistor. This is done to achieve around 30 dB of line-up gain. A lossy combiner and splitter were designed for each circuit, based on the techniques discussed in the next section. All were simulated at the schematic level without layout realization. The first one is a symmetric two-way Doherty. The second one is an asymmetric two-way Doherty. The power ratio between the main and peak amplifier is 1:2. The third one is a three-way Doherty. The power ratio between main, peak one and peak two is 1:2:1.

Figure 3 shows the simulated power-added efficiency of these three architectures and the distribution of an LTE signal with 8 dB PAR.

Applying this distribution to the three amplifier version the average efficiency at 8 dB back-off is 46.1% for the 1:1 version, 49.3% for the 1:2, and 51.4% for the 1:2:1, respectively (Fig. 4). In case of higher signal back-off which is the case of the driver application use case (from 9 to 13 dB OBO) the gap between the symmetric and the asymmetric Doherty PAs increases considerably. Moreover, for 5G low traffic operation, when base station is not working at full load (so in deep back-off) it is non-negligible to maintain high-modulated efficiency to avoid too much AAU power consumption.

In terms of efficiency, the three-way DPA is slightly better than the two-way asymmetrical DPA but at complexity cost. The real advantage given by the three-way DPA is the higher bandwidth compared to the two-way asymmetric Doherty. The parameter used to classify the three architectures in terms of bandwidth is based on the amplifier load modulation, as summarized in Table 1. The symmetric Doherty has a load modulation of 2,

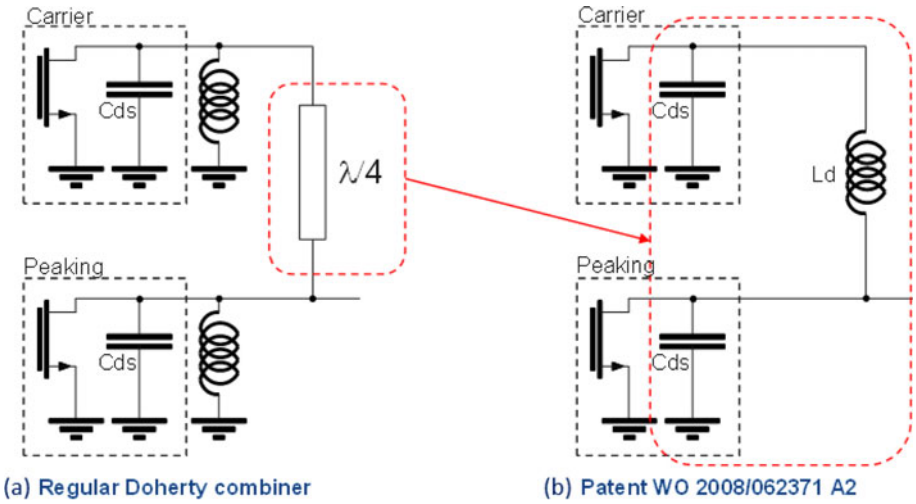

Fig. 5. (a) Impedance inverter using a quarter wave transmission line and (b) integrated compact combiner $C_{DS\_Carrier}$– L_d–$C_{DS\_Peaking}$ π-filter.

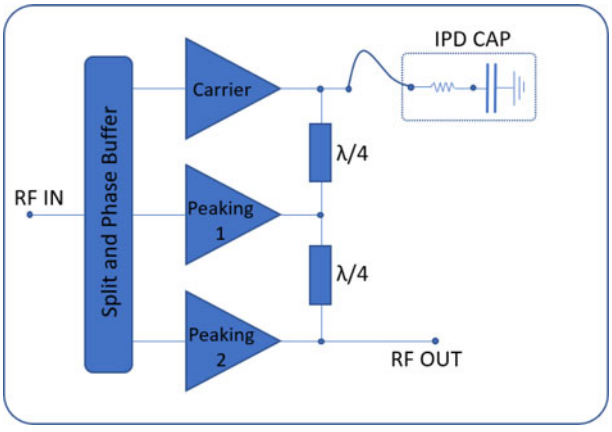

Fig. 6. Three-way integrated DPA configuration with IPD.

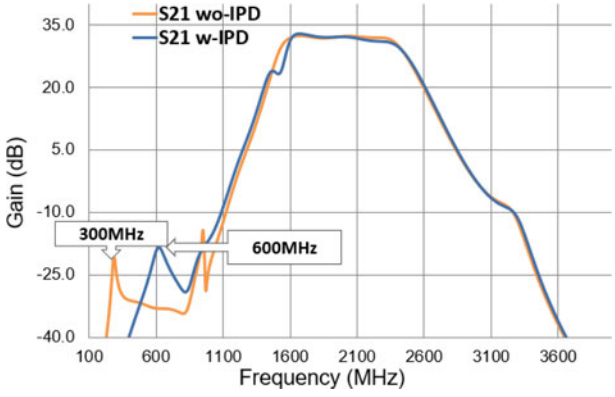

Fig. 7. Simulated *S*-parameters with and without IPD.

measurable by the voltage standing wave ratio (VSWR) concept (VSWR = Z_0/Z_L). In theory, a load modulation of 2 allows the amplifier to work in a relatively wide fractional bandwidth of 16.3%. Equation (1) shows the theoretical relation between fractional bandwidth and VSWR. Γ_m is the target reflection coefficient for the quality of the impedance matching, here assumed to be 0.045 (27 dB):

$$\frac{\Delta f}{f_0} = 2 - \frac{4}{\pi}\cos^{-1}\left[\frac{\Gamma_m}{\sqrt{(1-\Gamma_m^2)}}\frac{2\sqrt{(Z_L Z_0)}}{|Z_L - Z_0|}\right] \quad (1)$$

The asymmetric 1:2 Doherty has a VSWR of 3 that negatively impacts the fractional bandwidth of this architecture to 9.9%, in order to increase the back-off point $k2$ to −9.54 dB. The three-way DPA allows us to reduce the VSWR while preserving a high back-off efficiency. In case of an amplifier ratio of 1:2:1, the back-off point $k2$ remains at −9.54 dB, like for the two-way 1:2, but a VSWR of 2.25 is achieved, enabling broadband capabilities for the Doherty PA with 13.8% theoretical fractional bandwidth.

The concept of three-way Doherty exhibits great potential, however, its integration in a compact package remains a challenge. In the literature, one can find various flavors of Doherty architectures, even asymmetrical two-way Doherty with higher bandwidth. The price to pay to achieve this is a significant increase in space required by the combiner [7–10]. For that reason, the design of the output combiner is the heart of the integrated Doherty. In this study, the output combiner is fully integrated on the silicon die.

C_{DS} cancellation technique to improve combiner bandwidth and compactness

A common method employed to manage the output capacitance of an LDMOS transistor is to resonate the C_{DS} using a shunt inductor, followed by a $\lambda/4$ transmission line transformer to realize the Doherty combiner (Fig. 4(a)). This shunt inductor is implemented inside the package, close to the drain of the transistor, using bond wires connected to a large shunt capacitor, which acts as an RF short circuit. This approach has several limitations, which are the additional bandwidth limitation of the resulting parallel resonator, the losses of the shunt inductor wires, due to the limited quality factor of the network, and the shunt capacitor to decouple the supply voltage supply, which increases the total output capacitance of the amplifier with direct impact on the amplifier IBW. Another not neglectable drawback of this technique is the parasitic mutual coupling between the shunt wires and the other input and output wires, adding further challenges for compact integration in an *N*-way DPA.

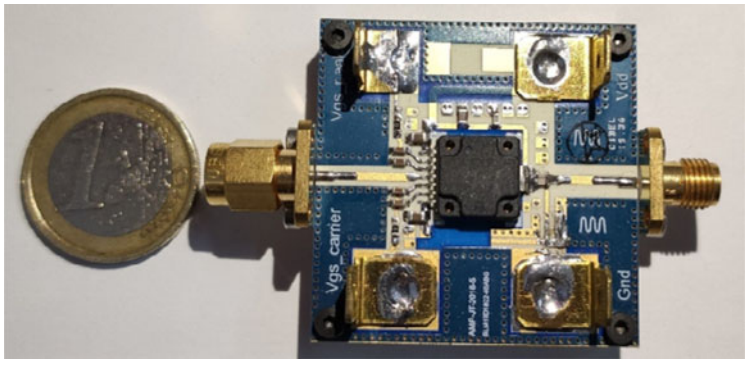

Fig. 8. PCB, effective area 18 × 22 mm^2.

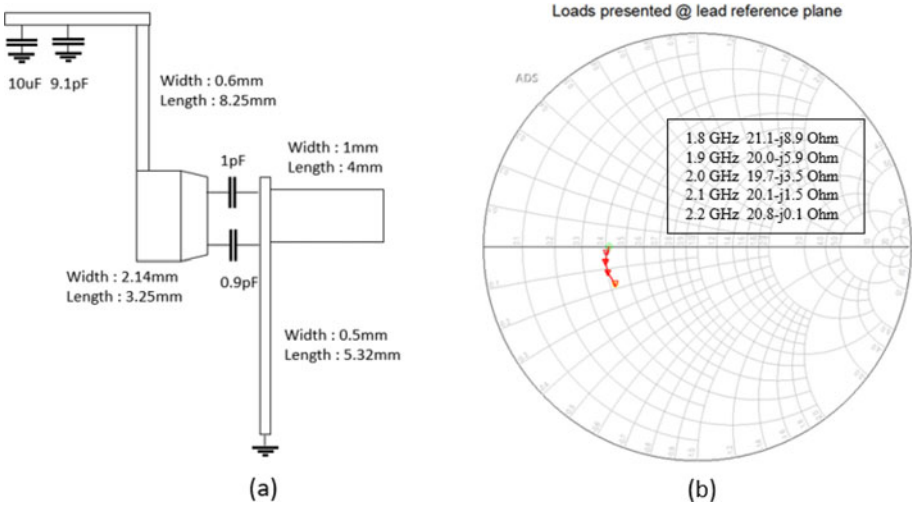

Fig. 9. (a) OMN schematic diagram and (b) loads presented at lead reference plane package at 2 GHz.

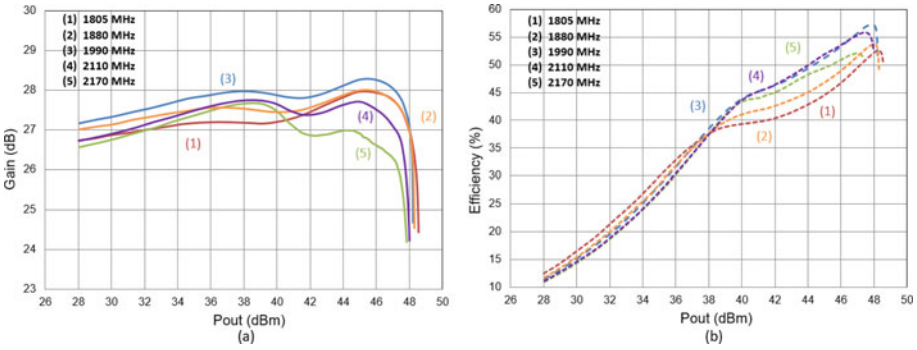

Fig. 10. (a) AM/AM and (b) efficiency in pulsed-CW.

To improve the impedance transformation bandwidth, in this study the so-called C_{DS} (drain-to-source capacitance) cancellation technique is used to design the combiner of the device, described in [15–17]. It is based on the absorption of the C_{DS} of the carrier and peak transistor into the combiner, by realizing a C–L–C π-network equivalent to a $\lambda/4$ transmission line transformer, acting as an impedance inverter of the Doherty (Fig. 5(b)).

The L_d inductance is realized with high-Q bond wires to limit efficiency losses and the capacitors are extracted from the C_{DS} of the LDMOS transistors. This makes the transistor more ideal, raising the output impedance, improving the quality factor of the network, thus resulting in higher bandwidth for impedance matching and, hence widening the operative bandwidth. The implementation of the C_{DS} absorption helps to significantly reduce the parasitic capacitance at the output of the PA seen by the baseband signal, when compared to the aforementioned shunt inductance network, due to the absence of any additional RF shunt capacitors. Another benefit of this method is the full integration of the DPA in a single compact MMIC device, which reduces the size of the package to follow the demands of miniaturization and integration which are key for 5G massive-MIMO application. To emphasize the importance of this point, note that due to this technique, the whole three-way Doherty combiner was realized in less than 1.5 mm^2 footprint area on the MMIC die, which is just slightly bigger than the footprint of a single 0603 SMD component.

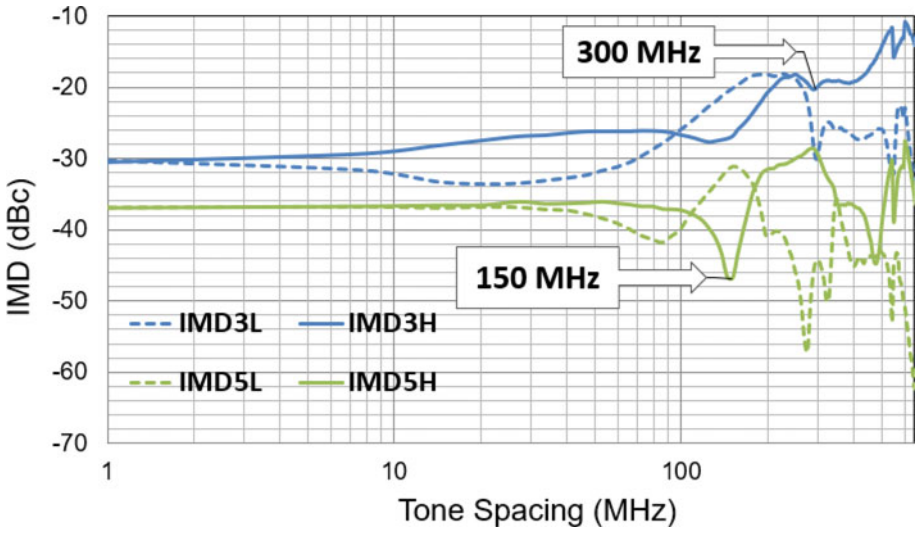

Fig. 11. IMDs at 38 dBm output power for various two-tones spacing with center frequency 1990 MHz.

MMIC DPA design considerations

The actual design of the Doherty combiner was done by matching the large signal optimum load impedances of the three final stage transistors (carrier, peaking 1, peaking 2) under different conditions in back-off and saturation, taking into account the boundary conditions of C_{DS} absorption in the combiner. The choice of total final stage transistor gate width was driven by the output power requirements considering all output losses. Furthermore, the multi-stage amplifiers (e.g. two-stage, with one driver stage, and one final stage) were realized using integrated MMIC passive components (thick Al metal inductors, MIM capacitor, and poly-Si resistors). The interstage matching between driver and final stage transistors as well as the input matching of the driver was fully EM simulated using Momentum. The driver stage size was chosen for sufficient output power margin over a temperature from −40 to 130°C at the plastic package interface to an underlying PCB. In this way, the linearizability of the whole DPA can be sustained even at high temperature, with some trade-off to consider on the driver power consumption and therefore line-up efficiency. The input splitter design of any Doherty PA is almost of equal importance to the combiner, as a wideband combiner is only as good as its splitter, which needs to provide the correct amplitude and phase to each amplifier branch over bandwidth and dynamic, with low losses to preserve a high line-up gain. A misaligned splitter causes undesired frequency dispersion in amplitude and phase (AM/AM, AM/PM, and delay), which in turn causes degraded linearizability, efficiency, and output power. The integration of splitter and combiner into the package and even into the MMIC die, allows not only a perfect adjustment of all those requirements by design, but also guarantees a good repeatability and reproducibility of the DPA performance in high volume production needed for 5G m-MIMO AAUs. The biasing of the DPA is using to two different gate voltages for application system reasons, which means that one gate voltage is used to bias the carrier amplifier in class-AB, while both peaking amplifiers use the same gate voltage in class-C. Therefore, driver and final stages of each amplifier branch use the same gate voltage. Note that ideally a three-way Doherty would use at least three different bias points (one for each final stage) to manage the correct turn-on behavior of the peaking amplifiers. Here, the input splitter was used to compensate for the different turn-of behavior of the two peaking amplifiers.

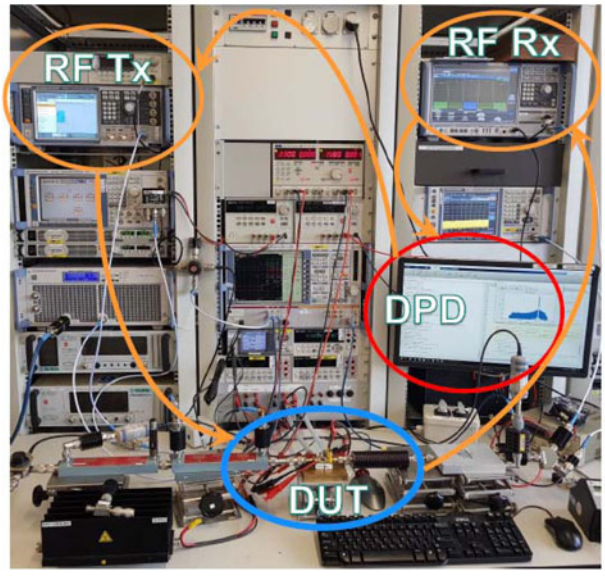

Fig. 12. Digital pre-distortion hardware setup.

Last but not least, the full circuit was verified for stability using non-linear stability methods (such as STAN), and traditional linear small signal stability measures (such as *k*-factor). The stability is analyzed including parasitic feedback loops in the package as well as the MMIC itself, by using EM simulation of passives on die and 3D FEM simulations of the package environment. Due to the high gain and high intrinsic isolation of a multi-stage amplifier, e.g. an isolation below −60 dB and gain of 30 dB from package input to output and even more on some nodes on the die, some parasitic feedback loops which are totally important for single stage amplifiers (with e.g. 15 dB of gain), suddenly become critical and have to be taken into account correctly.

Dual-band 60 W 1.8–2.2 GHz DPA

The motivation of this three-way DPA is to achieve a wide radio frequency bandwidth while having a high efficiency in deep back-

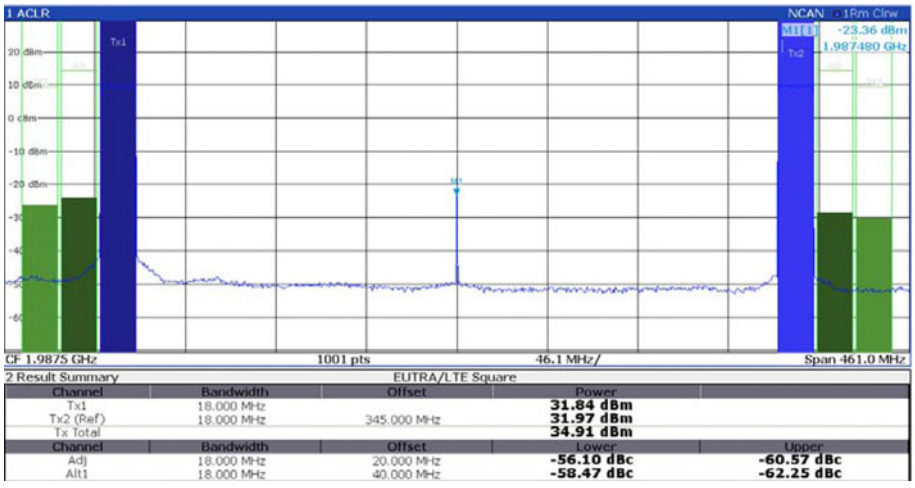

Fig. 13. ACLR result after DPD correction for 2cLTE 20 MHz spaced by 345 MHz.

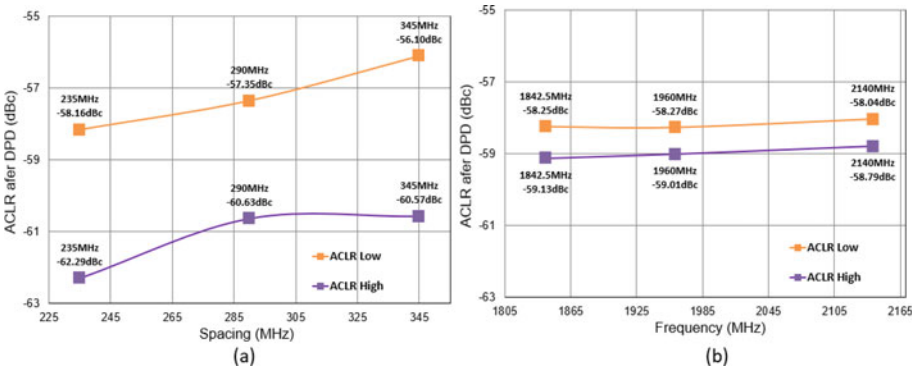

Fig. 14. ACLR result after DPD correction: (a) 2cLTE 20 MHz versus spacing and (b) 3cLTE 20 MHz versus B1, B2, and B3 band.

off for driver stage application. This will lead to big advantages for base station manufacturers such as improved line-up efficiency (~3 pts) which is crucial for the incoming 5G. Higher system integration which means, for example, only one compact device to handle two independent telecommunication bands. Also, a cheaper infrastructure under from many points of view like reduced number of PAs, more compact PCB, simpler power supply management, and minimization of DPD systems are the key to catch the bigger part of mobile infrastructure market.

For a designer, the main challenge is to optimize the PA's RF performances in its operative band. First criterion is to have a PA with as flat as possible transfer function (small signal gain). This involves having a reduced in-band ripple, almost zero phase dispersion, and stable group delay over the whole of frequency band. If those conditions are satisfied the PA will show limited short-term memory effects which have short time constant. This memory effects are mostly corrected by current DPD algorithms.

However, the PAs are also affected by long-term memory effects associated with the bias networks. These effects represent one of the main limitations for linearization capabilities because they are very difficult to predict and model. This is even more difficult if the resonance frequency of the biasing network is in the same range as the baseband envelope frequency of the input signal. Because of that, during the design phase the baseband resonances and impedances must be carefully optimized. Moreover, those parasitic resonances increase with transistor size, so in other words with the total PA power.

Instantaneous bandwidth extension technique

In view of the incredibly wide IBW required by 5G systems, which is up to 400 MHz. It is not possible to use a simple classical bias decoupling network like $\lambda/4$ feeders for the biasing of the amplifiers drain. The $\lambda/4$ feeder, for low frequencies such as the current design, is made with relatively long line. That line is invisible in the RF band, but it represents an inductive path for the base band. The sum of this inductance and the inductors L_d of the Doherty combiner gives a total base band inductance relatively high. The resonance of the inductance with the drain–source capacitor (C_{DS}) of the carrier determines the low-frequency resonance (LFR) of the amplifier and consequently limits to certain values the IBW achievable for the PA. To optimize the baseband impedances and push the LFR to higher frequencies, an integrated passive device (IPD) is embedded inside the package [18]. The IPD circuit is based on a separate silicon die interconnected to the Doherty MMIC through bond wires (Fig. 6).

The circuit implements a high value capacitor (nF range) and a series resistor. The resistor acts as a dumping network to mitigate the parasitic self-resonance of the bond wires and the tank capacitor. The presence of this energy tank close to the carrier amplifier of the Doherty increases considerably the LFR of the whole Doherty, thus boosting the IBW of the complete amplifier.

As Fig. 7 shows, the integration of the IPD circuit allows to have a higher LFR, moving the base band resonance of the amplifier from 300 up to 600 MHz. Of course, due to the presence of

Table 2. Performance comparison Doherty PA design for 2 GHz

Freq (GHz)	1.8–2.2	1.805–1.88	1.8–2.2	1.8–2.2
Pavg (dBm)	39	44.5	47.3	35
Max gain (dB)	16.7	20.3	15	27
ACLR DPD for 3cLTE[a]	−57.01/−54.58 dBc (B2)	−51.22/−52.08 dBc (B3)	NA	−58.04/−58.79 dBc (B1)
ACLR DPD for 2cLTE spaced[a]	NA	NA	−54.1/−52.3 dBc (B1 + B66)	−56.10/−60.57 dBc (B1 + B3)
DPD Eff	47% (8 dB OBO)	50% (8 dB OBO)	44.3% (8 dB OBO)	29% (13 dB OBO)
Doherty type	3-way iDPA	2-way DPA	2-way DPA	3-way iDPA
Techno	LDMOS	LDMOS	GaN	LDMOS
Reference	[16]	[29]	[18]	This study

[a]DPD results displayed are for the worst case in each case (B1, B2, B3 or spacing).

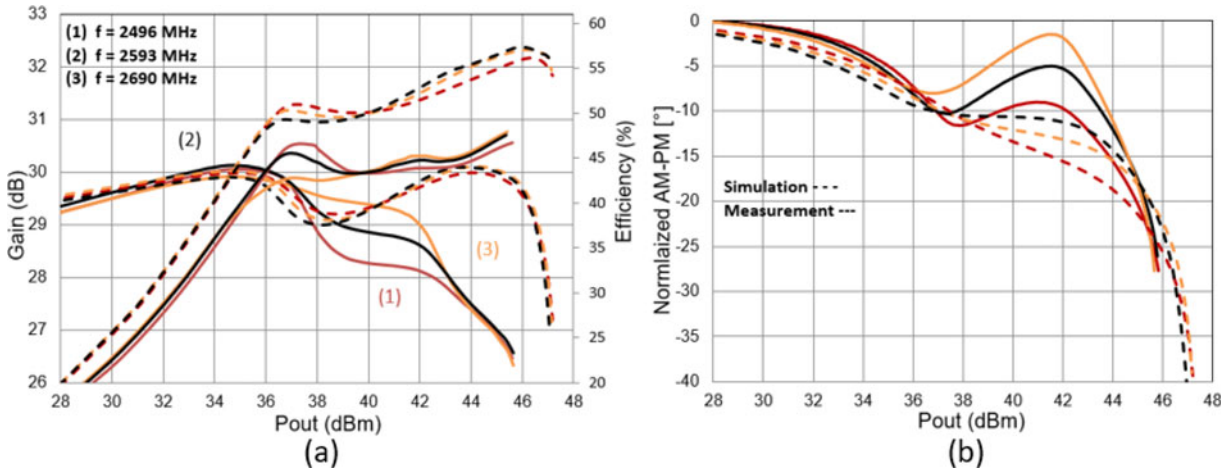

Fig. 15. Initial measured performance of the three-way Doherty with matching on PCB versus simulated one that shows: (a) lack of power for both peaking amplifiers and (b) strong phase and amplitude dispersion over frequency.

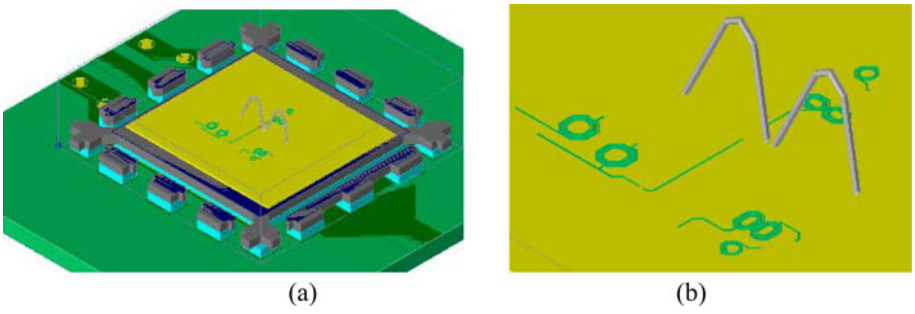

Fig. 16. 3D view of the package including MMIC passives and bond-wires for coupling simulation: (a) full view and (b) zoom on wires and inductors.

this new component the interaction between the IPD interconnection wires and the other wires of the combiner and input connection influences also the complete PA response. Because of that the integration of the IPD is not expensive. The design requires to be reworked to consider the mutual coupling and the additional parasitic losses. On the other hand, the advantage given by the IPD is not only the frequency shift of the LFR but also the lowering of the baseband impedances which reduces the complexity of the wideband DPD algorithm. The second resonance peak visible on the orange curves derives from a parasitic resonance between the RF capacitors placed at the end of the $\lambda/4$ feeder and the base band capacitor (10 µF) used to decouple the low frequency band. The same effect is visible on the blue curve but shifted higher in frequency due to the different circuit set-up.

Measurement results

The PA is assembled in a low-cost reliable compact solution, overmolded package (OMP400). Biasing network, part of base band decoupling and output matching network are implemented on a PCB using the Rogers RO4350B substrate of 20 mils of thickness.

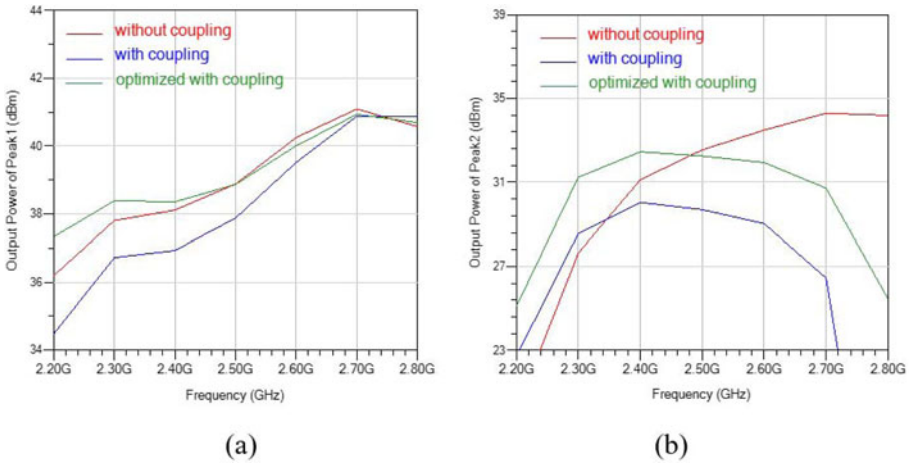

Fig. 17. Simulated output power over frequency for fixed input power level of (a) peak 1 amplifier and (b) peak 2 amplifier in Doherty operation; red, initial design but no 3D EM coupling considered; blue, initial design with parasitic 3D EM coupling; green, optimized design to compensate for parasitic 3D EM-coupling effects.

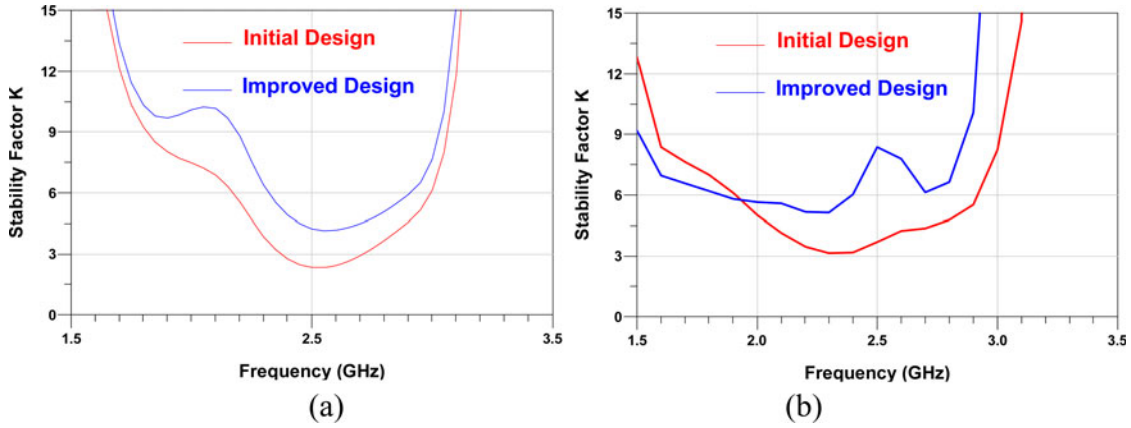

Fig. 18. Impact of design improvement to account for parasitic coupling effect on the small signal stability (*K*-factor) in (a) simulation and (b) measurements.

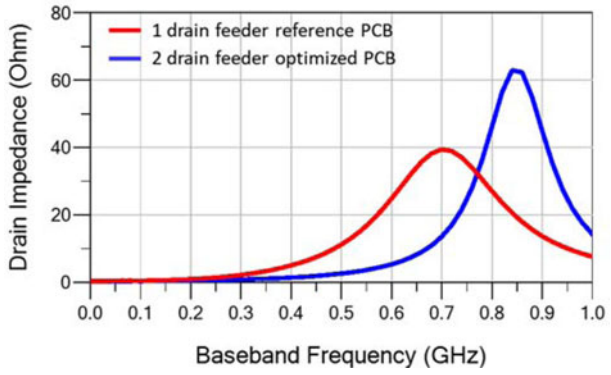

Fig. 19. Simulated LFR in baseband depending on drain decoupling network configuration.

Copper baseplate for heat dissipation is soldered directly at the backside of the PCB as shown in Fig. 8.

The effective matching area to ensure 50 Ω input 50 Ω output impedance is compact: only 18×22 mm^2 and only two gate bias voltages are used to supply carrier, peak 1, and peak 2 amplifiers to be more compact and easier to integrate. Measurements are performed at 25°C. V_{DS} voltage is set to 28 V while V_{gs_c} is set at 2.19 V to regulate the quiescent current at 100 mA.

For measurements, the MMIC is matched on maximum power impedance location for linearization capability in 1805–2170 MHz band to handle B1 and B3 simultaneously. The output matching network is a high pass filter as displayed in Fig. 9(a).

As shown in Fig. 9(b), the impedances are quite high and regroup over frequencies. It eases matching and reduces PCB losses.

AM/AM measurement results shown in Fig. 9(a) confirm the capability of a three-way integrated DPA to be wideband over 400 MHz bandwidth. The compression behavior is smooth with P1 dB close to P3 dB over the full band. This achievement, as discussed before, is mainly due to the reduced load modulation that guarantees not only a flat gain but also stable maximum output power, close to 48 dBm, and limited spread in efficiency (Fig. 10(b)). For driver application it is very important to underline that the amplifier exhibits an efficiency of above 27% at 13 dB OBO for all frequencies. This is an excellent result considering LDMOS driver PAs. Looking closer to the shape of efficiency curves the Doherty behavior exhibits a shift of *k*2 efficiency peak. This is mainly due to the broadband Doherty configuration. The relative bandwidth is close to 20% and due to the very stringent compactness constraints of the plastic package, the circuit does not guarantee a stable 9 dB back-off as expected by the theory. To mitigate this effect, during the design phase, the output combiner and the input splitter have been optimized, acting on

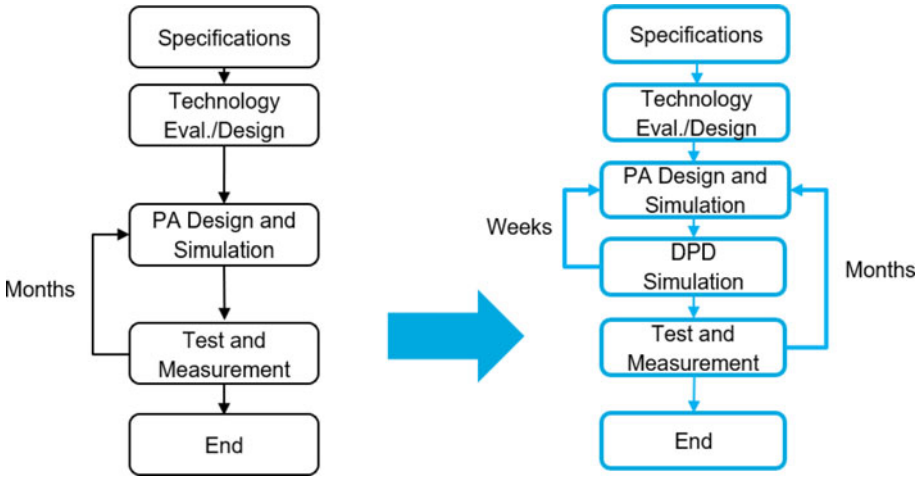

Fig. 20. Design workflow optimization.

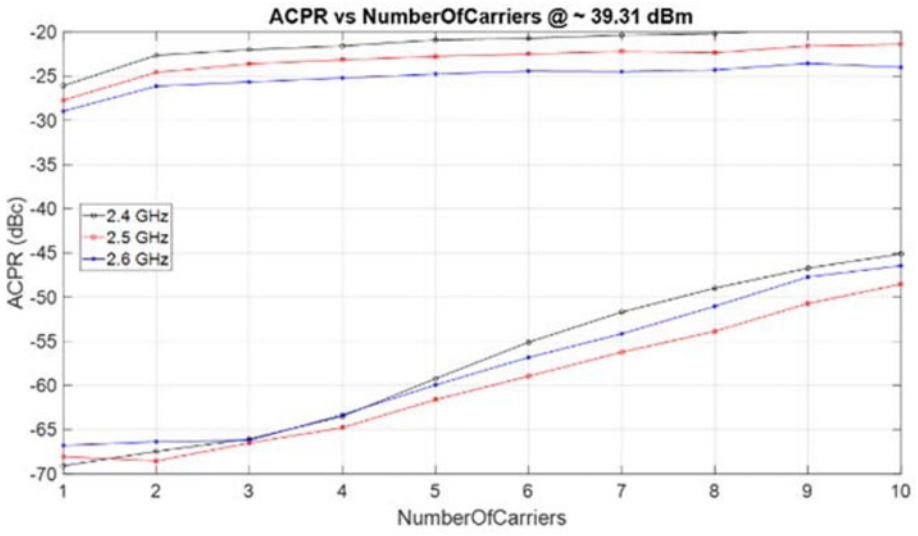

Fig. 21. Linearized ACLR (after DPD) over number of carriers of a multi-carrier 20 MHz LTE, simulated using a behavioral model of the DPA and VS-GMP DPD algorithm for linearization.

power magnitude and phase, to keep $k2$ between −8 and −10 dB for 1.805 and 2.170 GHz respectively. The final result is a consistent behavior of the PA performance over a relatively wide frequency spectrum.

Once verified the right features of the circuit in the operative band it is important to verify the behavior in the base band domain. Because of the broadband radio frequency spectrum, it is important that the PA shows the same capabilities in the base-band domain. For that reason, the focus is now moved on the evaluation of base band performance exploiting the video bandwidth (VBW) measurement. Thanks to this test it is possible to verify the maximum instantaneous band that the PA can handle. The amplifier is designed and used as a driver stage block. Under normal conditions, i.e. at 28 V and 25°C, it delivers an average output power of 35 dBm. However, the VBW test is then performed at 38 dBm. Indeed, the deeper back-off, 35 dBm will show a more linear PA because, mainly, only the carrier stage contribute to the signal amplification and is still far from his output compression. Moving 3 dB higher the average signal is more realistic because it better describes the worst case of the operative domain of the amplifier. The carrier starts to compress, and the two peaks amplifiers contribute more to the total PA output power. What is expected is a degradation and a resonance of IMD3 that is important to evaluate to ensure a good response of the amplifier. VBW measurement is performed thanks to two-tones CW with various spacing and maintaining a constant output power.

The IMD3 defines the VBW limit. The measurement, in Fig. 11, shows a resonance above 300 MHz which is in line with what is achieved by the LFR shown in Fig. 7. LFR is almost the double of the VBW (or IMD3 resonance) and four times the resonance of IMD5. In the measurement, the IMD5 (H) resonates close to 150 MHz. The two tones spacing, for IMD3 start to diverge before the IMD3 resonance. This is mainly due to the amplifier base band envelope impedance [19]. The IPD makes the difference on the drain amplifier side, by moving the LFR at higher frequencies. The two tones spread is also due to the gate envelope impedances that are treated mainly with an external base band decoupling circuit. To further optimize the shapes of IMDs a more powerful gate decoupling network must be implemented, preferably inside the package as in [20, 21].

Linearized dual-band operation

Linearization is performed with different tones spacing for 2cLTE 20 MHz with 8 dB PAR at 13 dB OBO, corresponding

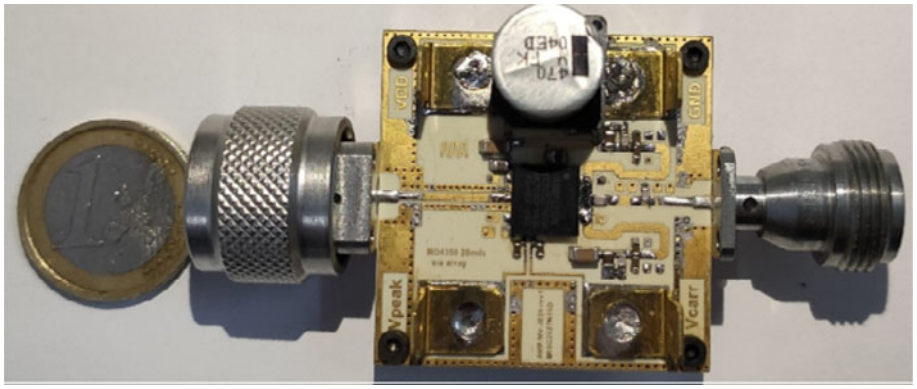

Fig. 22. PCB, effective area 19 × 23 mm^2.

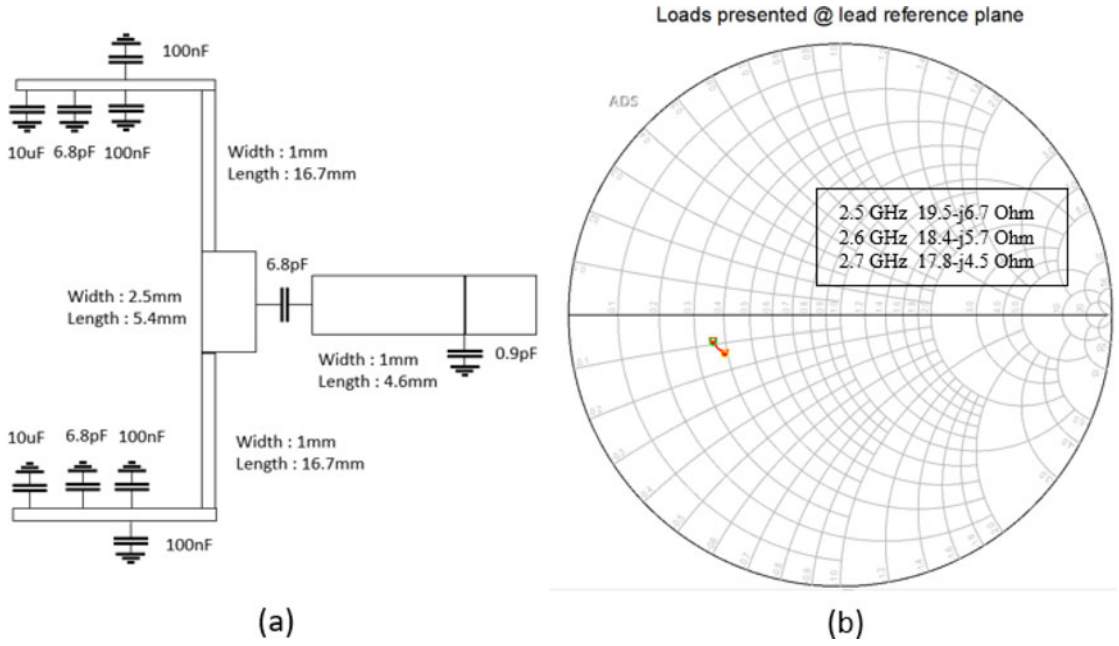

Fig. 23. (a) OMN schematic and (b) loads presented at lead reference plane package at 2.6 GHz.

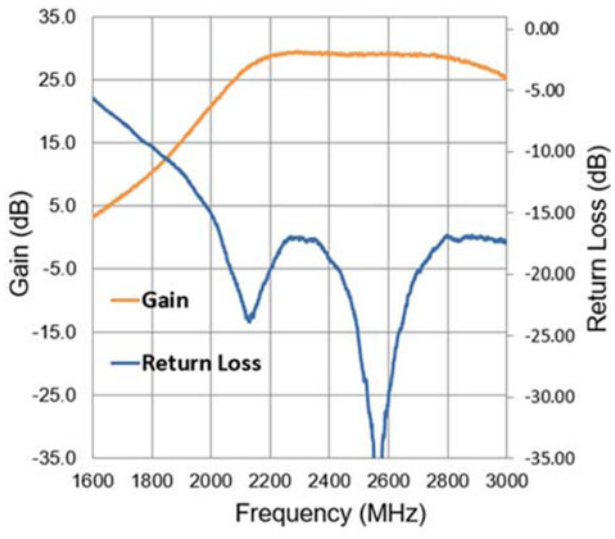

Fig. 24. Measured *S*-parameters on the board.

to 35 dBm average power. This is the typical test case scenario requested by BTS equipment manufacturers for 2 GHz true dual-band application. Moreover, to proof also the PA capability for multiband application, a 3cLTE 20 MHz 8 dB PAR modulated signal at the operating power was linearized in the three bands B1, B2, and B3. Generalized memory polynomial [22] and dynamic deviation reduction Volterra [23] series are widely used to model PA nonlinear dynamical behavior [24]. As DPAs have different power operating regions it is interesting to use piece-wise model as the VS-GMP model [25]. This allows to decompose the DPA behavior in the sub-region depending on the magnitude of the output power and models this region with different coefficients. This is a more effective approach to linearize strong nonlinear PAs without degrading the efficiency. An in-house DPD based on an algorithm of [25] is used with the following model: nonlinear order of 9, memory depth of 11, cross term of 3, and number of regions of 5. From a hardware point of view RF generator is used to generate the pre-distorted signal and a spectrum analyzer is used as feedback path, coefficient calculation is made thanks to signal processing software (Fig. 12).

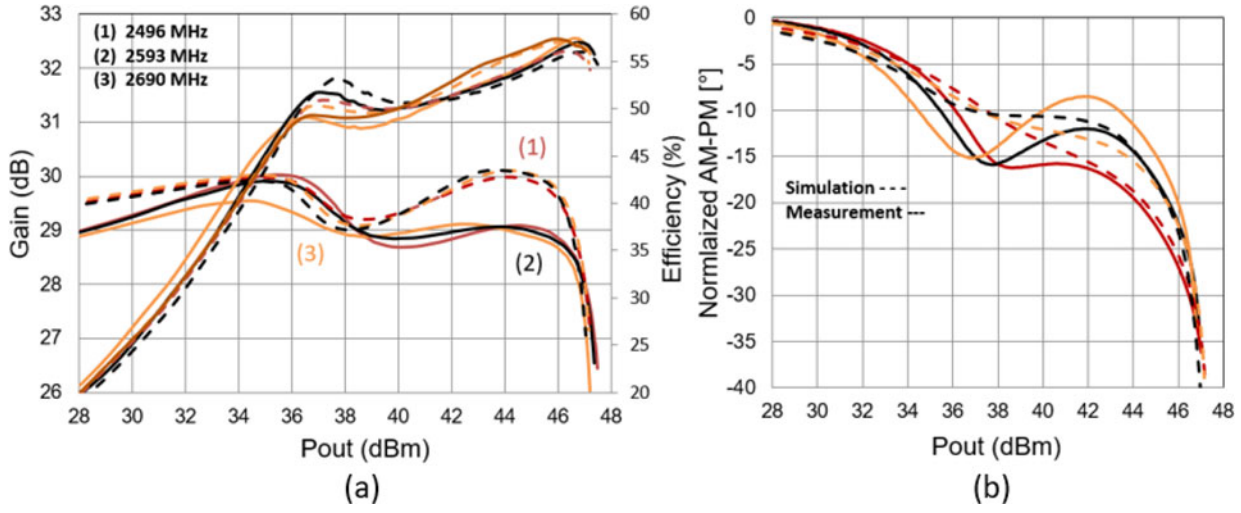

Fig. 25. Large signal RF performances of the 55 W 2.6 GHz DPA: (a) AM/AM and pulsed-CW efficiency (b) AM/PM.

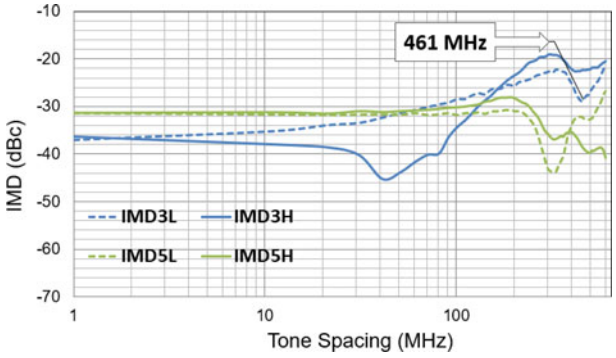

Fig. 26. Measured IMD3 and IMD5 at constant output power (39 dBm) for various two-tone spacing.

To confirm that this PA is suitable for industry application and that the chosen DPD model is not too complex (DPD complexity is hard to judge between different algorithms even if common number of coefficients or operation are used when they are disclosed). A commercial DPD is used. It achieves standard results with realistic solution and physical implementation (trade-off ASIC power consumption and DPD complexity). The same results are achieved.

Result in Fig. 13 displays ACLR below −56 dBc after DPD correction with an efficiency measured at 29%. This performance demonstrates that this PA is highly linear and can handle B1 and B3 bands simultaneously. Moreover, ACLR results can be improved with 2D-DPD [26].

In line with the expectations, this DPA is also suitable for multiband application, it is highly linear, always below −58 dBc (Fig. 14(b)) for 60 MHz IBW in each sub-band B1, B2, and B3.

Discussion of measurement results

Most publications focus only on final stage PAs to address multi-band/dual-band application at 2 GHz in LDMOS and GaN (Table 2) while driver application conditions are rarely considered. It appears that GaN solution is the easiest technology solution to address this concurrent dual-band final application for high power due to low C_{DS}. The DPA of this study represents a good compromise among linearity, efficiency, and compactness with excellent reproducibility [27]. In fact, the total linearized dual-band line-up efficiency at 8 dB OBO of a final stage in GaN as reported in [18] using the DPA of this study as the driver stage would result in 41%. Although the use of a classical class AB driver PA [28] would lead to a total line-up efficiency of only 38%, with even a larger matching area on the PCB. This clearly shows the potential of this study for base station manufacturers to save energy consumption and matching space of their overall line-up.

Table 2 compares this study with published DPA in the same frequency band, which present multiband or dual-band linearized results. As wideband linearized efficiency is the most stringent performance to achieve at 2 GHz telecommunication band it is misleading to compare DPAs without this key parameter. Compared to LDMOS-integrated DPA achieving 400 MHz RF bandwidth this study presents more than 20 dB higher gain for the smaller package. Compared to the newest three-way iDPA [16] which is designed for linearity this study achieves the same level of linearity for multiband application. The research presented in [16] achieved outstanding efficiency at 12 dB back-off. Compared to our study we need to balance the fact that to achieve 27 dB gain there are driver stages which have a non-negligible impact on the line-up efficiency and the fact that the linearized efficiency is for wider IBW. Then the PA presented in [29] highlights the complexity to realize dual-band DPA with LDMOS technology compared to GaN discrete solution [18]. Comparing linearized ACLR of this study and the GaN PA [18] for concurrent dual-band operation, it demonstrates the suitability of this architecture to answer simultaneously to these base station requirements: linearity, efficiency, compactness, and cost. To the best of author's knowledge, this is the first three-way multi-stage fully integrated DPA to address simultaneously two sub-band application at 2 GHz in LDMOS technology. Thanks to the implemented architecture concurrent band operation usually realized with GaN technology is reached with LDMOS.

m-MIMO 55 W 2.6 GHz DPA

This section presents the implementation of the three-way Doherty architecture in a 55 W 2.6 GHz DPA for

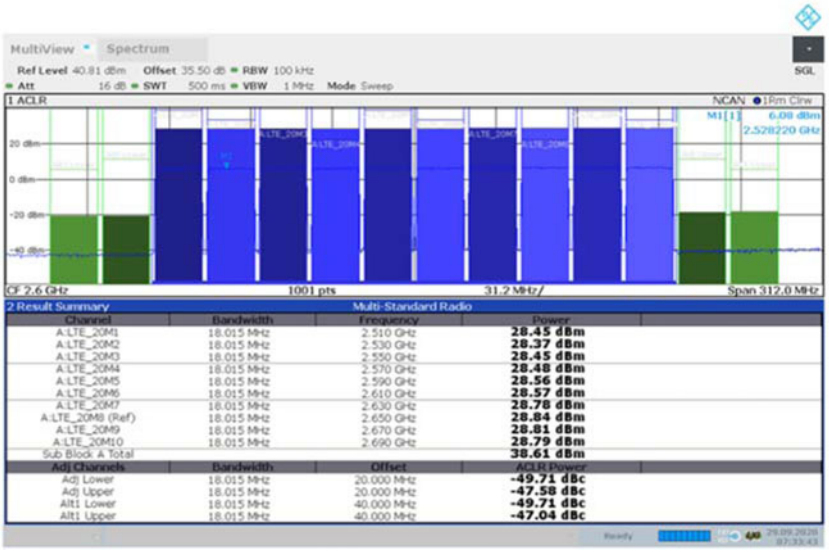

Fig. 27. ACLR result after DPD correction for 10cLTE 20 MHz at 2.6 GHz.

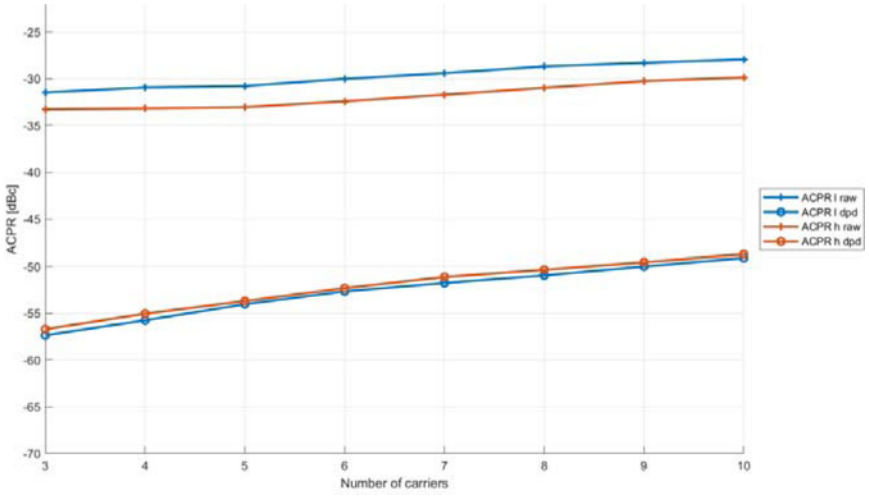

Fig. 28. ACLR result after DPD correction versus number of carriers at 39 dBm at 2.6 GHz.

massive-MIMO final stage applications, targeting for example 64 transceiver 320 W AAU in B41 band (2496–2690 MHz). The DPA is also based on a multi-stage LDMOS MMIC for high line-up gain, as described earlier. However, here the compactness is pushed another step further as the DPA is fully integrated into an $8 \times 8\ mm^2$ plastic over a molded plastic PQFN package. This brings additional thermal constraints along, due to the maximum temperature limitations in the application, which is a real challenge for LDMOS technology. High efficiency therefore also becomes thermally an important factor as the absolute dissipated power needs to be limited. Furthermore, the high compactness leads to an increasing impact of parasitic EM coupling inside the package, which results in an unwanted but significant frequency dispersion in measurements, and therefore to reduced linearizability. An improved simulation approach will be discussed to take those effects more precisely into account. Measured results of two different DPA design variants are evaluated to compare the impact to simulations. As an outcome, an excellent simulation to measurement predictability was achieved for a complex three-way, multi-stage integrated DPA.

Design and simulation

Simulation of frequency dispersion through in-package coupling effects

An increasing demand for compactness and wideband RF performance inevitably leads into an increasing importance of in-package parasitic coupling effects between the silicon LDMOS MMIC, bond wires and external connection to the package. Especially, the presence of a multitude of bond wires to realize the Doherty combiner and connections for output and input of the DPA inevitably causes EM-fields spreading over the die and consequently parasitic coupling. With higher compactness, the active and passive components inside the package will become closer and closer to each other, thus their interaction due to EM coupling increases. Especially, the combination with a high line-up gain of the multi-stage MMIC, which on some points of the die easily exceeds 35 dB, presents a severe challenge to handle from design point of view. One must consider that at 35 dB of gain, typically an isolation of better than −60 dB is required to avoid influence of unwanted coupling effects. However, a simple

Table 3. Performance comparison of integrated DPAs for 2.6 GHz

Freq (GHz)	2.6	2.65	2.6	2.655	2.6	2.5–2.7	2.5–2.7
Pavg (dBm)	33.3	33.1	31	35.6	37.4	34	39.0
Max gain (dB)	11.8	12.6	27	30.9	15	32	30
DPD signal	1cLTE 10 MHz	1cLTE 10 MHz	6cLTE 10 MHz	1cLTE 10 MHz	1cLTE 10 MHz	3cLTE/10cLTE 20 MHz	8cLTE/10cLTE 20 MHz
PAR (dB)	6.5	7.2	9	7	6.5	8	8
DPD Eff (%)	41.9	49	41	46.8	55.5	42/NA	50/49
ACLR DPD (dBc)	−45.2	−51.9	−51	−49.3	NA	−55.0/−50	−50.8/−47.5
Technology	GaN	GaN	LDMOS	GaN	GaN	LDMOS	LDMOS
Reference	[42]	[43]	[45]	[40]	[41]	[44]	This study

EM simulation in the 2–3 GHz range of the passive PCB environment to access the package leads, e.g. a 50 Ω line for RF input and output connections with about 8 mm of spacing (package dimensions), already degrades the isolation close to the critical order of magnitude.

To avoid unintended frequency dispersion leading to reduced wideband linearity or loss in wideband efficiency, these effects must be taken into account during the design phase. Amplifier stability is another criterion which is strongly impacted by these effects, and thus should be carefully simulated in order to keep reasonable margins.

In a typical industrial MMIC design, integrated passives such as inductors and capacitors, are commonly simulated with 2D or 2.5D EM simulators (good tradeoff between accuracy and simulation time), while the employ of bond wires and packaging requires 3D simulators. As mentioned before, bond wires radiate their EM-field throughout the package and MMIC, and part of this field can especially be captured by integrated inductors. This undesired coupling combined with the high gain can have a significant effect on the behavior of the complete RF performance of the DPA, especially as phase and amplitude of the individual amplifiers are quite different with respect to the output signal.

In order to verify these effects in measurements, the design and realization of a first iteration MMIC DPA has been realized by using separated simulation methods, meaning 2.5D EM simulation for the MMIC, and 3D EM simulation for the wires. As a consequence, one omits any impact of parasitic coupling effects. The measured results shown in Fig. 15 reveal that despite of a low frequency dispersion in simulation, especially the behavior of the two peaking amplifiers is heavily altered (characteristics for $P_{out} > 38$ dBm), leading to a strong amplitude and phase dispersion in addition to a low P3 dB, as a consequence of out-of-phase power combination. On the other hand, the carrier amplifier, seen by characteristics for $P_{out} < 36$ dBm of output power, shows good wideband RF performance as expected from the simulation. As is the PA is not industrialized.

After a detailed investigation to align the simulation results with the measurement, it has been found that the main contributor is the crosstalk between bond wires that compose the output combiner and the integrated passive structures on the silicon MMIC, thus confirming the significance of the more detailed simulation analysis to take these effects correctly into account.

Hence, a full 3D simulation flow has then developed and applied in order to anticipate the impact of the EM coupling. An example of the design flow is shown in Fig. 16 where inductors and wires are used at the same time in a full 3D EM simulator to evaluate their contribution.

By simulating the EM-coupling it is possible to correctly predict the measured performances of the first DPA shown before, thus allows optimization of the integrated MMIC circuitry to mitigate or compensate for the parasitic impact. Each inductor coupling can have a specific impact on the overall performance of the circuit depending on its physical location and functional location in the circuit schematic. Figure 17 shows the impact of different implementations of integrated inductors on the simulated output power dispersion (gain dispersion) of the two peak amplifiers over frequency when EM-coupling is taken into account by full 3D EM-simulations. One can see that the gain slope over frequency changes drastically by about 2 dB at low frequencies for the peak 1 amplifier, and several dB at high frequencies for the peak 2 amplifier, thus causing an imbalance in the power contributions of the Doherty, leading to characteristics presented in Fig. 14. It can also be seen that a correct simulation of the coupling allows to mitigate or compensate its impact by adapted MMIC design, in this case almost perfectly for the peak 1 amplifier, and partially but sufficiently for the peak 2 amplifier. The outcome of these improvements will be shown in the "Measurement results" section. Further comparison of final measurement results versus simulation data of the full Doherty will be completed in "Measurement results" of this section.

Another area of improvement was seen in stability and stability margin of the overall amplifier. By modifying integrated inductors inside the splitter and therefore impacting the phase shifting, the loop gain shows an important improvement, thus significantly improved the *K*-factor in small signal operation (Fig. 18). Note that this behavior is mainly related to the carrier amplifier, which showed no significant alteration of its large signal behavior (Fig. 15). Even so the simulated and measured small signal stability does not fit perfectly, the prediction of the relative improvement is very good from practical point of view, and design improvements to compensate for parasitic coupling effects are very well predicted by the new simulation flow.

Low frequency resonance optimization

To handle 200 MHz IBW in band B41 a similar circuitry is applied in this design as in the 60 W 1.8–2.2 GHz DPA presented in the previous section (*L*–*C* resonator). However, in this design extra dedicated attention is put on the PCB to reduce the parasitic inductance of the drain feeder and to optimize the drain bias network decoupling on linearizability. With the increase of the IBW

the impact of the remaining inductance of the drain feeder (RF-shorted $\lambda/4$ stub) is not negligible in baseband as shown in Fig. 19. As presented in [30] an interesting solution to reduce replace the $\lambda/4$ feeder is to use L–C discrete component. However, due to high Q of an L–C resonator it impacts PA performances for wideband signals. The main issue is that SMD inductor values are limited for a given current. Consequently, as shown by the simulations, in this study an optimized PCB configuration including a double drain feeder is used to increase the LFR by 20%, while simultaneously reducing the impedance level frequencies below the resonance, which is a significant improvement and has a positive impact on efficiency and linearity [31].

As mentioned previously, the simplest rule to estimate the VBW of a PA is to divide the value of the LFR by a factor of 2. Then, a VBW of around 400 MHz is expected. In view of 200 MHz of IBW this is expected to strongly improve the linearizability of that device.

Behavioral model for linearizability simulation

The importance of the tradeoff between linearity and efficiency is fundamental for any wideband PA used in base station applications. Although efficiency can easily be analyzed by a classical simulation approach, linearity or even linearizability of the PA is much more complex to anticipate. This is mainly due to the multitude of parameters which affects this amplifier characteristic, comprising gain slope over output power (AM/AM) [32], phase variation over output power (AM/PM) [32, 33], output power group delay, and finally memory effects with short and long time constants. All these parameters influence the capability of a DPD system to reach a clean and linear output signal, in particular when the IBW extends beyond 100 MHz. Many studies have been conducted to improve the raw linearity of RF PA, especially AM/PM nonlinearity [34–38]. Moreover, raw linearity given through third order intermodulation product or raw ACLR for modulated signal is no clear indicator for a good linearizability by DPD systems. Even if DPD algorithms are more and more powerful, it is a big challenge to achieve wideband DPD [1] while maintaining high efficiency. For the MMIC process, which has a long manufacturing time, it is highly important to be able to predict in simulation which level of ACLR after DPD that can be achieved as in Fig. 20.

Indeed, usually a DPD measurement is one of the last tests realized during measurement, while at the same time noncompliance with 3GPP and FCC linearity norms are a showstopper. Consequently, if the PA is not linearizable in application, a new and very time-consuming full design iteration is needed, which can take up to several months and is a critical factor in industry. Implementing a DPD simulation in the design flow, and to predict ACLR after DPD in simulation, allows directly to evaluate the design before even starting the fabrication.

Over time many workflows have been tried to predict linearizability, using harmonic balance or envelope simulation, but none of them were conclusive, too time consuming, or not accurate enough for wideband signal and complex PA architectures.

Here, a different approach has been implemented to model the DPA response in a mathematical way. The RF response of the DPA is extracted from harmonic balance simulation and a behavioral model is built based on a parallel Hammerstein model [39]. All the complex circuitry is replaced by a black box where for a given input, an output is generated. To predict the linearizability of this 2.6 GHz PA a VS-GMP DPD algorithm [25] is applied to the extracted behavioral model, simulated at 8 dB output power back-off like in the real application.

In the center of the B41 band the simulation predicts an ACLR of around −47 dBc for 10cLTE with 8 dB PAR as shown in Fig. 21. Those results are very encouraging even if baseband effects are not considered. But one can mitigate this lack of accuracy knowing that the baseband response, such as LFR, is optimized by design and pushed toward high frequencies, to assure that the baseband response does not become a mayor limitation for the DPD.

Measurement results

The PA is assembled in a low-cost reliable compact plastic package ($8 \times 8\ mm^2$ PQFN). The overall circuit is implemented on a PCB using an RO4350B substrate of 20 mils thickness. Copper baseplate for heat dissipation is soldered directly at the backside of the PCB as shown in Fig. 22. The effective matching area is compact, $19 \times 23\ mm^2$, and only two gate biases are used to supply carrier, peak 1 and peak 2 amplifiers to be more compact and easier to integrate at the system level.

Measurements are performed at ambient temperature 25°C. Drain voltage (V_{DS}) is set to 28 V while the gate of the carrier is set to 2.165 V, for a quiescent current of 42 mA.

The PCB is tuned to the maximum power load impedance of the DPA MMIC for best linearization capability, which also is close to best efficiency in 2496–2690 MHz B41 band as shown in Fig. 23(a).

As shown in Fig. 23(b), the output impedances of the package present very low Q-factor ($Q < 0.33$) at the high impedance level, with low dispersion over frequency, despite of the high output power. This is very beneficial to ease the matching and reduce PCB losses.

For m-MIMO 5G application, RF performances must be balanced between high efficiency and linearity. S-parameter measurements shown in Fig. 24 confirm that the three-way DPA can achieve wide small-signal bandwidth and has a flat gain of 29 dB over 400 MHz which eases the DPD linearization. The input matching to 50 Ω is integrated in the device and yields a return loss better than −20 dB from 2.4 to 2.7 GHz.

AM/AM and AM/PM results shown in Fig. 25(a) depict a very low frequency dispersion over the full dynamic range. They confirm all the previously discussed improvements achieved in simulation to correctly predict and account for parasitic EM-coupling effects between wires and MMIC inductors inside the package.

Pulsed-CW measurements show a P3 dB of at least 47.1 dBm and an efficiency above 50% at 9 dB OBO. Moreover, due to the three-way Doherty architecture, a high efficiency is maintained up to 10–11 dB OBO. As a result, at the targeted average output power of 39 dBm, the average efficiency measured with narrow band modulated signals (20 MHz LTE) is above 50% over all the frequency band. The good phase consistency, as displayed in Fig. 25(b) (AM/PM), is also highly in favor for wideband linearizability. Moreover, comparing to the simulated performance, there is a good fit of the efficiency and of the AM/AM behavior even if the peaks have lower gain. Measured AM/PM has phase inflexion, this is mostly coming from the splitter delay which could be adjusted on another iteration. Recovering the simulated AM/PM behavior should also impact the AM/AM response in the good way.

The VBW was measured at 39 dBm through an IMD resonance test (Fig. 26). An IMD3 resonance at 461 MHz was found,

very well in line with the simulation and optimization of the LFR by improved and drain feeder network PCB layout. This result is favorable for managing linearization of wideband modulated signals up to 200 MHz, as required by the application.

Linearity and digital pre-distortion correction results

Linearization is performed with the same setup compared to that in the previous section using a 10cLTE 20 MHz signal (200 MHz IBW) at 39 dBm of output power (8 dB PAR). This is the typical test case scenario requested by BTS equipment manufacturers for 2.6 GHz m-MIMO application.

Result in Fig. 27 displays ACLR below −47.5 dBc after DPD correction with an efficiency measured at 49%. For 8cLTE 20 MHz (160 MHz IBW), the same device yields 50% efficiency with −50.7 dBc ACLR linearized after DPD. This performance respects the ACLR below −45 dBc 3GPP norm and spectrum emission mask. This confirms the capability of this three-way fully integrated DPA to achieve high linearized efficiency over wideband modulated signal for 5G application.

A sweep of number of carriers (20 MHz LTE) at 2.6 GHz is done from 3 to 10 in order to compare the results to the simulation results. Even so we do not observe a perfect fit for narrowband signals, which can be related to the noise level generated by the pre-amplifier in the measurement setup, for wideband signals the prediction is quite good, especially knowing how delicate it is to predict, model, and anticipate DPD results (simulation is shown in Fig. 21, measurement is shown in Fig. 28).

Discussion of measurement results

Table 3 compares this study with the literature for DPAs at 2.6 GHz which include linearized m-MIMO signal results. Comparing to GaN DPAs [40–43] (only narrow band single carrier 10 MHz results are shown) this study achieves higher linearized efficiency for wider modulated signals (up to 200 MHz), and with 20 dB more gain. Moreover, as mentioned before, in this study the power consumption of the integrated driver stages is already taken into account (line-up efficiency), which is a severe difference compared to low gain single stage DPAs (drain efficiency). However, in terms of pure RF bandwidth the studies achieved in [40–43] are more broadband. The DPA [41] exhibits best drain efficiency before DPD even if the back-off region is reduced only at 6.5 dB, but the gain is 15 dB lower than that for our study. Estimating a line-up efficiency for comparison, for a driver with 30% efficiency to reach a line-up gain close to the one presented in this study with the DPA [41], the full line-up efficiency would be around 50% which is close to our MMIC one, even lower (48%) using a driver with 20%. Now compared to other DPAs realized in LDMOS with similar high gain, which also present linearized efficiency for wideband signals (160 MHz/200 MHz with high PAR 8–9 dB) this study shows slightly lower gain compared to DPAs [44, 45], around 1–2 dB below. The DPA [44] is more linear for 200 MHz LTE signals compared to this study. However, the presented design presents by far the highest linearized efficiency for 5G m-MIMO applications, with more than 49% efficiency after DPD.

From the best of author's knowledge (Table 3), this is the first published three-way fully multi-stage integrated DPA in such a compact package to address 5G application in the RF industry. In comparison with other DPA solutions at 2.6 GHz, the presented integrated three-way LDMOS DPA is a state-of-the-art solution for highly linear and efficient 5G m-MIMO applications with efficiency well comparable to GaN DPAs.

Conclusion

A fully integrated three-way Doherty architecture implemented in 28 V LDMOS MMIC technology has been presented to answer 5G high performance requirements and challenges. Through this paper investigations and solutions for several critical design challenges are elaborated such as how to improve the instantaneous signal bandwidth through bias network resonance (LFR) and baseband optimization, EM-coupling effects affecting the frequency dispersion and an improved DPD simulation approach for accurate prediction of linearizability. The Doherty combiner is fully integrated by the use of a C_{DS}–L_d–C_{DS} network, leveraging on the C_{DS} absorption principle to achieve the required wideband impedance transformation and high compactness at the same time.

The huge market request behind the release of 5G all over the world pushes PA manufacturers and designers for innovation and new solutions to better satisfy the requirement of these new AAU systems used for massive-MIMO. In answer to that, two suitable Doherty PA candidates to satisfy these demands are presented in this study, a true dual-band 60 W 1.8–2.2 GHz DPA for ultra-linear wideband driver applications with high average efficiency of 27% in deep back-off of more than 13 dB OBO, and a 55 W 2.6 GHz DPA in a compact 8 × 8 PQFN plastic package for use in final stage massive-MIMO AAUs for 160 and 200 MHz IBW multi-carrier LTE signals with a linearized average efficiency of up to 50% at 39 dBm output power level. Measurement results of both DPAs demonstrate the capability of this architecture to achieve high linearized efficiency for wideband modulated signal with a fully integrated compact solution. Moreover, in industry, LDMOS-integrated circuits present the high benefit to achieve reliable performances, with low component variation for part to part or reliability. At 2.6 GHz for the first time a 55 W LDMOS Doherty PA was successfully implemented in a compact and low cost 8 × 8 PQFN plastic package thanks to its high efficiency, which can be considered as a game changer for cost. In comparison with other published data in the same frequency bands, the achieved results, thanks to the three-way LDMOS-integrated DPA architecture, represented the state-of-the-art for 5G massive-MIMO application, even comparable to GaN solutions.

Supplementary material. The supplementary material for this article can be found at https://doi.org/10.1017/S1759078721000131.

Acknowledgement. The authors would like to thank all Ampleon colleagues and partners who contributed to this study, last but not least our customers, ever inventing higher and higher performance requirements which keep us striving for new design solutions.

References

1. **Chuang K** (2020) A perspective on linearization and digital pre-distortion for wireless radio systems. *IEEE Topical Conference on RF/Microwave Power Amplifiers for Radio and Wireless Applications*.
2. **Pengelly RS, Wood SM, Milligan JW, Sheppard ST and Pribble WL** (2012) A review of GaN on SiC high electron-mobility power transistors and MMICs. *IEEE Transactions on Microwave Theory and Techniques* **60**, 1764–1783.
3. **Nuttinck S, Gebara E, Laskar J, Rorsman N, Olsson J, Zirath H, Eklund K and Harris M** (Aug. 2002) Comparison between Si-LDMOS and

GaN-based microwave power transistors. IEEE Lester Eastman Conference on High Performance Devices.
4. **Theeuwen SJCH, Mollee H, Heeres R and Van Rijs F** (2018) LDMOS technology for power amplifiers up to 12 GHz. *13th European Microwave Integrated Circuits Conference*.
5. **Grebennikov A and Bulja S** (2012) High-efficiency Doherty power amplifiers: historical aspect and modern trends. *Proceedings of the IEEE* **100**, 3190–3219.
6. **Gajadharsing JR** (2009) Recent advances in Doherty amplifiers for wireless infrastructure. *IEEE MTT-S International Microwave Symposium Workshop*.
7. **Giofrè R, Piazzon L, Colontonio P and Giannini F** (2013) A Doherty architecture with high feasibility and defined bandwidth behavior. *IEEE Transactions on Microwave Theory and Techniques* **61**, 3308–3317.
8. **Giofrè R, Piazzon L, Colontonio P and Giannini F** (2014) A closed-form design technique for ultra-wideband Doherty power amplifiers. *IEEE Transactions on Microwave Theory and Techniques* **62**, 3414–3424.
9. **Moreno Rubio JJ, Camarchia V, Pirola M and Quaglia R** (2018) Design of an 87% fractional bandwidth Doherty power amplifier supported by a simplified bandwidth estimation method. *IEEE Transactions on Microwave Theory and Techniques* **66**, 1319–1327.
10. **Liu H, Fang X and Cheng KM** (2020) Bandwidth enhancement of frequency dispersive Doherty power amplifier. *IEEE Microwave and Wireless Components Letters* **30**, 185–188.
11. **Quaglia R and Cripps S** (2018) A load modulated balanced amplifier for telecom applications. *IEEE Transactions on Microwave Theory and Techniques* **66**, 1328–1338.
12. **Nikandish G, Staszewski RB and Zhu A** (2020) Breaking the bandwidth limit: a review of broadband Doherty power amplifier design for 5G. *IEEE Microwave Magazine* **21**, 57–75.
13. **Camarchia V, Pirola M, Quaglia R, Jee S, Chio Y and Kim B** (2015) The Doherty power amplifier: review of recent solutions and trends. *IEEE Transactions on Microwave Theory and Techniques* **63**, 559–571.
14. **Pengelly R, Fager C and Ozen M** (2016) Doherty's legacy: a history of the Doherty power amplifier from 1936 to the present day. *IEEE Microwave Magazine* **17**, 41–58.
15. **Moronval X and Gajadharsing JR** (2017) A compact 60 W MMIC amplifier based on a novel 3-way 1:2:1 Doherty architecture with best-in-class efficiency for small cells. *IEEE MTT-S IMS Symposium*.
16. **Zhang H, De Meyer S, Duvanaud C and Bachir S** (2018) A 50 W highly linear 3-way integrated wideband Doherty PA for small-cell application. *13th European Microwave Integrated Circuits Conference*.
17. **Moronval X and Gajadharsing JR** (2016) A 100 W multi-band four-way integrated Doherty amplifier. *IEEE MTT-S IMS Symposium*.
18. **Zhu N, McLaren R, Roberts JS, Holmes D, Masood M and Jones JK** (2019) Compact high efficiency high-power wideband GaN amplifier supporting 395 MHz instantaneous bandwidth. *IEEE MTT-S IMS Symposium*.
19. **Carvalho NB and Pedro JC** (2000) Two-tone IMD asymmetry in microwave power amplifiers. *IEEE MTT-S International Microwave Symposium Digest*.
20. **Ladhani H, Jones J, Staudinger J and Stevenson Kenney J** (2020) Impact of the input baseband impedance on the intermodulation distortion and linearizability of RF power transistors. *IEEE Radio and Wireless Symposium*.
21. **Barros DR, Nunes LC, Cabral PM and Pedro JC** (2019) Impact of the input baseband terminations on the efficiency of wideband power amplifiers under concurrent band operation. *IEEE Transactions on Microwave Theory and Techniques* **67**, 5127–5138.
22. **Morgan DR, Ma Z, Kim J, Zierdt MG and Pastalan J** (2006) A generalized memory polynomial model for digital predistortion of RF power amplifiers. *IEEE Transactions on Signal Processing* **54**, 3852–3860.
23. **Zhu A, Pedro JC and Brazil TJ** (2006) Dynamic deviation reduction-based Volterra behavioral modeling of RP power amplifiers. *IEEE Transactions on Microwave Theory and Techniques* **54**, 4323–4332.
24. **Wood J** (2015) Digital pre-distortion of RF power amplifiers: progress to date and future challenges. *IEEE MTTS-S International Microwave Symposium*.
25. **Afsardoost S, Eriksson T and Fager C** (2012) Digital predistortion using a vector-switched model. *IEEE Transactions on Microwave Theory and Techniques* **60**, 1166–1174.
26. **Bassam SA, Helaoui M and Ghannouchi FM** (Oct. 2011) 2-D digital predistortion (2-D-DPD) architecture for concurrent dual-band transmitters. *IEEE Transactions on Microwave Theory and Techniques* **59**, 2547–2553.
27. **BLM10D1822-61ABG data sheet. Ampleon, Netherland.**
28. **BLM7G1822S-40PB data sheet. Ampleon, Netherland.**
29. **Xu A, Lu M and Wang E** (2018) A 150 W high efficiency integrated Doherty amplifier for LTE-advanced applications. *IEEE MTT-S IMS Symposium*.
30. **Ma C, Pan W, Shao S, Qing C and Tang Y** (2013) A wideband Doherty power amplifier with 100 MHz instantaneous bandwidth for LTE-advanced applications. *IEEE Microwave and Wireless Components Letters* **23**, 614–616.
31. **Nunes LC, Barros DR, Cabral PM and Pedro JC** (2018) Efficiency degradation analysis in wideband power amplifiers. *IEEE Transactions on Microwave Theory and Techniques* **66**, 5640–5651.
32. **Nunes LC, Cabral PM and Pedro JC** (2014) AM/AM and AM/PM distortion generation mechanisms in Si LDMOS and GaN HEMT based RF power amplifiers. *IEEE Transactions on Microwave Theory and Techniques* **62**, 799–809.
33. **Nunes LC, Cabral PM and Pedro JC** (2016) AM/PM distortion physical origins in Si LDMOS Doherty power amplifiers. *IEEE MTT-S International Microwave Symposium*.
34. **Fang X, Chung A and Boumaiza S** (2019) Linearity-enhanced Doherty power amplifier using output combining network with predefined AM-PM characteristics. *IEEE Transactions on Microwave Theory and Techniques* **67**, 195–204.
35. **Zhao S, Yang L, Ren Y and Xu Y** (2019) Linearity improved Doherty power amplifier using non-foster circuits. *IEEE Access* **7**, 40109–40113.
36. **Camarchia V, Colantonio P, Giannini F, Giofrè R, Jiang T, Pirola M, Quaglia R and Ramella C** (2017) A design strategy for AM/PM compensation in GaN Doherty power amplifiers. *IEEE Access* **5**, 22244–22251.
37. **Giofrè R, Colantonio P and Giannini F** (2018) A design approach to maximize the efficiency vs. linearity trade-off in fixed and modulated load GaN power amplifiers. *IEEE Access* **6**, 9247–9255.
38. **Giofrè R and Colantonio P** (2017) A high efficiency and low distortion 6 W GaN MMIC Doherty amplifier for 7 GHz radio links. *IEEE Microwave and Wireless Components Letters* **27**, 70–72.
39. **Ngoya E, Quindroit C and Nebus JM** (2009) On the continuous-time model for nonlinear-memory modeling of RF power amplifiers. *IEEE Transactions on Microwave Theory and Techniques* **57**, 3278–3292.
40. **Kim CH and Park B** (2016) Fully-integrated two-stage GaN MMIC Doherty power amplifier for LTE small cells. *IEEE Microwave and Wireless Components Letters* **26**, 918–920.
41. **Lee H, Lim W, Bae J, Lee W, Kang H and Yang Y** (2017) 2.6 GHz GaN-HEMT Doherty power amplifier integrated circuit with 55.5% efficiency based on a compact load network. *IEEE MTT-S IMS Symposium*.
42. **Jee S, Lee J, Park B, Kim CH and Kim B** (2013) GaN MMIC broadband Doherty power amplifier. *Asia-Pacific Microwave Conference Proceedings*.
43. **Jee S, Lee J, Son J, Kim S, Kim CH, Moon J and Kim B** (2015) Asymmetric broadband Doherty power amplifier using GaN MMIC for femto-cell base-station. *IEEE Transactions on Microwave Theory and Techniques* **63**, 2802–2810.
44. **Ladhani H, Maalouf E, Jones J, Masood M and Kenney JS** (2019) A compact, 42% PAE, two-stage, LDMOS Doherty PA module for massive MIMO applications. *IEEE MTT-S International Microwave Conference on Hardware and Systems for 5G and Beyond*.
45. **Lin L, Yang L, Zheng S and Peng J** (2019) A 10 W fully-integrated LDMOS MMIC Doherty in LGA package for 2.7 GHz small cell application. *IEEE MTT-S International Microwave Symposium*.

Marc Vigneau received his master's degree in electronics from The National Institute of Electrical Engineering, Electronics, Computer Science, Fluid mechanics & Telecommunications and Networks Engineering School, France, in 2018. His role today is RF Application Engineer in Ampleon, Toulouse, France. His research interests are related to RF power amplifier efficiency and linearizability for base station.

Mariano Ercoli was born in Cascia, Italy, in 1982. He received his master's degree in electronic engineering from the University of Perugia, Italy, in 2009. He received his Ph.D. degree in millimeter wave electronic engineering from INSA Toulouse, France, in 2012, in collaboration with LAAS-CNRS in Toulouse, France. The work during Ph.D. was mainly focused on the modeling, design, and characterization of millimeter wave structures and the design of complete transceiver in RF-CMOS. His role today is Senior Principal Design Engineer in Ampleon, Toulouse, France. His research interests are related to novel energy saver power amplifier architectures for base station systems based on LDMOS and GaN.

Stephan Maroldt received his Dipl.-Ing. degree in electrical engineering from Technical University Ilmenau, Germany, in 2006, and his Doctor of Engineering from University Freiburg, Germany, in 2010, in the field of novel GaN-based switch-mode power amplifier MMICs for mobile communications. From 2008 to 2015 he was with Fraunhofer IAF, Freiburg/Germany, where his field of research covered design and technology of GaN high power devices and PAs, as well as GaAs- and GaN-based MMICs for applications in mobile communications, wireless transceivers, and radar in the microwave and millimeter-wave frequency range. In the end of 2015, Stephan joined Ampleon, Toulouse, France, where he is working on design of integrated Doherty PAs for 5G applications in GaN and LDMOS technologies.