Base Line General Overview: Building block characterization

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Overview “Building block characterization”

- Two main approaches:
  1. **Empirical approach**:
     - Objective: Provide foundation data for building hybrid device model
     - Tasks:
       - Foundation data (database):
         - Empirical mapping of large RF GaN device geometries (DoE) by means of chip & wire devices (RF GaN transistor and MOSCAP) on 2-layer PCB – Mini Pac
         - Pre-selection of RF GaN device for PA module design
       - Verification:
         - Characterization of pre-selected RF GaN transistor database with pre-matching on 2-layer PCB
         - Characterization of pre-selected RF GaN transistor database on application-like package (5-layer laminate)
  2. **Compact model improvement** (Running independently: receivable of I-project)
     - Objective: Update current RF GaN C1 compact model
     - Tasks:
       - Update of RF GaN device model by means of small devices on Mini Pac

Building block characterization summary table

	Empirical approach database	Empirical approach verification	Compact model improvement (not part of I-project)
Target	• Empirical mapping of device geometries (DoE) • Pre-selection of PA module devices	Verification of pre-selected devices	Update of RF GaN device compact model
Method	DoE characterization of large devices on Mini Pac	• Characterization of large devices with pre-matching on Mini Pac • PAM blocks characterization on application-like package (5-layer laminate)	DoE characterization of small devices on Mini Pac
Test devices	Large device Mini Pac: Chip & Wire (large RF GaN transistor and MOSCAP) on PCB (2 layer laminate)	• Large device Mini Pac with pre-matching • Large devices on 5-layer laminate	Device Mini Pac: Chip & Wire (small RF GaN transistor and MOSCAP) on PCB (2 layer laminate)

Building block characterization steps

Larger Device Characterization

1. Package design
2. Active Die Variants list
3. GaN + Moscap (Chip and Wire) variant design
4. Assembly Drawing of variants
5. Build and assembly of Mini Pac
6. Test fixture design for each package
7. Build and assembly of test fixture
8. Assembly of DUT package on test fixture
9. Measurement and characterization (LP/SP)
10. Device down selection for each sections
11. Data analysis (Model improvement topics)

1. Package design

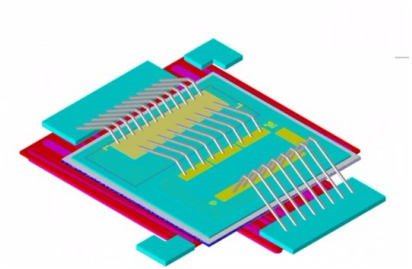
Package design

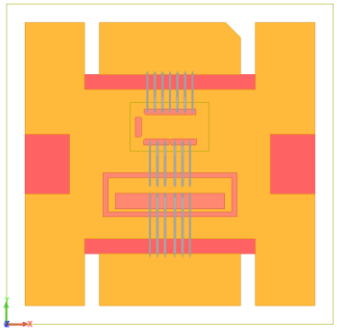
Owner: A. Shamsafar

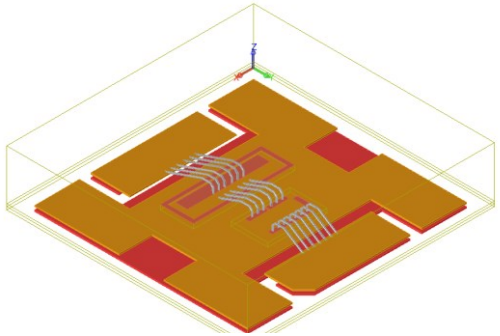
Package design for Chip & Wire (Minipack on PCB- Minipack on laminate-Ceramic package)

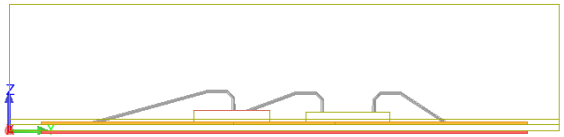
- Design package as close as final application
  - › Need to calculate bond wire shape and Moscap value
    - › The build possibly will be used as it is PA module

The reference plane will be package lead
(Empirical or Behavioral model approach)









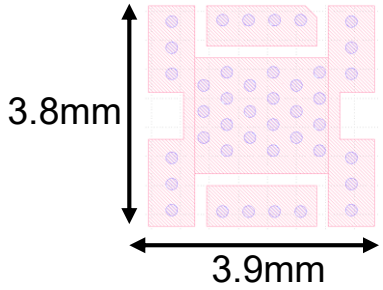
The reference plane will be package lead
(Empirical or Behavioral model approach)

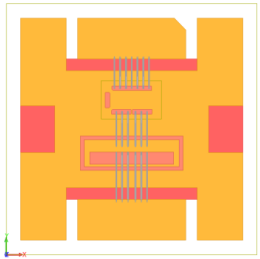
Package design

Minipack on PCB V3 (LF0004)➔ **PLP3839**

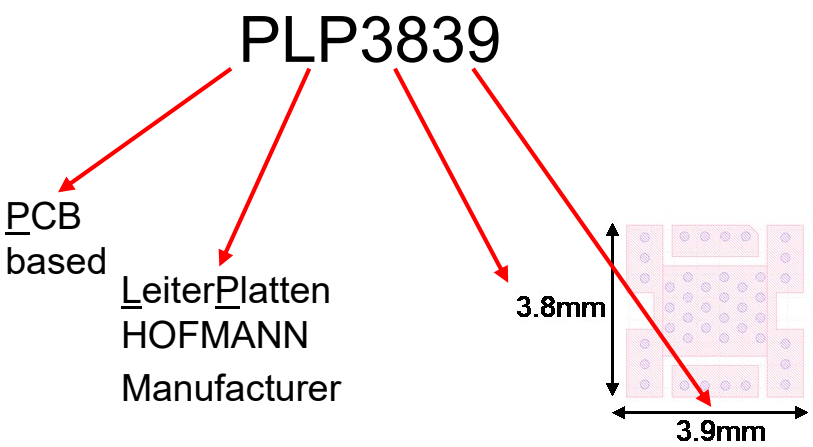
Owner: A. Levanto

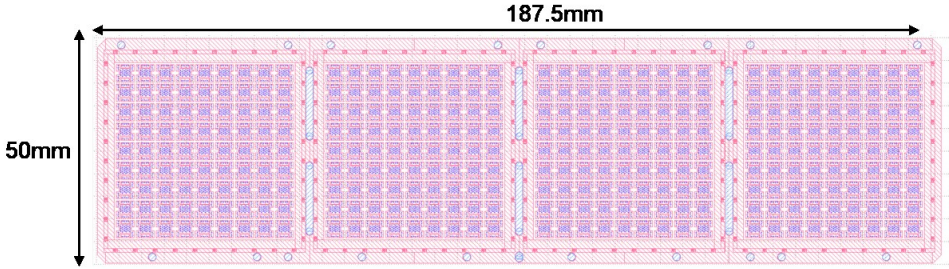
Done in MUC & RGB as initial version.
It's PCB based RO4350B (0.51mm)
Its under manufacturing (@ HOFMANN Leiterplatten)
Will be available in mid Jan 2022
20 strips (each strip include 4*9*9 package)
Size is manageable to be used as final solution in module!





Considered as our main DUT Package for now





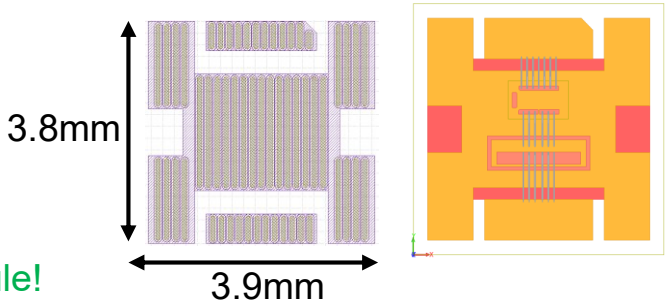
The reference plane will be package lead
(Empirical or Behavioral model approach)

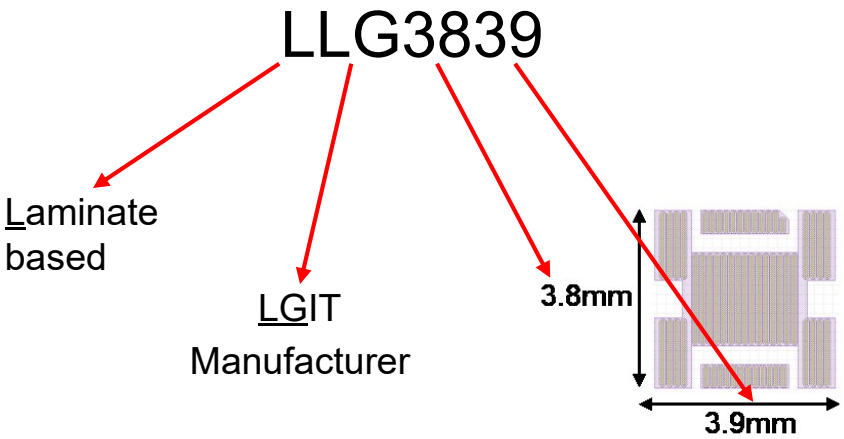
Package design on 5-layer laminate

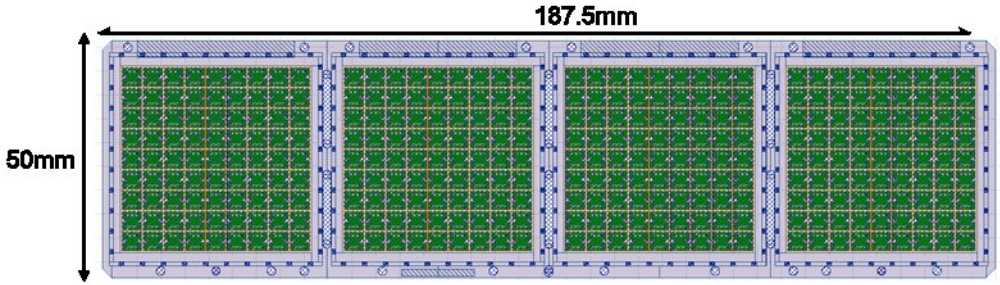
Minipack on Laminate V1 ➔ **LLG3839**

Owner: A. Levanto

Done in VIL as initial version.
It's Laminate based 5 layers laminate (same as PD3)
Its under revision (@ LGIT)
Will be available in end of Feb 2022
200 strips (each strip include 4*9*9 package)
Size and material is manageable to be used as final solution in module!







The reference plane will be package lead
(Empirical or Behavioral model approach)

Package design: device level

Minipack on PCB V1(LF0001) ➔ **LF0001**

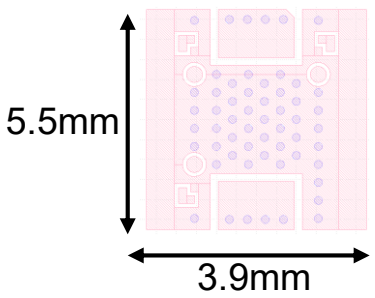
Owner: T. Canning

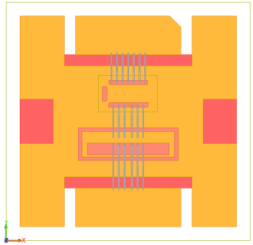
Compact model improvement - Not part of I-project

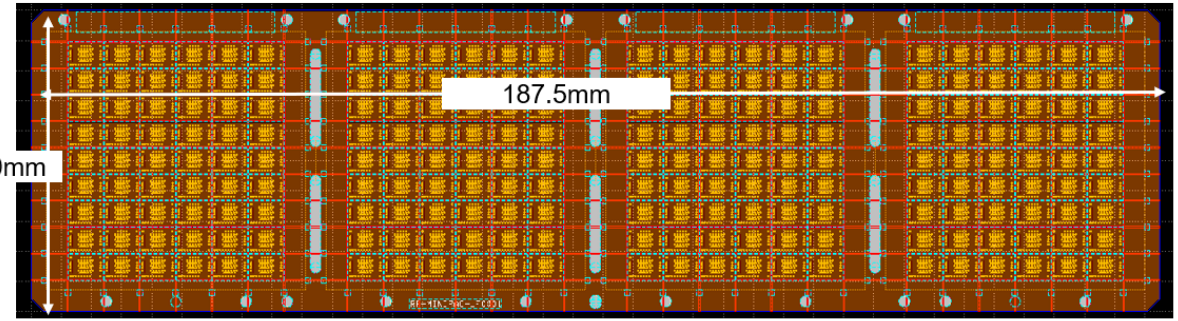
Done in RGB as first trial.

Size is big to be used as final solution in module!

The reference plane will be transistor pads (compact model improvement)







Package design: device level

Minipack on PCB V2(LF0003) ➔ **LF0003**

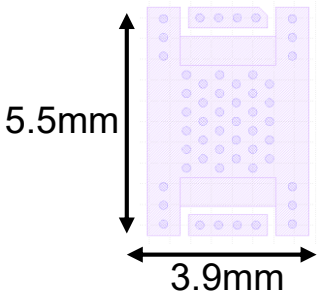
Owner: T. Canning

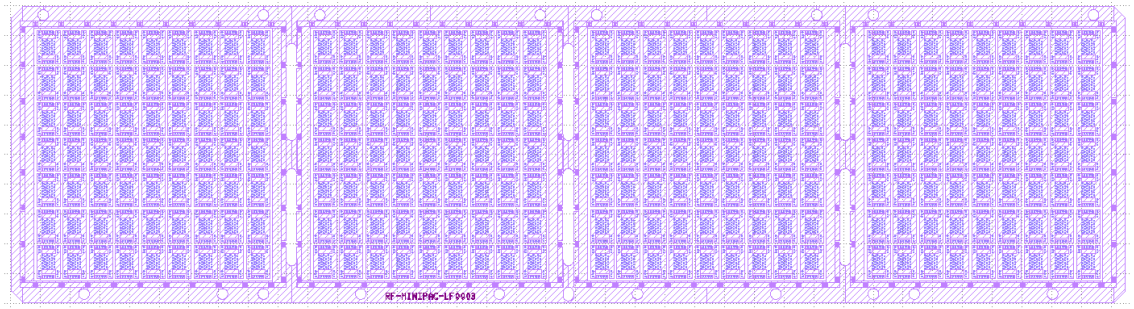
Compact model improvement - Not part of I-project

Done in RGB as improved version.

Size is still big to be used as final solution in module!

The reference plane will be transistor pads
(compact model improvement)





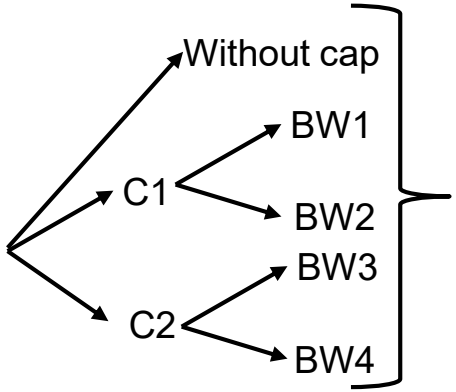
2. Active Die Variants list

Active Die Variants list

Owner: A. Shamsafar

- 5.76 (24*240um) (10-20 pcs)
- 3.84 (16*240um) (10-20 pcs)
- 10.1 (42*240um) (Not available)
- 4.8 (12*400um) (10-20 pcs)
- 12 (30*400um) (10-20 pcs)
- 3.84 (12*320um) (10-20 pcs)
- 5.12 (32*160um) (10-20 pcs)
- 5.12 (16*320um) (10-20 pcs)
- 5.76 (36*160um) (10-20 pcs)
- 4.8 (30*160um) (10-20 pcs)
- 11.52 (36*320um) (10-20 pcs)
- 10.24 (32*320 um) (10-20 pcs) ›
- 2.4 (10*240um) (Not available) ›
- 1.92 (8*240um) (Not available) ›
- ›

14 dies(6dies from PD +8 new dies)



Green: Used in PD3 A/B

Red: Will be avaialble in Jan 2022

Orange: Will be avaialble in Feb 2022

Blue : Availiable in requied quanitiy

5variants for each device size
(2 die attaches and 4 bond-wire shapes)

14*5=70 Variants

Device build prio list

1) 5.76 (24*240um) T9502A_2 (P19) available
1) 4.8 (12*400um) **R9505A P55 critical availability**, T9505A_2 availability Jan.22 (PAM -> clarification w/ Mohamed needed)
2) 5.76 (36*160um) R9505A P6 critical availability (10-20 should be ok?)
2) 12 (16*320um) ~~R9505A P4 (7.9 GD pitch) &~~ P5 critical availability (10-20 should be ok?)
3) 10.1 (42*240um) R9507A P76 not available (T9503A eo Jan.2022), R9507A P91 critical availability (10-20 should be ok)
3) 12 (30*400um) T9505A_1 availability Jan.22 (PAM -> clarification w/ Mohamed needed), R9507A P52&P104 critical availability
4) 11.52 (36*320um) R9505A P39 & P53 critical availability (10-20 should be ok?)
4) 10.24 (32*320 um) ~~R9505A P30 (7.9 GD pitch) &~~ P35 critical availability (10-20 should be ok?)
5) 2.4 (10*240um) **T9501R 2P4 not available (-> Feb. 2022)**
5) 1.92 (8*240um) **T9501R 2P4 not available (-> Feb. 2022)**
6) 3.84 (12*320um) T9504A availability Jan.22 (PAM -> clarification w/ Mohamed needed), **R9505A P13 not available** & P47
6) 3.84 (16*240um) R9505A P10 critical availability (10-20 should be ok?)
7) 5.12 (32*160um) R9505A P14 critical availability (10-20 should be ok?)
7) 4.8 (30*160um) R9505A P3 critical availability (10-20 should be ok?)
8) LDMOS (optional depend on time)
8) LDMOS (optional depend on time)

8 orders → 10 variants in each order

- Green & red:T8 process & layout
- Blue & blue: Pre T8 material

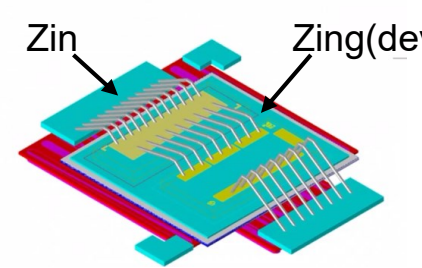
3. GaN + Moscap (Chip and Wire) variant design

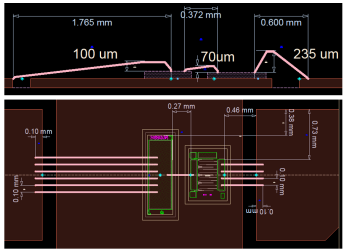
GaN + Moscap (Chip and Wire) variant design

Owner: Y. Lim

GaN + Moscap (Chip and Wire) variant design

- Design prematch for Gain-Eff improvement
  - › Need to calculate bond wire shape and Moscap value





Drawing example

Zing➔ small value (not accurately modeled or measurable),difficult to match and vary versus frequency and power

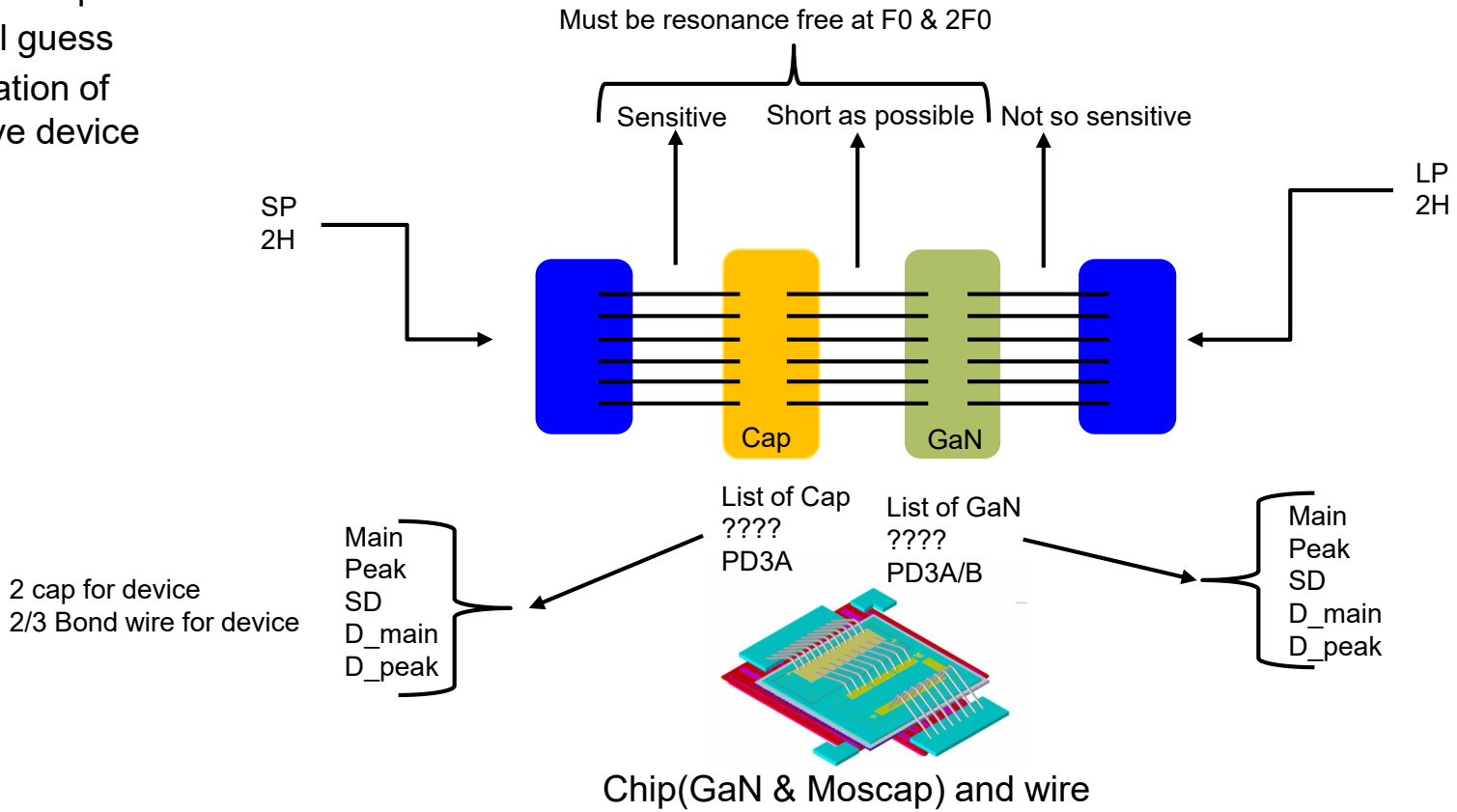
Zin➔ larger value (accurately measurable), easier to match, less changes vs frequency and power

Smith chart need to be added

Build insight

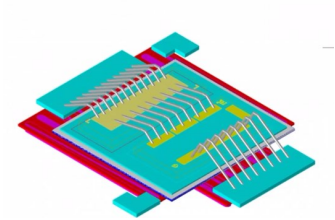
Owner: Y. Lim

Simulation of wire and Cap
Using model as initial guess
Checking and verification of Cgs/Cgd/Cds of active device
LP/SP of full section



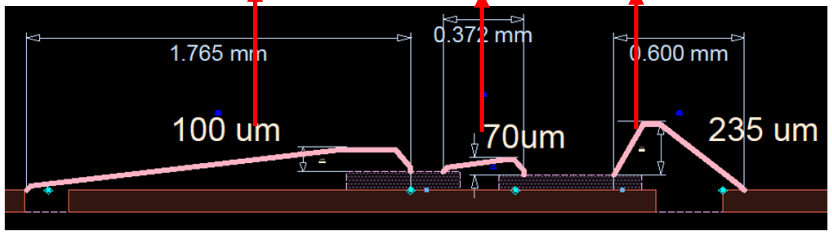
Build insight

Owner: Y. Lim



Must be resonance free at F0 & 2F0

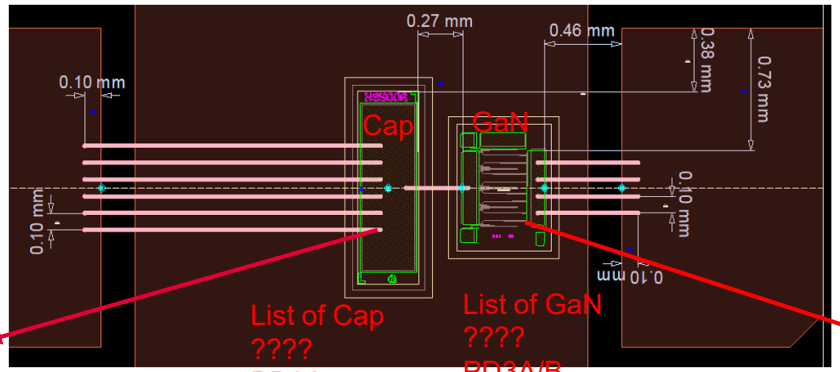
Sensitive | Short as possible | Not so sensitive



SP
2H

LP
2H

3.4GHz
3.8GHz

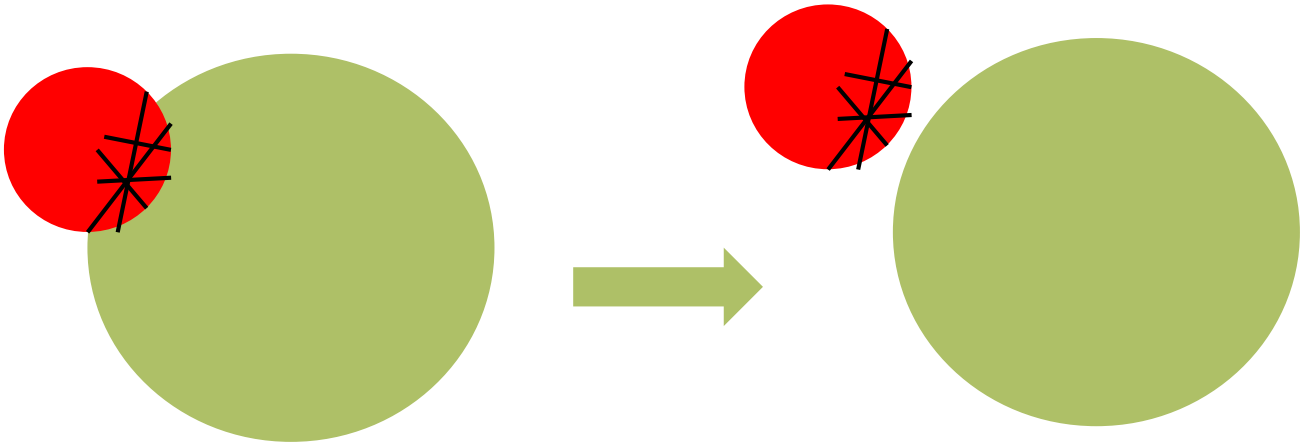


Main
Peak
SD
D_main
D_peak

Main
Peak
SD
D_main
D_peak

2 cap for device
2/3 Bond wire for device

Chip(GaN & Moscap) and wire

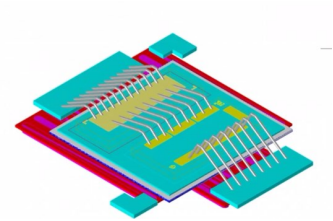


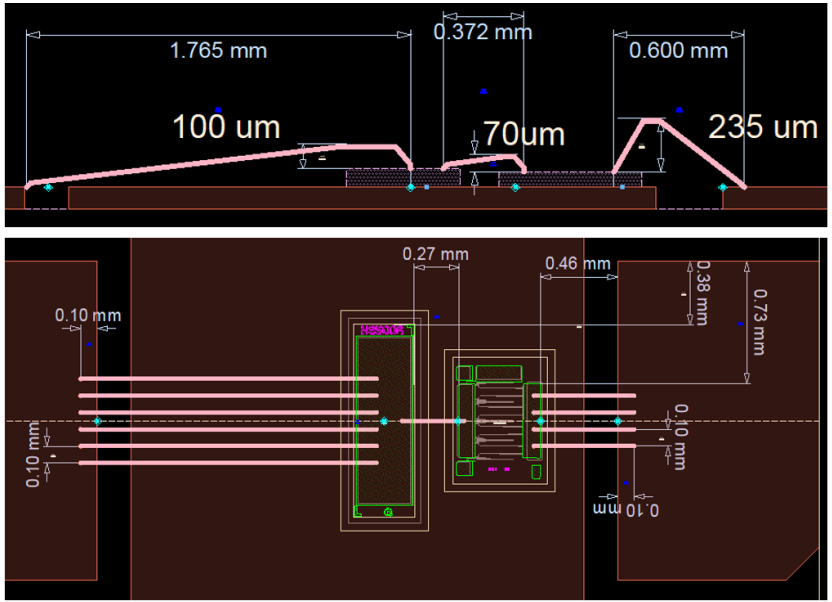
4. Assembly Drawing of variants

Assembly Drawing of variants

Owner: A. Levanto

Drawing of wires and die location of all variants
compatible with RGB (and Amkor/MSE)





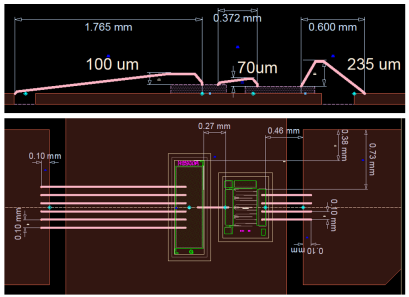
Chip(GaN & Moscap) and wire

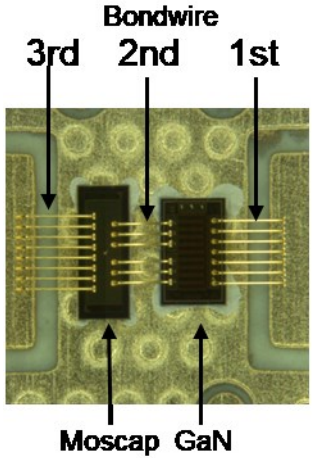
5. Build and assembly of Mini Pac

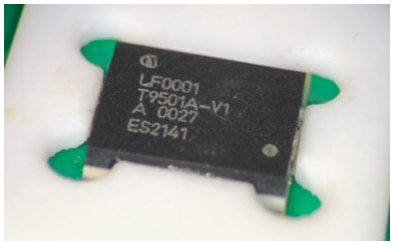
Build and Assembly

Owner: B. Goller

Build and assembly will be done in RGB
Die attached
Bonding
Molding
Laser Marking (Naming need to be decided)
Sawing
Delivery type (gel pack)





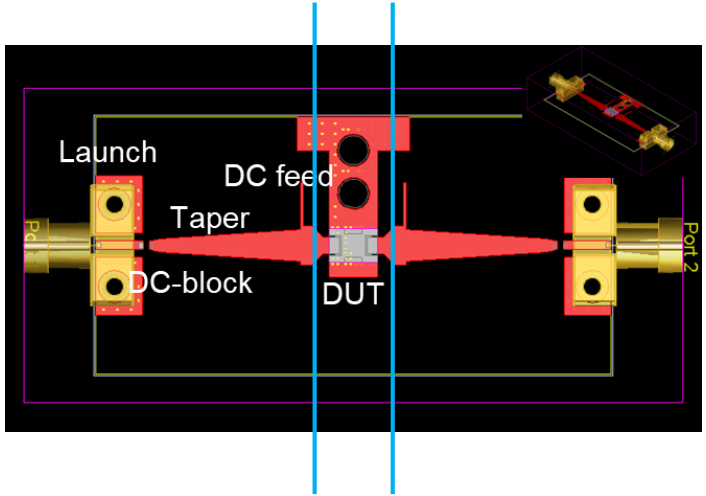


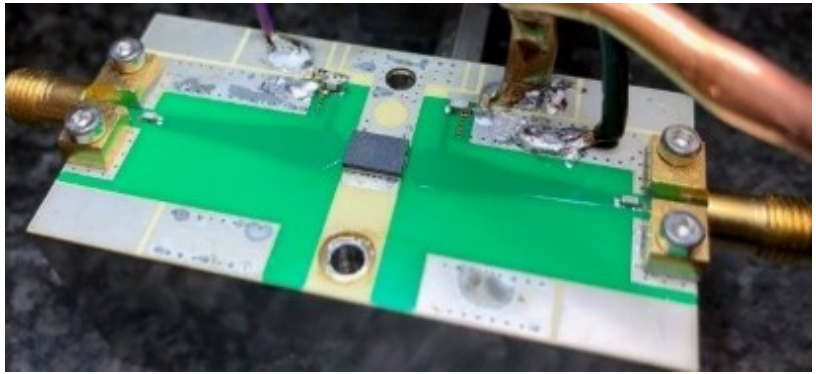
6. Test fixture design for each package

Test fixture design for each package

Owner: A. Shamsafar

Design of reliable and robust test fixture
Higher impedance transformation (More Source Pull friendly)
Thermal awareness and quality
Calibration accuracy up to 3f0
Repeatability of assembly and measurement

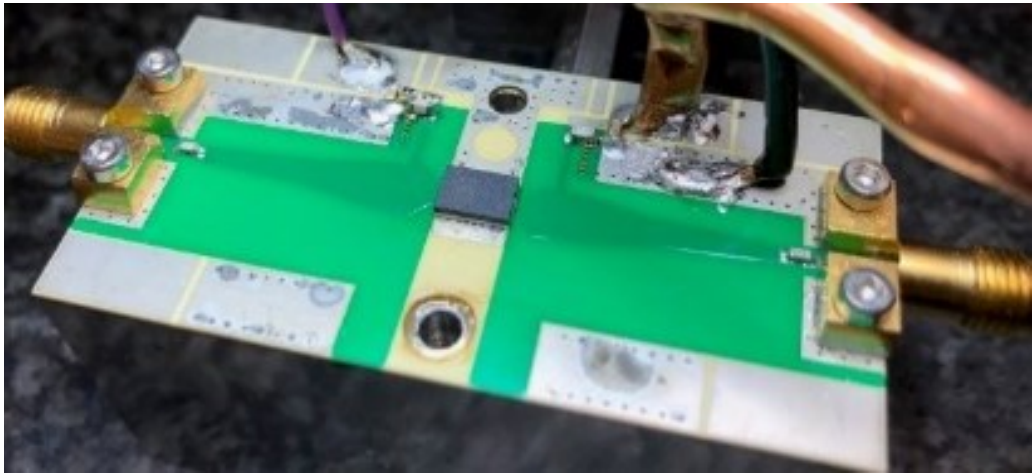




7. Build and assembly of test fixture

Build and assembly of test fixture

Owner: S. Halim



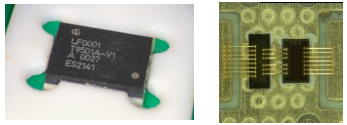
Test fixture example

8. Assembly of DUT package on test fixture

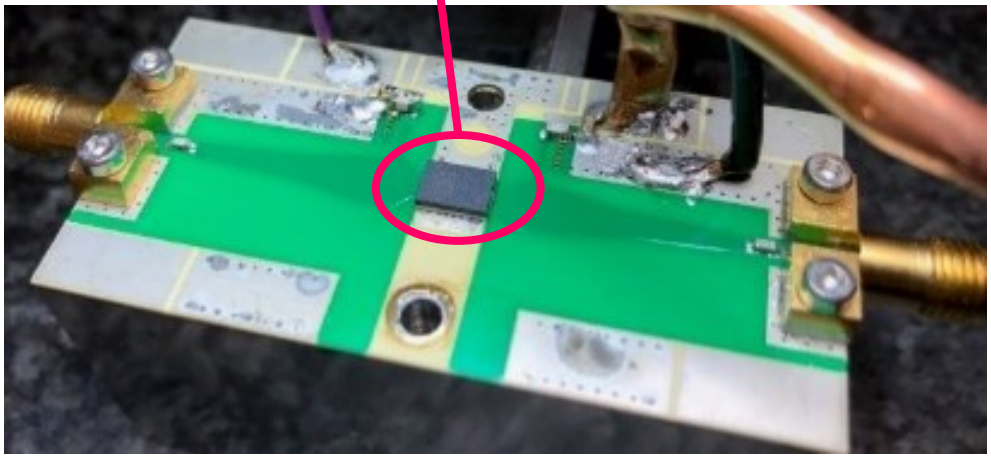
Assembly of DUT package on test fixture

Owner: B. Goller

2 possible options
Option 1 (Soldering)
Option 2 (Mechanical press)



Package(DUT)



Test fixture example

9. Measurement and characterization (LP/SP)

Measurement and characterization (LP/SP)

Owner: T. Hartig

10. Device down selection for each sections

Device down selection for each sections

Owner: A. Shamsafar

11. Data analysis (Model improvement topics)

Data analysis (Model improvement topics)

Owner: C. Musolff

Part of your life. Part of tomorrow.