Nonlinear-Embedding Design Methodology Oriented to LDMOS Power Amplifiers

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***Abstract*—In this paper, we apply for the first time the nonlinear-embedding technique to the design of power amplifiers (PAs) based on laterally-diffused metal-oxide-semiconductor (LDMOS) field-effect transistors. Such a design technique is based on setting the transistor load line at the intrinsic current-generator plane, according to well-known theoretical guidelines. Then, the selected operating condition can be transposed at any design frequency at the extrinsic transistor terminals, by means of a model of the device nonidealities, such as the nonlinear intrinsic capacitances and the linear parasitic effects. A harmonically-tuned high-efficiency class-F and a wideband class-AB PAs operating within the FM broadcasting band 88 ÷ 108 MHz based on a 10-W LDMOS are then designed and realized. To definitely assess the validity of the proposed approach for the LDMOS technology, we compare the measured performance on the fabricated PAs with the expected predictions.**

***Index Terms*—Power amplifiers (PAs), power MOSFETs, power semiconductor devices, semiconductor device measurement, semiconductor device modeling.**

I. Introduction

POWER management is one of the most critical issues in modern electronic systems. Besides reducing the energy costs, an efficiency-oriented design translates itself into a simplified cooling system, a better component reliability, and therefore, a reduction of the maintenance costs.

In the majority of electronic apparatuses, apart from the power-supply system, the electronic elements that draw the greatest part of the energy are the power amplifiers (PAs). Today, their impact on the overall energy consumption of an electronic system is of paramount importance for any kind of application, like audio [1], [2], medical [3], radiofrequency (RF) [4], [5], etc.

The use of operating classes based on a reduced conduction angle (e.g., class B and C) surely improves the efficiency, at the price of a reduction of other important parameters, such as linearity and power gain [6], [7]. New classes of operation [6]–[10] have been developed to increase the PA efficiency. They are mainly based on tuning the transistor harmonic terminations to shape the transistor waveforms and get two theoretical requirements.

1) No overlap between the output current and voltage waveforms to reduce the power dissipated on the active device.
2) No active power delivered at the harmonic frequencies.

If these conditions are both satisfied, a theoretical 100%-efficiency is achievable [7]. As an example, the switching class-E PA is a very common choice for PA operating in the megahertz range, whereas for application at RF and microwaves, class-J [11] and class-F [12] operations are largely diffused together with some architectural implementations oriented to further improve the efficiency [5], [13].

On the other hand, increasing the efficiency by harmonic manipulation typically implies conditions that may be harmful for the transistor reliability, in particular for the high electric fields induced by the peaks of the voltage waveforms [14], that have to be properly controlled to avoid any premature failure of the active devices [15]–[17].

Another drawback is related to the frequency selectivity of the matching networks, which is necessary when harmonic terminations need to be controlled. In Table I, we report some examples of state-of-art PAs. It is clear that for harmonically-tuned amplifiers, the efficiency becomes lower with respect to the theoretical values as larger design bandwidths are considered [18] because of the physical limitations of implementing the harmonic terminations over a wide range of frequencies. In some cases, the use of a reduced conduction angle condition (e.g., class-AB) may be more convenient since tuning the matching networks only at the

TABLE I
State-of-Art PAs

Year	Technology	Class of operation	Fractional bandwidth	Output power	Efficiency
2013 [18]	GaN HEMT	AB	58%	100 W	51 ÷ 61%
2014 [19]	LDMOS	E	24%	6.5 W	>60%
2014 [20]	GaN HEMT	F	0%	7.7 W	80.2%
2015 [21]	LDMOS	E	20%	>70 W	82%
2016 [22]	GaN HEMT	AB	27%	4.9 W	68% (PAE)
2016 [23]	GaN HEMT	F	62%	9 ÷ 11 W	>60%
2017 [24]	GaN HEMT	J	30%	4 ÷ 4.7 W	40 ÷ 50% (PAE)
2017 [25]	LDMOS	F^{-1}	62%	6.3 ÷ 10 W	73 ÷ 79%
This work	LDMOS	AB	20%	10 W	55 ÷ 63%
		F	0%	8 W	76%

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fundamental frequency reduces the complexity of the circuit, guaranteeing a sufficient performance over a large bandwidth.

From a theoretical point of view, the waveforms at the input and output port of the transistor in a PA are defined by considering the active device either as a switch (e.g., class E) or, more generally, as a controlled current generator. Indeed, this is a strong simplification, because in an actual device, nonlinear intrinsic capacitances, and linear parasitic effects alter the ideal device behavior and, as a consequence, hide the transistor reference plane where the proper waveforms should be implemented. Designers can deal with these effects by using some simplified models. As an example, for a class-E design, the capacitive behavior of the output port is typically modeled as either a linear or a nonlinear capacitor [15], [16], [21], according to the level of accuracy the designer wants to achieve.

In this paper, we discuss a general methodology for the design of laterally-diffused metal-oxide-semiconductor (LDMOS) field-effect transistor (FET) PAs, which exploits the waveforms measured at the current-generator plane as the starting point. Successively, by using a model of the device nonlinear capacitances and parasitic elements, we can embed their contributions and get the proper terminations at the actual device terminals. This technique is referred as *nonlinear embedding* [26], since in the most general case such models are nonlinear. Although already presented within the framework of microwave applications, we want to extend this methodology to a different kind of devices and applications, showing how it can be successfully adopted also in the field of power electronics.

With respect to conventional approaches, the nonlinear-embedding methodology does not require extensive, time-consuming load/source-pull measurements or simulations for identifying the device optimum operating condition. This is due to the fact that the optimum condition, that is univocally defined by the power-amplifier design theory for each class of operation [7], represents the starting point of the nonlinear-embedding approach. We will use this approach for the design of two different PAs oriented to FM broadcasting systems. The first PA is targeted to operate under a high-efficiency condition by using harmonic manipulation. The design of the second PA is targeted to achieve a wideband performance. Both design examples put in evidence the capabilities of the nonlinear-embedding methodology. We will also compare this design approach with conventional ones which exploit a simplified linear model of the intrinsic capacitances showing how the nonlinear-embedding methodology allows more accurate results.

Apart from being of great interest for researchers because of its continuous improvements [27]–[29], the choice of investigating the LDMOS technology is mainly related to its large diffusion in the telecommunication systems for operating frequencies up to some gigahertz [30]–[32]. Nevertheless, thanks to its generality, the nonlinear-embedding technique can be also applied to very different transistor technologies [33], [34].

II. Nonlinear-Embedding Approach

The theory of PA design [6], [7] assumes the transistor as a controlled nonlinear current generator, where, for an FET, the controlling variables are the input (gate) and output (drain) voltages according to well-known algebraic relationships [35]–[37]. This is clearly a simplistic approximation of the transistor behavior, which works well for a preliminary theoretical analysis but has severe limitations. To explain better this aspect, we can look at the general topology for an LDMOS-transistor model depicted in Fig. 1. Apart from the current generator, which is part of the so-called *resistive core*, as the operating frequency increases, we have to take into account the contribution of some intrinsic nonlinear dynamic effects. They are typically modeled as nonlinear capacitances [38] connected in parallel with the current generator, although some series resistors may also be included for improving the model predictions at the very end of the device bandwidth [39]. The current generator together with the capacitive network constitute the intrinsic device for which we define the *intrinsic reference plane*. To get to the actual device terminals, the so-called *extrinsic reference plane*, there exist some structures (bonding wires, package, etc.), that introduce linear parasitic effects that must be also considered. All these elements tend to hide the device current generator as the operating frequency increases, making it practically impossible to directly control and obtain the desired waveforms at its terminals, as defined by the design theory. This aspect may become of crucial importance, especially when harmonic tuning has to be performed [40].

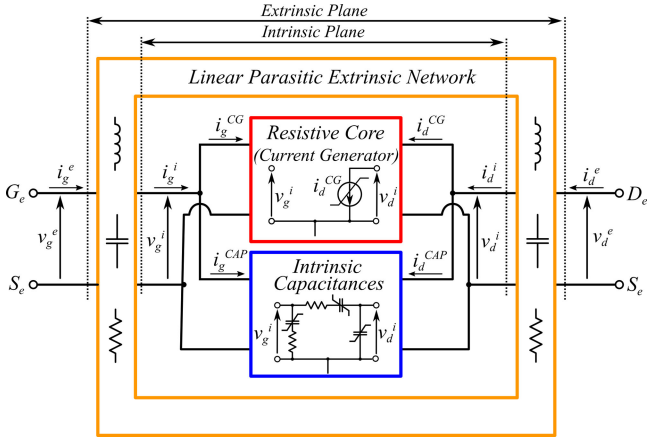

Fig. 1. Topology of a nonlinear model for an LDMOS device.

The nonlinear-embedding approach starts from the waveforms at the current-generator plane corresponding to the specific operating condition of interest. In the frequency domain, we can define them as

$$V^i\left(k\omega_{\mathrm{HF}}\right) = \left[V_g^i\left(k\omega_{\mathrm{HF}}\right), V_d^i\left(k\omega_{\mathrm{HF}}\right)\right] \qquad k = 0, 1, 2, \ldots, N$$

$$I^{\mathrm{CG}}\left(k\omega_{\mathrm{HF}}\right) = \left[I_g^{\mathrm{CG}}\left(k\omega_{\mathrm{HF}}\right), I_d^{\mathrm{CG}}\left(k\omega_{\mathrm{HF}}\right)\right] \tag{1}$$

where $\omega_{\mathrm{HF}} = 2\pi f_{\mathrm{HF}}$ is the design frequency and N is a suitable number of harmonics sufficient for an accurate description of the waveforms. It should be noticed that, in principle, since the current generator is a frequency-independent element, we can achieve the waveforms in (1) at any frequency in terms of amplitudes and phases of their spectral components.

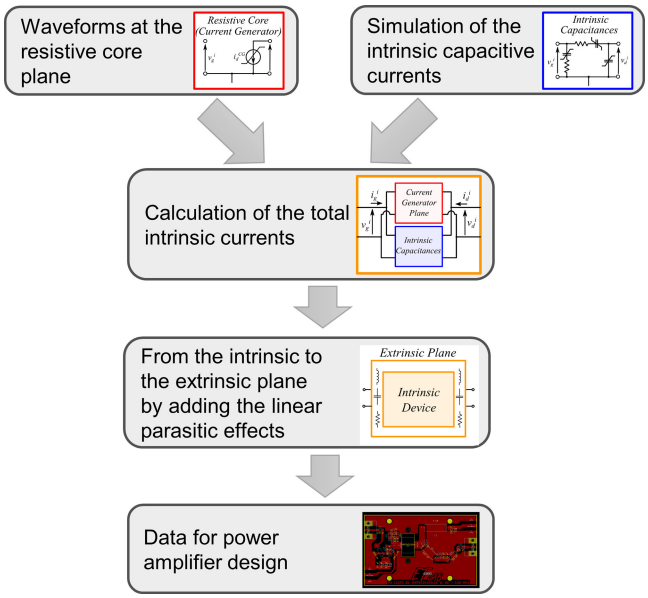

Fig. 2. Flowchart of the nonlinear-embedding methodology.

However, they will correspond to different waveforms at the extrinsic plane, owing to the contributions of the nonlinear intrinsic capacitances and the linear parasitic elements at the selected ω_{HF}. As a consequence, the waveforms at the current-generator plane must be shifted at the extrinsic plane accounting for those contributions.

If models of the intrinsic capacitances and of the parasitic network are available, we can derive the corresponding waveforms at the extrinsic plane following these steps, summarized in Fig. 2.

1) Accordingly with Fig. 1, we assume the intrinsic capacitances in parallel with the resistive-core that includes the current generator, and thus, subject to the same voltage phasors in (1). Therefore, we can use the capacitance model to calculate the displacement current contribution at ω_{HF} (and its harmonics) for the specific operating regime selected at the current-generator plane, i.e.,

$$I^{\mathrm{CAP}}\left(k\omega_{\mathrm{HF}}\right) = \left[I_g^{\mathrm{CAP}}\left(k\omega_{\mathrm{HF}}\right), I_d^{\mathrm{CAP}}\left(k\omega_{\mathrm{HF}}\right)\right], \quad k = 0, 1, 2, \ldots, N. \tag{2}$$

2) The total intrinsic current can now be calculated as the sum of the resistive-core (i.e., current generator) and the capacitive contributions, i.e.,

$$I^{i}\left(k\omega_{\mathrm{HF}}\right) = I^{\mathrm{CG}}\left(k\omega_{\mathrm{HF}}\right) + I^{\mathrm{CAP}}\left(k\omega_{\mathrm{HF}}\right) \quad k = 0, 1, 2, \ldots, N. \tag{3}$$

3) By using the parasitic-element descriptions, we can now shift the current and the voltage waveforms from the intrinsic to the extrinsic plane, thus obtaining

$$V^{e}\left(k\omega_{\mathrm{HF}}\right) = \left[V_g^{e}\left(k\omega_{\mathrm{HF}}\right), V_d^{e}\left(k\omega_{\mathrm{HF}}\right)\right] \quad k = 0, 1, 2, \ldots, N.$$

$$I^{e}\left(k\omega_{\mathrm{HF}}\right) = \left[I_g^{e}\left(k\omega_{\mathrm{HF}}\right), I_d^{e}\left(k\omega_{\mathrm{HF}}\right)\right] \tag{4}$$

These quantities correspond, in the frequency domain, to the time-domain waveforms we must guarantee at the accessible extrinsic terminals of the device to impose the selected operating condition at the current-generator plane.

From the extrinsic current and voltage phasors, we can get all the related data, such as the performance (e.g., output power, efficiency, etc.), together with the required input and output terminations at both the fundamental frequency and harmonics. For example, the load terminations will be given by

$$Z_L^{e} = -\frac{V_d^{e}\left(k\omega_{\mathrm{HF}}\right)}{I_d^{e}\left(k\omega_{\mathrm{HF}}\right)} \quad k = 1, 2, \ldots, N \tag{5}$$

and the input impedance of the device, which can be used for the design of the input matching network [41], is

$$Z_{\mathrm{in}}^{e} = \frac{V_g^{e}\left(k\omega_{\mathrm{HF}}\right)}{I_g^{e}\left(k\omega_{\mathrm{HF}}\right)} \quad k = 1, 2, \ldots, N. \tag{6}$$

The whole procedure may be limited by some prematching networks included in the packaged device to ease the matching-network design for very high-power transistors. This typically has the drawback of limiting the device bandwidth and, as a consequence, the capability of externally tuning the harmonic terminations. However, if the prematching circuit is known, the nonlinear-embedding approach could be still applied by including it in the parasitic-network model for assessing the fundamental termination to be synthesized at the device plane.

III. Characterization Setup

The time-domain waveforms at the current-generator plane, corresponding to the selected operating condition, are the first data we need to define for applying the nonlinear-embedding procedure. We might exploit a model of the device current generator [34], perform some simulations in a CAD environment, and get the desired time-domain voltage and current waveforms. In this case, the accuracy of the model is a crucial aspect, especially when dealing with devices strongly affected by thermal effects as large-periphery LDMOS transistors. These effects can significantly alter the dynamic behavior of the current generator with respect to the conventional dc I/V description, typically assumed as a reference. This issue is further emphasized when new transistor technologies are investigated [42], for which the accurate modeling of the current generator is still an open research problem because of complex nonlinear phenomena affecting these devices.

A valuable alternative to simulations is to directly measure the current-generator behavior for the load line that meets the design requirements. As stated in Section II, this cannot be immediate at high frequency because of the linear and nonlinear reactive contributions due to the intrinsic capacitances and other parasitic elements. However, this problem can be overcome by measuring the device at lower frequencies. To this end, we have developed the setup shown in Fig. 3 [43]. It is a time-domain load-pull system that performs an active synthesis of the device terminations at both the fundamental frequency and harmonics. The operating condition for the device under test (DUT) is imposed by injecting two incident waves at its

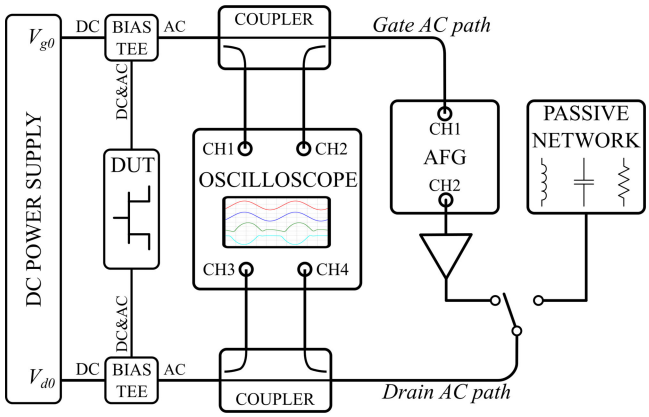

Fig. 3. Block diagram of the low-frequency measurement setup implementing the time-domain active load-pull system.

input and output ports. By means of two dual-directional couplers connected to a 4-GHz oscilloscope, we can monitor both the incident and reflected waves, whose combination defines the voltage and current waveforms at the DUT plane. The injected signals are provided by means of an arbitrary function generator (AFG), which allows one to control not only the fundamental components but also the harmonic ones. On the drain path, an amplifier may be inserted when the output power levels are too high to be handled by the AFG only. Alternatively to the active synthesis of the load, the output port of the DUT can be terminated by a passive network properly designed to implement the desired load conditions. The bias condition is imposed by a dc power supply and coupled with the ac signals by means of two bias tees. The actual implementation of the system allows controlling the incident waves up to 120 MHz under multiharmonic regime, whereas the setup bandwidth is limited by the couplers at 400 MHz. The correction of the measurements for the cable losses and phase shifts is implemented by using a characterization of the signal paths based on their *S*-parameter measurements. This procedure allows shifting the acquired data from the oscilloscope to the DUT plane [43].

For the characterization of the current generator, in order to get data consistent with the RF operation, we need to select a frequency $\omega_{\rm LF} = 2\pi f_{\rm LF}$ above the thermal-phenomena cutoff, for which a value of 1 MHz is commonly accepted [35]. Such a cutoff frequency is also suitable for taking into account deep-level trapping effects, which, although not affecting the Si LDMOS performance, strongly influence the transistor behavior in more recent technologies.

In addition, the characterization frequency has to be sufficiently low to neglect any contribution from the reactive effects of the device. Under this condition, the measured data refer to the current-generator plane only. Indeed, ohmic parasitic effects due to the access structures (i.e., package flanges, bonding wires, transmission lines, etc.) do exist, although they can be easily de-embedded from the measured data.

Once the desired load line is measured, the thermal and trap-occupation states are fixed and the I/V relationship will not change with frequency as long as it is measured above the low-frequency cutoff. Moreover, there should exist a condition at the

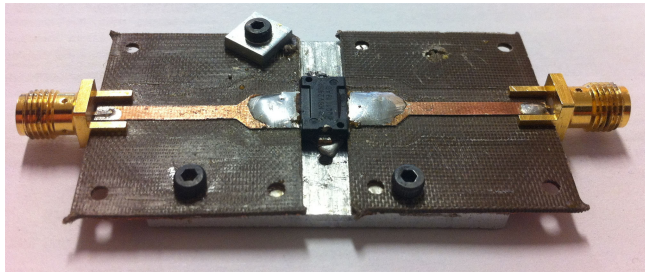

Fig. 4. LDMOS transistor mounted on the PCB board for the low-frequency characterization.

extrinsic plane for any higher frequency $\omega_{\rm HF} = 2\pi f_{\rm HF}$ such that the current and voltage waveforms at the current-generator plane correspond to the measured ones at $\omega_{\rm LF}$. Such a condition can be investigated by exploiting the nonlinear-embedding procedure, using as a starting point the low-frequency measured phasors, whose spectra are rigidly shifted from $\omega_{\rm LF}$ to $\omega_{\rm HF}$, i.e.,

$$\begin{matrix} V^{\rm CG}\left(k\omega_{\rm LF}\right) \\ I^{\rm CG}\left(k\omega_{\rm LF}\right) \end{matrix} \xrightarrow{\text{from LF to HF}} \begin{matrix} V^{\rm CG}\left(k\omega_{\rm HF}\right) \\ I^{\rm CG}\left(k\omega_{\rm HF}\right) \end{matrix} \quad k = 0, 1, 2, \ldots, N. \tag{7}$$

It is worth noticing that, in principle, the whole procedure is frequency independent, so that we can transpose the measured data to any design frequency that allows for waveform harmonic control at the intrinsic current-generator plane. This feature becomes extremely useful when wideband circuits need to be designed; the only limitation is related to the accuracy of the available parasitic and capacitance models in the bandwidth of interest.

IV. Design of Two PAs

We now discuss the design of two PAs based on the 10-W LDMOS MRF6V2010N by Freescale, which can operate within the band $10 \div 450$ MHz, covering the FM broadcasting band we are interested to, i.e., $88 \div 108$ MHz.

The aim of the two designs is to point out the capabilities of the nonlinear-embedding methodology, by selecting two different operating conditions. For the first PA, we focused on the maximization of its efficiency, keeping the output power at a sufficiently high level under continuous-wave regime. In this case, tuning the load only at the fundamental frequency is not sufficient, and we needed to properly control also the harmonics [17], [30]. Such a kind of evaluation may be easily performed by exploiting the setup described in Section III. The availability of an AFG as a signal source allows controlling also the harmonic components of the signals injected at the DUT ports. Harmonic tuning tends to limit the PA bandwidth because of the selectivity required for the matching networks. Therefore, as a second design, we considered a wideband PA. In this case, only the load impedance at the fundamental frequency is tuned and the nonlinear-embedding approach is used to derive the transistor terminations within the whole FM broadcasting band.

To connect the transistor to the setup, we mounted it on a customized PCB board fabricated on a Diclad 527 substrate (see Fig. 4). The device gate and drain flanges are soldered to two

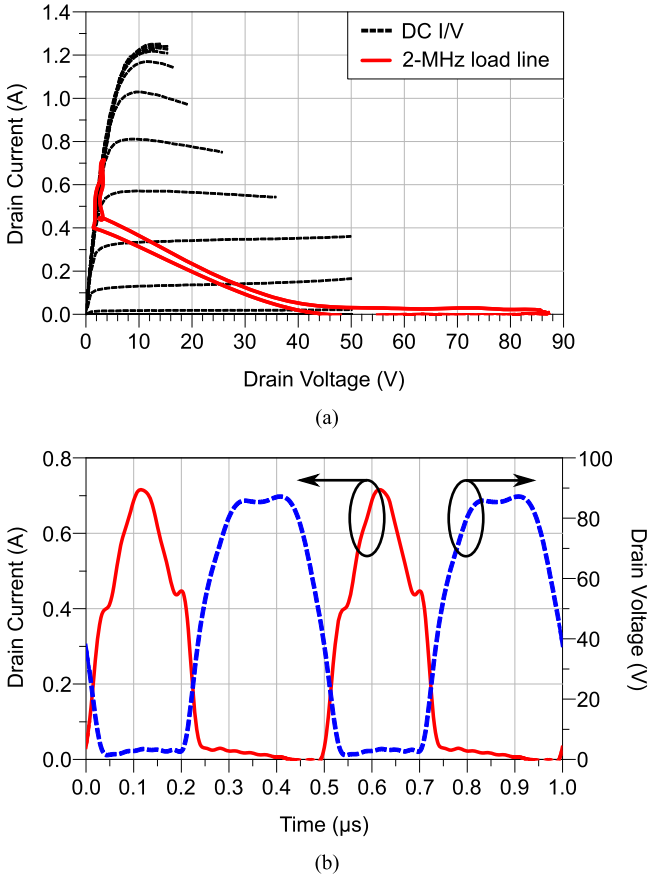

Fig. 5. High-efficiency class-F load line synthesized at 2 MHz superimposed to the dc I/V characteristics (a) and corresponding waveforms (b).

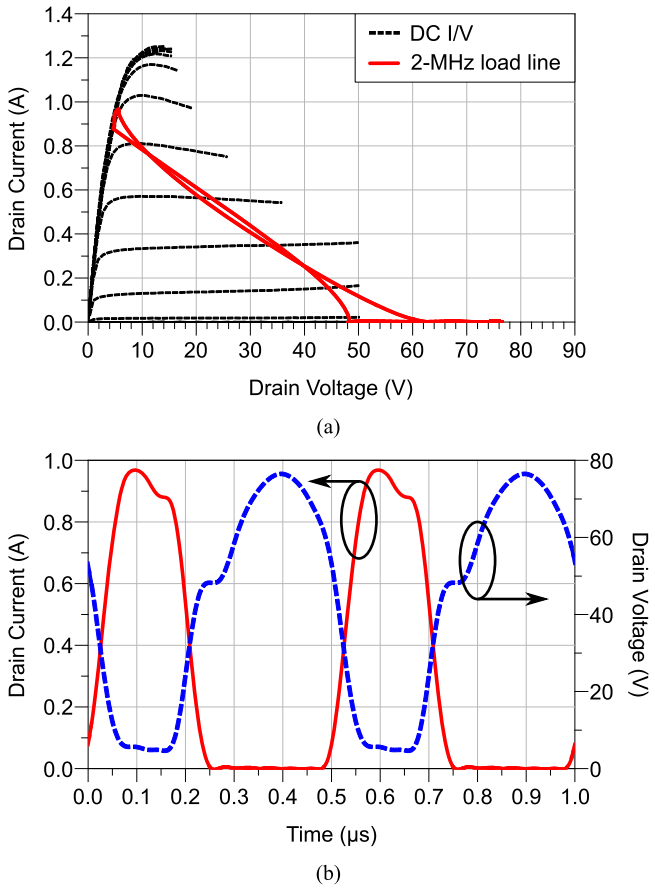

Fig. 6. Class-AB load line synthesized at 2 MHz superimposed to the dc I/V characteristics (a) and corresponding waveforms (b).

TABLE II
LOAD IMPEDANCES CORRESPONDING TO THE LOW-FREQUENCY LOAD LINES

Frequency	Class-F load impedance	Class-AB load impedance
2 MHz	145.6 + j6.5 Ω	73 – j10 Ω
4 MHz	0 + j6.2 Ω	30 + j17 Ω
6 MHz	1.3 + j1.0 kΩ	39 + j26 Ω

50-Ω microstrip lines reaching the external SMA connectors. The characteristics of the lines have been designed to have negligible influence at low frequency (i.e., 2 MHz).

The transistor was preliminarily characterized by means of dc I/V conventional measurements for evaluating the best operating point for the device and a first estimation of its performance. Once the bias point was selected, i.e., $V_{g0} = 2.4$ V, $V_{d0} = 42.5$ V, and $I_{d0} = 20$ mA, we identified the load lines corresponding to the two operations of interest, which are reported in Figs. 5 and 6, together with the output waveforms. The high-efficiency load line [see Fig. 5(a)] was obtained by actively synthesizing the load impedances reported in Table II. They realize a class-F operation, which allows a higher output power than other conventional classes of operation with a reduced conduction angle (e.g., class C). In particular, with this load line, we achieved an RF output power of 8.5 W with a drain efficiency of 86.7%. By looking at the measured waveforms in Fig. 5(b), we can see that their shapes are consistent with the theoretical ones, i.e., a square wave for the voltage and a half-truncated sinusoid for the current, with a minimum superposition. In addition, we can easily monitor if the selected dynamic condition may affect the transistor reliability by comparing the data with the device maximum ratings. As an example, the maximum drain voltage allowed for this device is 110 V, whereas the load line highlights a maximum dynamic value of approximately 88 V, which is sufficiently low to avoid any reliability issue.

We show the class-AB load line under saturated output power operation and the corresponding waveforms in Fig. 6. As reported in Table II, the impedances at harmonics were not set, focusing only on the fundamental one. Nevertheless, their values were controlled in order to keep them sufficiently low to avoid a strong influence on the PA performance. The measured performance in this case was 9.4 W with a drain efficiency of 68.2%, which is consistent with the selected class of operation. It is also evident that the absence of harmonic tuning keeps the maximum value of the drain voltage lower than the class-F load line.

To apply the nonlinear-embedding procedure, we first need models of both the intrinsic capacitances and the extrinsic parasitic elements. In this particular case, we identified these models from multibias *S*-parameter measurements [44], [45]. The parasitic network has been identified by means of cold-FET data by using a conventional approach [46]. Then, by de-embedding the parasitic effects from the *S*-parameters, the intrinsic capacitive network can be easily determined and implemented as a

TABLE III
LOAD/SOURCE IMPEDANCES AT THE DESIGN FREQUENCY FOR THE CLASS-F LOAD LINE

Frequency	Load impedances	Source impedances
100 MHz	77.8 + j71.1 Ω	9.1 + j72.6 Ω
200 MHz	j2.0 Ω	-j2.1 Ω
300 MHz	j59.7 Ω	j1.8 Ω

TABLE IV
LOAD/SOURCE IMPEDANCES AT THE DESIGN FREQUENCIES FOR THE CLASS-AB LOAD LINE

Frequency	Load impedances	Source impedances
88 MHz	69.7 + j17.5 Ω	14.1 + j94.5 Ω
98 MHz	68.2 + j20.1 Ω	13.7 + j84.8 Ω
108 MHz	66.5 + j22.5 Ω	13.3 + j76.9 Ω

look-up-table model for direct nonlinear simulations [38], [46]. Indeed, the use of a customized model is not mandatory. Alternative solutions, such as the use of manufacturer models, could be adopted, provided that the description of the intrinsic capacitances and the extrinsic parasitic elements are available.

As a next step, we transposed the low-frequency load lines of the two classes of operation, to the design frequency by exploiting the nonlinear-embedding procedure described in Section II. For the high-efficiency class-F condition, we considered a design frequency of 100 MHz. In Table III, we report the load and source impedances predicted by the nonlinear-embedding methodology and used for the synthesis of the PA matching networks. Since harmonic tuning was performed, we list the first three harmonics.

Regarding the class-AB load line, we applied the nonlinear embedding from 88 to 108 MHz to get the design data for a wideband PA. For the sake of brevity, we report in Table IV the source and load impedances just at the edges and at the center of the selected FM bandwidth. It is worth noticing how, differently from conventional approaches, the impedance trajectory to be synthesized can be simply retrieved by applying (2)–(5) in the entire bandwidth, avoiding time-consuming optimization procedures.

In Fig. 7, we report the predictions of the load lines at the extrinsic plane compared with the measurements at the current-generator plane. It is evident how the latter are masked by the contributions of the reactive elements of the device. In Fig. 7(b), it is also evident a slight variation of the extrinsic load lines with frequency, which reflects the values of the load impedances reported in Table IV.

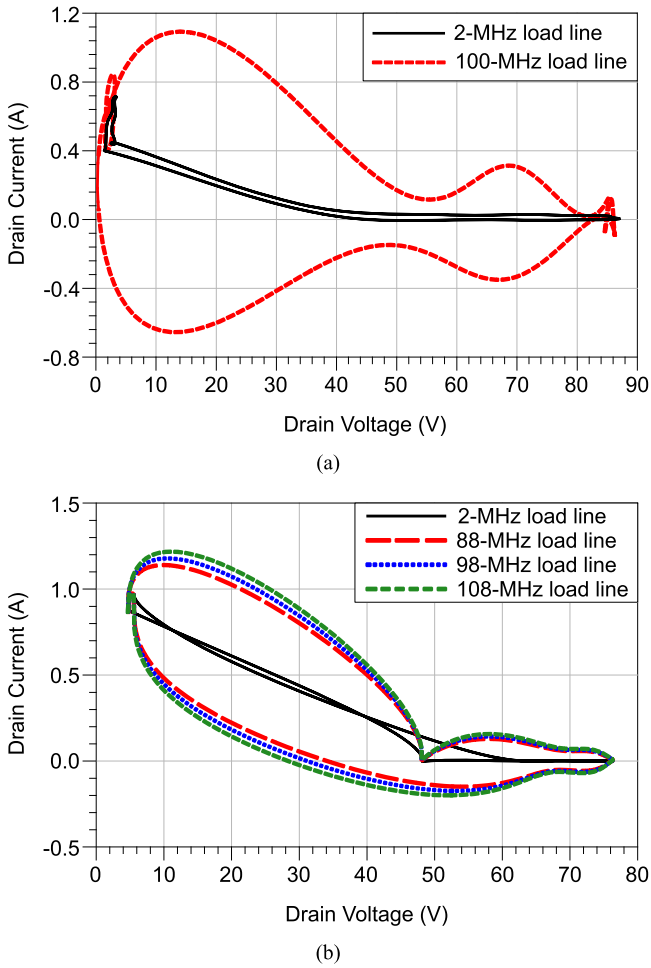

Fig. 7. Low-frequency load lines (solid lines) and predicted load lines at design frequency (dashed lines) for the high-efficiency class-F (a) and the wideband class-AB (b) conditions.

V. PA FABRICATION

In Fig. 8, we report the schematics implemented for the fabrication of the PAs, where the matching and bias networks have been designed to synthesize the impedances derived from the nonlinear-embedding procedure.

The output-matching networks are quite complex in both cases, although for different reasons: the need for harmonic control in the high-efficiency class-F PA and the wideband requirement for the class-AB PA.

Regarding the input network, the R-C shunt has been introduced for stability issues in both cases. Moreover, to guarantee adequate matching also under small-signal operation, we realized a tradeoff between the source impedance values in Tables III and IV and the ones, derived from *S*-parameter measurements at the selected bias point, that maximize the small-signal matching over the bandwidth 88 ÷ 108 MHz. The same L-C-L input matching network was sufficient to get good performance over the required bandwidth in both the PAs, as will be shown in the following.

The circuits were fabricated on a conventional FR-4 substrate, and are reported in Fig. 9.

VI. PA VALIDATION

A. Small-Signal Verification

We first measured the small-signal behavior of the PAs for their nominal bias point, i.e., $V_{g0} = 2.4$ V and $V_{d0} = 42.5$ V, by using a vector network analyzer. We show the results in terms of input matching and small-signal gain in Fig. 10. In the bandwidth for which the input matching network was designed, we obtained an input matching better than −14 dB and –16 dB for

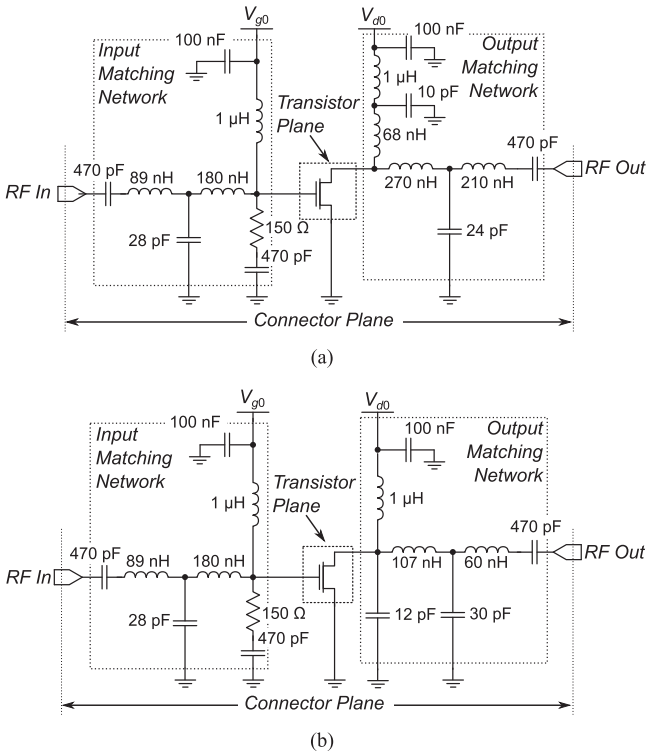

Fig. 8. Schematics of the class-F (a) and class-AB (b) fabricated PAs with the indication of the connector and transistor planes.

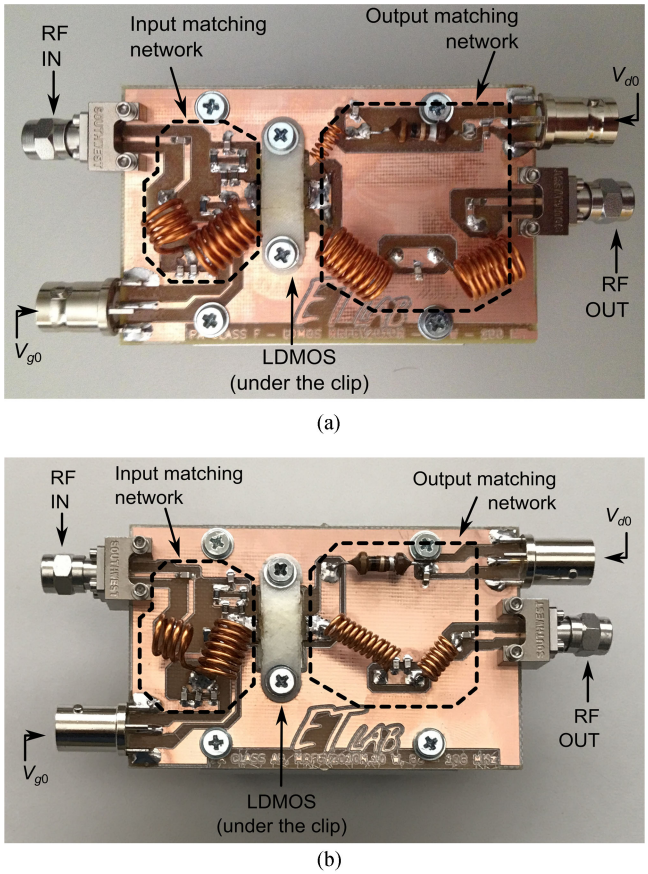

Fig. 9. Photos of the fabricated PAs: class F (a) and class AB (b).

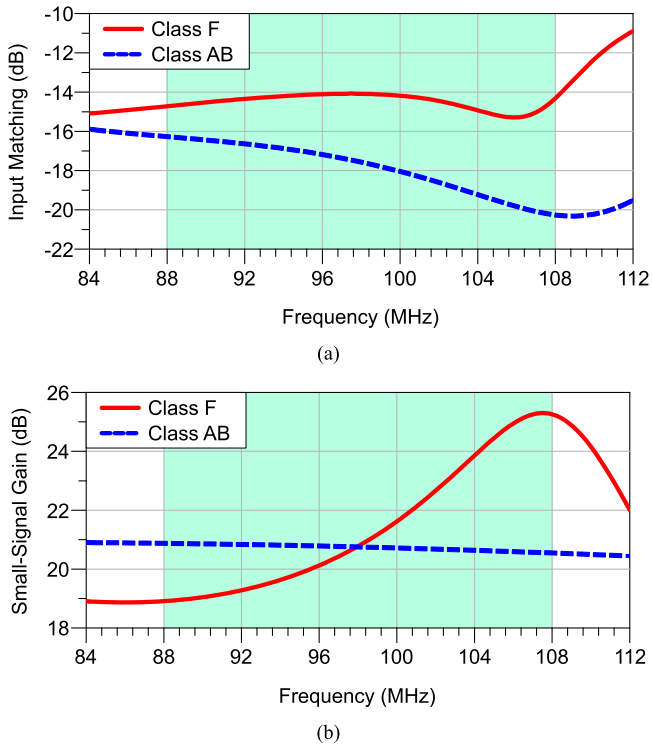

Fig. 10. Input matching (a) and small-signal gain (b) of the fabricated PAs. The shaded areas highlight the bandwidth 88 ÷ 108 MHz.

the class-F and the class-AB Pas, respectively. The small-signal gain of the class-F PA shows a large variability in frequency related to the selectivity of the output-matching network. We expected the peak gain not lying at the design frequency, since no specification has been considered for this parameter in the design phase, giving priority to the output power and efficiency under large-signal operation. On the contrary, the class-AB amplifier, for which the matching networks were optimized within the whole FM bandwidth, has an approximately flat gain, with a variability limited to 0.5 dB.

B. Large-Signal Measurements

The next step was to verify the PAs performance under actual operation, i.e., large-signal conditions. To this aim, we exploited a simplified version of the setup described in Section III, removing the bias-tees (which are included in the fabricated PAs) and terminating the output port on a constant 50-Ω load.

We first measured the PAs performance for a constant input power level over the bandwidth 88 ÷ 108 MHz. The results are reported in Fig. 11. The class-F PA achieves a maximum output power at 100 MHz, whereas the maximum efficiency is reached at 105 MHz. The class-AB PA performance is instead more constant over frequency, consistently with its wideband design. As expected from this class of operation and for the selected design condition, it delivers higher power with a lower efficiency.

In both cases the performance is lower than the designed one. This is indeed an expected result since the measurements include the losses of the matching networks, which lower the

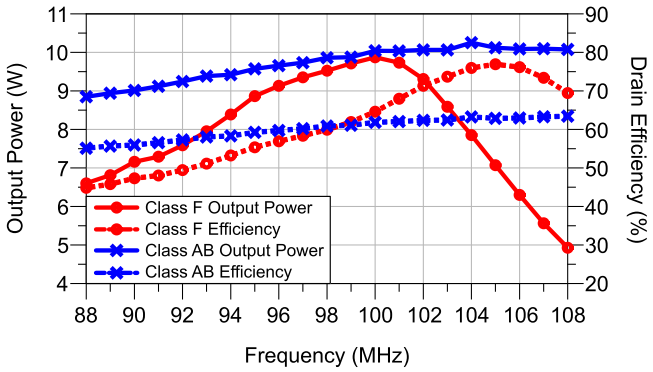

Fig. 11. Measured output power (solid red line) and drain efficiency (dotted blue line) for an input power of 14.4 dBm (class F) and 16.9 dBm (class AB) over the bandwidth 88 ÷ 108 MHz. Data refers to the connector plane (Fig. 8).

TABLE V
PREDICTED AND MEASURED TRANSISTOR PERFORMANCE AT 104 MHZ FOR THE CLASS-F PA

Performance	Nonlinear embedding	High-frequency measurement
Output power	8.5 W	8.6 W
Drain efficiency	86.7%	83.2%

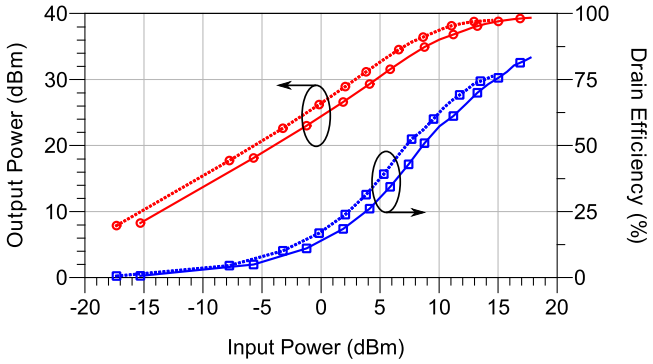

Fig. 12. Output power (red circled lines) and drain efficiency (blue squared lines) at 104 MHz. Solid lines refer to the transistor extrinsic plane, dotted lines to the PA connector plane.

overall efficiency. On the contrary, the design data are referred to the transistor extrinsic reference plane. Therefore, for a fair comparison, we measured the *S*-parameters of the fabricated matching networks to shift the large-signal data at the transistor plane (see Fig. 8).

The *S*-parameters of the class-F output-matching-network showed a frequency shift with respect to the designed network due to fabrication issues, so that the best match with the theoretical load impedances is achieved at 104 MHz. The best performance at the transistor plane is reported in Table V compared with the prediction of the nonlinear-embedding procedure. The good agreement suggests the transistor is operating with the same load line we have measured at low frequency at the current-generator plane. In Fig. 12, we show the corresponding performance as a function of the input power.

It is also significant to observe the spectrum of the output power to monitor the harmonic distortion. In Fig. 13, we show

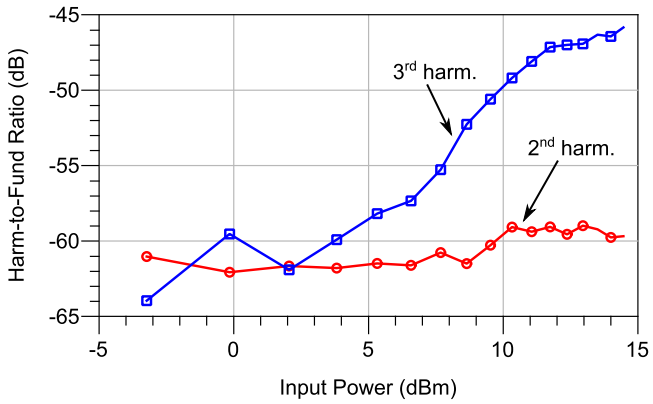

Fig. 13. Harmonic-to-fundamental output-power ratio for a fundamental frequency of 104 MHz.

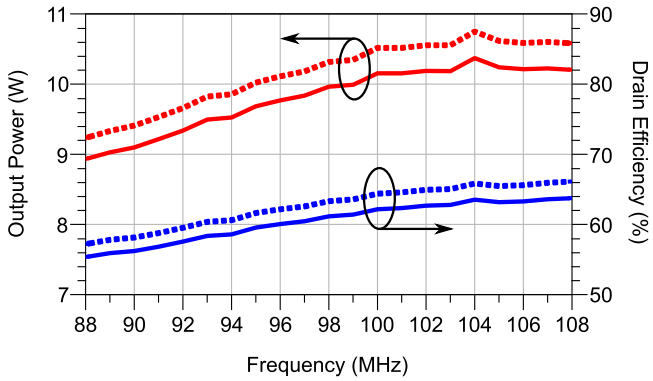

Fig. 14. Output power and drain efficiency for the class-AB PA for an input power of 17 dBm (50 mW). Dotted lines refer to the transistor extrinsic plane, solid lines to the PA connector plane.

the harmonic-to-fundamental output-power ratio for a fundamental frequency of 104 MHz as a function of the input power. The second harmonic is practically absent in the output spectrum, whereas there is a small third-harmonic component, which becomes evident only for the higher power levels. This result is indeed consistent, since one of the aims of the class-F operation is to minimize the output power at harmonics to improve the PA efficiency.

In the same way, we shifted the measured data at the transistor reference plane for the class-AB PA. We report the results in Fig. 14 over the FM bandwidth for a constant input power (i.e., 50 mW). The achieved performance is slightly lower than the expected one in terms of efficiency. The analysis of the output-matching-network S-parameters showed that the terminations at harmonics presented at the DUT plane, which were not controlled, were higher than expected, which cause a slight detrimental effect on the PA efficiency.

C. Validation and Comparison With Conventional Design Approaches

As shown so far, the nonlinear-embedding methodology transposes the current-generator waveforms to the extrinsic plane by considering a full nonlinear model of the intrinsic capacitances and a complete linear parasitic network. This surely

TABLE VI
LOAD IMPEDANCES PREDICTED BY LINEAR AND NONLINEAR-EMBEDDING APPROACHES AT 100 MHZ

Class	Freq.	Linear embedding A	Linear embedding B	Nonlinear embedding
F	100 MHz	105 + j67 Ω	101 + j67.8 Ω	77.8 + j71.1 Ω
	200 MHz	j6.5 Ω	j6.1 Ω	j2.0 Ω
	300 MHz	3.2 + j79.7 Ω	0.8 + j77.7 Ω	j59.7 Ω
AB	100 MHz	74.3 + j13.2 Ω	71.9 + j13.5 Ω	67.9 + j20.6 Ω

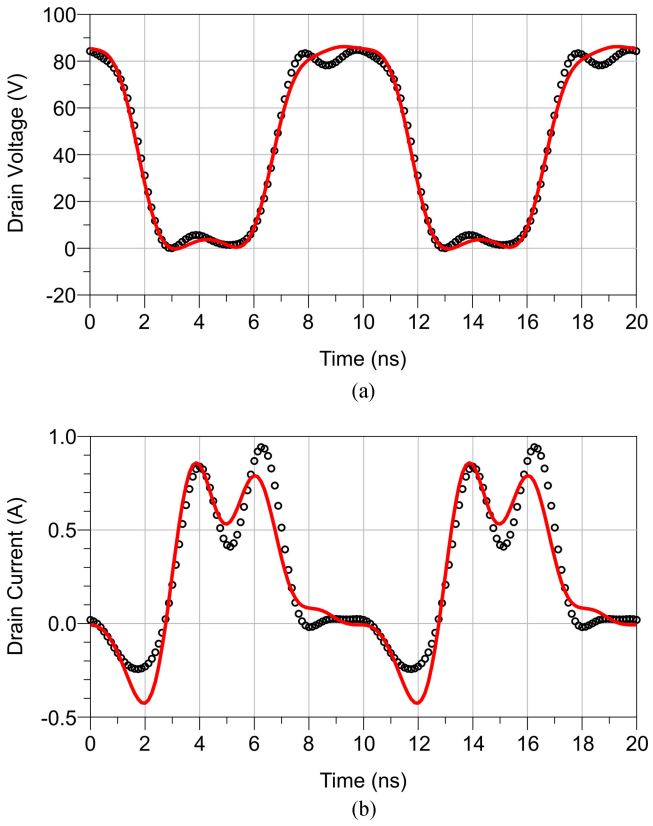

Fig. 15. Drain voltage (a) and drain current (b) waveforms at the transistor extrinsic plane for the class-F PA measured at 100 MHz for an input power of 14.5 dBm (28 mW): expected waveforms derived by the nonlinear embedding (solid lines) and measured waveforms (symbols).

makes it more complicated than conventional but less accurate approaches usually based on a simplified linear approximation of the transistor nonidealities, can lead, as a consequence, to less accurate results. To provide some comparison, we applied two "linear" embedding procedures [47] starting from the class-F and class-AB load lines at the current-generator plane. For the first case (A), we only considered two linear capacitances, $C_{\rm gs}$ and $C_{\rm ds}$, as the capacitive core and no parasitic elements have been included to transpose the data at the extrinsic plane. For the second case (B), we also included the effects of the parasitic elements and the linear capacitance $C_{\rm gd}$. In case A, there is no feedback element between the input and output ports of the device. Such a practical hypothesis is commonly adopted [15], [19]–[21], [24] since it strongly simplifies the evaluation of the extrinsic load impedances, by reversely isolating the two ports of the device. In case B, we introduced the capacitance $C_{\rm gd}$ as a feedback element, in order to show that the limited accuracy is largely ascribable to the linearity hyphothesis.

In Table VI, we report results of the impedances predicted by the linear approaches in comparison with the nonlinear one. The data provided by the linear approaches are very similar, which confirms the small influence of the parasitic network and of the feedback capacitance $C_{\rm gd}$. On the contrary, compared with the nonlinear embedding, we note a considerable difference, especially for the class-F condition, where the effects of the capacitance nonlinearities is more noticeable and strongly influence the transistor operation.

To further confirm the validity of the nonlinear-embedding procedure, we characterized the transistor performance at the design frequency. Starting from the impedances derived at design frequency (see Tables III and IV), we can directly synthesize them at the extrinsic plane by means of a time-domain load-pull setup based on a 4-channel 50-GHz oscilloscope [48], and compare the measured time-domain waveforms with the ones predicted by the nonlinear embedding. This comparison becomes very interesting for the class-F operation, since it involves some harmonic tuning up to the third harmonic. We report the results for a design frequency of 100 MHz in Fig. 15. The main difference between predicted and measured waves is related to the limitation of synthesizing harmonic terminations with a theoretically zero real part, which increases the magnitude of the harmonics with respect to the ideal case. Despite this aspect, the agreement is very good and proves the accuracy of the predicted results.

VII. CONCLUSION

In this paper, we applied the nonlinear-embedding technique [26] as a general approach for the design of LDMOS PAs. We designed and realized a high-efficiency class-F PA and a wideband class-AB PA operating in the FM broadcasting band. The performance of the fabricated PAs shows very good agreement with design predictions, proving the effectiveness of the proposed approach and paving the way for further development of the nonlinear-embedding approach oriented to LDMOS technology.

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