Baseline project overview

(Introduction + status)

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Market, current performance and possible scenarios

DRAFT

WI 21H2

		Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3
		2021				2022				2023				2024		
Sub System	mMIMO TX Module (PAM)				x				x				x			
Sub System Features	RFBW/Instantaneous BW [MHz]				100 - 400				100 - 400				100 - 600			
	Total Radiated Power [W] / max oBW [MHz]				320 / 200				400 / 200				640 / 320			
	Unit power per element at PAM level (uPE) [W]				8				2 / 4 / 8 / 10				2 / 4 / 8 / 10 / 12			
	Linear efficiency [%] (N40,N41/N77/N79)				50 / 48 / NA / NA				52 / 48 / 43 / NA				53 / 50 / 45 / tbd			
	Linear efficiency [%] (N40,N41/N77/N79) @uPE-4dB				tbd / tbd / NA / NA				tbd / tbd / tbd / NA				tbd / tbd / tbd / tbd			
	Frequency range [GHz]				2.3 - 4.2				2.3 - 5.0				2.3 - 7			
	Gain {fixed Pin} [dB]				>31				>32				>33			
	Package Size [mm] / Without special feat. [mm]				12x8 / 10x6				12x8 / 10x6				12x8 / 10x6			
	Cost {FSP} [Eur]				2.5				2.1				1.7			
	EVM [% / Mod QAM], TDD mode with DPD				<2				<2				<2			
	Transmitters [#]				32 / 64				32 / 64 / 128				32 / 64 / 128 / 256			
	System constraints				Single VDD [14-50V]				Single VDD [14-50V]				Single VDD [14-50V]			
	Special features				B&C				B&C				B&C			

RFBW/iBW = 400MHz
Pavg = 8W (39dBm), PAPR = 8.5dB
Fc = 3.6 GHz
PAE = 48 %
Gain = 31 dB
Cost = 2.1Eur

Introduction

Integral Roadmap

- System
- Sub-System
- Block
- Circuit
- Technology

Concept and Pre-Dev

Development

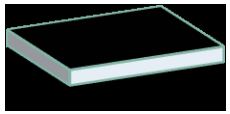
System architecture defined
Product Specs mapped

Spec to architecture

Re-definition, optimization and validation

Technology capabilities

RFGaN defined, other semi. open
Passive techs open



Different frequency bands
Different power levels

Prototyping

Integration and Release

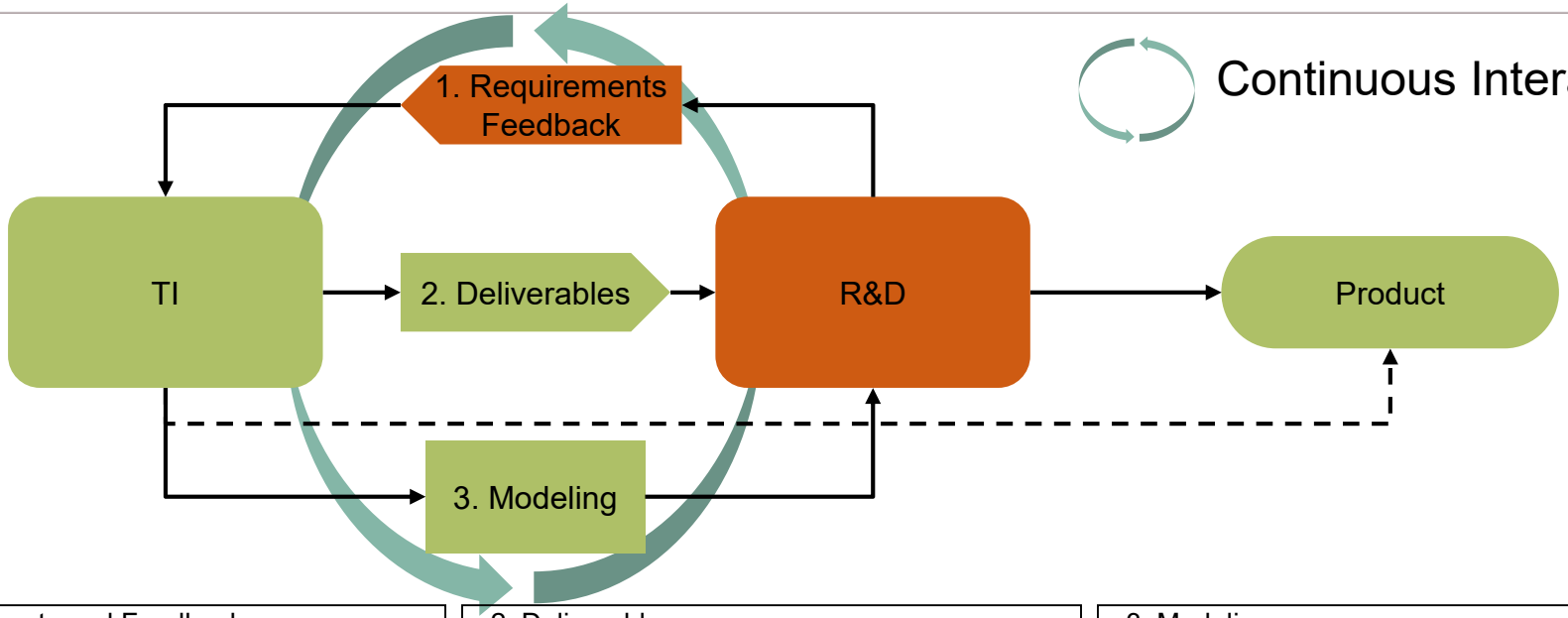
Replication

Topics

- Technology interaction and inputs
- IPD
- Device data base and characterization
- Proposed architecture and their potential implementation
- Ongoing activity and open items

Technology interaction and inputs

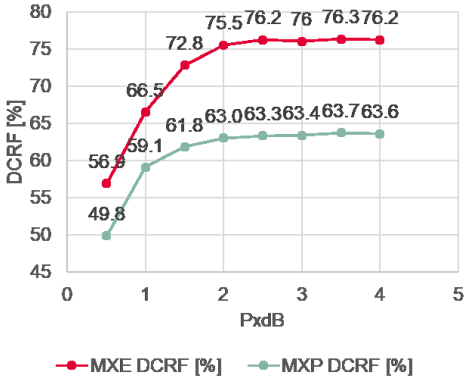
R&D – TI Interaction

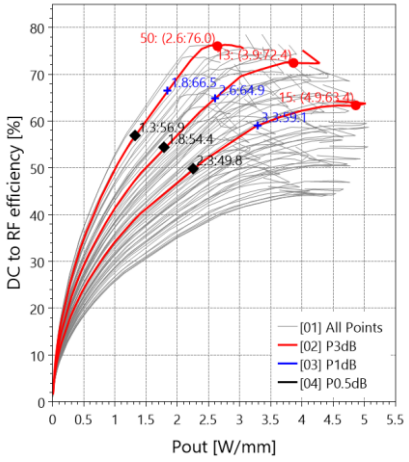


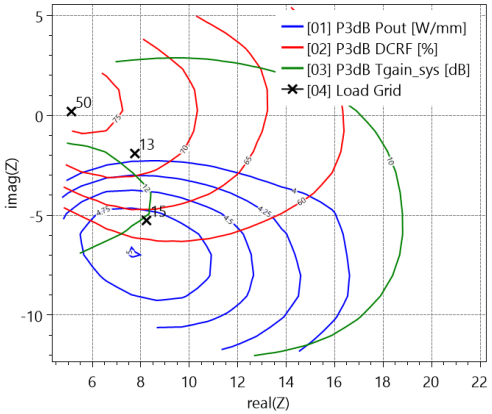
- 1. Requirements and Feedback
  - Technology main performance parameters
  - Model specs (features and accuracy)
  - Technology performance indication at product level
- 2. Deliverables
  - Qualified technology
  - Transistor layout optimization
    - Performance / Stability
    - Thermal
    - Cost
  - Technology evaluation
    - Report
- 3. Modeling
  - Model and report

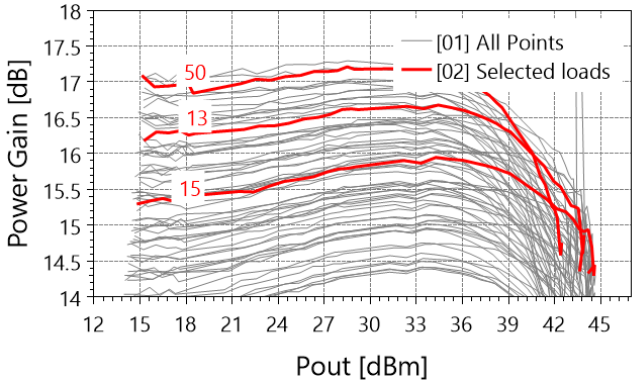
Technology open topic examples

Pcell and geometry selection criteria➔
DE vs frequency for given size➔
Gain vs frequency for given size➔
Gain and DE vs figure length vs frequency➔
Power vs frequency for given size➔
Harmonic terminations vs frequency for given size➔









P19 (24*240um) @3.5GHz @30°C NoDmbd I1/O2 harm opt

IPD

Evolution of passives

Used mainly in Initial phase
Tuning
Reliability issue (Cost)
Tolerances
Overall cost (assembly, test ..)
Size and area …
Short development time
Limited design freedom

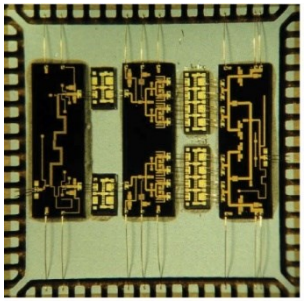
Advanced phase (products in the market)
Tuning (very limited)
Good Reliability
Good tolerances
Lower cost (assembly, test ..)
Smaller size and area
Shorter development time
More design freedom (more options)

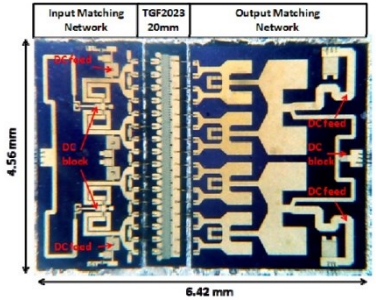
In development phase
Tuning (very limited)
Good Reliability
Good tolerances
Lowest cost (assembly, test ..)
Smaller size and area
Longer development time
Best for design option
Alternatives for bond wires

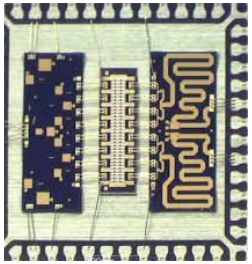
Win semi IPM3-01
Mature
In production
Reliable
PDK
Good performance
Costly
Good for inter-stage

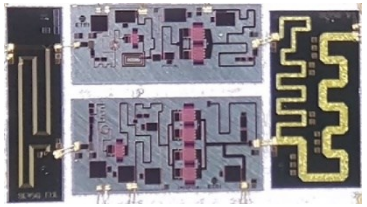
In house BEOL on LDMOS
Not qualified yet
In development
Reliable (need to be verified)
PDK (Only EM stack)
Moderate Performance(need to be checked)
Very cheap
Good for input of pre driver or driver

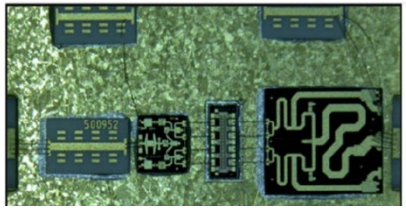
IPD examples

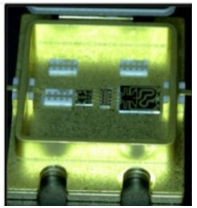


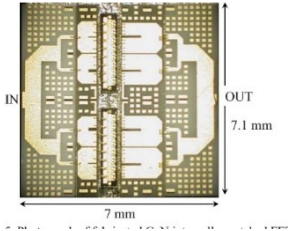


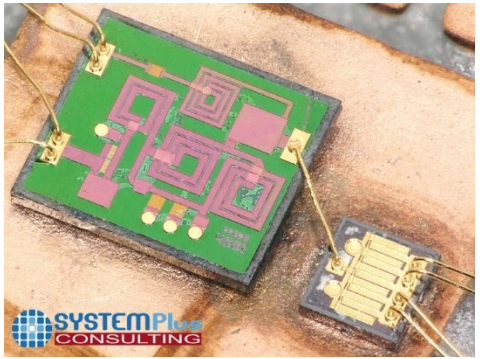


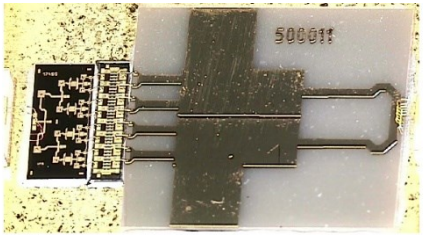


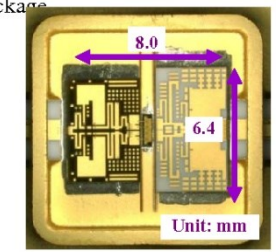












GaAs IPD Build up

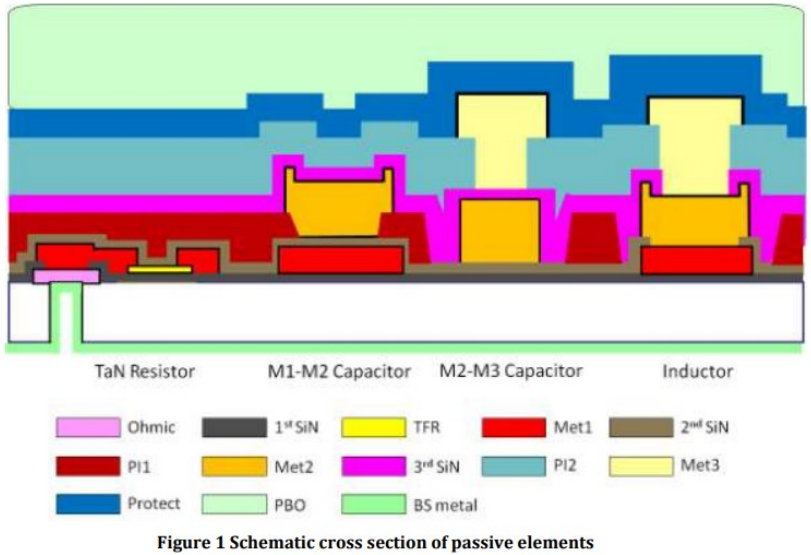
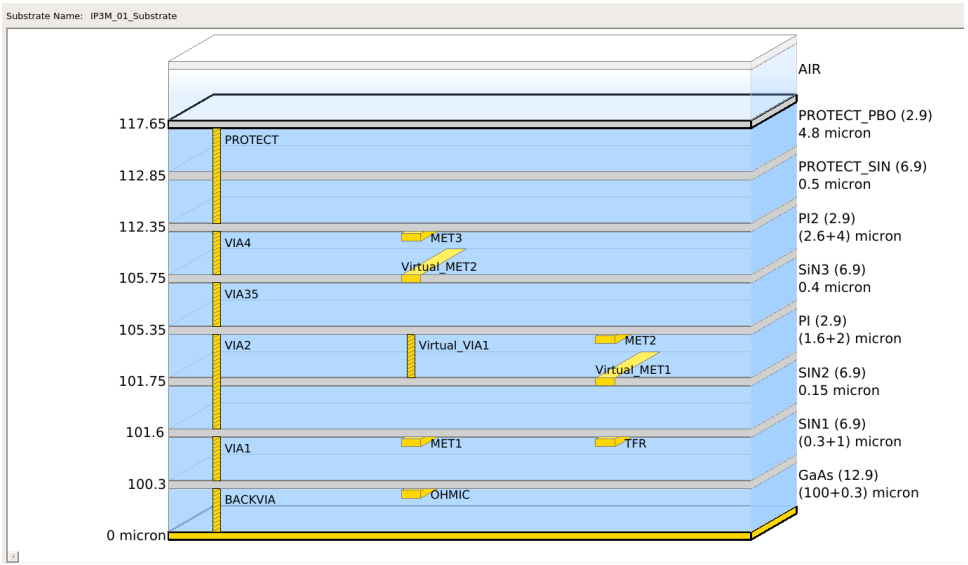


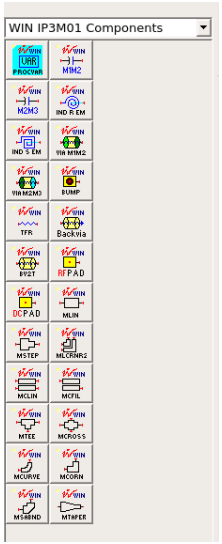
Figure 1 Schematic cross section of passive elements

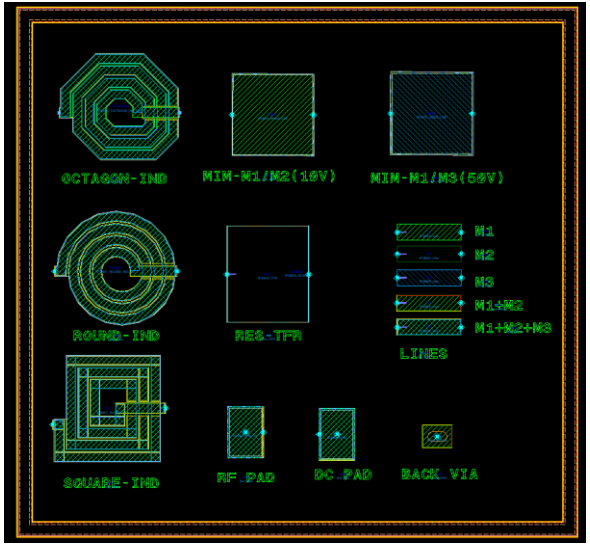


3 Metal layers (MET1,MET2,MET3) with fully back side metallization and conductive via between each layer

PDK

\\mucsdv534.infineon.com\RFS\PG_WI\20_CE\5__Status_Core_Technologies\8__PDK\0__Win_PDK\IP3M_01





Features

- Manufactured on 150mm GaAs wafers
- Low-K dielectric crossovers
- 3 metal layers, 7µm total thickness
- 400 pF/mm² capacitor, VB>80V
- 190pF/mm² capacitor, VB>300V
- 150pF/mm² capacitor, VB>370V
- 50Ω/square thin film resistors
- Moisture rugged at 28V and 50V
- Through wafer via for grounding
- Available with hot via and AuSn eutectic back metal

M1➔ 400mA per 100um
M2➔ 800mA per 100um
M3➔ 1600mA per 100um
M1+M2➔ 1200mA per 100um
M1+M2+M3➔ 2800mA per 100um

Qualification and Reliability

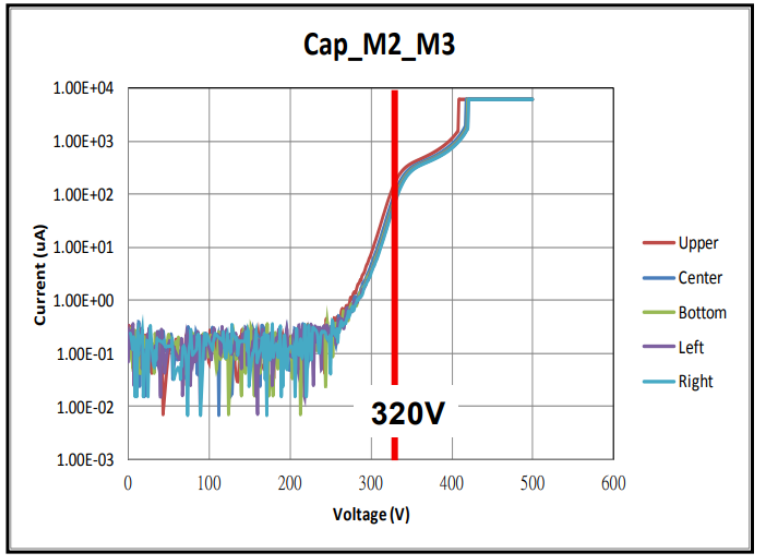


Figure 5 Capacitor breakdown curve for IP3M-01 M2-M3 capacitor

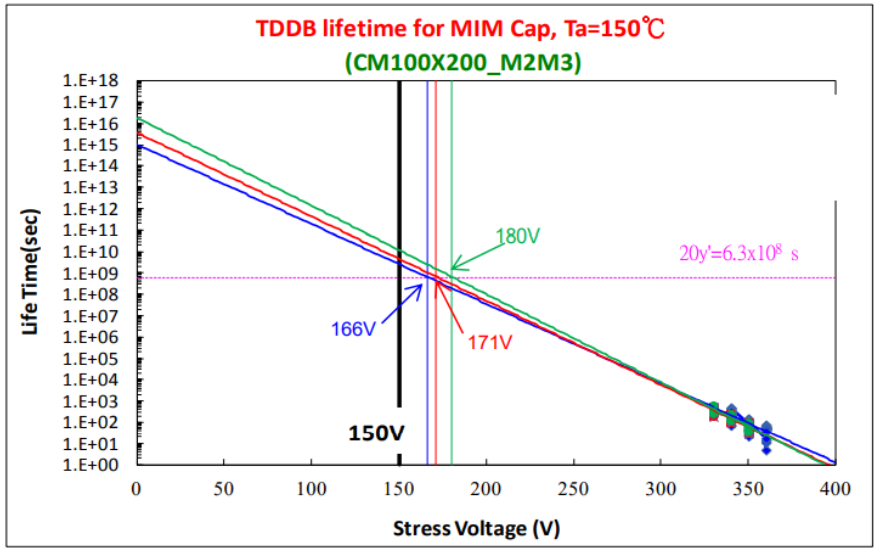


Figure 12 Capacitor TDDB results for the IP3M-01 M2-M3 configuration

Device data base and characterization

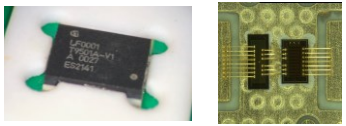
Device database

			Duration	Owner
A1.0	GaN die database creation/update	Checking available database and update that with rough number of dies, sizes and characteristics, history, will this die available for production in future?, …	1w	MH
A1.1	Moscap database creation/update	Checking available database and update that with rough number of dies, sizes and characteristics, history, will this die available for production in future?, …	1w	MH
A1.2	LDMOS die database creation/update	Checking available database and update that with rough number of dies, sizes and characteristics, history, will this die available for production in future?, …	1w	MH

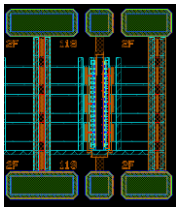
Larger Device Characterization

Goals :

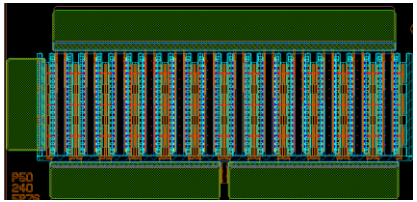
- **Characterize** different devices that can be used for **main peak** and **drivers** (single and dual)
- **Maximum** achievable performance of each configuration in terms of **Efficiency**, **Gain** and **Power**
- Better **device selection** for each section and **different architectures**
- **Model** verification/modification /creation
- **Technology** evaluation and **feedback** on larger devices



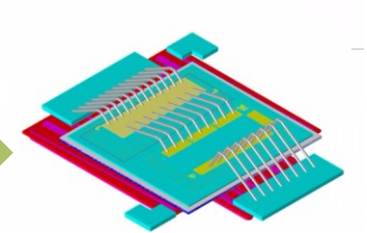
Package(Minipack)



GSG device



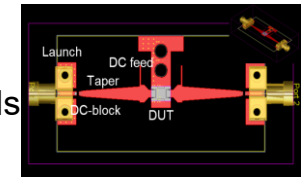
Power bar device

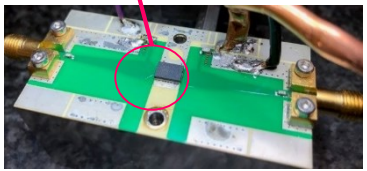


Chip(GaN & Moscap) and wire

What is needed :

- Right **package** design (close as possible to module environment)
- Assembly of **GaN dies** and **IPD** (Moscap initially)
- Design reliable and proper **test fixture** with **accurate calibration** standards
- **Measurement** setup (DC-Spar and load/source pull)

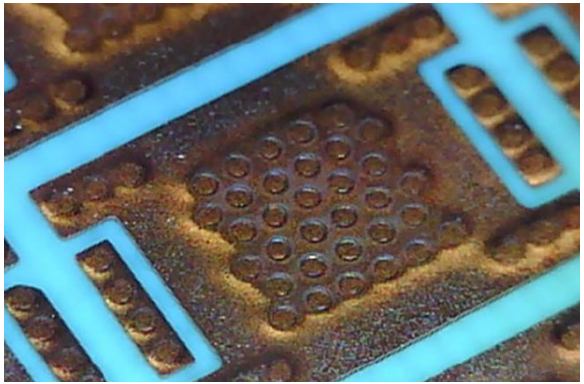




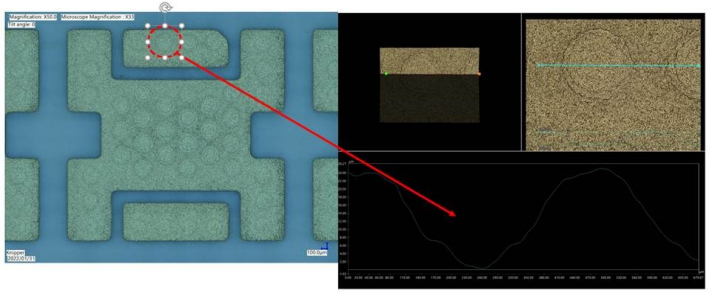
Test fixture example

Package selection

PCB base (LP Hoffman)

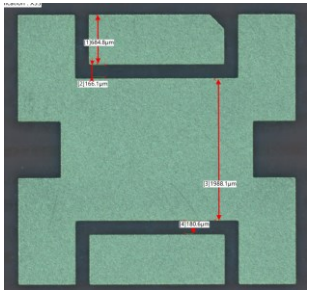


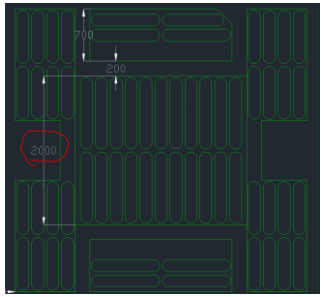
MiniPac HLP LF#04 (old version)

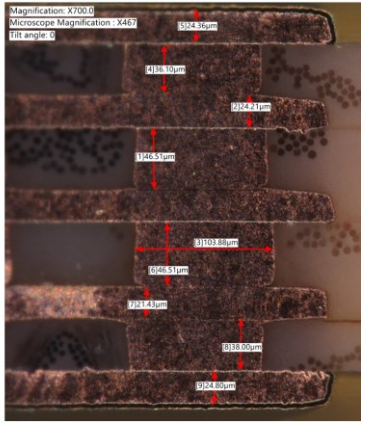


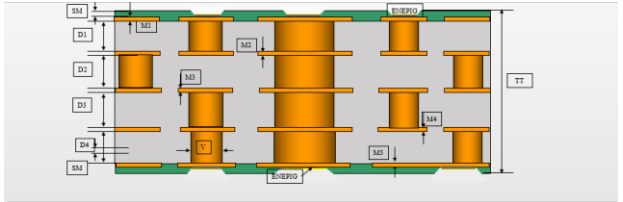
› „via hole“ ~ 20µm depths

Laminate base (Access)





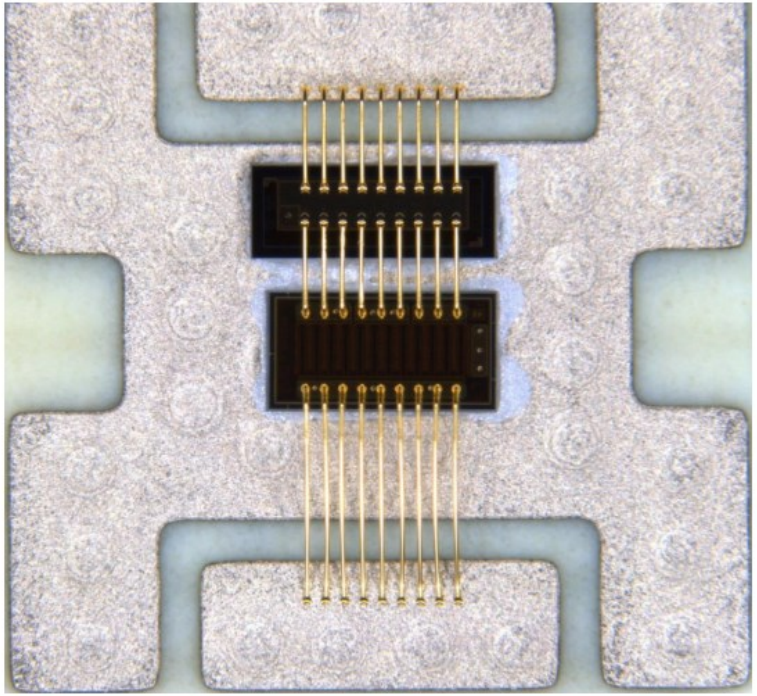




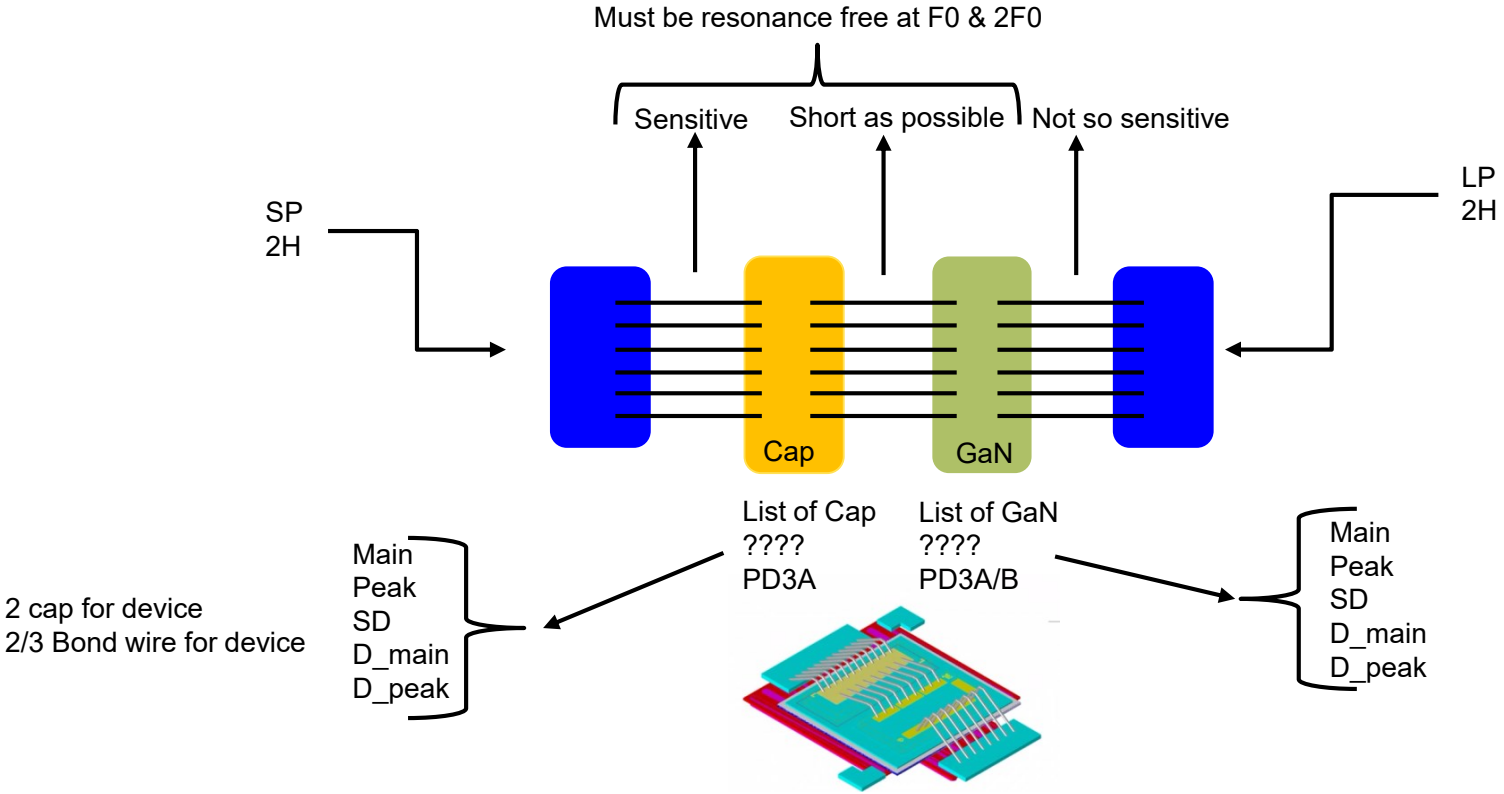
Unit size: um		Strip size : 187.5x50mm	Units/strip:324
Items		ACCESS Structure	
D1, D4	Dielectric thickness	40±15µm	
D2, D3,	Dielectric thickness	50±15µm	
M1 ~ M5	Metal thickness	20±7µm	
SM	Solder mask thickness(above metal)	15+/-7µm	
TT	Total thickness (Exclude Tsm & Bsm)	285± 30µm	
Solder Mask Type: AUS308		Prepreg Material: GEA-705G	
Top metal finish: ENEPIG		ENEPIG Ni: 2~5µm, Pd: 0.11~0.18µm, Au: 0.07~0.12µm	
Bottom metal finish: ENEPIG		ENEPIG Ni: 2~5µm, Pd: 0.11~0.18µm, Au: 0.07~0.12µm	

Example of assy of 1 variant (PCB version)

DoE No.	Wire Group	peak loop distance[µm]		loop height[µm]		projected wire length[µm]	
		target	measurements	target	measurements	target	measurements
1_3	G1_BW	106,88	104	185	178	525	535
1_3	G1_BW	106,88	110	185	180	525	534
1_3	G1_BW	106,88	114	185	180	525	533
1_3	G1_BW	106,88	115	185	182	525	525
1_3	G1_BW	106,88	113	185	185	525	526
1_3	G1_BW	106,88	125	185	186	525	526
1_3	G1_BW	106,88	112	185	184	525	528
1_3	G1_BW	106,88	115	185	186	525	527
1_3	G1_BW	106,88	113	185	186	525	527
1_3	G1_BW	106,88	118	185	180	525	528
1_3	D_BW	243	239	220	222	1130	1129
1_3	D_BW	243	225	220	223	1130	1130
1_3	D_BW	243	228	220	226	1130	1131
1_3	D_BW	243	232	220	219	1130	1131
1_3	D_BW	243	225	220	218	1130	1132
1_3	D_BW	243	217	220	222	1130	1132
1_3	D_BW	243	234	220	224	1130	1131
1_3	D_BW	243	232	220	220	1130	1131
1_3	D_BW	243	227	220	221	1130	1130
1_3	D_BW	243	230	220	220	1130	1129
1_3	G2_BW	110,3	54	135	129	490,2	490
1_3	G2_BW	110,3	53	135	133	490,2	488
1_3	G2_BW	110,3	54	135	128	490,2	488
1_3	G2_BW	110,3	52	135	132	490,2	488
1_3	G2_BW	110,3	53	135	130	490,2	488
1_3	G2_BW	110,3	53	135	133	490,2	487
1_3	G2_BW	110,3	60	135	133	490,2	489
1_3	G2_BW	110,3	54	135	128	490,2	488
1_3	G2_BW	110,3	53	135	131	490,2	488
1_3	G2_BW	110,3	50	135	131	490,2	489



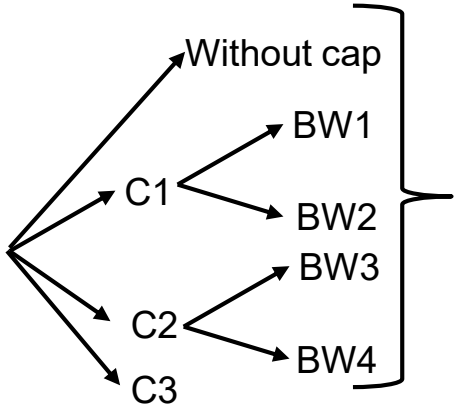
Build insight



Variants list

- 5.76 (24*240um) (10-20 pcs)
- 3.84 (16*240um) (10-20 pcs)
- 10.1 (42*240um) (Not available)
- 4.8 (12*400um) (10-20 pcs)
- 12 (30*400um) (10-20 pcs)
- 3.84 (12*320um) (10-20 pcs)
- 5.12 (32*160um) (10-20 pcs)
- 5.12 (16*320um) (10-20 pcs)
- 5.76 (36*160um) (10-20 pcs)
- 4.8 (30*160um) (10-20 pcs)
- 11.52 (36*320um) (10-20 pcs)
- 10.24 (32*320 um) (10-20 pcs)
- 2.4 (10*240um) (Not available)
- 1.92 (8*240um) (Not available)

14 dies(6dies from PD +8 new dies)



Green: Used in PD3 A/B

Red: Will be avaialble in Jan 2022

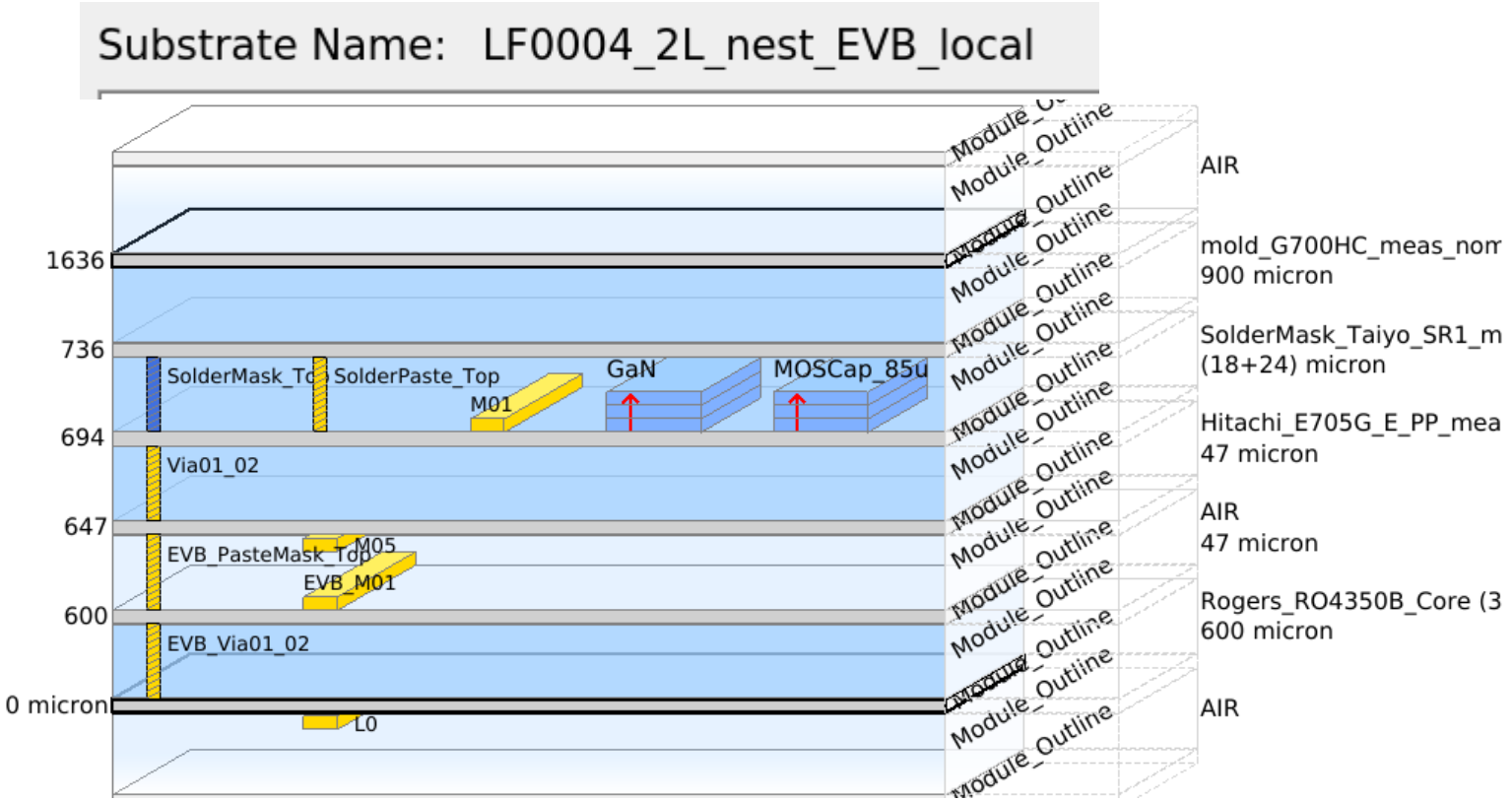
Orange: Will be avaialble in Feb 2022

Blue : Availiable in requied quanitiy

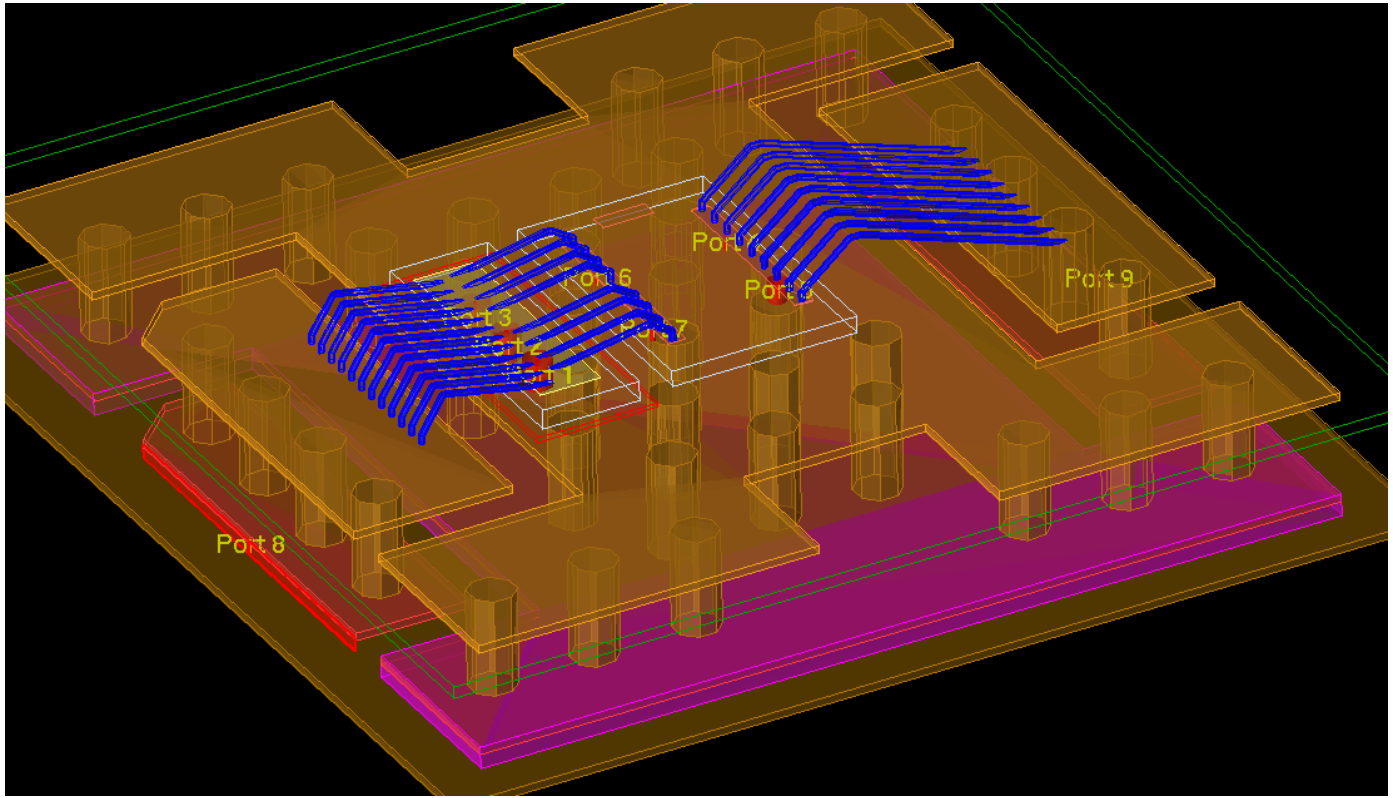
8variants for each device size
(2 die attaches and 4 bond-wire shapes)

14*5=70 Variants

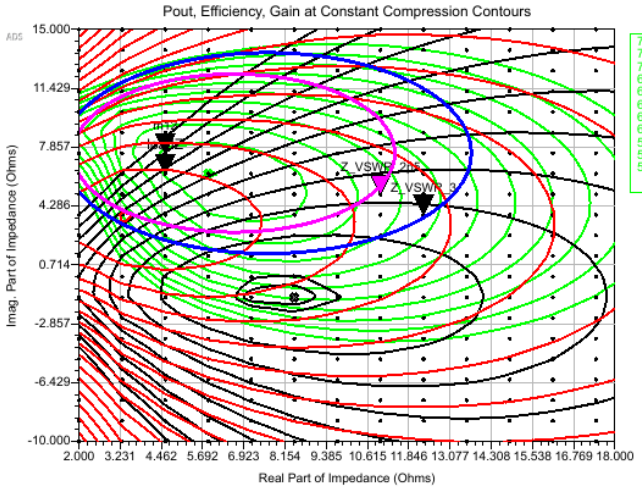
PCB pacakge (PLP3839) : Substrate



PLP3839: 3D View



C=5.56pF
DOE3_2



Eff	Gt	Pout
73.6	15.5	43.5
72.0	15.0	43.5
70.0	14.5	43.0
68.0	14.0	42.5
66.0	13.5	42.0
64.0	13.0	41.5
62.0	12.5	41.0
60.0	12.0	40.5
58.0	11.5	40.0
56.0	11.0	39.5
54.0	10.5	39.0
	10.0	

Power Sweep Inspector

Move Marker 'loadZ' to desired impedance point.

VSWR Locus of Points selector is located on Constant Compression Loadpull page.

VSWR Locus center Impedance = VSWR=3: 8.43 - j1.25

Eqn VSWRVal=3 Eqn VSWRVal1=2.5

VSWR Locus of Points selector is located on Constant Compression Loadpull page.

VSWR Locus center Impedance = VSWR=3: 4.57 + j7.50

Summary of Performance at Compression

Marker Impedance	Marker Gamma	Reference Compression Level (dB)
4.57 + j6.25	0.83 / 165.63	3

Pout (dBm)	Eff (%)	Gt (dB)
40.20	72.25	15.07

AMPM (dBm)	IRL (dB)	Zin (Ohm)
-7.34	-2.17	0.57 + j6.63

✖ In plots below corresponds to this data.

Summary of Performance at Compression

Marker Impedance	Marker Gamma	Reference Compression Level (dB)
4.57 + j7.50	0.84 / 162.80	3

Pout (dBm)	Eff (%)	Gt (dB)
39.52	72.40	14.72

AMPM (dBm)	IRL (dB)	Zin (Ohm)
-4.92	-2.54	0.72 + j6.77

✖ In plots below corresponds to this data.

VSWR = 2.5 point DATA

Marker Impedance	Marker Gamma	Reference Compression Level (dB)
11.00 + j5.00	0.64 / 168.01	3

Pout (dBm)	Eff (%)	Gt (dB)
42.37	69.08	14.31

AMPM (dBm)	IRL (dB)	Zin (Ohm)
-0.94	-4.78	0.95 + j6.03

✖ In plots below corresponds to this data.

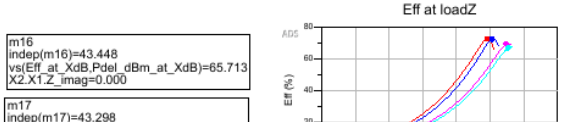
VSWR = 3 point DATA

Marker Impedance	Marker Gamma	Reference Compression Level (dB)
12.29 + j3.75	0.61 / 170.88	3

Pout (dBm)	Eff (%)	Gt (dB)
42.64	66.81	14.14

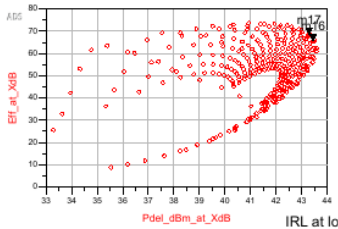
AMPM (dBm)	IRL (dB)	Zin (Ohm)
-0.20	-5.22	0.96 + j5.89

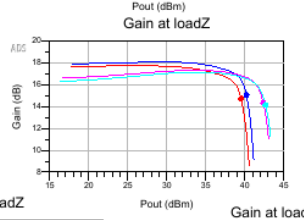
✖ In plots below corresponds to this data.

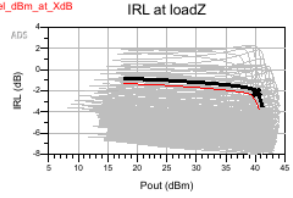


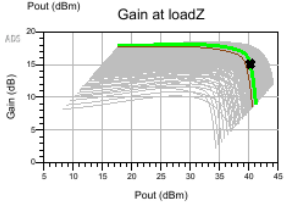
m16
indep(m16)=43.448
vs(Eff_at_XdB,Pdel_dBm_at_XdB)=65.713
X2.X1.Z_Imag=0.000

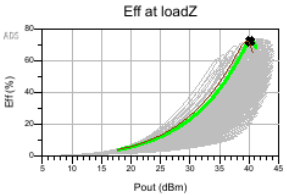
m17
indep(m17)=43.298
vs(Eff_at_XdB,Pdel_dBm_at_XdB)=68.762
X2.X1.Z_Imag=1.250

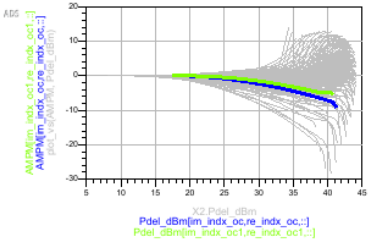








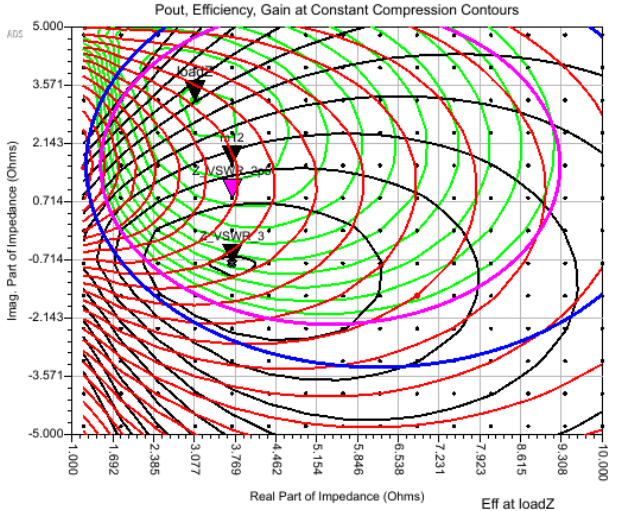




DOE5_5

C=3.55pF

Class C
Lg2=260um



Eff	Gt	Pout
76.5	19.8	47.0
76.0	19.5	46.5
74.0	19.0	46.0
72.0	18.5	45.5
70.0	18.0	45.0
68.0	17.5	44.5
66.0	17.0	44.0
64.0	16.5	43.5
62.0	16.0	43.0
60.0	15.5	42.5
58.0	15.0	42.0
	14.5	

Power Sweep Inspector

Move Marker 'loadZ' to desired impedance point.

VSWR Locus of Points selector is located on Constant Compression Loadpull page.

VSWR Locus center Impedance = VSWR=3: 3.71 - j0.80

Eqn VSWRVal=3 Eqn VSWRVal1=2.5

VSWR Locus of Points selector is located on Constant Compression Loadpull page.

VSWR Locus center Impedance = VSWR=3: 3.71 + j1.60

Summary of Performance at Compression

Marker Impedance	Marker Gamma	Reference Compression Level (dB)
3.09 + j3.20	0.88 / 172.65	3

Pout (dBm)	Eff (%)	Gt (dB)
43.96	76.57	15.86

AMPM (dBm)	IRL (dB)	Zin (Ohm)
-64.79	-7.40	0.61 + j3.63

✖ In plots below corresponds to this data.

Summary of Performance at Compression

Marker Impedance	Marker Gamma	Reference Compression Level (dB)
3.71 + j1.60	0.86 / 176.31	3

Pout (dBm)	Eff (%)	Gt (dB)
45.81	75.11	16.08

AMPM (dBm)	IRL (dB)	Zin (Ohm)
-55.07	-9.16	0.57 + j3.37

✖ In plots below corresponds to this data.

VSWR = 2.5 point DATA

Marker Impedance	Marker Gamma	Reference Compression Level (dB)
3.71 + j0.80	0.86 / 178.16	3

Pout (dBm)	Eff (%)	Gt (dB)
46.41	72.88	16.07

AMPM (dBm)	IRL (dB)	Zin (Ohm)
-50.37	-9.48	0.54 + j3.24

✖ In plots below corresponds to this data.

VSWR = 3 point DATA

Marker Impedance	Marker Gamma	Reference Compression Level (dB)
3.71 - j0.80	0.86 / -178.16	3

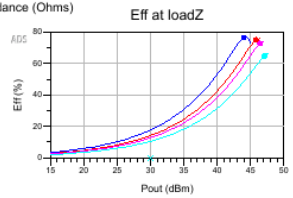
Pout (dBm)	Eff (%)	Gt (dB)
47.04	64.83	15.31

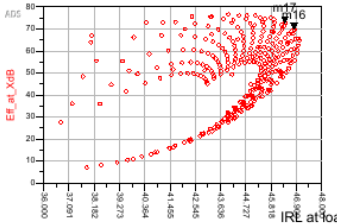
AMPM (dBm)	IRL (dB)	Zin (Ohm)
-35.98	-10.14	0.53 + j2.93

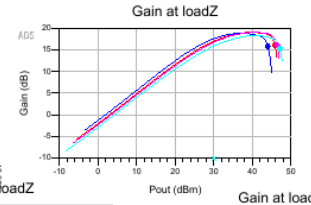
✖ In plots below corresponds to this data.

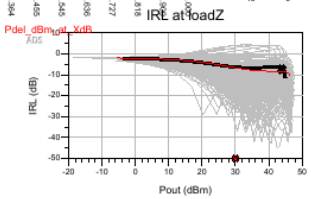
m16
indep(m16)=46.802
vs(Eff_at_XdB,Pdel_dBm_at_XdB)=69.783
X2.X1.Z_imag=-1.110E-15

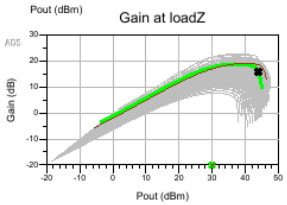
m17
indep(m17)=46.409
vs(Eff_at_XdB,Pdel_dBm_at_XdB)=72.882
X2.X1.Z_imag=0.800

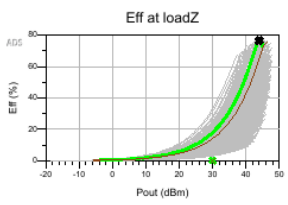


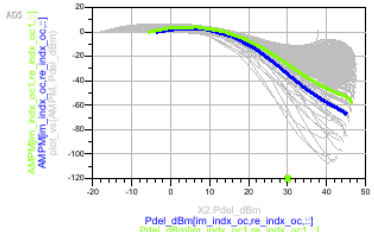












Compression = 3, Class C, 5_1, 5_2, 5_3,5_4, 5_5

DOE	Cap (pF)	Zout (ohm)		Pout(dBm)	Eff	Gt (dB)	Zin(ohm)	
5_1	-	4	j2.3	45	68.7	18.7	0.38	j2.6
5_2_P018	6.5	3.71	j1.6	45.77	76	15.88	0.54	j2.94
5_2 N044	6.5	3.71	j1.6	45.91	71	16.8	0.47	j3.09
5_3_P018	6.5	3.09	j0.8	46	74	14.69	0.89	j3.15
5_3 N044	6.5	3.71	j0.8	46.32	68.8	17.52	0.48	j3.48
5_3 N044_V1	6.5	3.71	j0.8	46.5	70	16.84	0.49	j4
5_3 N044_V2	6.5	3.71	j0.8	46.4	68.5	17.3	0.5	j3.44
5_4	3.55	3.71	j1.6	45.9	74	16.6	0.45	j2.87
5_5	3.55	3.71	j1.6	45.8	75	16	0.57	j3.37

Selected Varients

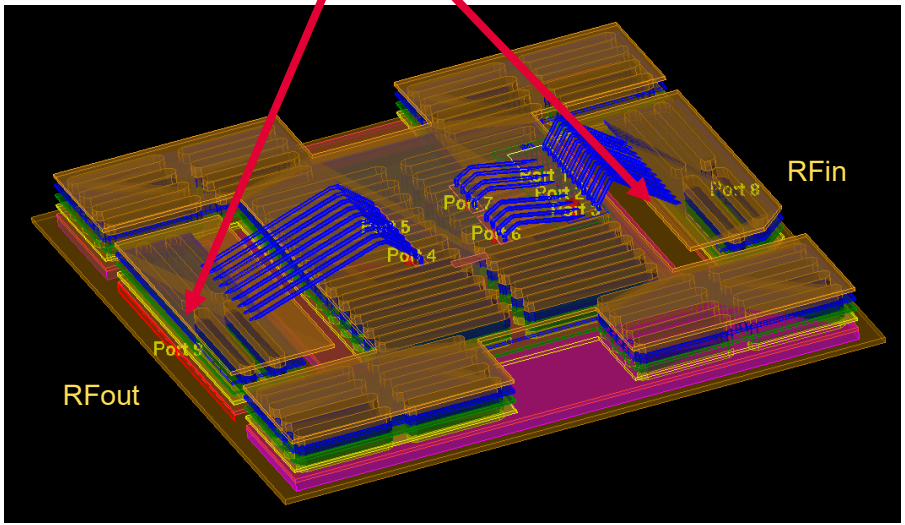
- Two main substrates, the POR and N044
- The N044 is better than the POR for the Gain by 1dB for DOE 5_2 & 5_3.
- F0r N9501B below 5.6pF , Moscap are not available in N044 substrate.

DOE	Cap (pF)	Zout (ohm)		Pout(dBm)	Eff	Gt (dB)	Zin(ohm)	
5_1	-	4	j2.3	45	68.7	18.7	0.38	j2.6
5_2 N044	6.5	3.71	j1.6	45.91	71	16.8	0.47	j3.09
5_3 N044	6.5	3.71	j0.8	46.32	68.8	17.52	0.48	j3.48
5_4	3.55	3.71	j1.6	45.9	74	16.6	0.45	j2.87
5_5	3.55	3.71	j1.6	45.8	75	16	0.57	j3.37

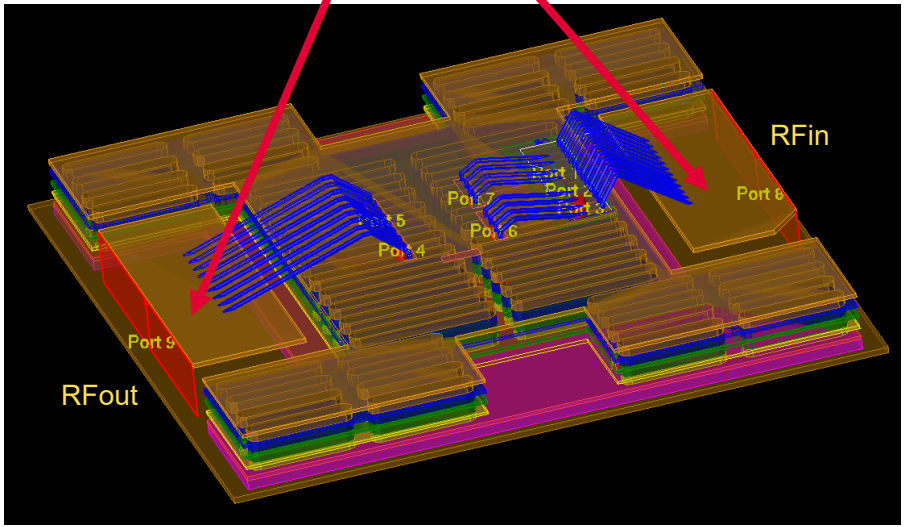
Models

detail model for MOSCap → IC_LD8C_lib:Cap_1010x270W_10p19 oxide 900nm

› "full" model with bondpad via



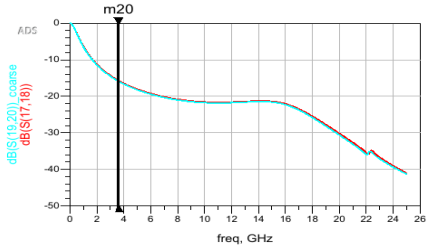
› "reduced" model w/o bondpad via



S-Parameters

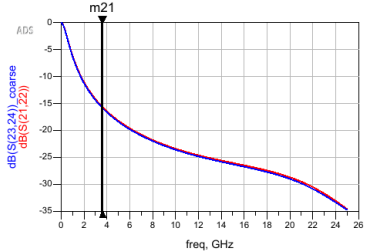
RFin-gate loop
Full model

m20
freq=3.600GHz
dB(S(17,18))=-15.663
dB(S(19,20))_coarse=-15.860



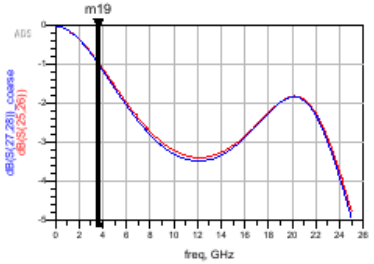
RFin-gate loop
Reduced model

m21
freq=3.600GHz
dB(S(21,22))=-15.627
dB(S(23,24))_coarse=-15.829



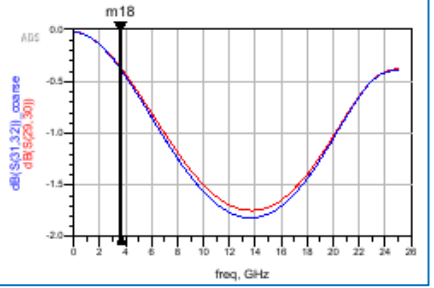
MOSCap-GaN
Full model

m19
freq=3.600GHz
dB(S(25,26))=-0.942
dB(S(27,28))_coarse=-0.981



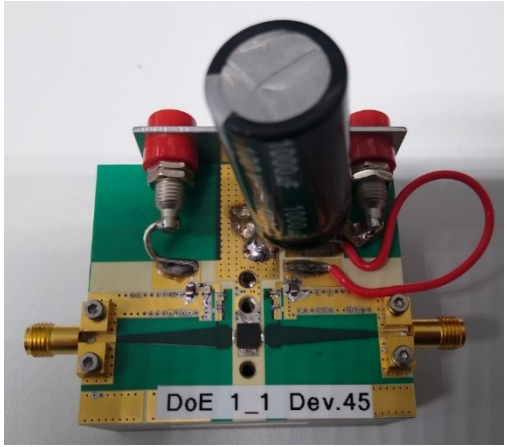
MOSCap-GaN
Reduced model

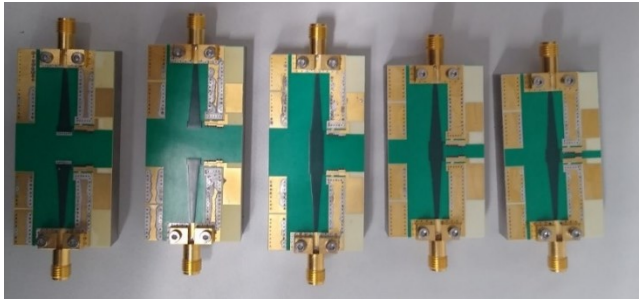
m18
freq=3.600GHz
dB(S(29,30))=-0.362
dB(S(31,32))_coarse=-0.382



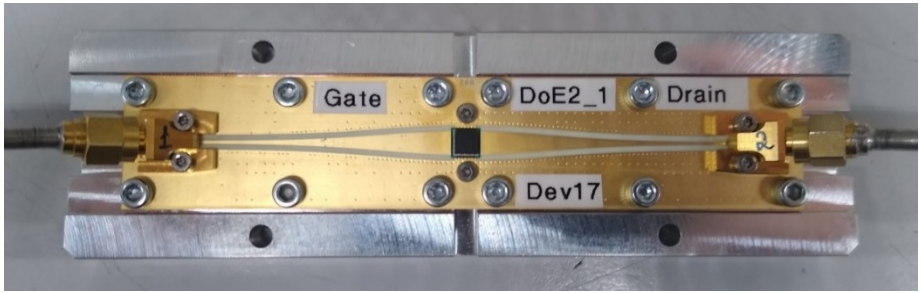
Two test fixtures

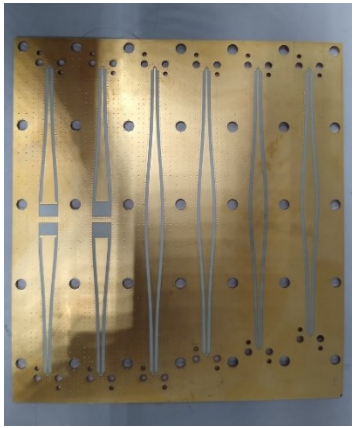
Test fixture with DC feed



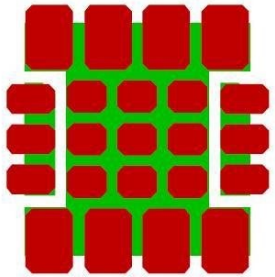


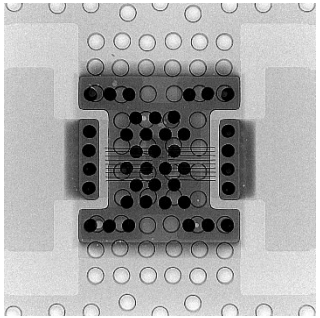
Test fixture with external DC feed

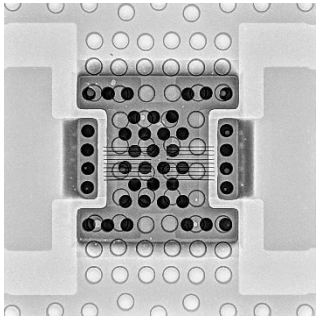


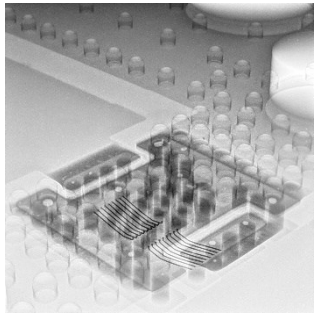


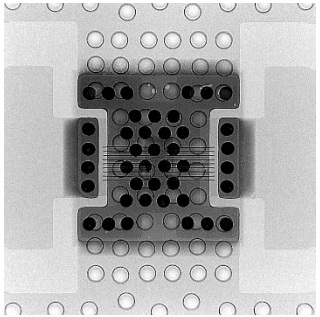
AST01

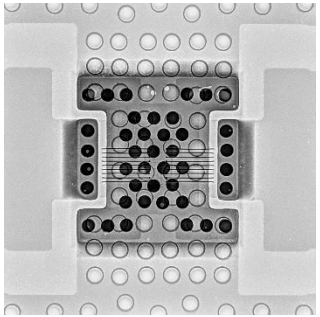


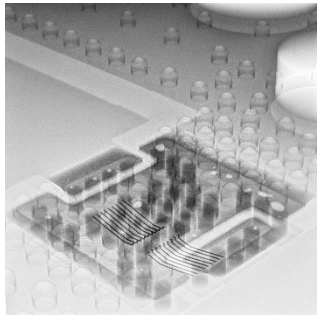




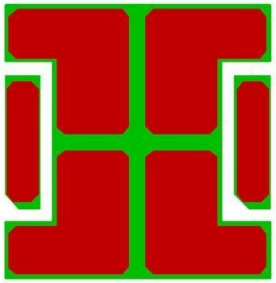


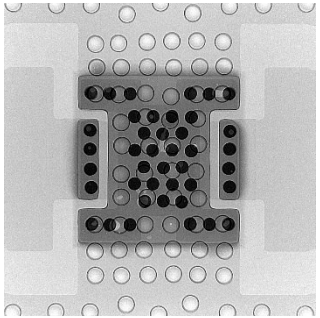


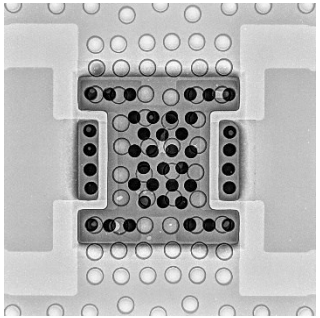


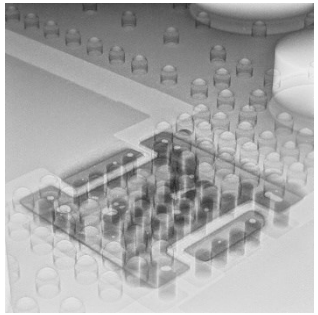


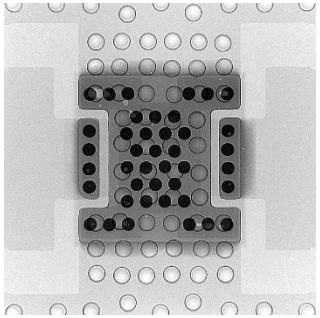
AST02

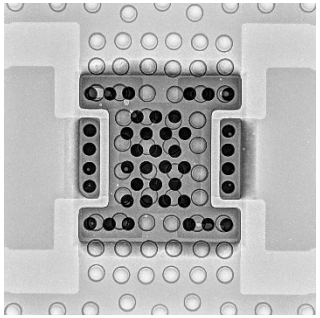


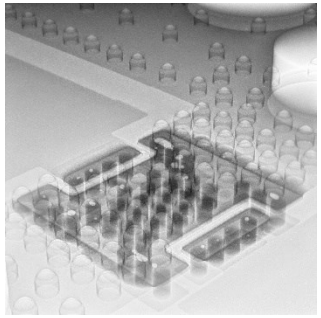




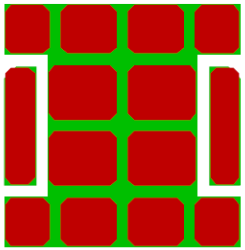


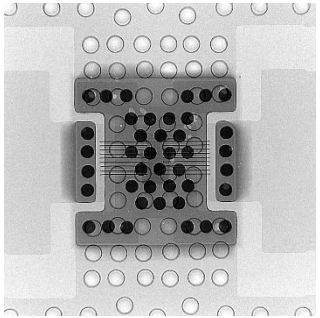


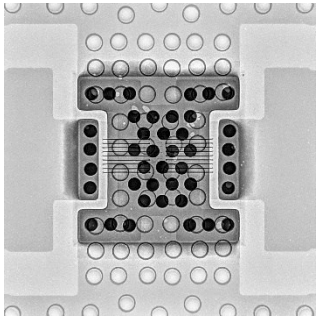


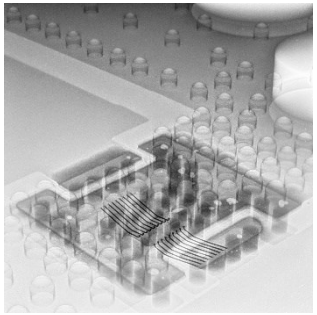


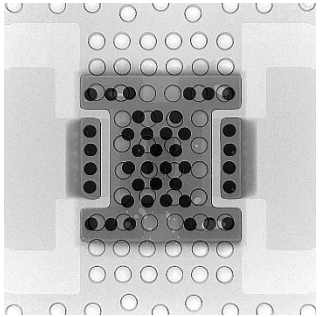
SIEB01

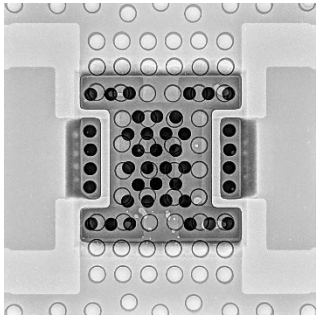


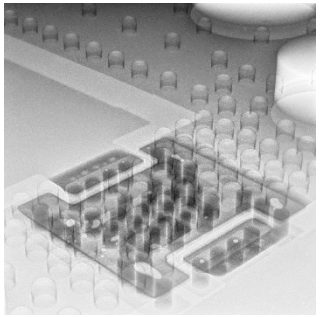






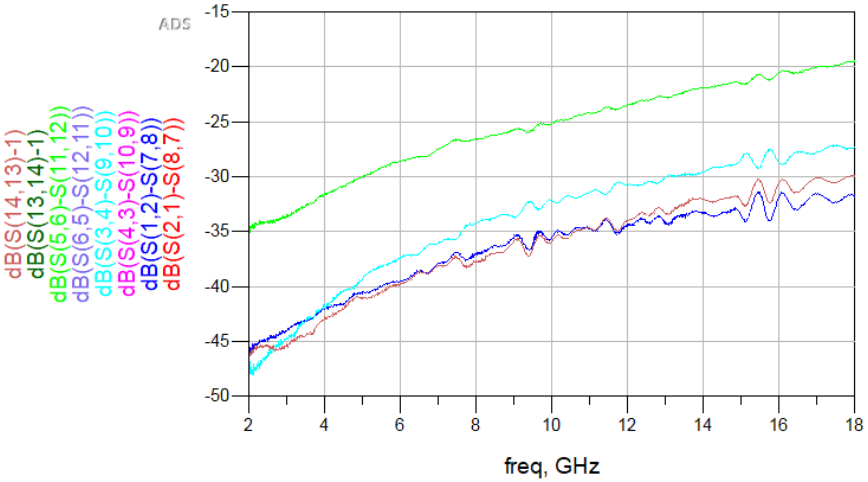




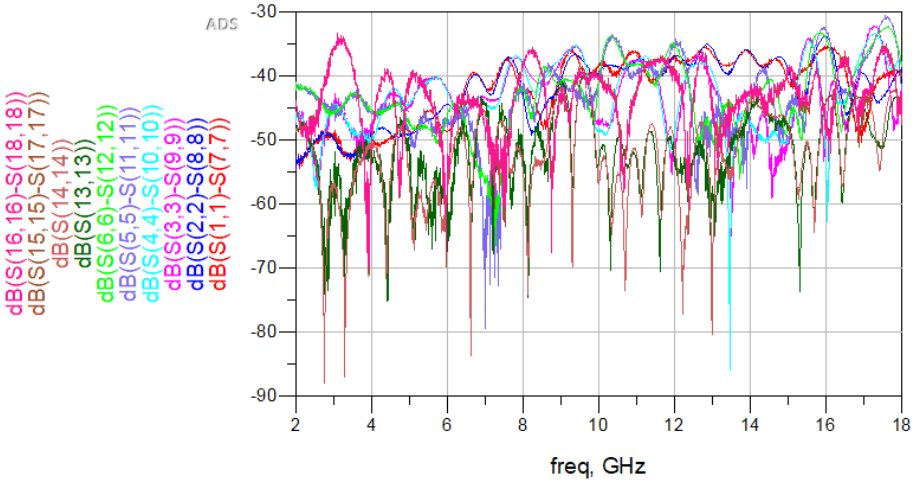


Residual Test – Thru , Line1 , Line2 , Line3, Short

Transmission Residuals (S12, S21)

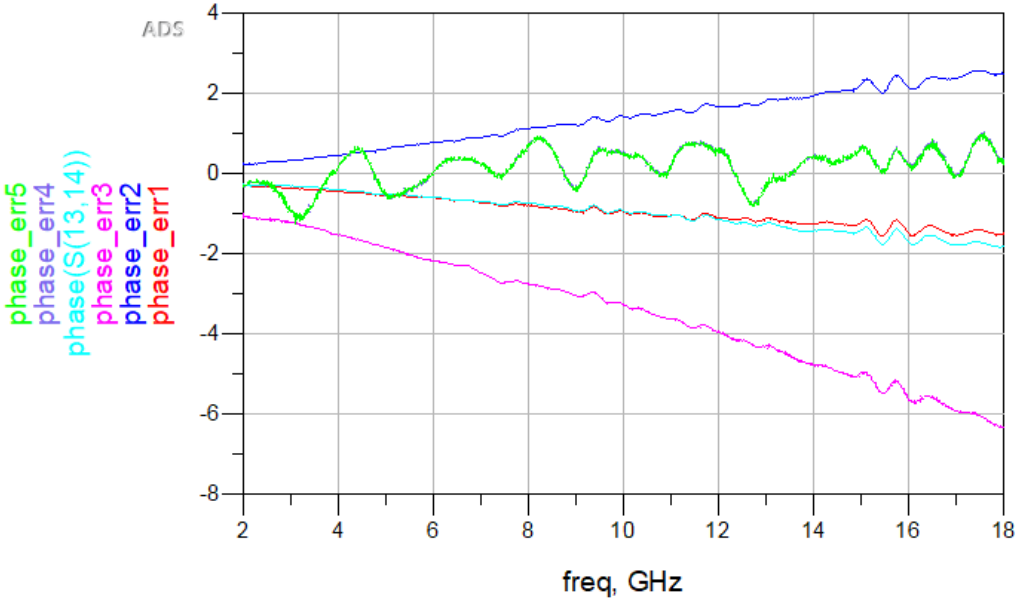


Reflection Residuals (S12, S21)

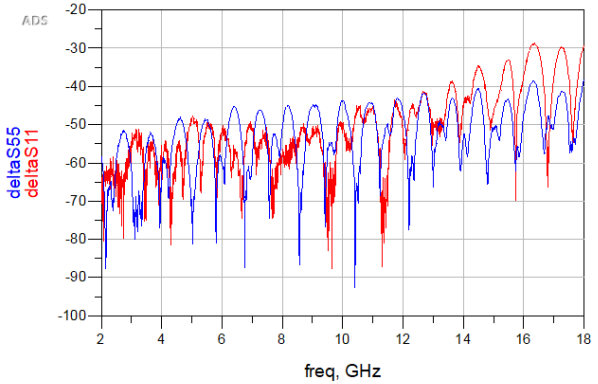


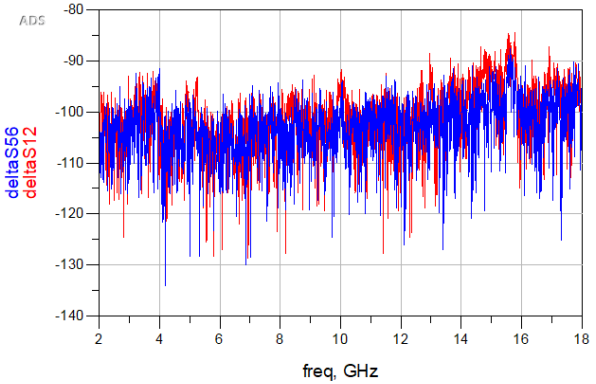
Residual Test – Transmission phase error

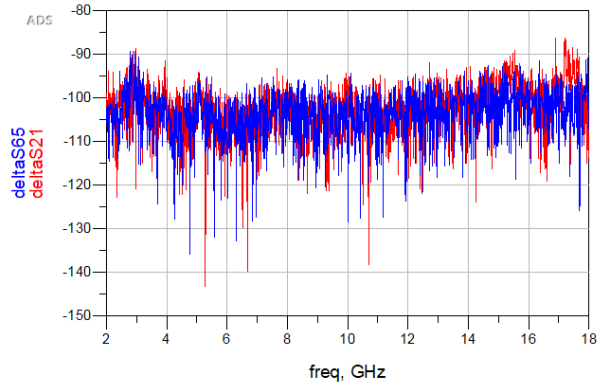
› The degredation of the transmition residuals at higher frequencies is almost entirely caused by phase difference of S(1,2) and S(2,1) between measured & simulated PCB standard

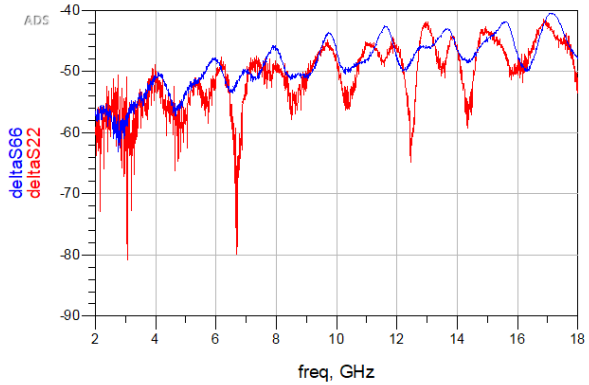


Repeatability test: short





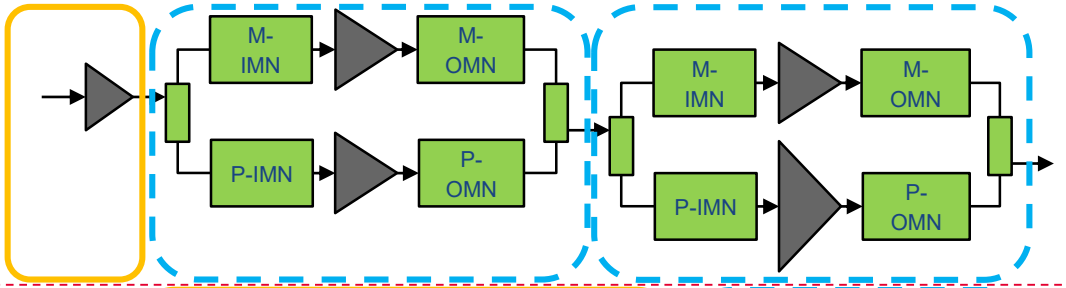




Proposed architectures and their potential implementation

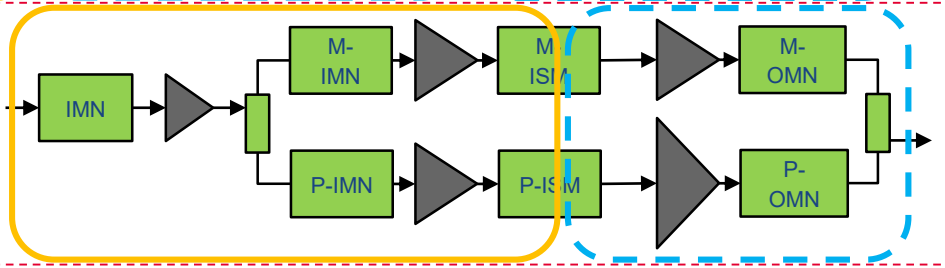
Alternative architectures

RF GaN:Si on laminate
MMIC/RFIC (LDMOS/B11)
Building block (RF GaN:Si, LDMOS, IPD)



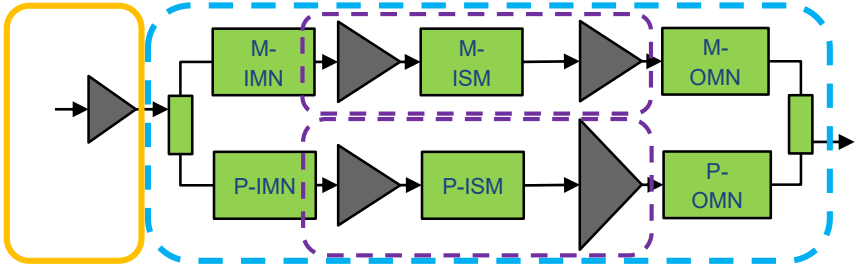
Description:
- Driver in DOH mode
- FS similar to PD3

Prelim. conclusion:
- FS input impedance variation not compatible with the Driver DOH output load sensitivity



Description:
- Dual driver and pre-driver integrated in MMIC. Dual output
- FS with dual input and similar output as PD3

Prelim. conclusion:
- Good potential for achieving higher integration
- Development timeline might not fit



Description:
- Dual driver and FS
- Building block per branch
- FS with similar output as PD3
- Separate pre-driver

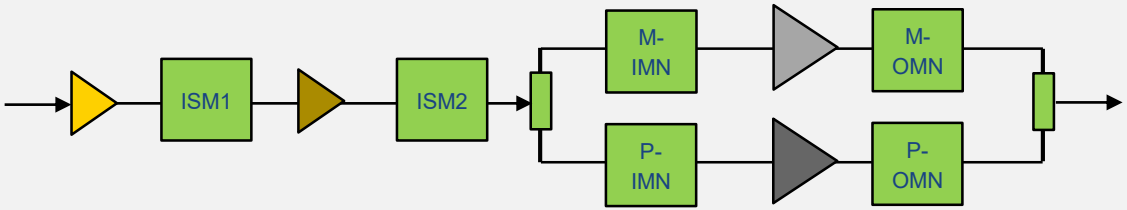
Prelim. conclusion:
- Most suitable option as alternative to the current architecture
- Enables the option to go to 3W DOH

Architectures

matching network | pre-driver | driver | main | peak

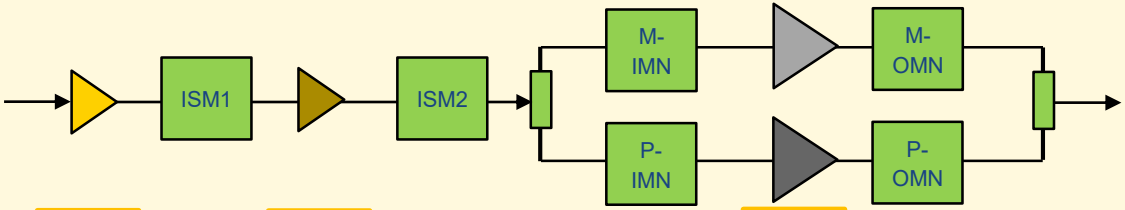
Target with current RF GaN C1 technology

Current



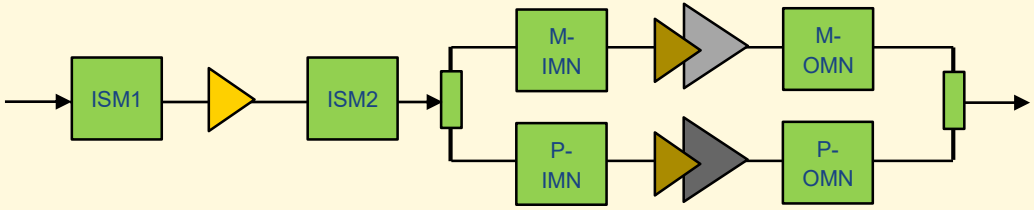
Efficiency 40%

A1: Improved



Efficiency 43%

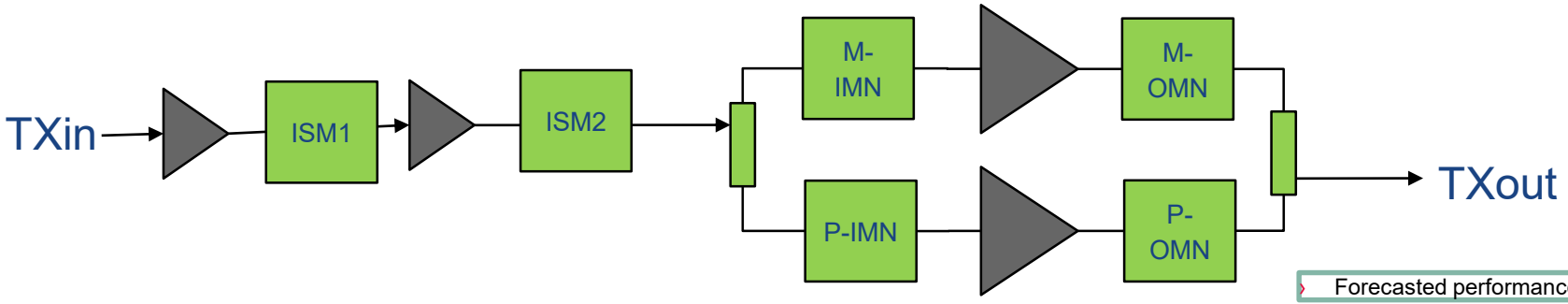
A2: New concept



Efficiency 45%

back

Single Driver 2Way Doherty



- PD3 expected performance after tuning
  - 42-44%
- Forecasted performance after re-design
  - **45-47%**

- Re-Design
  - +0.5%
- Smaller periphery
- LDMOS
- GaAs
- IPD for matching
  - +0.5%
- Input Splitter:
  - IPD usage (BW vs Perf)
  - Hybrid
    - Non 50Ω
    - Reflective ??
- Output Combiner:
  - Harmonic matching
  - Peak power margin
  - Stack-up material
  - Ceramic circuit ??
  - +2%
  - +3%

New predictions assume that the current PD3 HW will correspond to the simulated performance

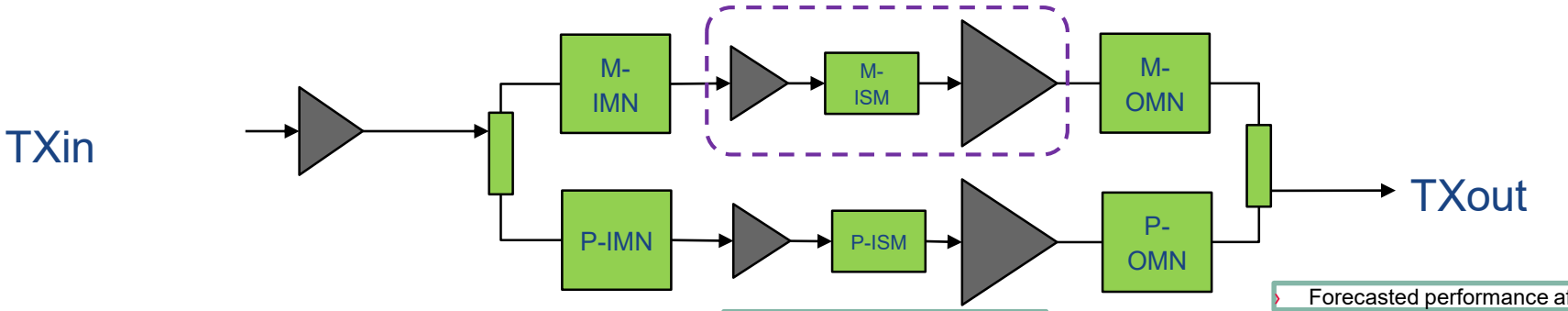
Single Driver 2Way Doherty

	Activities
A1	› More measurements on RF GaN – Refine measurements capability (speed, resources,…)
A2	› Optimization of RFGaN die size (FS Main & Peak, Driver) – Target performance, Lifetime, Process variation
A3	› Devices with input pre-match – Access to existing work – Measure (LP, s-par,…) → Model re-fit → Adjust design flow
A4	› Fit output combiner in 6x10 mm – Include improvements (2nd Harm, VBW, Production variation,…)
A5	› Define the IPD strategy (GaAs, Si, …) – Verify internal IPD availability – Verify the commercial feasibility of WIN GaAs IPD sourcing
A6	› Input splitter integration (IPD) – Identify and keep some level of tuneability
A7	› Assess the production trimming for yield
A8	› Verify the LDMOS availability (existing material, PDK, etc)
A9	› Benchmark the use of GaAs for the Driver
A10	› Assess the performance improvement of the re-design of the pre-driver – Define first the ideal requisites

Dual Driver 2Way Doherty

› PD3 expected performance after tuning

42-44%



› Forecasted performance after re-design

47-49%

› Re-Design

Input Splitter:
- › IPD usage (BW vs Perf)
- › Hybrid
  - Non 50Ω
  - Reflective ??

Driver optimization:
- › Split between main and peak allow for a smaller driver in main
- › Even better potential if Vdd driver is reduced

Output Combiner:
- › Harmonic matching
- › Peak power margin
- › Stack-up material
- › Ceramic circuit ??

+0.5%

+4.5%

+5%

New predictions assume that the current PD3 HW will correspond to the simulated performance

Dual Driver 2Way Doherty

	Activities
B1	› Compile and summarize current work (simulation based) – Include the analysis of the advantages and disadvantages
B2	› Design and implement the building block (Driver + IPD + Main/Peak) – Phased approach (DM + M, DP + P, IPD + M,...) – Include the modeling adjustment
B3	› Design and implement 2Way Assy DOH – Phased approach (dual input → single input) – Reuse as much as possible the A4 output combiner design – Prepare the path for future integration of the splitter in the pre-driver output (OCTOPUS project)
B4	› Reuse the pre-driver redesign, A10, for the full lineup
B5	› Assess the feasibility of mix technologies – LDMOS & GaAs → Simulation based

Activities list

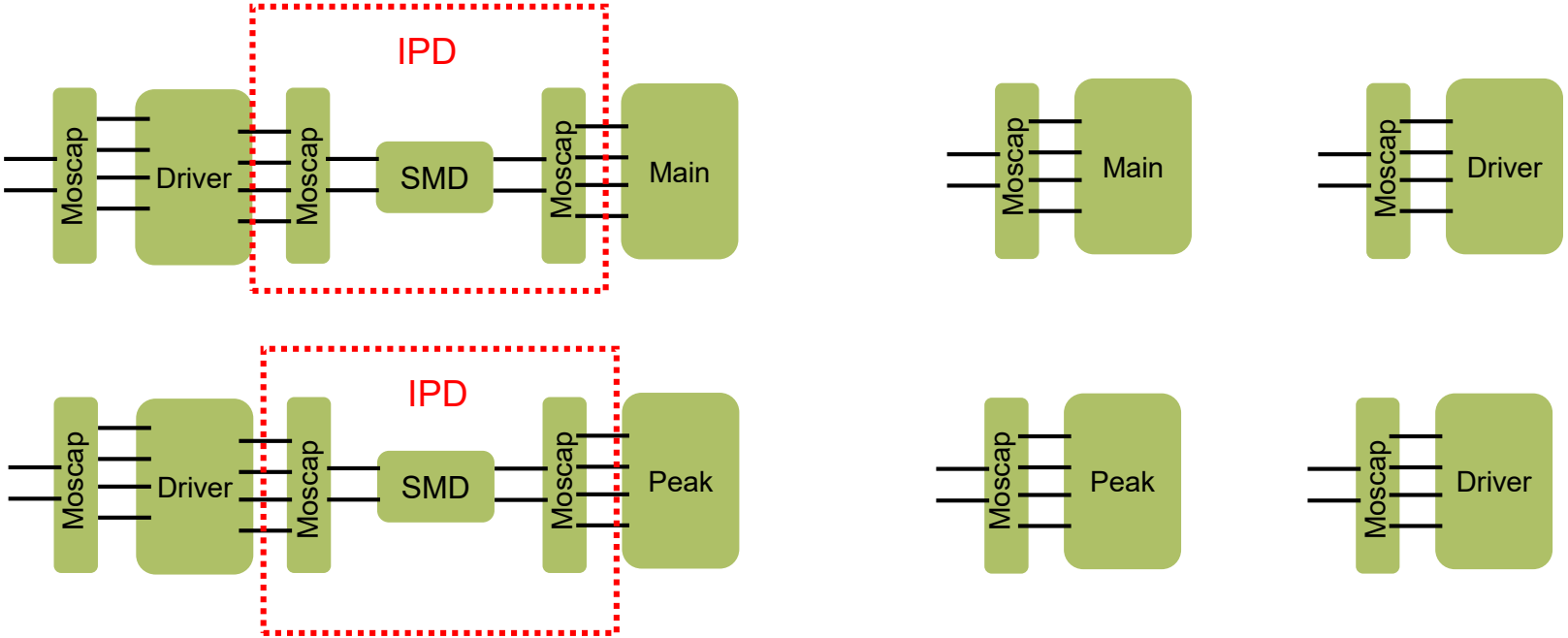
A1	Device database	
A2	Die and measurement selection	
A3	PCB(minipack)/Fixture design	
A4	Measurements of single stage (taper)	
A5	Data analysis	
A6	Matched PCB design of single device	
A7	Measurements of matched devices	★ Deliverable 1.0
A8	Interstage matching design	
A9	Measurements of each branches (taper)	
A10	Matched PCB design for each branch	
A11	Measurements of each branch	★ Deliverable 1.1
A12	DPA design in PCB	
A13	Measurements of DPA	★ Deliverable 2.0
A14	DPA design in Laminate	
A15	Measurements of DPA	★ Deliverable 2.1
A16	Predriver design	★ Deliverable 3.0

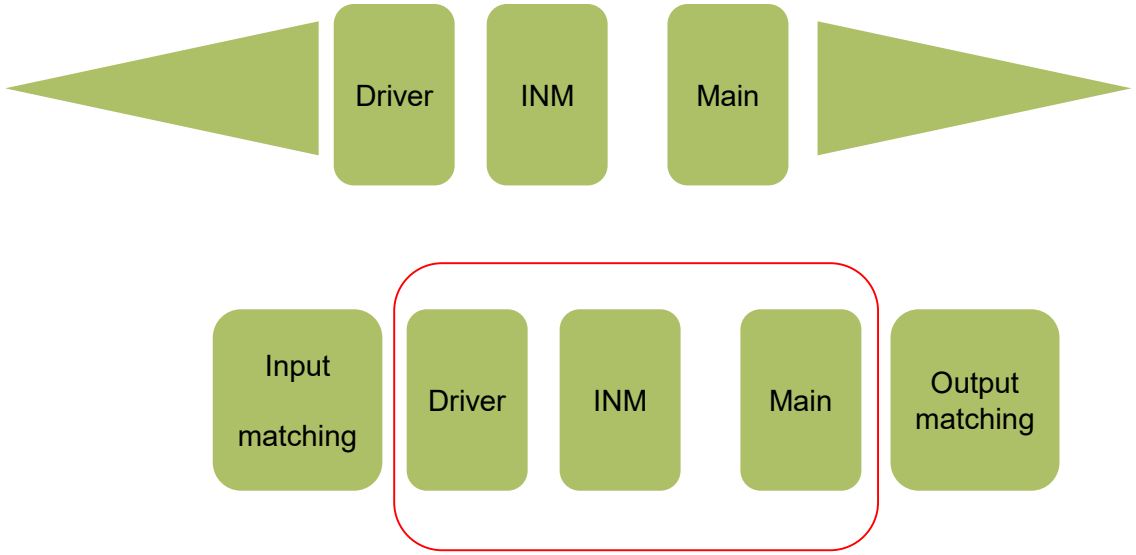
Ongoing activity and open items

Open topics

- Different driver technology (LDMOS)
- Quasi load insensitive design (Combiner optimization)
- Broadband design techniques mainly on INM and combiner
- Model verification or LP data extraction techniques to the design
- IPD integration on different section on different IPDs technology (even combiner ?)
- Smaller package or higher power on different laminates such as PHS …etc.

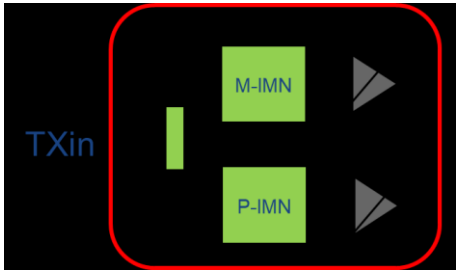
INM design on PCB / IPD



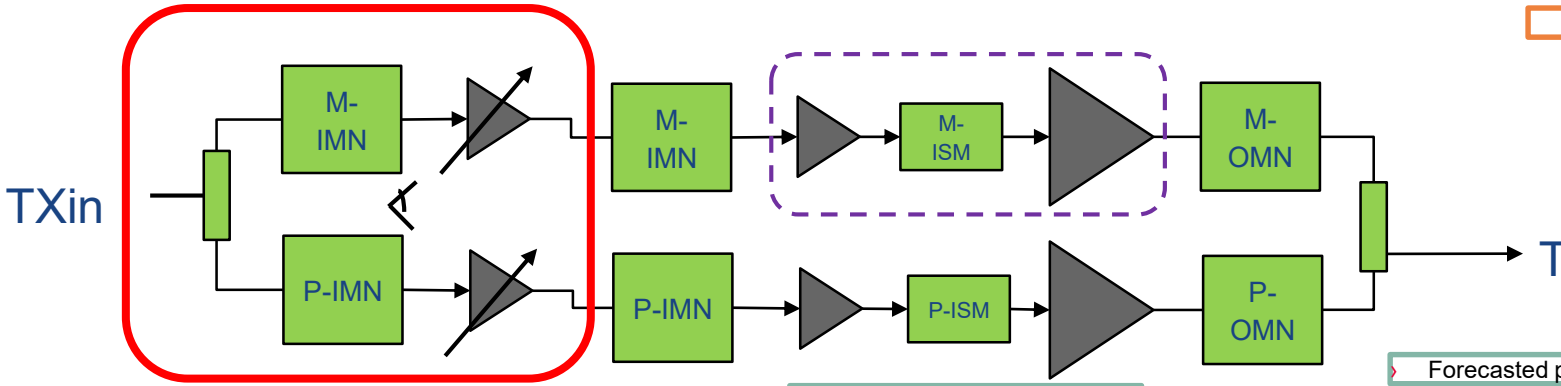


Predriver design

			Duration	Owner
A16.0	Predriver blocks	Checking availability of bocks in desired frequency band of interest		
A16.1	Predriver design	Re-simulate the blocks and tune for our specs		
A16.2	Predriver design	Integration of all blocks in single chip and do tapeout in shared reticle		



Dual Driver 2Way Doherty



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+4.5%

+5%

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Part of your life. Part of tomorrow.