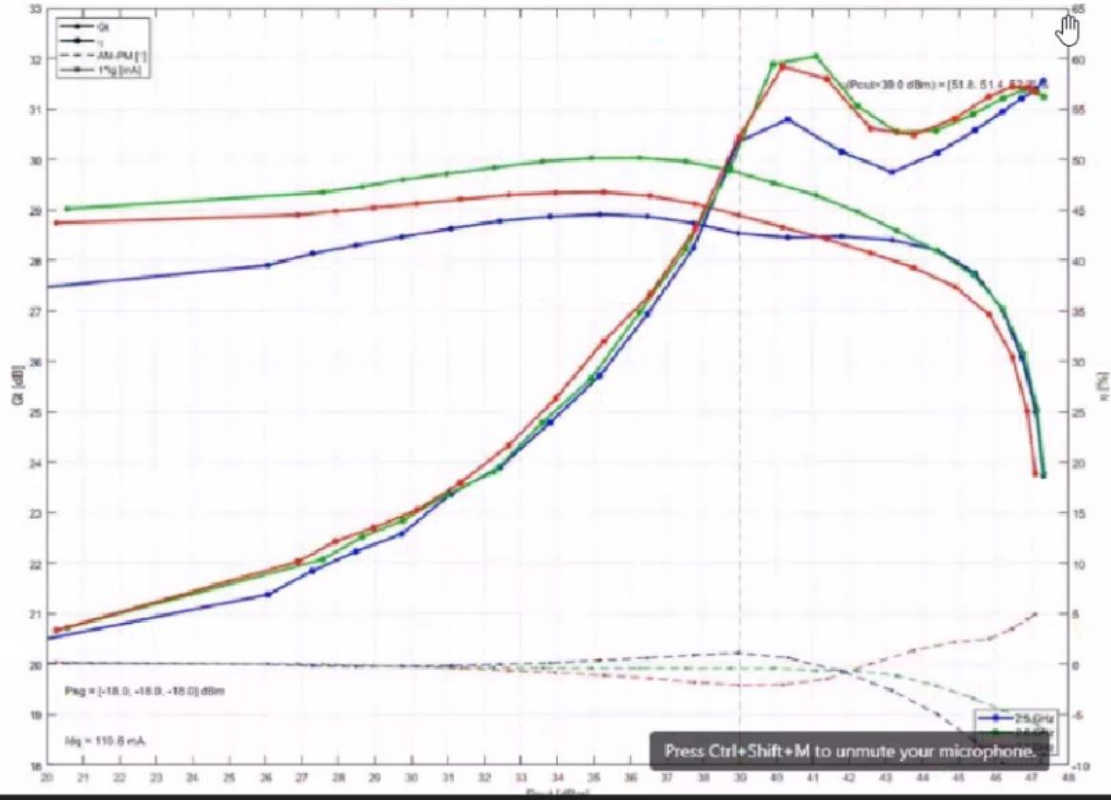
PAM

Measurements from competition

E///

B41 Measurements – power sweep



B41 (200MHz wide)

Similar performance as in pulsed measurements can be achieved bu gate-lag makes biasing difficult.

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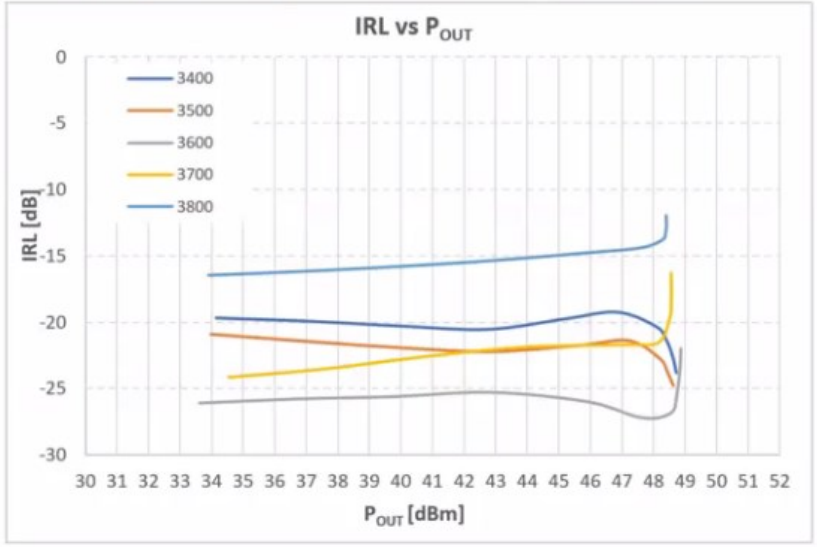
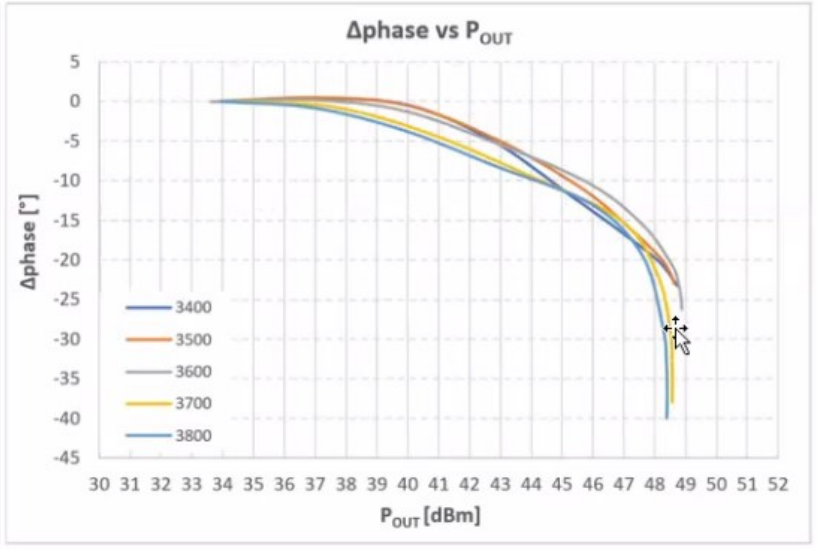
Analysis of competition - NXP Eval Board A5M36TG140-TC - 04 Sep 2023

Measurement results *Date of meas execution: 24 Aug 2023*





Test conditions:

Test signal: **Pulsed Signal 20uS/10%**

Test frequency: 3400, 3500, 3600, 3700, 3800 MHz Air temperature: T= +25° C

V_{DD1} = 5Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 145 mA, I_{DQC2} = 25 mA, I_{DQP1} = 35 mA, V_{GP2} = V_{Bias} – 0.31 Vdc*

** Increase VGP2 (peaking side) until IDQP2 = 40 mA current is attained, and then subtract 0.31 V for final VGP2 bias voltage*

Figure 11 – IRL and AMPM curves of complete lineup across band

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Analysis of competition - NXP Eval Board A5M36TG140-TC - 04 Sep 2023

Measurement results *Date of meas execution: 01 Sep 2023*

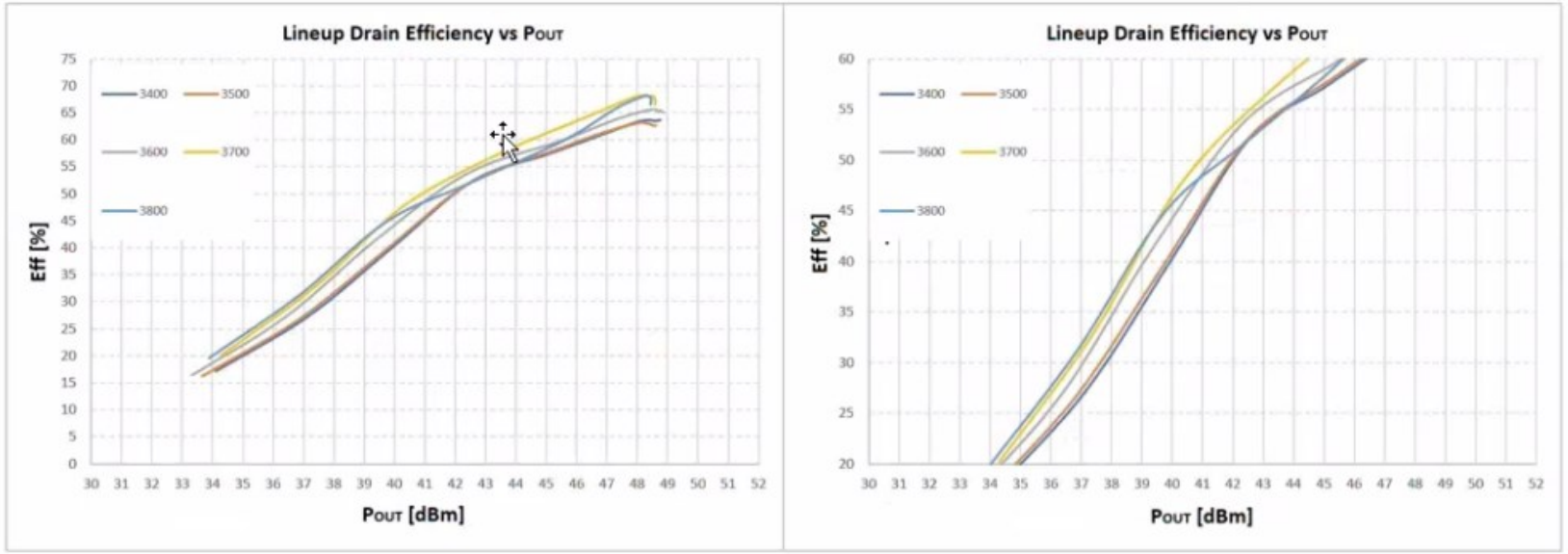

Figure 9

Lineup Drain Efficiency across band with pulsed CW signal

Test conditions:

Test signal: **Pulsed Signal 20uS/10%**

Test frequency: 3400, 3500, 3600, 3700, 3800 MHz Air temperature: T= +25° C

V_{DD1} = 5 Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 145 mA, I_{DQC2} = 25 mA, I_{DQP1} = 35 mA, V_{GP2} = V_{Bias} – 0.31 Vdc*

** Increase VGP2 (peaking side) until IDQP2 = 40 mA current is attained, and then subtract 0.31 V for final VGP2 bias voltage*

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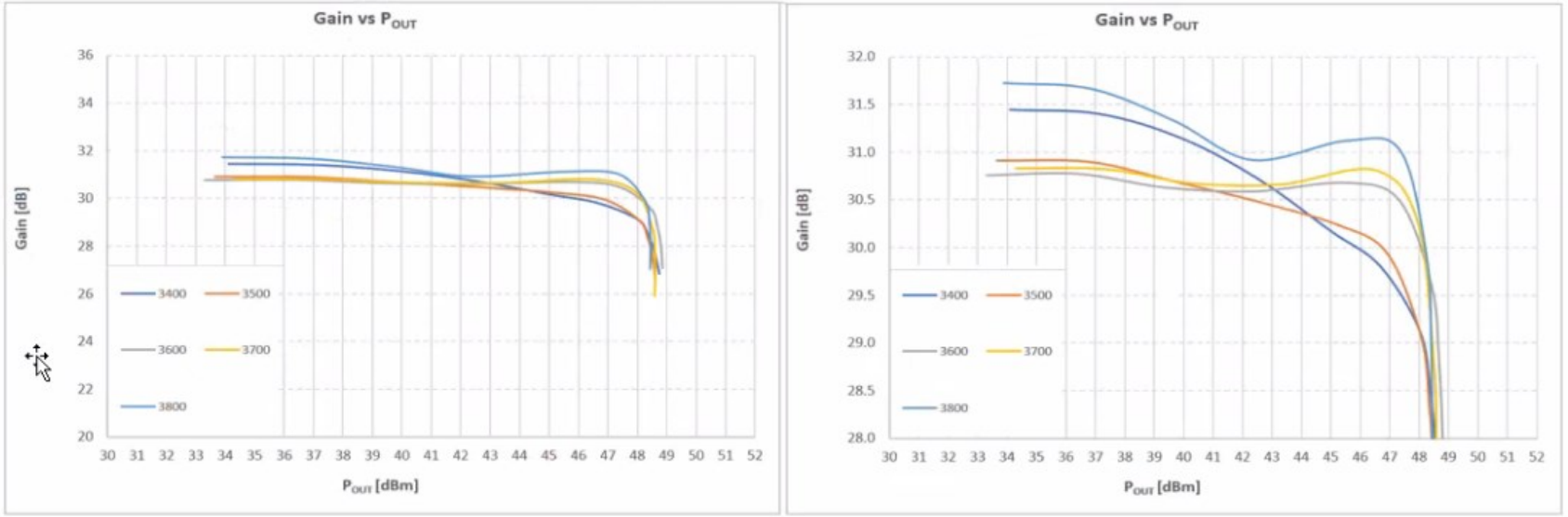
Analysis of competition - NXP Eval Board A5M36TG140-TC - 04 Sep 2023

Measurement results *Date of meas execution: 01 Sep 2023*



Test conditions:

Figure 8
Gain vs Pout power sweep curves

Test signal: **Pulsed Signal 20uS/10%**

Test frequency: 3400, 3500, 3600, 3700, 3800 MHz Air temperature: T= +25° C

V_{DD1} = 5 Vdc, V_{DD2} = 48 Vdc, I_{DQC1} = 145 mA, I_{DQC2} = 25 mA, I_{DQP1} = 35 mA, V_{GP2} = V_{Bias} – 0.31 Vdc*

** Increase VGP2 (peaking side) until IDQP2 = 40 mA current is attained, and then subtract 0.31 V for final VGP2 bias voltage*