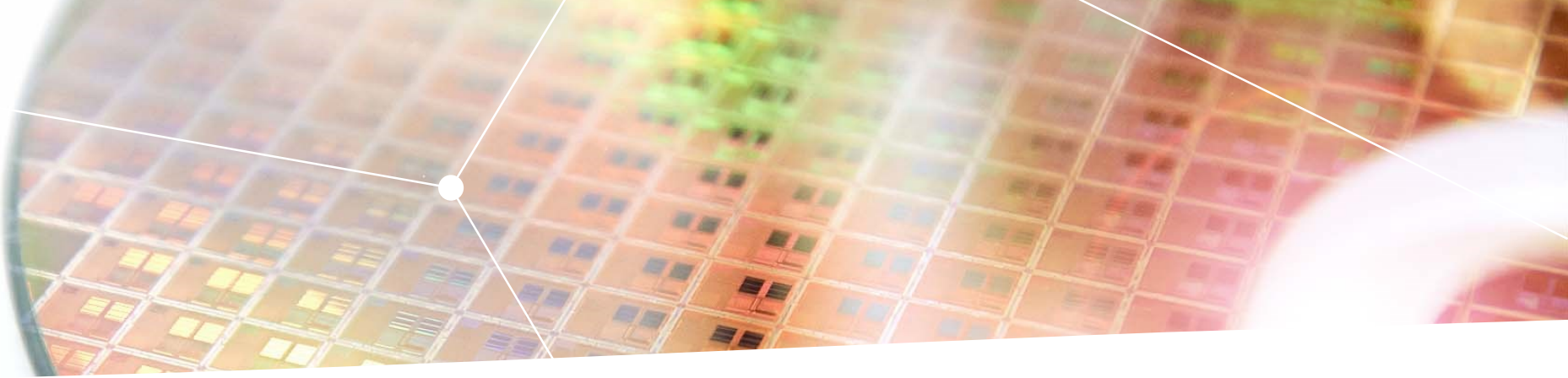
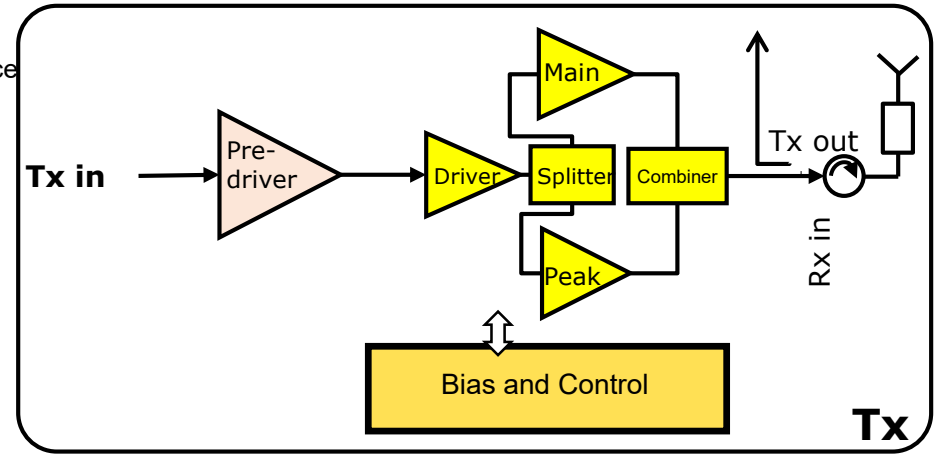


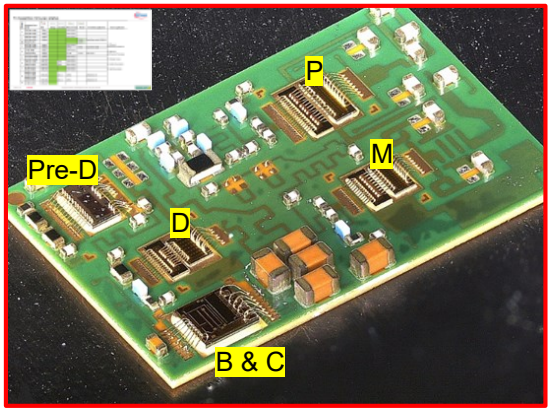
TX Baseline overview & status

09.01.2023

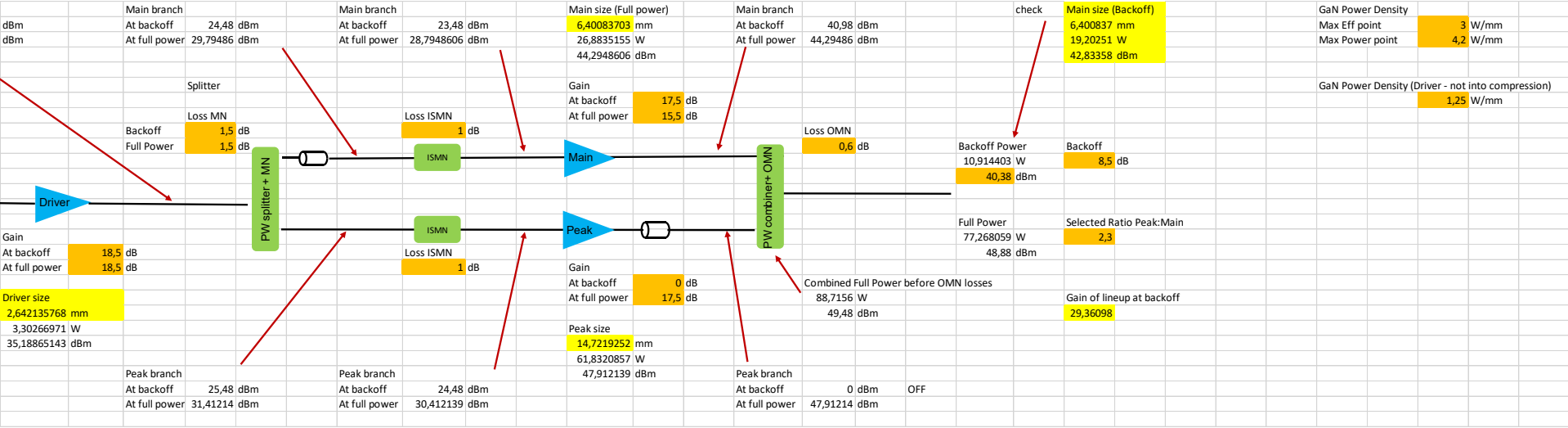
Tx baseline activity background

- **Big picture (goal):** “First pass module design”
  - Theoretical calculation = Simulation results = Measured performance
- **Ingredients:** Accurate passive + active model
- **Challenges:**
  - Complexity
  - Too many variables at a time
    - Architecture choices
    - Driver & final stage topology (power ratio)
    - Performance vs badwidth vs linearity trade-offs
    - Matchable impedance
    - Assembly & process tolerances
  - Model not accurate enough (absolute value vs trend)
  - Non availability of building blocks evaluation with final mold material
- **Consequences:** Every non-detectable change early on would lead to re-spin of the module design

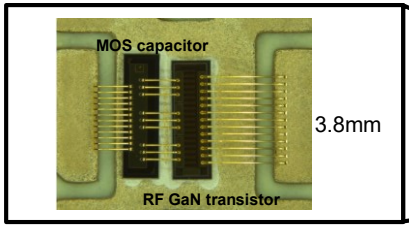




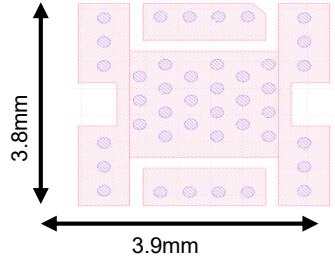
Line-up calculations



Mini-pac build matrix



Mini Pac



		MOS Capacitor	N9500B_V6	N9500B_V6	N9500B_V5	N9500B_V5	-	N9501B_V1	N9501B_V1	N9501B_V4	N9501B_V4	-	...	...
			•	•	•	•	•							
[illegible]	P6							•	•	•	•	•		
4.8 (30x160µm)	P3												⋮	⋮
5.12 (16x320µm)	P14													
10.1 (42x240µm)	P76													
12 (30x400µm)	P53													
11.52 (36x320µm)	P39													
10.24 (32x320µm)	P35													
2.4 (6x400µm)	T9507B_2													
1.92 (8x240µm)	2P4													
3.84 (12x320µm)	P13													
3.84 (16x240µm)	P10													
6.40 (20x320µm)	P15													
4.8 (12x400µm)	P55													

› Goal of Mini Pac matrix
- Down-selection of dies for dual driver
- Enabling of active + passive model
- Database for future designs

- Design
- Assembly
- Measurements
- Model

Mini-pac design

Power calculation: Asymmetric Doherty

Specification				
Project	**Frequency-Range (MHz)**	**P3dB (dBm)**	**P3dB (W)**	**PAR**
PAM 2.0+	3400 - 3800	47,4	54,95	8,4
		Pavg (dBm)	**Pavg (W)**	
		39	7,94	

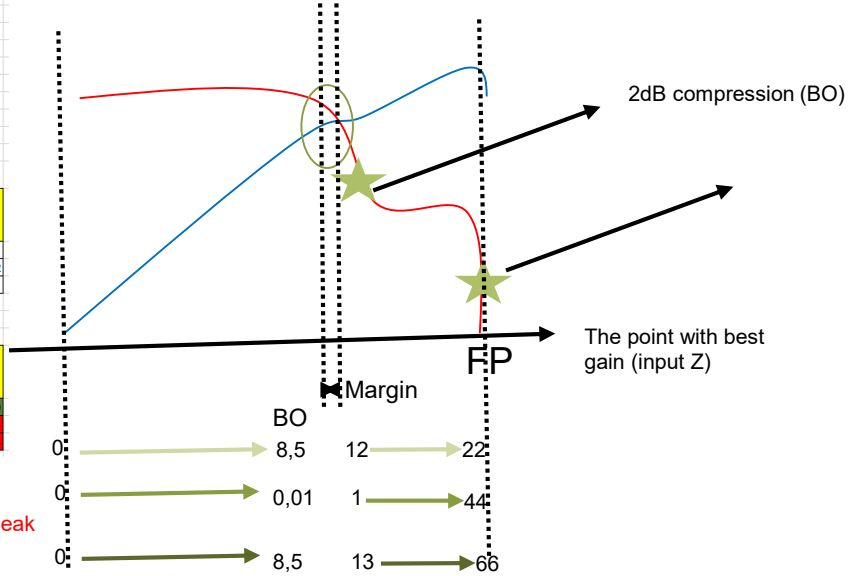
Doherty Topology	**Remark**	**Ratio**	**Main (W)**	**Peak (W)**
2-way asymmetric	To maximize efficiency	2	18,32	36,64

Estimation including loss

	Required power (W)	**Required power (dBm)**	**Loss (dBm)**	**Total required power (dBm)**	**Total required power (W)**	**Ratio**	**Total power (W)**	**Total power (dBm)**
Main	18,32	42,63	0,8	43,43	22,02			
						3,01	**66,07**	**48,2**
Peak	36,64	45,64	0,8	46,44	44,05			

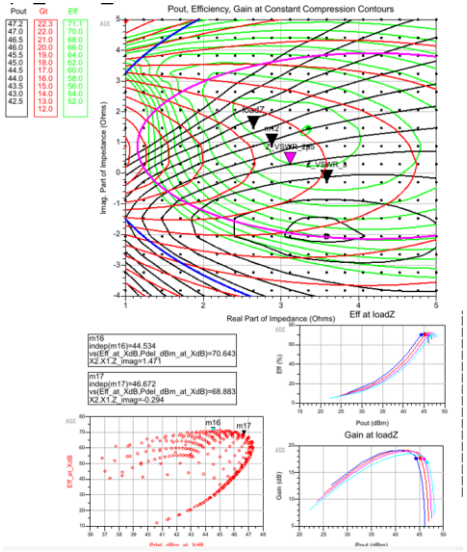
	Total output power (dBm)	**PAR**	**Power @ MXE (dBm)**	**Margin (dB)**	**Power @ MXE (dB**	**Power @ MXE (W)**	**MXP (W)**	**MXP(dBm)**
	48,2	8,4					66,07	48,20
Main			39,8	1,00	40,80	12,02	22,02	43,43
Peak			Peak_start_ideal		Peak_start	0,01	44,05	46,44

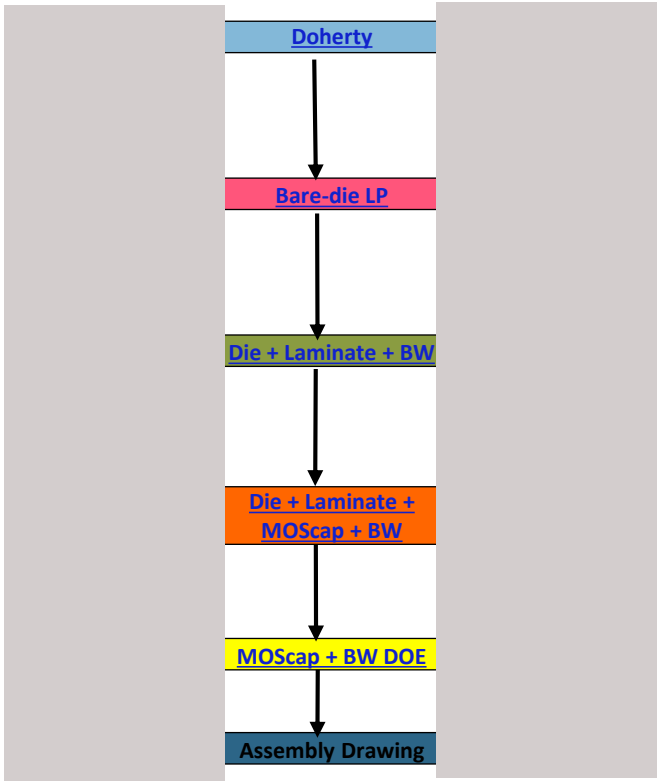
Required power from peak

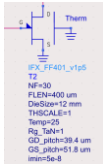


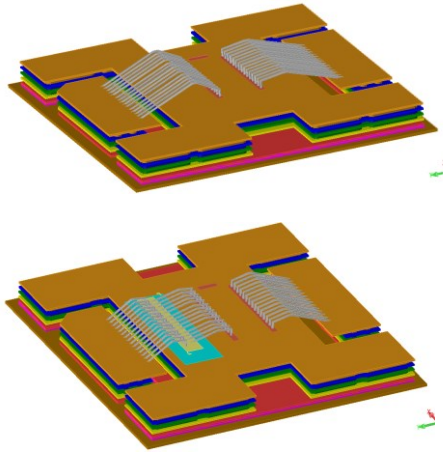
- Maximize Gain
  - Main section gain as high as possible while maintaining Power @ MXE
  - Peak section gain as high as possible while maintaining MXP

Design approach mini-pac



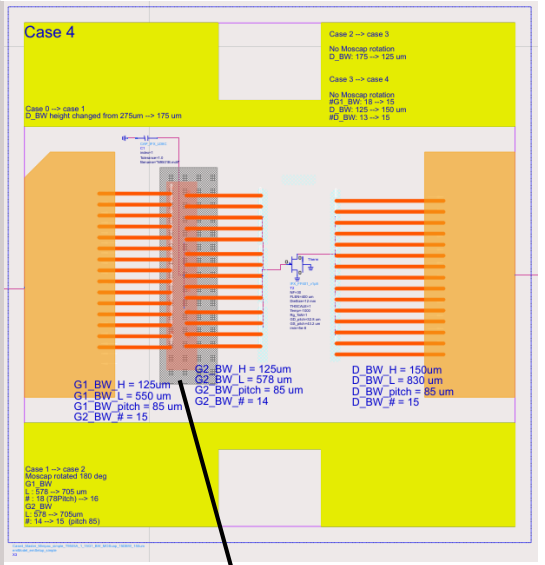






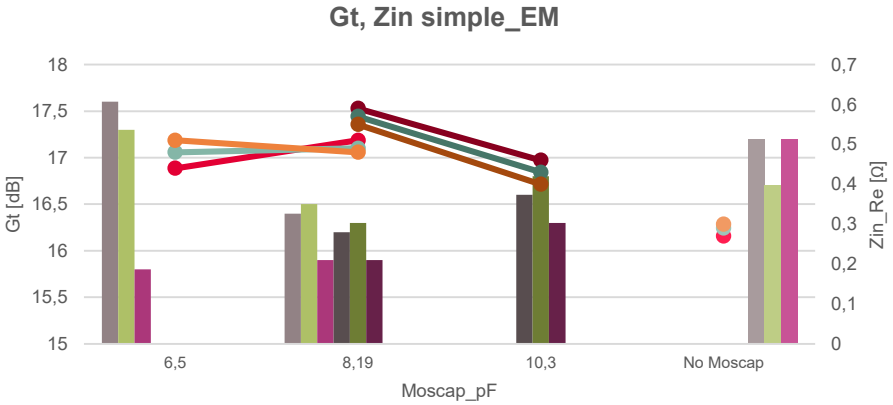
DOE6_simulated performance: MOScap (5) X (5) BW profile (with simple EM model)

P1.5dB	Moscap	
Simuation case_BW_ profile	Name	Value (pF)
Case 0	N9501B_V8	5,5
Case 0	N9501B_V5	6,58
Case 0	N9501B_V8	8,19
Case 0	N9501B_V4	10,3
Case 0	N9501B_V1	12,89
Case 1		
Case 1		
Case 1		
Case 1		
Case 1		
Case 2		
Case 2		
Case 2		
Case 2		
Case 2		
Case 3		
Case 3		
Case 3		
Case 3		
Case 3		
Case 4		
Case 4		
Case 4		
Case 4		
Case 4		



Index	L	W	Ls	Ws	d	Value_pF
1	1446	328	1678	444	1300	12,89
5	1446	261	1678	444	1300	10,3
6	1446	244	1678	444	1950	6,5
10	1446	207	1678	444	1950	5,5
19	1446	207	1770	536	1300	8,19

Selected variants (MOScaps) for assembly

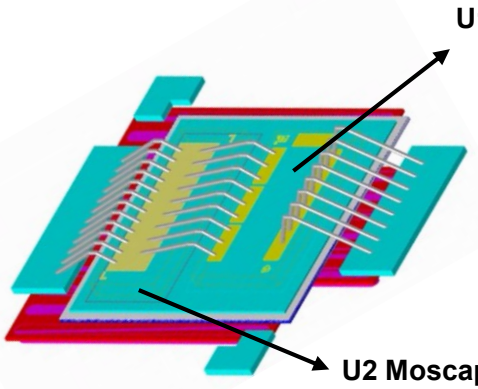


Variant	BW profile	MOScap (pF)	
DOEx_2	Case 1	N9501B_V5	6,5
DOEx_3	Case 1	N9501B_V8	8,19
DOEx_4	Case 4	N9501B_V8	8,19
DOEx_5	Case 4	N9501B_V4	10,3

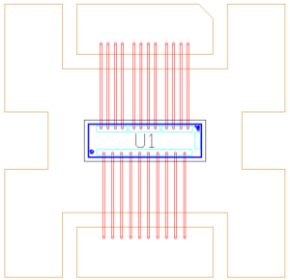
- Design
- Assembly
- Measurements
- Model

Assembly

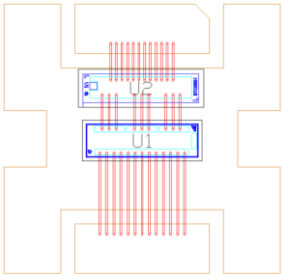
Background - Package overview

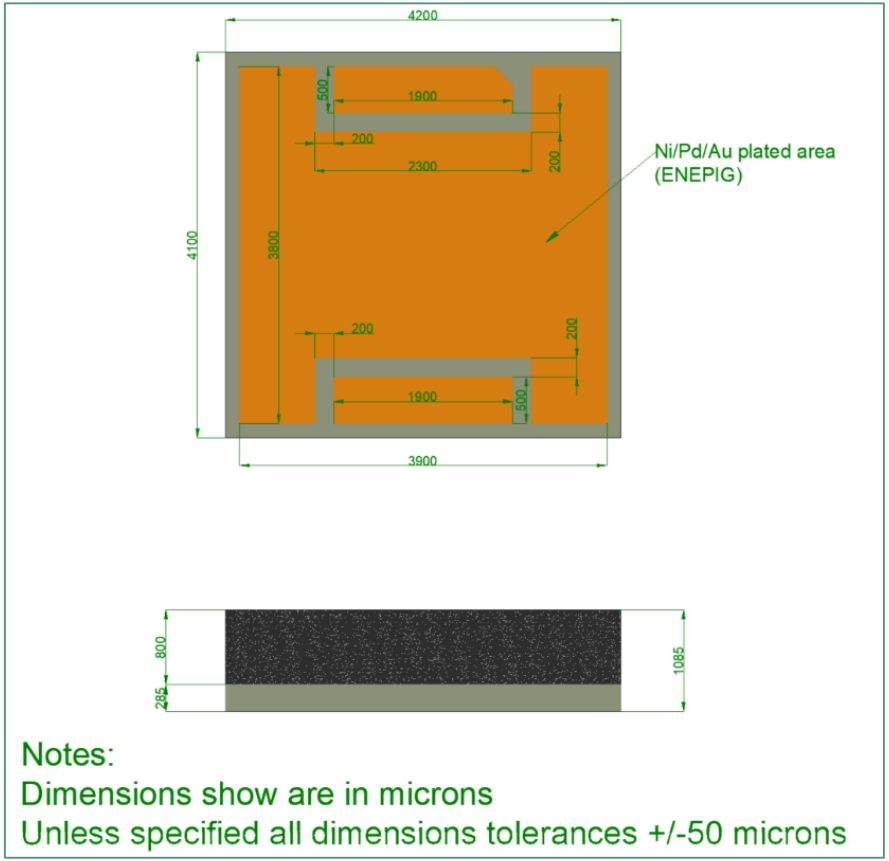


Only 1die version (GaN)



2 dies version (GaN/moscap)

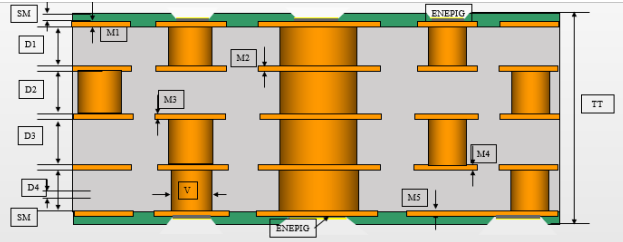




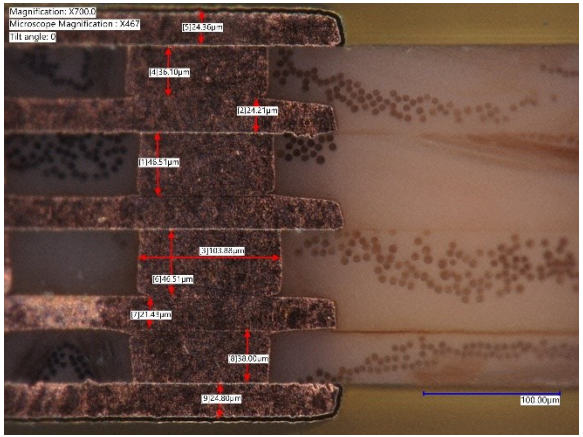
Background - Substrate overview

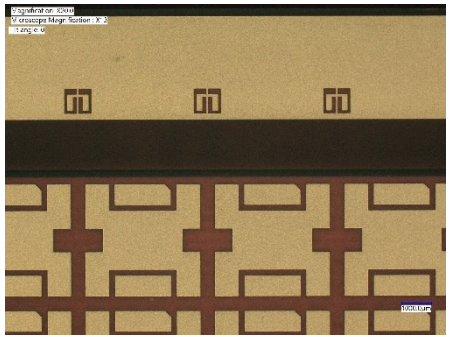
Package	Technology	Supplier	Package size	Heat spread	Stacking
LLG3839	Laminate	Access	4.2x4.1	Bars	5 layers GEA-705G, 0.285mm

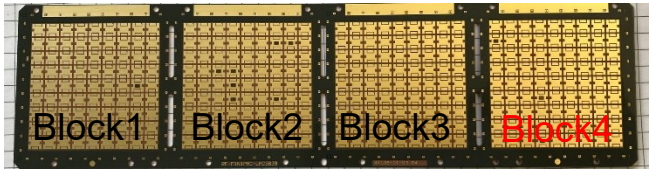
5 layers Access

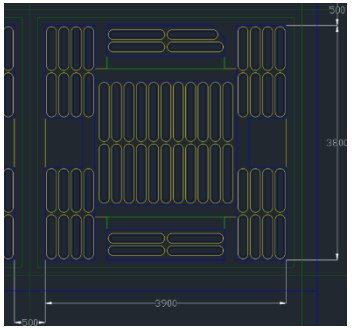


Unit size: um		Strip size : 187.5x50mm	Units/strip:324
Items		ACCESS Structure	
D1, D4	Dielectric thickness	40±15μm	
D2, D3,	Dielectric thickness	50±15μm	
M1 ~ M5	Metal thickness	20±7μm	
SM	Solder mask thickness(above metal)	15+/-7μm	
TT	Total thickness (Exclude Tsm & Bsm)	285± 30μm	
Solder Mask Type: AUS308		Prepreg Material: GEA-705G	
Top metal finish: ENEPIG		ENEPIG Ni: 2~5μm, Pd: 0.11~0.18μm, Au: 0.07~0.12μm	
Bottom metal finish: ENEPIG		ENEPIG Ni: 2~5μm, Pd: 0.11~0.18μm, Au: 0.07~0.12μm	



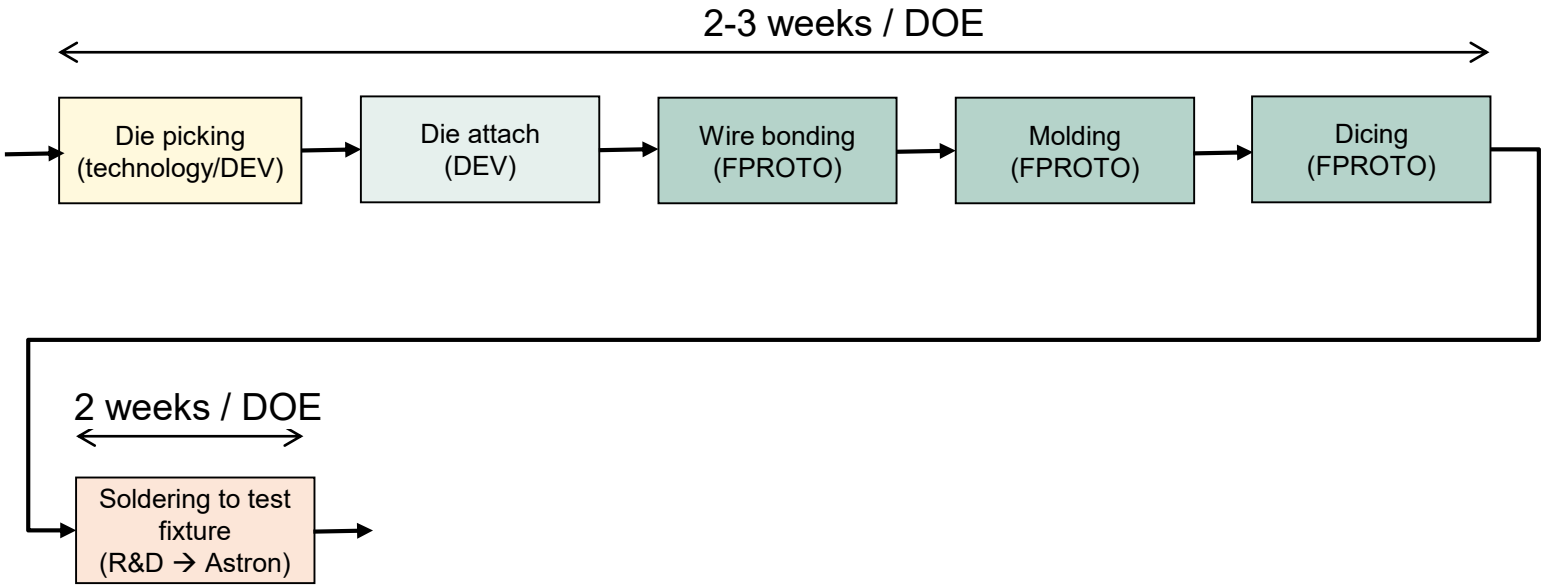




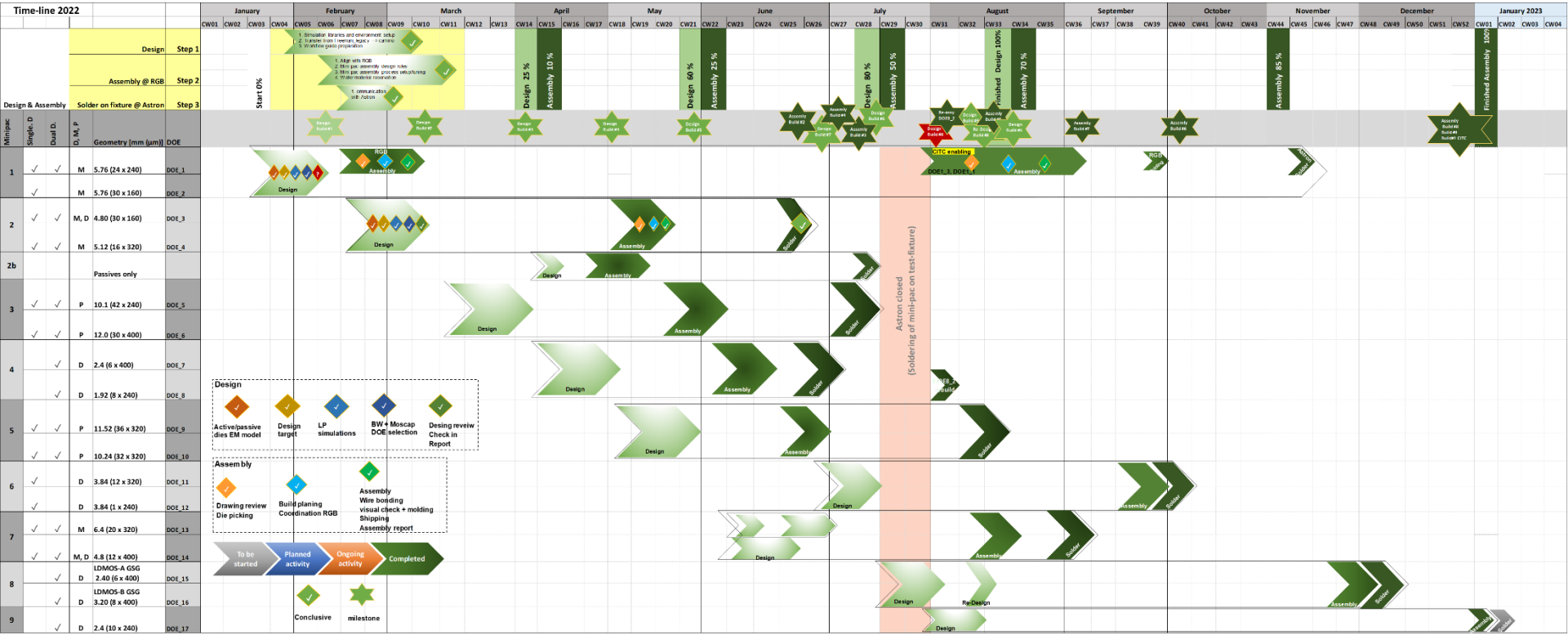


Reserved for setup (dummies)

Mini-pac assembly flow



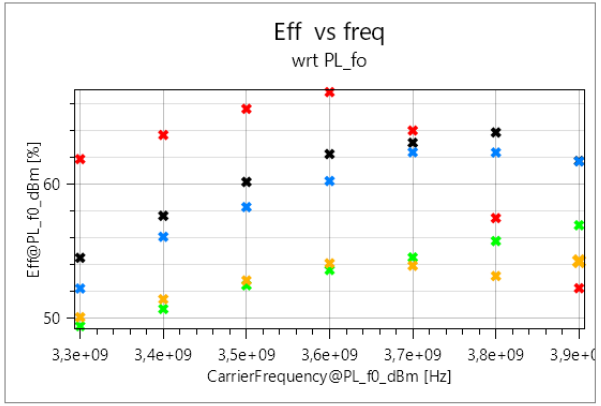
Timeline Design & Assembly

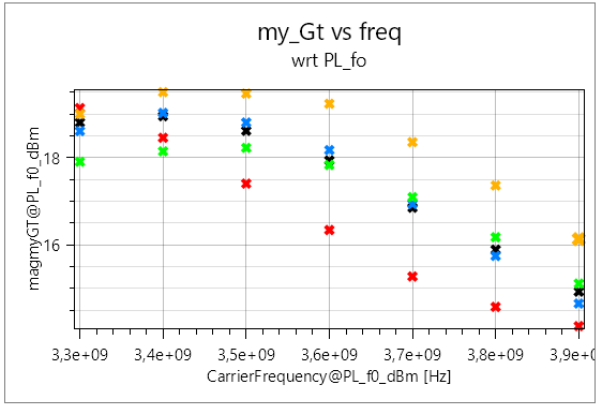


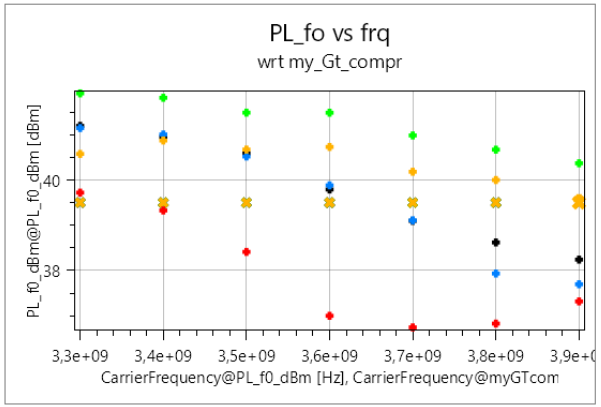
LP measurements

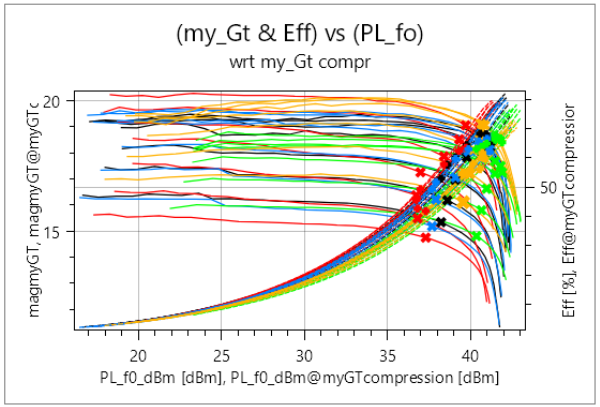
- Design
- Assembly
- Measurements
- Model

MOS cap down-selection (Back-off)

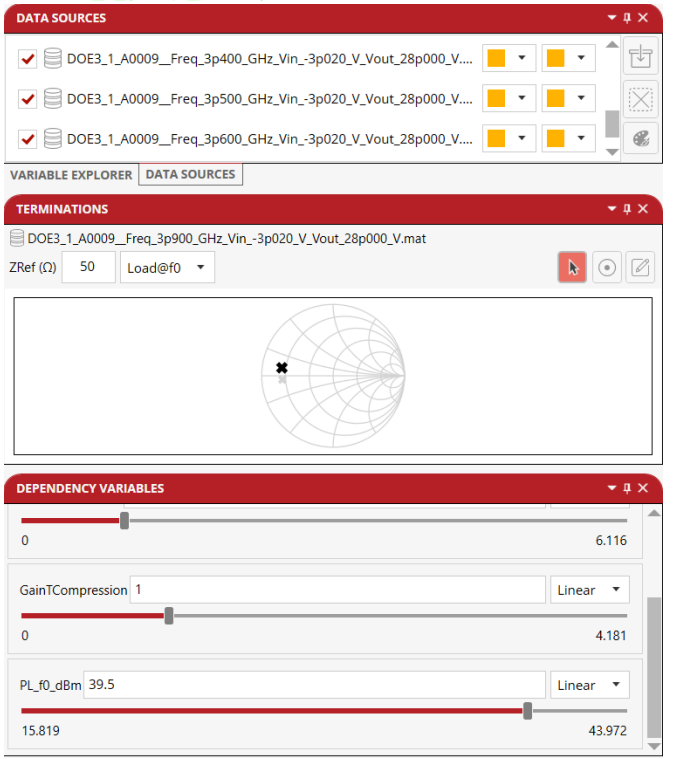




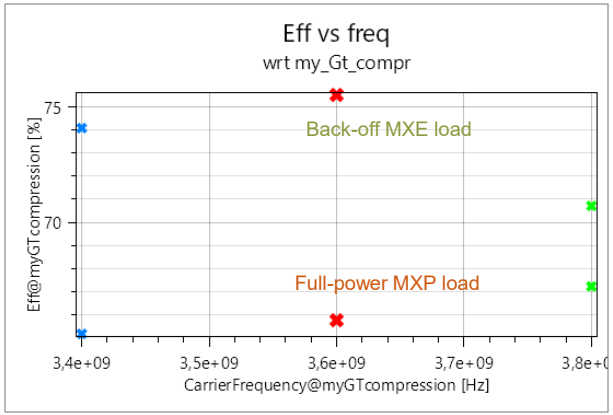


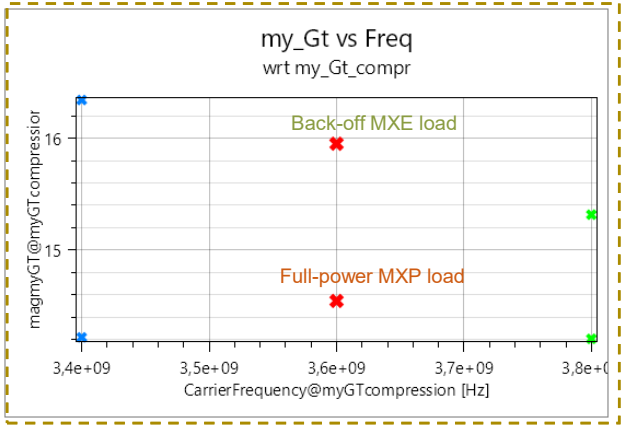


- DOE3_1_(bare_die)
- DOE3_2_(5.57pF_160um)
- DOE3_3_(5.57pF_300um)
- DOE3_4_(6.23pF_160um)
- DOE3_5_(6.23pf_260um)

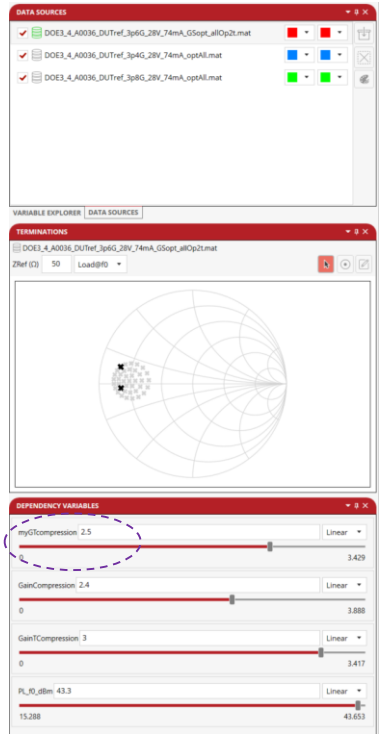


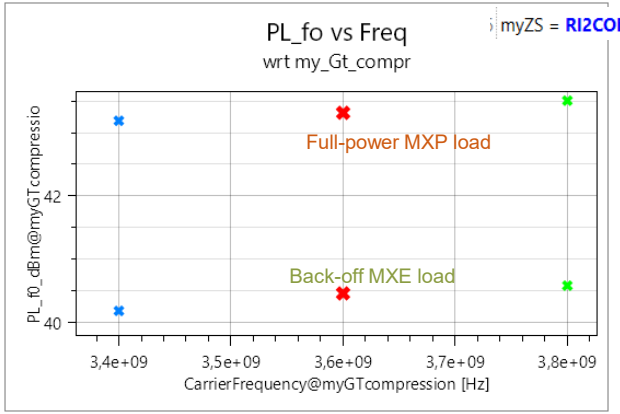
Design recommendation DOE3_4 (re-calculated Zs = 1.8 – j 8.4)



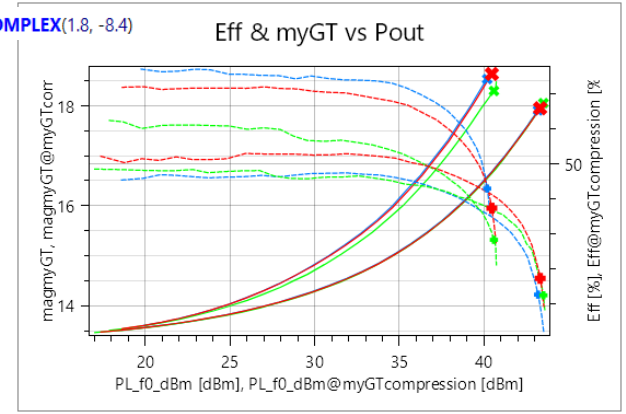


- DOE3_4_A0036_3.4 GHz
- DOE3_4_A0036_3.6 GHz
- DOE3_4_A0036_3.8 GHz



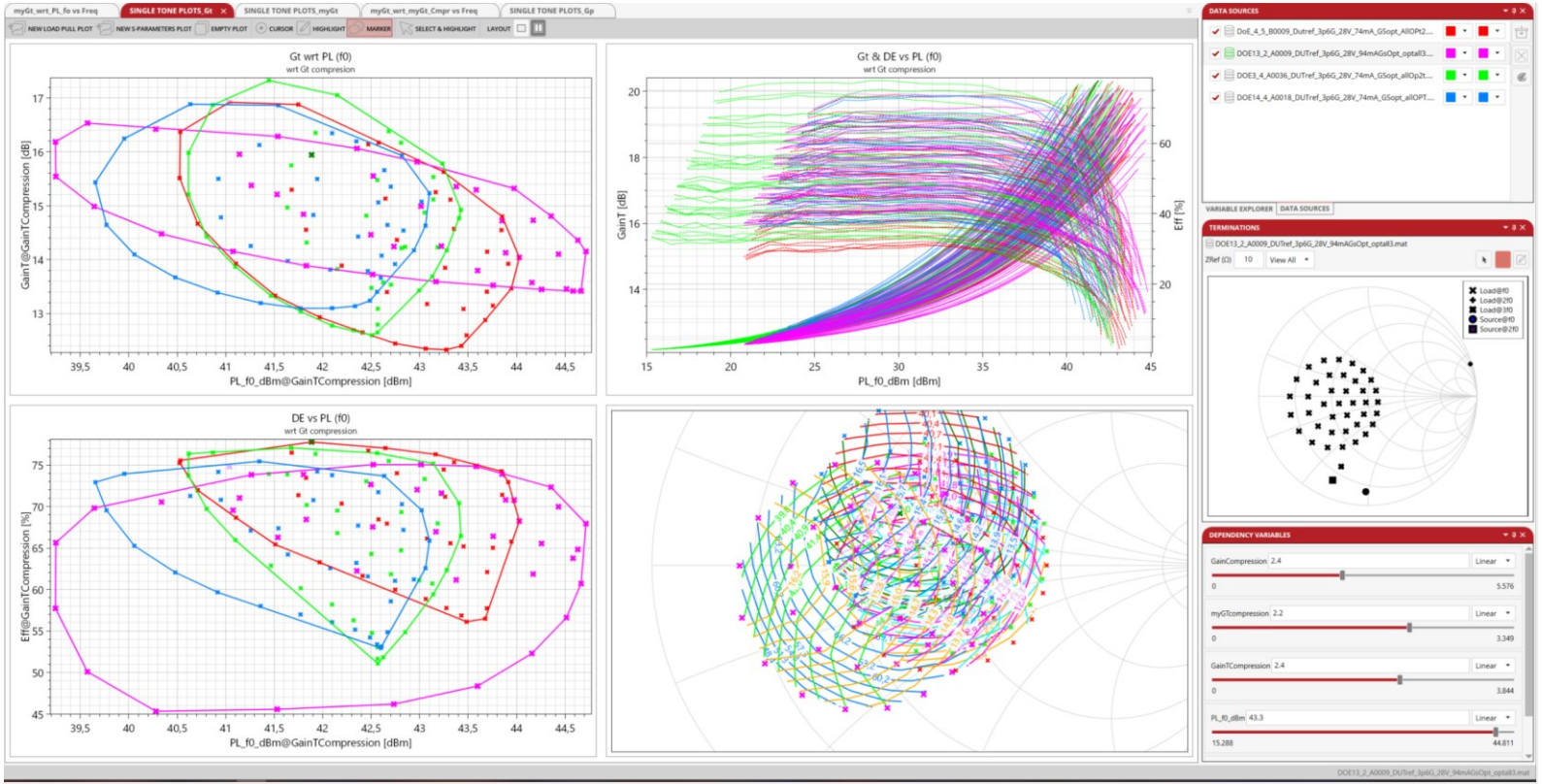


myZS = RI2COMPLEX(1.8, -8.4)

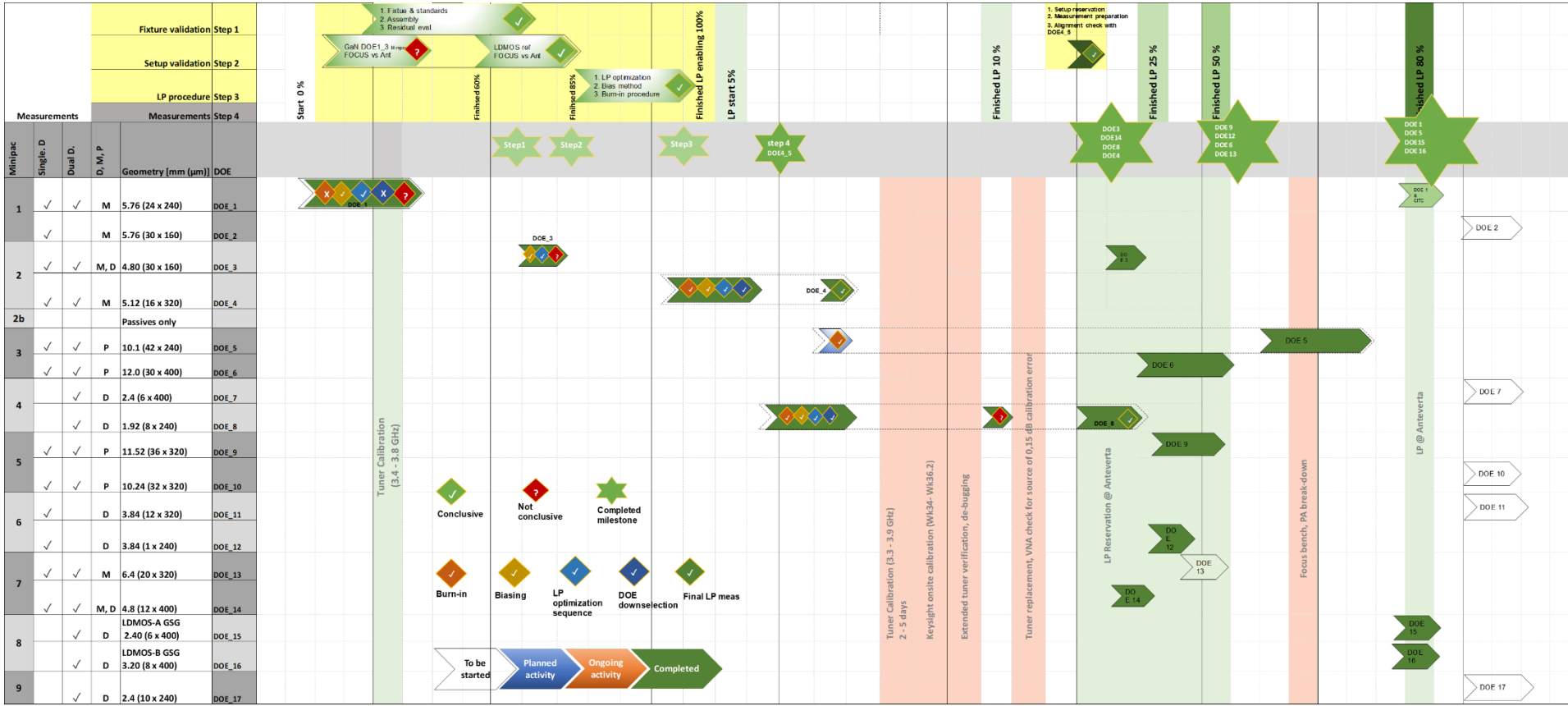


P_2.5dB ≈ 43.3 dBm

Device down-selection for (Main)



Timeline LP measurements



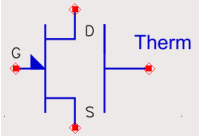
Minipac	Single. D	Dual D.	D, M, P	Geometry [mm (µm)]	DOE
1	✓	✓	M	5.76 (24 x 240)	DOE_1
	✓		M	5.76 (30 x 160)	DOE_2
2	✓	✓	M, D	4.80 (30 x 160)	DOE_3
	✓	✓	M	5.12 (16 x 320)	DOE_4
2b				Passives only	
3	✓	✓	P	10.1 (42 x 240)	DOE_5
	✓	✓	P	12.0 (30 x 400)	DOE_6
4		✓	D	2.4 (6 x 400)	DOE_7
		✓	D	1.92 (8 x 240)	DOE_8
5	✓	✓	P	11.52 (36 x 320)	DOE_9
	✓	✓	P	10.24 (32 x 320)	DOE_10
6	✓		D	3.84 (12 x 320)	DOE_11
	✓		D	3.84 (1 x 240)	DOE_12
7	✓	✓	M	6.4 (20 x 320)	DOE_13
	✓	✓	M, D	4.8 (12 x 400)	DOE_14
8		✓	D	LDMOS-A GSG 2.40 (6 x 400)	DOE_15
		✓	D	LDMOS-B GSG 3.20 (8 x 400)	DOE_16
9		✓	D	2.4 (10 x 240)	DOE_17

Model

- Design
- Assembly
- Measurements
- Model

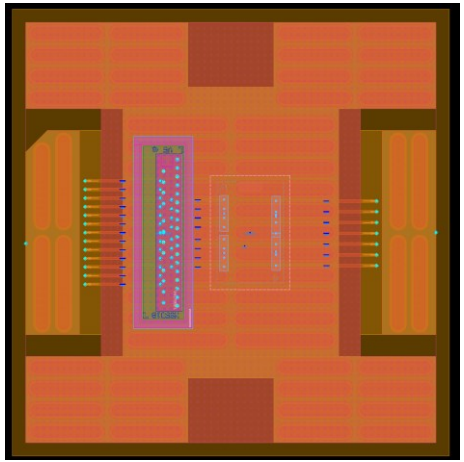
Model ingridents

Compact model

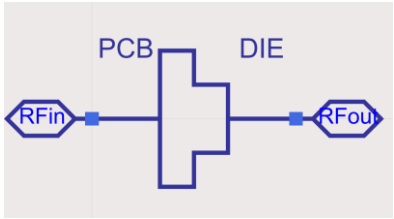


IFX_FF401_v1p5
T3
NF=16
FLEN=320 um
DieSize=5.12 mm
THSCALE=1
Temp=25
Rg_TaN=1
GD_pitch=46.2 um
GS_pitch=45.9 um
imin=5e-8

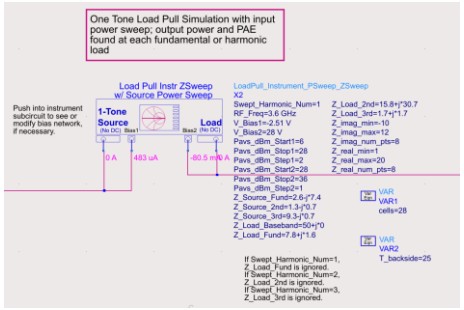
EM_model minipac



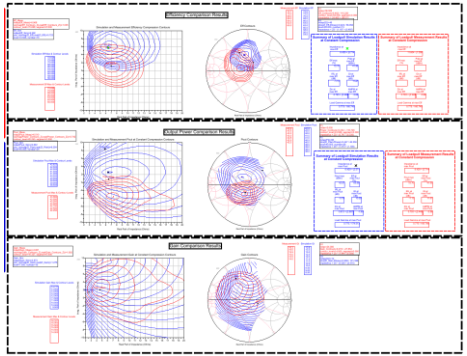
EM_model PCB_step



LP template

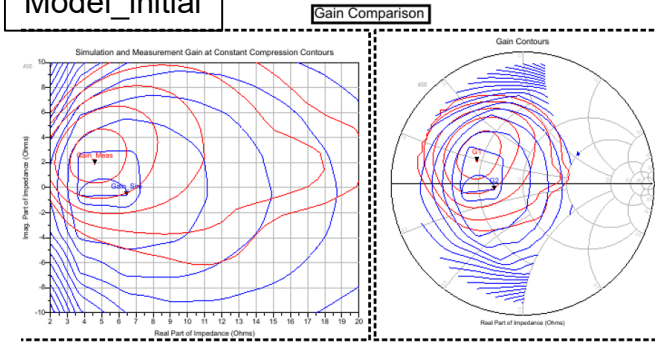


Measurement vs simulation DDS template



Mini-pac model vs meas

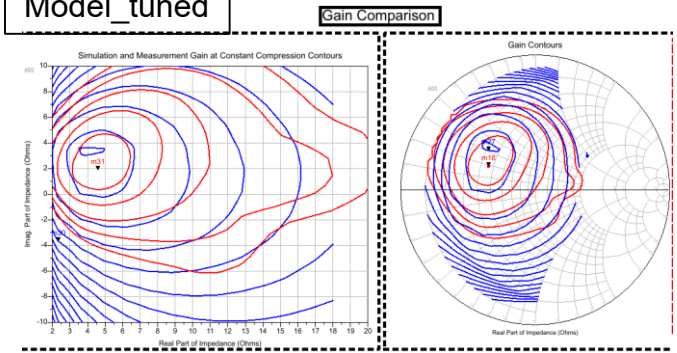
Model_initial

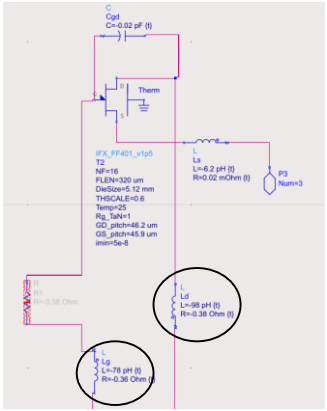


› Model › Meas

@ 3.6 GHz / P2dB	MXE	MXP	MXG
Measurement	70.7	43.57	16.3
Model	76	43.2	15.1
Model _ Tuned	73.9	43.5	15.2

Model_tuned

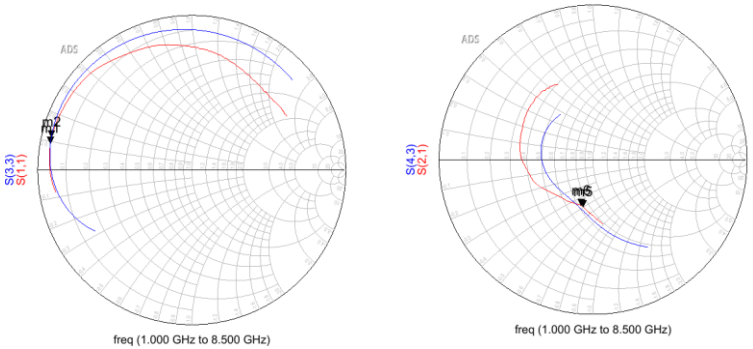


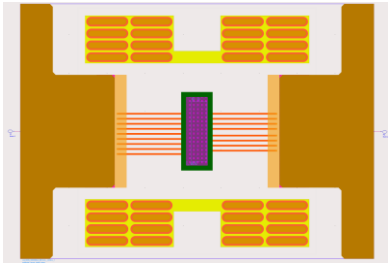


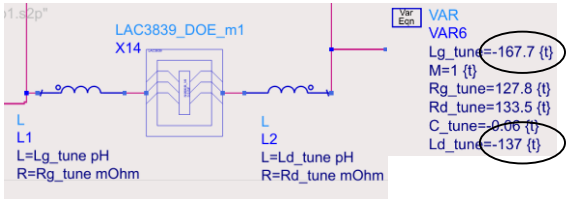
- First pass without tuning model is ok
- Better fit after tuning but,
  - Deltas in performance for Gt, η
  - Delta is bigger at 3.8GHz
- Lg and Ld significant contributors but –ve
- Next step is to look passive only

Passive only model vs meas

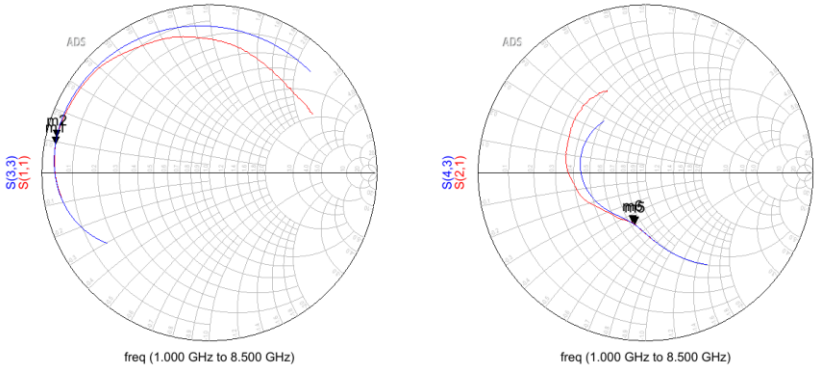
Model_initial





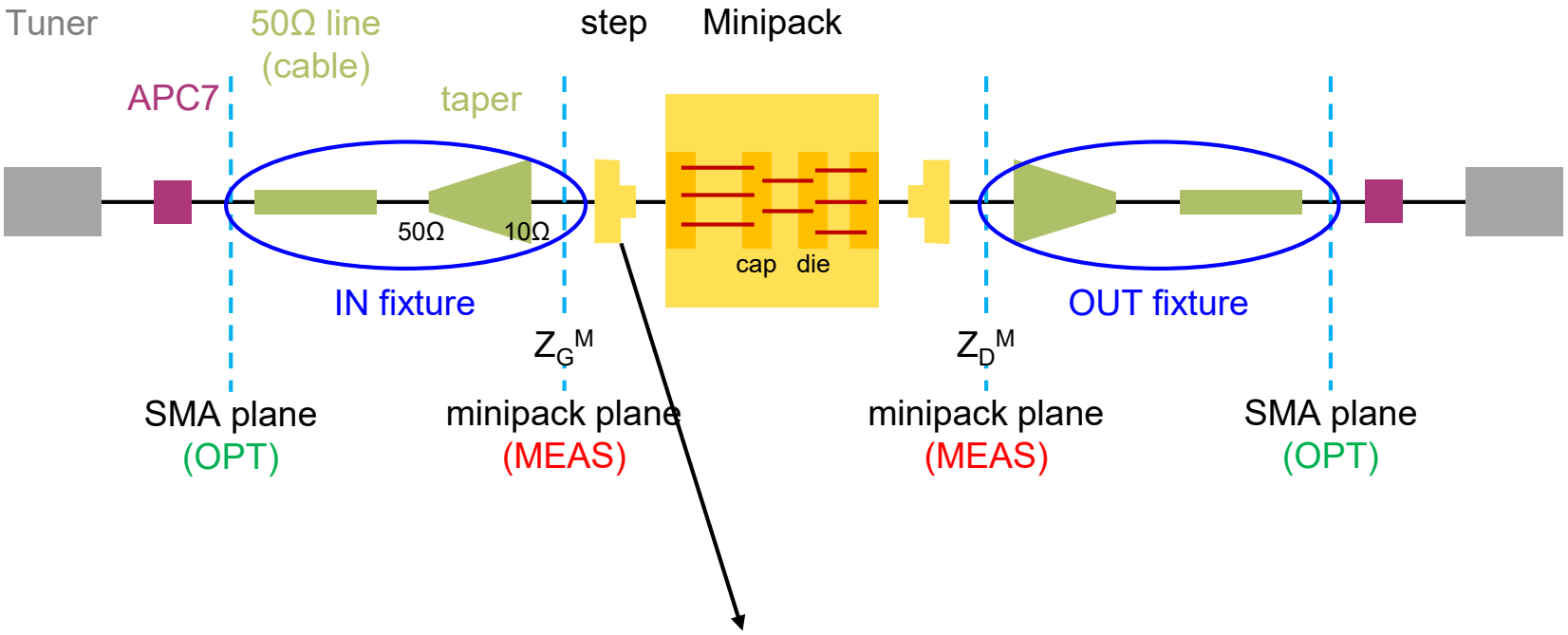


Model_tuned › Model › Meas



- Good fit until 4 GHz
- Improved fitting with BW tuning
  - Lg, Ld need to be tuned (-ve)
  - Similar to mini-pac tuning
  - BW modeling is not accurate ?
- Next steps
  - Optimize simulation settings in ADS
  - Simulation with HFSS
  - Cross-section of BW's and measure loop height/shapes
  - Parameterize and tune mini-pac layers / properties

Measurement strategy



› Modeling effort needed

To be continued.....

› Thank you!

Part of your life. Part of tomorrow.