A New Approach to Microwave Power Amplifier Design Based on the Experimental Characterization of the Intrinsic Electron-Device Load Line

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***Abstract*—This paper presents a new original approach to power amplifier design, which is mainly based on low-frequency nonlinear empirical electron device (ED) characterization. The proposed technique enables the same level of accuracy provided by expensive load–pull measurement systems to be obtained through a relatively simple and low-cost setup. Moreover, ED currents and voltages related to reliability issues can be directly monitored.**

Different experimental examples based on power GaAs and GaN field-effect transistors are provided to demonstrate the validity of the proposed approach.

***Index Terms*—Design automation, field-effect transistors (FETs), integrated-circuit design, integrated-circuit measurements, microwave amplifiers, semiconductor device measurements.**

I. Introduction

POWER amplifier design represents a key aspect in order to meet the severe performance (e.g., efficiency, reliability) required for modern microwave and millimeter-wave systems. Such a type of circuit is usually designed by exploiting a mix of three different approaches [1], [2]: Cripps load-line theory, load–pull (LP) measurements, and iterative harmonic-balance analyses based on nonlinear models of electron devices (EDs).

The Cripps load-line theory [3] exploits, in its original version, an elementary ED description (i.e., zero knee voltage, zero output conductance, and constant transconductance, except for the pinchoff and hard saturation at the maximum allowable current) based on static current/voltage (*I/V*) output characteristics. Such an approach is limited by the simplified device description. For instance, due to the hard saturation mechanism, it cannot be adopted when dealing with high gain-compression regimes. Moreover, since low-frequency (LF) dispersion (i.e., traps and thermal effects [4]–[8]) is totally neglected, the Cripps load-line method is not particularly adequate for exploring emerging technologies (e.g., GaN, SiC) where dispersive effects usually play a major role. Finally, as clearly stated in [3], such a technique has to be considered only as a starting point for power amplifier design.

LP measurements [9]–[12], based on both passive or active load synthesis, represent the most common aid for power amplifier design. Indeed, EDs can be characterized under actual operating conditions, by imposing different input and output impedances at the device ports. However, LP setups are frequency and power limited, and their cost dramatically increases when high operating power and/or frequencies are required.

A major limitation of this technique is related to the difficulty in synthesizing the full range of device terminations: especially when on-wafer devices having a large periphery are considered, passive LP suffers from the inability to synthesize very low impedances, whereas active LP may become critical from the stability point of view [2]. Moreover, once LP contours have been drawn, no information is given about the intrinsic ED load line: loading conditions, which show similar microwave performance, can correspond to very different load lines at the intrinsic device. This is a vital aspect since reliability conditions are defined at the intrinsic ED ports [13] as the passive access structures to the active area do not have any major impact on reliability (e.g., the device breakdown condition is related to the breakdown of the intrinsic gate–drain diode).

High-frequency time-domain measurement systems [large-signal network analyzers (LSNAs)] [14]–[16], which provide a vectorial information, do not overcome the above problem since the measured load line still refers to the extrinsic device. Moreover, the frequency restriction of LSNAs limits their application.

Preliminary design choices carried out by means of load-line theory and/or LP measurements represent the starting point for successive power amplifier design refinements based on harmonic-balance analyses. These obviously rely on the accuracy of the ED models adopted.

An accurate model could overcome the need for LP measurements: in principle, LP contours could be traced by using simulation results only. In practice, however, ED models usually available from the foundries provide accurate nonlinear performance prediction only in a relatively narrow neighborhood of given bias and load conditions [16]. Thus, the availability of a LP (or a similar one) measurement system is always a valuable aid.

In this paper, an alternative original approach to power amplifier design is proposed, which overcomes the major problems previously mentioned. It is mainly based on LF nonlinear experimental ED characterization and enables the same level of accuracy provided by LP measurements to be obtained through a

Manuscript received December 09, 2008; revised March 30, 2009. First published June 12, 2009; current version published July 09, 2009. This work was supported in part by the Italian Ministry of Instruction, University and Research (MIUR).

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Digital Object Identifier 10.1109/TMTT.2009.2022816

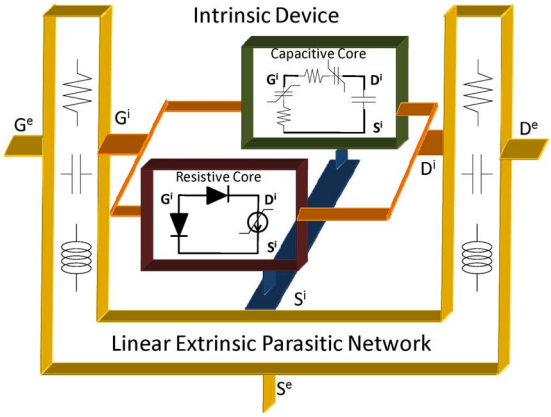

Fig. 1. Nonlinear equivalent circuit for an FET ED.

relatively simple and low-cost setup. Moreover, device currents and voltages compatible with reliability requirements can be directly monitored.

The aim of this work is to demonstrate the validity of the proposed approach in providing valuable information for power amplifier design, whereas specific design techniques are not dealt with.

This paper is organized as follows. In Section II, some nonlinear device modeling issues and commonly adopted assumptions, which pose the basis for the proposed approach, are discussed. Section III describes the proposed method by highlighting the differences with respect to other commonly adopted approaches. Finally, in Section IV, different experimental examples will be shown.

II. Nonlinear Device Modeling Issues

In the following discussion, the generic nonlinear equivalent-circuit model depicted in Fig. 1 will be considered without loss of generality. In particular, we will focus on a field-effect transistor (FET) ED since it plays a major role in microwave and millimeter-wave power amplifier design, nevertheless the following considerations could also be extended to bipolar transistors.

The linear extrinsic parasitic network in Fig. 1 describes the access passive structure to the device active area and accounts for metallization and dielectric losses, as well as for associated inductive and capacitive effects. Its correct modeling is a fundamental issue to obtain accurate model predictions. Parasitic elements can be characterized by exploiting conventional lumped descriptions [17], [18], which can be identified by only using small-signal measurements, or, alternatively, by adopting electromagnetic simulations of the device layout [19], [20].

As clearly shown in Fig. 1, the *intrinsic device* can be divided into two parts, which can be considered strictly in parallel: a *capacitive core* describing the nonlinear dynamic phenomena, and a *resistive core* accounting for the dc and LF *I/V* device characteristics. The latter ones differ from the dc response due to surface state densities, deep-level traps, and thermal phenomena. More rigorously, a dynamic term should also be considered for the LF device behavior, but the most commonly adopted equivalent-circuit models do not accurately model such dynamics and accounts only for device response at dc and above the traps cutoff frequency. In any case, the LF dynamic term can be ignored for the purpose of this study.

The ED resistive core modeling is extremely complex, not only because a number of important nonlinear phenomena must be considered (e.g., breakdown, forward conduction of the gate–source diode, knee of the *I/V* curves, etc.), but also due to the nonnegligible presence of dispersive effects [4]–[8], which, *de facto*, impose the exploitation of nonlinear dynamic measurements in order to obtain good prediction capabilities.

To probe further this issue, we must consider that the drain and gate currents at the intrinsic ED ports, above the cutoff of LF dispersive effects (i.e., some hundreds of kilohertz), but at frequencies low enough to neglect the reactive effects related to the capacitive core, can be expressed as follows:

$$\begin{aligned} i_g(t) &= h\left(\underline{v}(t), P_0, \theta_{\text{case}}\right) \\ i_d(t) &= f\left(\underline{v}(t), \underline{V}_0, P_0, \theta_{\text{case}}\right). \end{aligned} \tag{1}$$

In (1), h and f are two algebraic (i.e., memoryless) functions, $\underline{v}$ is the vector of the intrinsic voltages, $\underline{V}_0$ its average value, P_0 is the average dissipated power, and, lastly, θ_{case} is the device case temperature.

The dependence on $\underline{V}_0$ accounts for the influence of traps and surface state densities [4]–[7], while P_0 and θ_{case} determine, through the thermal resistance, the device *I/V* characteristic dependence on the junction temperature.

Identification of (1), in particular, the drain current equation, is quite a prohibitive task mostly due to the complex dependence on its large number of controlling variables. Moreover, traps and thermal effects cannot be separately dealt with, both because the time constants of those phenomena are not always different and also since the device thermal state influences the trapping state [5]–[21]. Thus, identification of (1) necessarily requires the introduction of suitable approximations to make the problem affordable.

A number of LF modeling approaches have been proposed in the literature [4]–[8], both based on lookup tables or analytical expressions. Some of them introduce assumptions, which enable the models to be identified on the basis of bias-dependent dc and ac small-signal differential measurements carried out above the cutoff of LF dispersion. However, in practice, model accuracy is commonly improved by exploiting in the identification phase, besides ac and dc measurements, large-signal dynamic measurements as, for instance, pulsed *I/V* characteristics [22][23].

Despite the use of quite expensive, special-purpose pulsed *I/V* setups, the identification of an accurate *global* model for the resistive core still remains a very complex and hard task, and this justifies why foundry models often properly work in a limited number of given quiescent bias conditions: typically, a limited set of pulsed *I/V* measurements is fitted. Such a type of approach inevitably leads to *local* models, which cannot provide accurate information outside the range of the few quiescent bias conditions considered.

As far as the capacitive core is concerned, dispersive phenomena due to traps and thermal behavior represent second-order effects (whose evidence has rarely been dealt with in the literature [24], [25]) regularly neglected in ED

models oriented to power amplifier design [25]–[31]. A π model of capacitors[1] (usually assuming $C_{\rm gs}$ and $C_{\rm gd}$ nonlinearly dependent on the intrinsic device voltages, and $C_{\rm ds}$ constant) is often adopted and better prediction capabilities can be obtained at higher frequencies by introducing gate–source and gate–drain *RC* series, as shown in Fig. 1, to describe nonquasi-static effects, which accounts for a finite device memory time [25]–[27]. Other nonquasi-static phenomena can be described in terms of trans-capacitances or delay times. Nevertheless, the procedures described in the following can be applied, whichever is the approach adopted for the capacitive-core description.

Provided a careful deembedding of the parasitic network is carried out, small-signal bias/frequency-dependent S-parameter measurements are usually sufficient to accurately determine the voltage-dependent capacitive-core parameters. These can be "fitted" through suitable analytical expressions or directly stored into lookup tables [28]–[31] to build a nonlinear dynamic model. Even problems related to charge conservation, although dealt with in the literature, do not seem to represent a major problem once suitable expedients are adopted [32]–[34].

To summarize, mostly due to LF dispersion phenomena and important nonlinear effects, the modeling of the resistive core is by far the most complex issues in nonlinear ED modeling, while the capacitive core can be more easily identified. This assumption represents the basis of the new design approach introduced in the following and preliminarily justifies why it provides excellent results despite its inherent simplicity.

III. Proposed Approach

As a possible alternative and additional aid to power amplifier design based on nonlinear ED models and LP measurements, a new approach is presented here. The aim is to overcome the accuracy limitations due to the complex modeling of the ED resistive core by using a direct experimental characterization of the LF *I/V* load line. To this end, the measurement system shown in Fig. 2 has been adopted, which is based on sinusoidal excitations: a 2-MHz fundamental frequency is conveniently adopted in order to operate well above the cutoff of LF dispersive effects, but low enough to neglect dynamic effects related to the linear extrinsic parasitic network and the capacitive core. Such a setup is similar to the single-source ones adopted in [35] and [36] for LF dispersion characterization, but in the present study, a two-channel function generator is exploited in order to achieve active load synthesis capabilities in the framework of power amplifier design. More precisely, for a given bias, different load conditions can be synthesized by controlling the gate and drain incident signal amplitudes (A_g and A_d) and their relative phase ($\Delta\varphi$). It is worth observing that such a setup can be implemented by means of only general-purpose instrumentation (typically available in any microwave laboratory), whereas the most expensive instrument, considering the LF excitation, is a 100-MHz four-channel oscilloscope.

[1]The capacitive core can be equivalently and correctly described by adopting nonlinear charge sources (e.g., [28]) instead of nonlinear capacitors. The two descriptions are obviously inherently related, and are definitely equivalent for the application of the proposed approach.

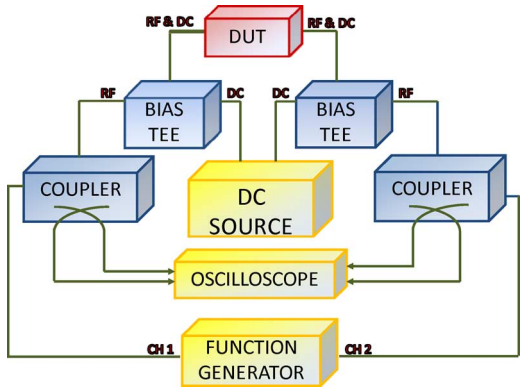

Fig. 2. Block diagram of the measurement system adopted for the LF device characterization.

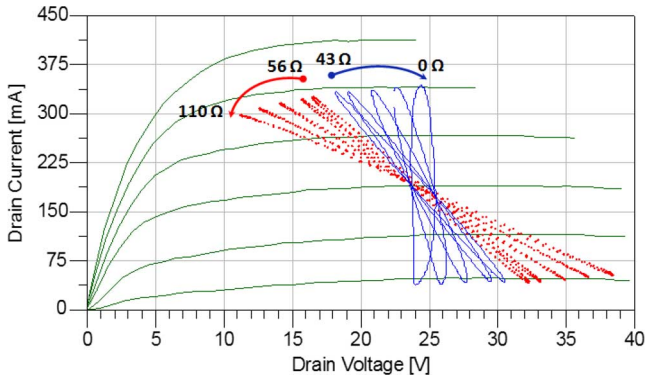

Fig. 3. Measurements performed, by exploiting the LF measurement system, on an 800-μm GaN HEMT device biased at ($V_{g0} = -2$ V, $V_{d0} = 25$ V). Amplitude of the gate incident signal ($A_g = 1$ V), amplitude of the drain incident signal ($1\,\text{V} \le A_d \le 8$ V), relative phase ($\Delta\varphi = 0°$ continuous lines, $\Delta\varphi = 180°$, dotted lines), signal frequency ($f_{\rm LF} = 2$ MHz). Load lines are superimposed to pulsed characteristics ($-3\,\text{V} \le V_g \le -0.5$ V) carried out from the considered quiescent bias condition.

At the frequencies of few megahertz, the FET representation in Fig. 1 is strongly simplified since the parasitic network can be represented by means of parasitic resistances (accounting for metallization and channel access losses), while the reactive elements can be completely neglected. Therefore, the LF load line synthesized at the external terminals is practically coincident[2] with the load line imposed at the resistive core of the intrinsic ED. Since the associated electrical regime uniquely identifies [2], [3] the ED delivered power and efficiency, the setup in Fig. 2 provides an easy way to carry out the choice of the load line, which defines given power amplifier performance, as will be shown in more detail in the following. Moreover, reliability issues related to high-field operations [37]–[39], which must be considered at the intrinsic device drain–gate terminals [13], can be directly controlled.

An example of the measurement system capabilities is shown in Fig. 3 where measurements performed on an 800-μm GaN HEMT device biased under class-A operation are shown. The different load lines were obtained by imposing a constant amplitude of the gate incident signal and sweeping the amplitude of the drain incident signal; moreover, two different values of the

[2]Voltage drops on parasitic resistances, although very low, will be anyway accounted for in the procedure described in the following.

signals relative phase were considered. It is well evident that the system is fully able to synthesize desired load lines at the intrinsic device.

It is worth noticing that similar approaches have been successfully adopted by different research groups [40]–[42] to characterize the nonlinear device behavior at microwave frequencies. However, under such conditions, the nonnegligible capacitive core contribution makes it difficult to accurately characterize the *I/V* load line at the device resistive core.

In order to explain how the LF load line measured at the extrinsic ED ports can be used for power amplifier design, it is convenient to express intrinsic and extrinsic voltages and currents in terms of their practically finite number M of spectral components

$$x(t) = \sum_{k=-M}^{M} X(k\omega) e^{jk\omega t}. \tag{2}$$

By considering for the parasitic network in Fig. 1 any possible topology (based on lumped or distributed elements), intrinsic and extrinsic electrical variables are conveniently related by the following equations in the frequency domain:

$$\begin{bmatrix} V_{\rm gs}^i(k\omega) \\ V_{\rm ds}^i(k\omega) \\ I_g^i(k\omega) \\ I_d^i(k\omega) \end{bmatrix} = \underline{H}(k\omega) \begin{bmatrix} V_{\rm gs}^e(k\omega) \\ V_{\rm ds}^e(k\omega) \\ I_g^e(k\omega) \\ I_d^e(k\omega) \end{bmatrix}, \qquad k = -M, \ldots, M \tag{3}$$

where $\underline{H}(\omega)$ is a suitable hybrid-matrix description of the linear extrinsic parasitic network.

At microwave frequencies, the harmonic components of the "global" intrinsic currents are composed of the sum of the conduction[3] and displacement currents denoted with the superscripts R and C, respectively,

$$\begin{bmatrix} I_g^i(k\omega_{\rm RF}) \\ I_d^i(k\omega_{\rm RF}) \end{bmatrix} = \begin{bmatrix} I_g^{i,R}(k\omega_{\rm RF}) + I_g^{i,C}(k\omega_{\rm RF}) \\ I_d^{i,R}(k\omega_{\rm RF}) + I_d^{i,C}(k\omega_{\rm RF}) \end{bmatrix}, \quad k = -M, \ldots, M \tag{4}$$

When considering the LF load-line characterization carried out with sinusoidal excitations at the fundamental frequency $\omega = \omega_{\rm LF}$ through the setup in Fig. 2, the displacement current can be totally neglected. Moreover, $\underline{H}(\omega)$ practically becomes a real and frequency-independent matrix (which, when considering the most common case of lumped parasitic description, reduces to the series parasitic resistors). In such a case, (3) enables to directly compute, starting from the knowledge of the LF harmonic components of the extrinsic voltages and currents, the intrinsic electrical variables (and, as consequence, the intrinsic load line) at the ED resistive core $V_{\rm gs}^i(k\omega_{\rm LF})$,$V_{\rm ds}^i(k\omega_{\rm LF})$,$I_g^{i,R}(k\omega_{\rm LF})$, and $I_d^{i,R}(k\omega_{\rm LF})$.

In order to exploit the LF load-line characterization for microwave power amplifier design, the extrinsic device load and source conditions must be computed, which enables the electrical regime corresponding to the chosen intrinsic load line to be imposed at the design frequency. To this end, the displacement currents related to the ED capacitive core must be evaluated according to the following explicit equations:

$$\begin{aligned} \begin{bmatrix} i_g^{i,C}(t) \\ i_d^{i,C}(t) \end{bmatrix} &= \begin{bmatrix} \sum_{k=-M}^{M} I_g^{i,C}(k\omega_{\rm RF}) e^{jk\omega_{\rm RF}t} \\ \sum_{k=-M}^{M} I_d^{i,C}(k\omega_{\rm RF}) e^{jk\omega_{\rm RF}t} \end{bmatrix} \\ &= \sum_{k=-M}^{M} jk\omega_{\rm RF} \underline{C}\left(v_{\rm gs}^i(t), v_{\rm ds}^i(t)\right) \\ &\quad \times \begin{bmatrix} V_{\rm gs}^i(k\omega_{\rm LF}) e^{jk\omega_{\rm RF}t} \\ V_{\rm ds}^i(k\omega_{\rm LF}) e^{jk\omega_{\rm RF}t} \end{bmatrix} \end{aligned} \tag{5}$$

where $\omega_{\rm RF}$ is the fundamental operating frequency of the power amplifier with

$$\begin{aligned} v_{\rm gs}^i(t) &= \sum_{k=-M}^{M} V_{\rm gs}^i(k\omega_{\rm LF}) e^{jk\omega_{\rm RF}t} \\ v_{\rm ds}^i(t) &= \sum_{k=-M}^{M} V_{\rm ds}^i(k\omega_{\rm LF}) e^{jk\omega_{\rm RF}t}. \end{aligned} \tag{6}$$

As previously said, the capacitance matrix[4] $\underline{C}$ in (5) can be identified on the basis of frequency- and bias-dependent S-parameter measurements. Alternatively, the capacitive core of a suitable already available nonlinear model can be used.

It must be outlined that when high-frequency nonquasi-static effects are not negligible, the displacement currents cannot be explicitly evaluated in terms of a capacitance matrix only as in (5), but nonlinear circuit analysis is required. To this end, any frequency- or time-domain available computer-aided design (CAD) environment can be easily adopted.

Once the harmonic components of the "global" intrinsic currents have been evaluated by (4), the extrinsic electrical variables, which define the load and source extrinsic regime, can be computed by

$$\begin{bmatrix} V_{\rm gs}^e(k\omega_{\rm RF}) \\ V_{\rm ds}^e(k\omega_{\rm RF}) \\ I_g^e(k\omega_{\rm RF}) \\ I_d^e(k\omega_{\rm RF}) \end{bmatrix} = \underline{H}^{-1}(k\omega_{\rm RF}) \begin{bmatrix} V_{\rm gs}^i(k\omega_{\rm RF}) \\ V_{\rm ds}^i(k\omega_{\rm RF}) \\ I_g^i(k\omega_{\rm RF}) \\ I_d^i(k\omega_{\rm RF}) \end{bmatrix}, \quad k = -M, \ldots, M \tag{7}$$

and finally, the load impedance at the fundamental and harmonic frequencies can be obtained as follows:

$$Z_L(k\omega_{\rm RF}) = -\frac{V_{\rm ds}^e(k\omega_{\rm RF})}{I_d^e(k\omega_{\rm RF})}. \tag{8}$$

In addition, the input device "large-signal impedance" can also be easily computed as follows:

$$Z_{\rm IN}(k\omega_{\rm RF}) = \frac{V_{\rm gs}^e(k\omega_{\rm RF})}{I_g^e(k\omega_{\rm RF})}. \tag{9}$$

[3]Due to the frequency-independence of the conduction current, its harmonic RF components simply coincide with the LF ones, i.e., $I_x^{i,R}(k\omega_{\rm RF}) = I_x^{i,R}(k\omega_{\rm LF})$.

[4]Note that the difference existing, given a bias condition, among the imaginary parts of the admittance parameters Y_{12} and Y_{21} (typically modeled by a transcapacitance) can be accounted for by (5) without any approximation.

which, for instance, can be used to synthesize the optimum source impedance (i.e., $Z_s = \mathrm{conj}(Z_{\mathrm{IN}})$), which provides a matching condition under large-signal operation. It should be outlined that this information is not obtainable through scalar LP systems [10]–[12], but only by adopting a time-domain LP measurement setup [14]–[16].

To summarize, the proposed approach, which is based on LF large-signal measurements and bias/frequency-dependent small-signal measurements performed in the frequency range of interest for the considered design, is fully able to provide the same kind of information obtainable by means of expensive nonlinear measurement setups operating at microwave frequencies. The only assumption is that a negligible uncertainty can be achieved in the description of the intrinsic ED capacitive core whose accuracy ultimately defines the frequency limitations. As will be demonstrated in Section IV, by adopting very different experimental examples, such an hypothesis is more than reasonable from a practical point of view.

The flowchart reported in Fig. 4 summarizes the fundamental steps of the proposed design techniques.

IV. Experimental Examples

The validation of the proposed approach has been carried out by considering several power amplifier designs. With the aim of validating the method, a rough, although more than reasonable, choice of the load line was carried out for the different designs.

As a first example, an on-wafer $0.35 \times 960\ \mu\mathrm{m}^2$ GaAs pseudomorphic HEMT (pHEMT) device, suitable for X-band power amplifier design, has been considered: the foundry specifications for such a technology are listed in Table I. The goal is to exploit the technology under class-AB operation. To this end, the device has been biased at $(V_{g0} = -0.6\ \mathrm{V}, V_{d0} = 10\ \mathrm{V}, I_{d0} = 90\ \mathrm{mA})$. LF measurements have been carried out and the load line plotted in Fig. 5 has been chosen, which corresponds to an output power of 30.2 dBm (1.1 W/mm) and a 67% drain efficiency.

Two design examples (at 4 and 10 GHz) have then been considered and, according to the procedure described in Section III, the capacitive core of the foundry model, also accounting for nonquasi-static phenomena, has been adopted to compute the displacement currents (5), and successively, the total intrinsic currents (4).

Fig. 6(a) shows, for the 10-GHz case, the drain current and its conduction and displacement components, while in Fig. 6(b), the gate current (which practically coincides with its displacement component) is plotted. Finally, by adopting the linear parasitic network description of the foundry model, the extrinsic currents and voltages have been obtained.

Table II shows the obtained load impedance values, whereas the source impedance has been chosen to avoid highly mismatched impedances, which, as clearly stated in [10] and [11], would emphasize the uncertainty of the high-frequency LP measurements exploited to validate the consistence of the proposed approach. In particular, large-signal measurements were carried out by exploiting a 4-26 GHz LP system [11], which enables device source and load impedances at the fundamental frequency to be controlled by means of two computer-controlled microwave tuners. Moreover, the system is equipped with an Anritsu MG3694B signal generator (2–40 GHz), an Agilent N6705A dc power analyzer, an Anritsu 37397D vector network analyzer (40 MHz–65 GHz), an Agilent E4446A

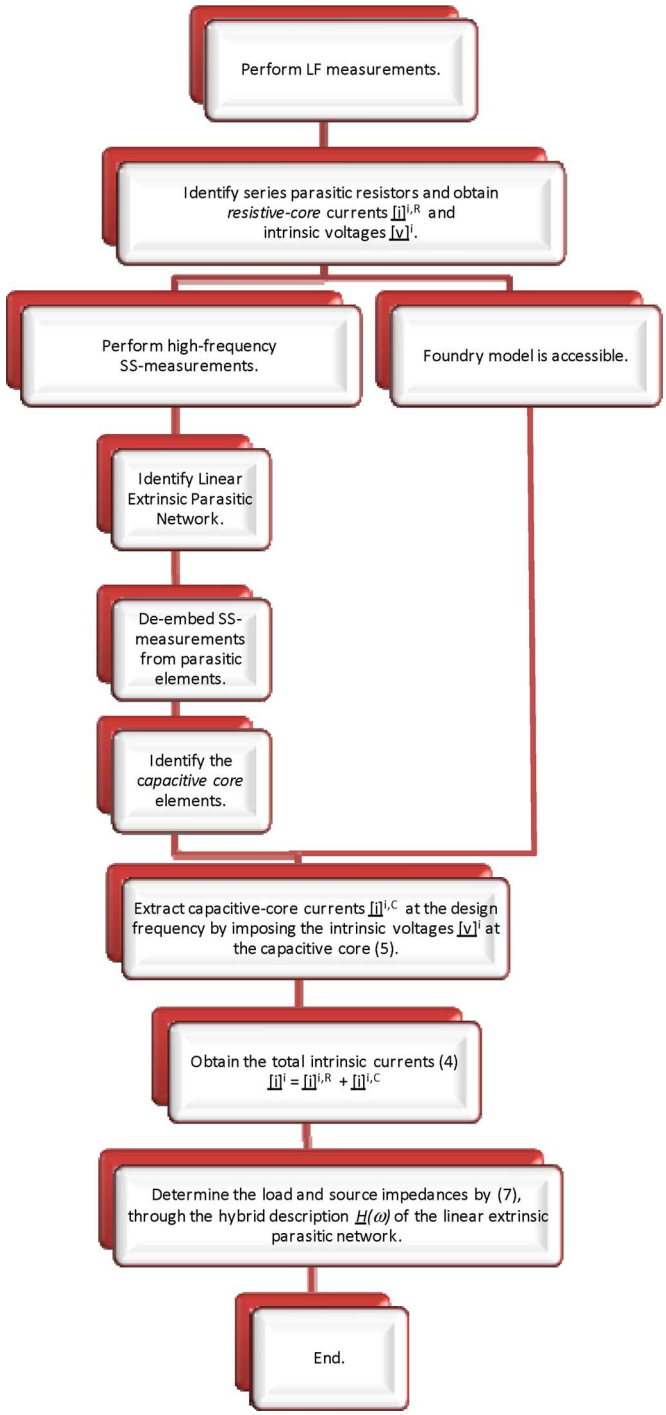

Fig. 4. Flowchart describing the proposed design technique.

TABLE I
0.35-μm GaAs pHEMT Technology Specifications

Quantity	*Value*
Breakdown Voltage	22 V
Pinch-off Voltage	-1 V
Idss	300 mA/mm
Saturated Output Power	1.2 W/mm

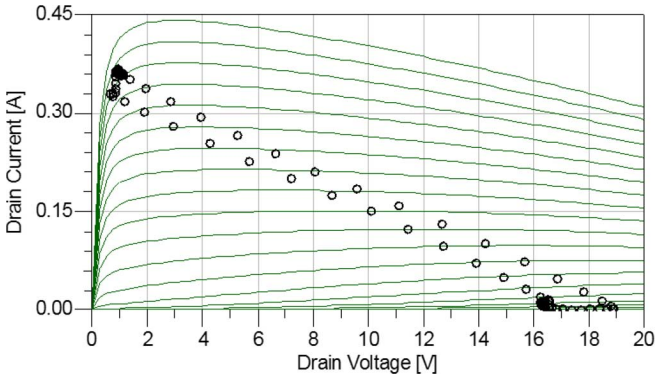

Fig. 5. Load line chosen for a 960-μm GaAs pHEMT biased at ($V_{g0} = -0.6$ V, $V_{d0} = 10$ V, $I_{d0} = 90$ mA) by exploiting the LF measurement system shown in Fig. 2. Amplitude of the gate incident signal ($A_g = 2$ V), amplitude of the drain incident signal ($A_d = 1$ V), signals relative phase ($\Delta\varphi = 0°$), and signal frequency ($f_{\rm LF} = 2$ MHz). The load line is superimposed to dc characteristics (-1.3 V $\leq V_g \leq 0.5$ V, step 0.1 V).

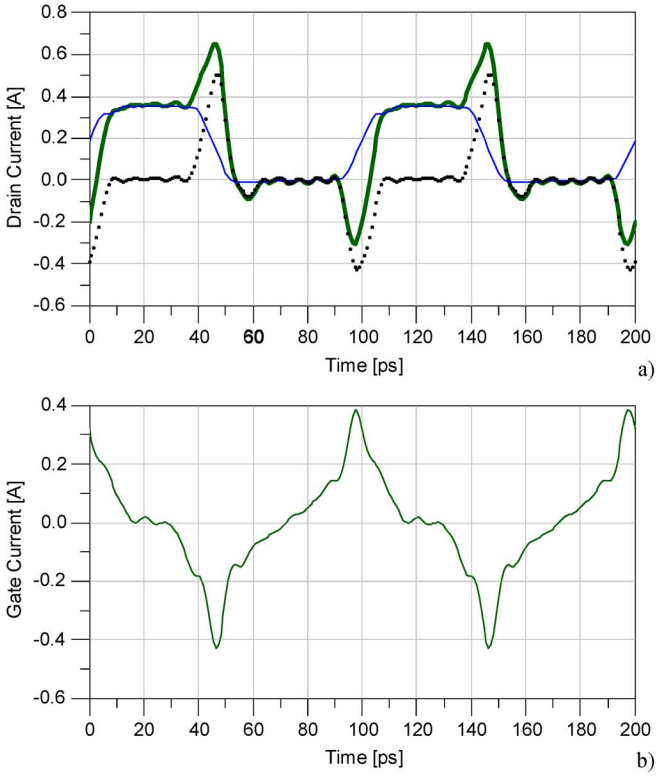

Fig. 6. (a) Drain current at the intrinsic device I_d^i (green thick solid line in online version) and its two components: the capacitive one (dots) and the resistive one (blue thin solid line in online version). (b) Total gate current at the intrinsic device I_g^i. $f_{\rm RF} = 10$ GHz.

spectrum analyzer (3 Hz–44 GHz), and an Agilent N1912A dual-channel power meter.

Measurements carried out at 4 GHz on the selected device, by adopting the impedance values reported in Table II, are shown in Fig. 7.

The experimental results in Table III compare predictions obtained by means of the proposed approach and LP data for the output power level of interest (i.e., 30.2 dBm). The good agreement is evident despite, especially at 10 GHz, the importance of the displacement currents (see Fig. 6). In particular, a good prediction has been obtained of the high level of converted dc drain

TABLE II
SYNTHESIZED SOURCE AND LOAD IMPEDANCES FOR THE 4- AND 10-GHz GaAs pHEMT POWER AMPLIFIER DESIGNS

Source Impedance	*Frequency*	*Load Impedance*
9.40 + i·11.62 Ω	4 GHz	39.44 + i·14.75 Ω
	8 GHz	34.43 + i·23.07 Ω
	12 GHz	23.40 + i·27.98 Ω
8.26 + i·5.7 Ω	10 GHz	26.5 + i·21.53 Ω
	20 GHz	14.43 + i·19.93 Ω
	30 GHz	5.97 + i·15.33 Ω

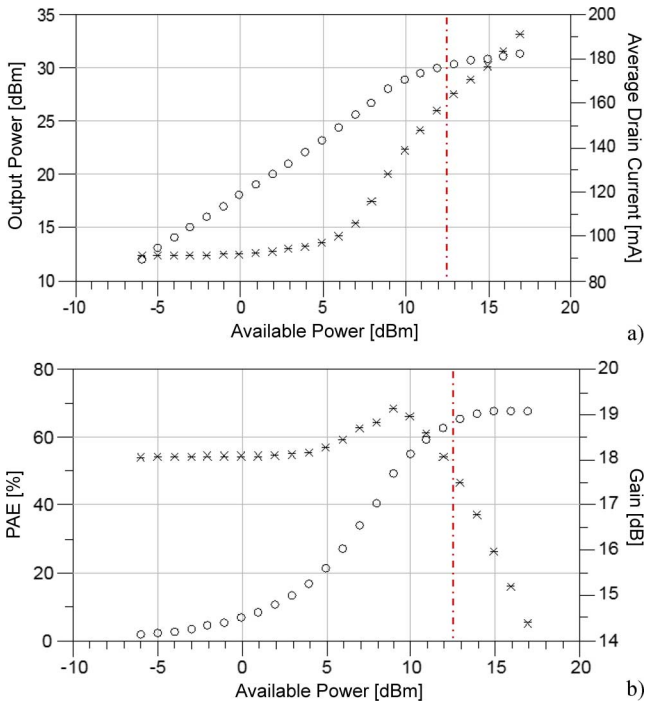

Fig. 7. LP measurements carried out at 4 GHz by imposing the load and source impedances synthesized through the proposed approach (Table II). The dotted vertical lines identify the values corresponding to the output power level of interest. (a) Output power (circles) and average drain current (stars). (b) Power-added efficiency (circles) and transducer power gain (stars).

TABLE III
COMPARISON BETWEEN DEVICE PERFORMANCE PREDICTED BY THE PROPOSED TECHNIQUE AND MEASUREMENT DATA ($P_{\rm out} = 30.2$ dBm)

Predicted 4 GHz \ 10 GHz	*Quantity*	*Measured 4 GHz \ 10 GHz*
159 mA	Average drain current	160.5 mA \ 170 mA
66.7 %	Drain Efficiency	65.9 % \ 62 %
15.9 dB \ 10.8 dB	Gain	17.8 dB \ 12.3 dB
65 % \ 61.2 %	PAE	64.3 % \ 58.3 %

current (159 mA starting from a quiescent condition of 90 mA). The acceptable discrepancies (more evident at 10 GHz) between large-signal measurements and predictions are essentially associated to two problems: the uncertainty related to the LP setup and the accuracy of the capacitive core description. In fact, in the present example, a nonlinear model based on analytical expressions for the capacitive core (which allows for optimum simulation times, but cannot guarantee the same level of accuracy of

TABLE IV
0.7-μm GaN HEMT TECHNOLOGY SPECIFICATIONS

Quantity	*Value*
Breakdown Voltage	80 V
Pinch-off Voltage	-3.5 V
Idss	700 mA/mm
Saturated Output Power	4 W/mm

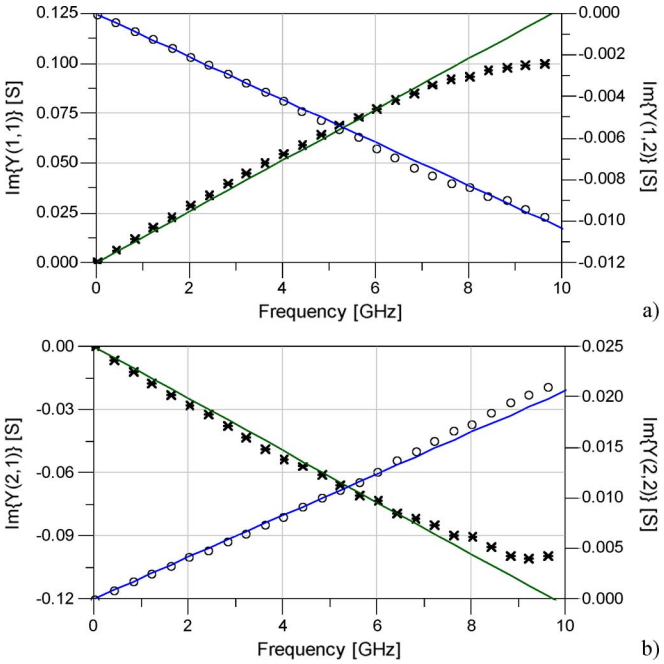

Fig. 8. Measurements (symbols) versus predictions (continuous lines) at ($V_{g0} = -2$ V, $V_{d0} = 25$ V) of the Y-parameter imaginary parts at the intrinsic device. (a) $Y(1,1)$ (stars) and $Y(1,2)$ (circles). (b) $Y(2,1)$ (stars) and $Y(2,2)$ (circles).

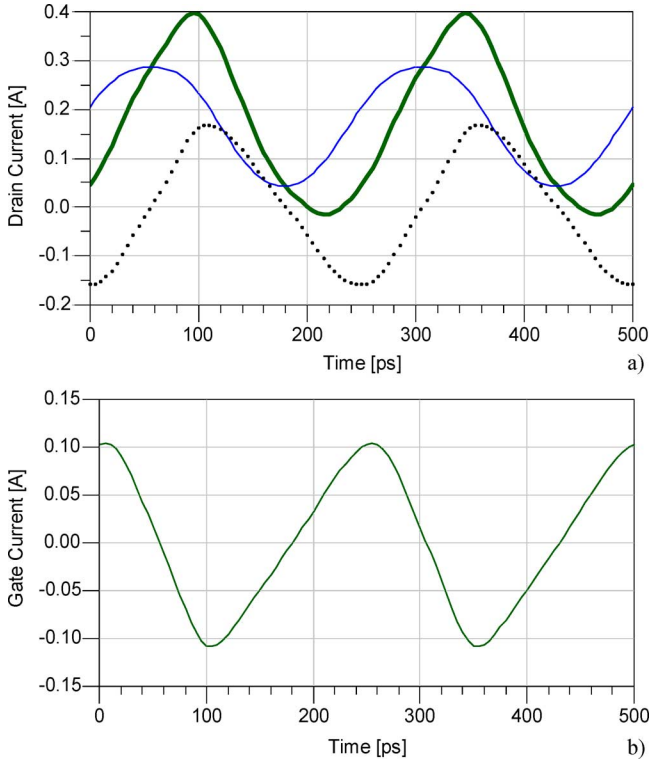

Fig. 9. (a) Drain current at the intrinsic device I_d^i (green thick solid line in online version) and its two portions: the capacitive one (dots) and the resistive one (blue thin solid line in online version). (b) Total gate current at the intrinsic device I_g^i.

TABLE V
SYNTHESIZED SOURCE AND LOAD IMPEDANCES FOR THE 800-μm GaN HEMT

Source Impedance	*Frequency*	*Load Impedance*
3.41 + i·10.21 Ω	4 GHz	42.42 + i·54.22 Ω
	8 GHz	16.28 - i·12.18 Ω
	12 GHz	14.55 + i·25.79 Ω

lookup-table approaches) has been adopted. The lack of control on the harmonic LP terminations also has a noticeable influence: they might be responsible for a 5% discrepancy on the converted dc current, as indicated by simulations carried out with the nonlinear model.

As a further example, an on-wafer C-band 0.7 × 800 μm^2 GaN HEMT device has been considered whose foundry specifications are reported in Table IV.

The bias condition has been chosen under the constraints of operating under weakly nonlinear operation ($V_{g0} = -2$ V) and limiting, for safety reasons, the quiescent dissipated power to 4.75 W ($V_{d0} = 25$ V, $I_{d0} = 190$ mA). A 110-Ω loading condition (see Fig. 3) has been considered, which provides an output power ($P_{\rm out}$) of 29.5 dBm and a drain efficiency of 20.5%.

In this case, S-parameter measurements (40 MHz–40 GHz) were performed in a wide range of bias conditions (-8 V $< V_{g0} < 1$ V, 0 V $< V_{d0} < 40$ V), and after the identification and deembedding of the parasitic network, (5) was adopted for the computation of the capacitive-core behavior. Nonquasi-static effects have been neglected since, assuming a design frequency of 4 GHz, they are of minor importance up to 8 GHz, as clearly shown in Fig. 8.

The gate and drain currents are shown in Fig. 9. The large contribution deriving from the capacitive core is quite evident.

The synthesized load and source impedances (in this case, the latter has been chosen equal to the conjugate of the large-signal device input impedance) are listed in Table V, while the corresponding LP measurements are shown in Fig. 10. The experimental results corresponding to the output power of 29.5 dBm are summarized in Table VI and demonstrate an impressive agreement. The accuracy improvement obtainable, with respect to the previous example, when using a lookup-table based model of the capacitive core is evident.

Finally, the proposed procedure has been adopted for the design and realization of a hybrid L-band high-power amplifier exploiting a discrete GaN HEMT power bar of the same process previously described. The bar is composed of six 2-mm cells for a total gate periphery of 12 mm and is capable of delivering a saturated output power of about 46.8 dBm.

The proposed approach has been applied to the 2-mm elementary cell in order to define the optimum load impedance. The bias condition has been chosen for class-AB operation ($V_{g0} = -3$ V, $V_{d0} = 35$ V, $I_{d0} = 140$ mA), and the load line shown in

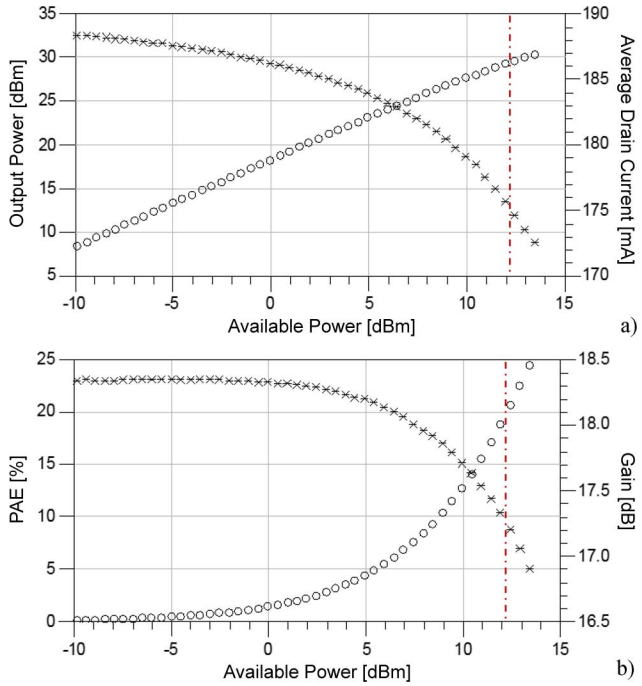

Fig. 10. LP measurements carried out at 4 GHz by imposing the load and source impedances synthesized through the proposed approach (Table V). The dotted vertical lines identify the values corresponding to the output power level of interest. (a) Output power (circles) and average drain current (stars). (b) Power-added efficiency (circles) and transducer power gain (stars).

TABLE VI
COMPARISON BETWEEN DEVICE PERFORMANCE PREDICTED BY THE PROPOSED TECHNIQUE AND MEASUREMENT DATA ($P_{\rm out} = 29.5$ dBm, DESIGN FREQUENCY = 4 GHz)

Predicted	*Quantity*	*Measured*
172 mA	Average drain current	175 mA
20.5 %	Drain Efficiency	20.1 %
17.3 dB	Gain	17.3 dB
20.1 %	PAE	19.7 %

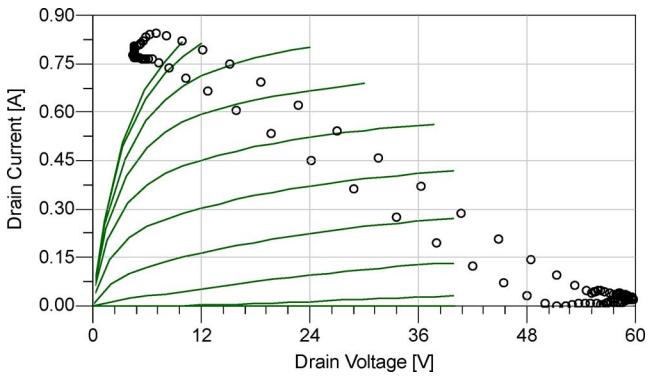

Fig. 11. Load line of a 2-mm GaN HEMT device biased at ($V_{g0} = -3$ V, $V_{d0} = 35$ V), chosen by exploiting the LF measurement system shown in Fig. 2. Amplitude of the gate incident signal ($A_g = 5$ V), amplitude of the drain incident signal ($A_d = 9$ V), signals relative phase ($\Delta\varphi = 180°$), and signal frequency ($f_{\rm LF} = 2$ MHz). The load line is superimposed to pulsed characteristics (-5.5 V $\leq V_g \leq 1.5$ V, step 0.5 V) carried out from the considered quiescent bias condition.

Fig. 11 has been selected, which provides a single-cell output power of 38.8 dBm (3.8 W/mm) and a drain efficiency of 67%.

TABLE VII
SYNTHESIZED SOURCE AND LOAD IMPEDANCES FOR THE 2-mm GaN HEMT

Source Impedance	*Frequency*	*Load Impedance*
9.31 + i·23.58 Ω	1.275 GHz	58.32 + i·23.06 Ω
	2.550 GHz	31.05 + i·25.80 Ω
	3.825 GHz	26.10 + i·22.52 Ω

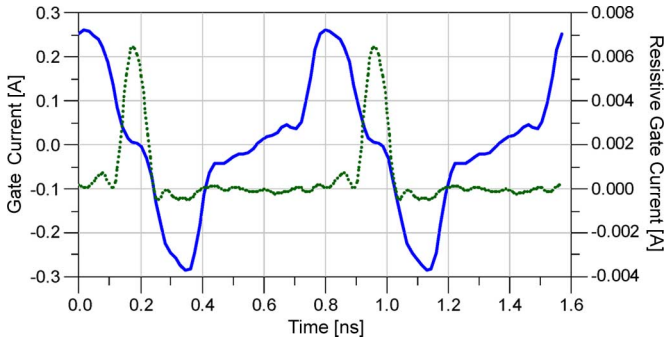

Fig. 12. Gate current at the intrinsic device I_g^i (solid line) and its resistive portion (dots). $f_{\rm RF} = 1.275$ GHz.

The capacitive core of the foundry models, also accounting for nonquasi-static phenomena, was exploited in order to compute the displacement currents. The load impedance has then been evaluated according to the already described procedure, while the source impedance was chosen equal to the conjugate of the device input large-signal impedance (see Table VII).

In Fig. 12, the device total gate current and its resistive component are shown. It is well evident that the latter is also negligible with respect to the capacitive current in high-compression amplifier operation. Nevertheless, the average value of the gate current, which is dependent only on the resistive current, is a widely adopted marker for device reliability issues (i.e., gate–source diode conduction and gate–drain diode breakdown). Average gate current values are easily used for this purpose since they are easily put in relationship with reliability characterization based on static device characterization (e.g., [37]–[39]). The proposed approach enables the resistive gate current to be directly controlled when choosing the device operating conditions. Moreover, the time-dependent waveform of the gate current is also directly measured, which could be useful for more in-depth analysis of reliability issues [13].

The L-band power amplifier has been designed by synthesizing, on a high-frequency laminate, an output network, which provides the chosen load impedance (Table VII) to each single 2-mm cell of the power bar. A photograph of the realized amplifier is shown in Fig. 13.

The high load impedance required by the GaN devices allows for impedance transformation through a simple microstrip step-impedance network connected to the six elementary cells by means of six bonding wires. An input network composed of a radial stub and a step-impedance solution optimizes the transducer gain. Furthermore, a combined series-shunt *RC* stabilizing network, implemented by means of surface mount device (SMD) resistors and ceramic capacitors, makes the device unconditionally stable from dc to the cutoff frequency. Gate and drain bias networks employ high impedance $\lambda/4$ microstrip lines with shunted SMD chip capacitors.

Fig. 13. GaN Amplifier for L-band application exploiting a coplanar technology integrated circuit. The active device is a 12-mm GaN power bar combining six 2-mm elementary cells.

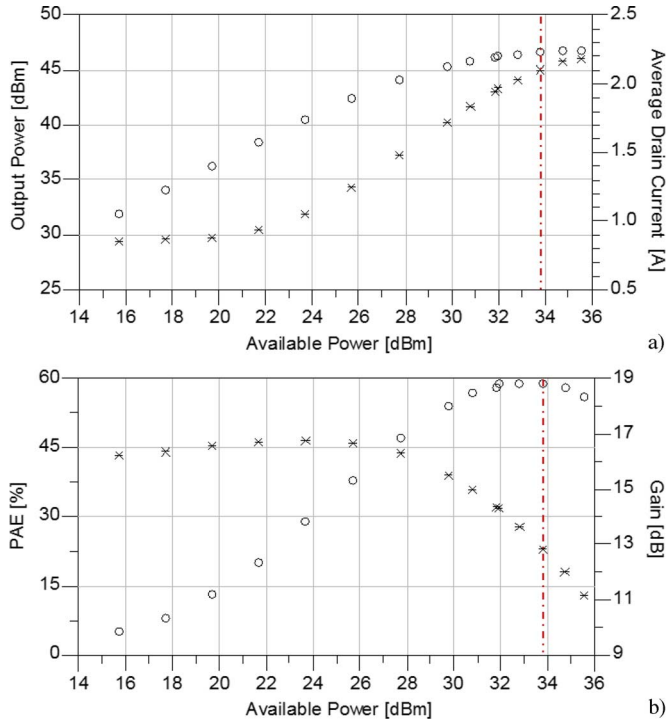

Fig. 14. Measured performance of the hybrid L-band high-power amplifier. The dotted vertical lines identify the values corresponding to the output power level of interest. (a) Output power (circles) and average drain current (stars). (b) Efficiency (circles) and transducer power gain (stars).

TABLE VIII
COMPARISON BETWEEN DEVICE PERFORMANCE PREDICTED BY THE PROPOSED TECHNIQUE AND MEASUREMENT DATA ($P_{\rm out} = 46.64$ dBm, DESIGN FREQUENCY $= 1.275$ GHz)

Predicted	*Quantity*	*Measured*
1.95 A	Average drain current	2.1 A
67 %	Drain Efficiency	63 %
13.4 dB	Gain	12.8 dB
64 %	PAE	59 %

Fig. 14 shows the main performance of the amplifier: a saturated output power of about 46.75 dBm and a 63% efficiency fully comply with the expected performance of the technology.

In Table VIII, the L-band power amplifier measured performance are compared with the predictions obtained through the proposed technique with reference to the same level of output power (46.64 dBm). Considering the unavoidable dispersion in the realization phases and that only the load impedance at the fundamental frequency has been accurately synthesized, the results definitely indicate the effectiveness of the proposed approach for the design of power amplifiers. In particular, a good prediction has been obtained of the high level of converted dc drain current (2.1 A starting from a quiescent condition of 840 mA).

V. CONCLUSION

A new approach to power amplifier design based on the experimental characterization of the ED load line has been proposed. The method mainly relies on large-signal measurements carried out at low frequency, which enables the most important ED nonlinear effects to be exactly accounted for. Bias/frequency-dependent small-signal measurements are used to identify the ED capacitive core and compute the displacement currents. Alternatively, the capacitive core of an existing nonlinear device model can be adopted.

The method has provided excellent agreement with experimental results obtained by means of complex and expensive high-frequency LP setups. Finally, the design of an L-band high-power GaN amplifier has been carried out in order to definitely confirm the effectiveness of the proposed approach.

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