200-W GaN PA Design Based on Accurate Multicell Transistor Modeling

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***Abstract*—In this paper, a model extraction technique suitable for GaN transistors with very large periphery is described. The technique is based on the accurate nonlinear model extraction of a reference size device that is then scaled to a larger periphery preserving its original accuracy. The proposed model has been extensively validated with microwave nonlinear load-pull measurements and with the design of a 200-W S-band power amplifier.**

***Keywords*— microwave FET, nonlinear transistor modeling, power amplifiers.**

I. Introduction

Gallium Nitride (GaN) technology has unique capabilities that make it very attractive for a large variety of applications as satellite communications, radar, and wireless systems [1], [2]. High-power operation is for sure one of its strengths that is crucial for all those applications that require more and more power, e.g., to extend the transmission range, or that need to operate at back-off from the peak power to avoid distortion. The impressive physical and electrical characteristics of GaN in terms of high-voltage and high-frequency operations enable very high-power density in small-size chips with reduced weight, and this justifies the growing and growing attention to this technology by the marketplace.

Non-communications applications at S band are primarily radars used in air-traffic control and airspace surveillance at 2.7 – 3.5 GHz. Beyond this, GaN is used for RF generators in particle accelerators at 2.856 GHz and 2.998 GHz, medical (MRI) and recently industrial (heating) equipment at 2.45 GHz, and power transmission as well [3].

In this paper, the nonlinear modelling of high-power GaN HEMT dice, accounting for low-frequency dispersion effects, is discussed and the extraction technique suitable to obtain an accurate model of large periphery devices, starting from a "reference size device" named unit-cell device (UC), is detailed. Section II describes the proposed modeling technique whereas in Section III and IV the nonlinear model extraction is discussed for the case of the 3.3-mm UC device, and for the multicell device composed by eight UCs, for a total periphery of 26.4 mm. Section V reports the validation of the model on a designed S-band high-power amplifier (HPA) with 200-W of output power and 55 % drain efficiency.

II. Modeling Technique

The direct extraction of a nonlinear model for large-periphery devices is a hard task, and this is mainly due to the difficulties in performing an extensive experimental characterization of the investigated device under very high-power operations (i.e., hundreds of watt). Experimental data, consistent with actual operating regime, are crucial to obtain an accurate and global model especially when the devices are made by GaN technology that, as well known from literature, is affected by trapping and thermal effects [4]-[6], which limit microwave performance.

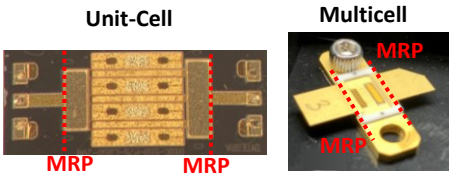

Fig. 1. Picture of the unit-cell (3.3 mm) and multicell (26.4 mm) GaN devices. The pre-matched multicell is used in HPA design.

For the above reasons, we propose a model extraction technique suitable for the modeling of GaN devices with large peripheries (i.e., > 20 mm). The main idea is to start with an extensive characterization of the UC device, with the aim of extracting its nonlinear model. After that, the UC model can be scaled up to the largest periphery of interest. Typically, the critical point in scaling a nonlinear model is the passive access structure that does not scale linearly with periphery. Another critical aspect for large devices is the different thermal and electrical conditions existing between central and peripheral devices that could lead to reduced power performance. This aspect makes useless increasing the device area beyond a suitable limit, so that in this paper we considered a device whose periphery and layout have been optimized to minimize these effects at the selected design frequency [7]. On the other hand, the scaling of the intrinsic active area is commonly less critical and good predictions can be obtained by conveniently multiplying by the scaling factor the parameters of the model. For this reason, it is crucial to perform the characterization of the UC by keeping the measurement reference plane (MRP) as close as possible to the active area of the device, to minimize the impact of extrinsic access structures. When the nonlinear model of the UC is validated, the model of the multicell is built by simply combining N instances of the UC model through the models of the package and bonding wires, which are obtained by electromagnetic (EM) simulations. Fig. 1 shows the UC device exploited in this work, that is a 3.3-mm GaN HEMT, and the pre-matched multicell (MC) device used

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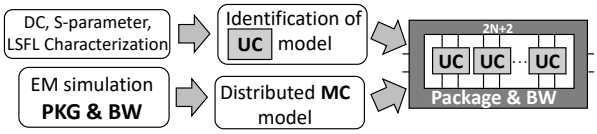

Fig. 2. Flowchart describing the extraction procedure of the multicell model.

in HPA design, that is a packaged device composed by 8 UCs in parallel, with total periphery of 26.4 mm, and a pre-matching network at the central frequency of 3.3 GHz. Fig. 2 summarizes the extraction steps of the UC and MC models. First, DC I/V characterization in a wide grid of biases and large-signal low-frequency measurements (LSLF) under different biases and loading conditions are carried out on the UC to extract the model of the drain-source current generator [5]. After that, multi-bias S-parameter measurements are used to extract the model of the nonlinear capacitances [8].

Since it is not feasible to completely remove all passive access structure contributions, in the model of the UC a linear extrinsic parasitic network (EPN) is present that models the residual contribution of metallization and vias. Cold-FET S-parameter measurements are carried out to extract the EPN parameters [8], [9].

The MC model requires EM simulations of the package (PKG), bonding wires (BW), and internal match structures as shown in Fig. 3, implemented as a (2*N*+2)-port network. Eventually, *N* instances of the UC model can be appropriately connected to the (2*N*+2)-port network to obtain the MC nonlinear model (see Fig. 2). The MC model has been verified by extensive load-pull measurements; then, the definitive validation has been performed by the design of a class-B HPA.

III. UC Model Identification and Validation

The equations used to model the UC are based on the Angelov's formulation both for the current generator and nonlinear capacitances [8]. To correctly account for thermal and trapping effects affecting GaN transistor operation [4], a custom dispersion model is integrated to the Angelov's formulation [5]. It is based on purely-dynamic correction terms that modify the static characteristics. As explained in section II, DC I/V measurements are carried out over an extensive grid of biases: V_{GS0} = -3 V to 2 V and V_{DS0} = 0 V to 50 V, with a compliance on maximum dissipated power of 15 W. The optimization of the DC I/V model parameters are performed against these measurements. Eventually, to extract the purely-dynamic correction terms accounting for dispersion effects, we used low-frequency load-pull measurements carried out under class AB, B and C for V_{DS0} = 35 V, 40 V, and 50 V, and for different loading conditions, shown in Fig. 4a. Measurements under a different operating class (i.e., class F) are used for validating the model. The results, after the numerical optimization of the whole current-generator model parameters, are shown in Figs. 4b-4e. Measurements from index 0 up to 450 were used to extract the model whereas the additional ones were used for the validation. As it can be noticed, the current-generator model shows a good level of accuracy for all the operating conditions considered. Once the current-generator model is extracted, the nonlinear-capacitance parameters are obtained by numerical optimization against the multi-bias S-parameters. After that, the model was validated by means of time-domain load-pull measurements at 3.3 GHz, under class B, V_{DS0} = 50 V and I_{DS0} = 3 mA [10]. The measured grid is shown in Fig. 4f. The results of validation are shown in Figs. 4g-4j where simulations are compared to the model for the operating condition corresponding to the output-power optimum, highlighted in Fig. 4f with filled red circle. This definitely assesses the accuracy of the nonlinear UC model so that the MC model can be derived as described in Fig. 2.

IV. MC Model

After extracting and validating the model of the UC, the next step is to build the model of the MC device as described in Section II. To this end, it is necessary to combine N = 8 instances of the UC model and to add the models of the package and bond wires. The latter are obtained by means of EM simulations performed in AWR.

The package and wire bond were simulated with 3D EM model that incorporated the exact wire bond dimensions and package dimensions. In the most general case, the package model included all elements of the ceramic ring frame and metallization structures as well as any internal match structures. Fig. 3 shows the 3D structure for the gate side EM simulation, that uses 8 separate ports for the wire bond connections to the die and a single wave port at the exterior of the package for the gate lead. The wire bond connections and package for the drain was simulated with the same concept, although the drain does not have an internal matching structure. EM simulation of the gate side without considering the internal match structure was also performed.

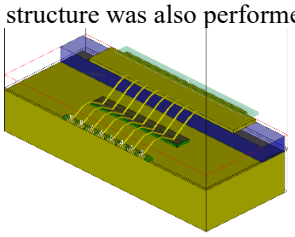

Fig 3. 3D EM simulation structure for the gate side, with reference planes at the gate bonding pads and the exterior MRP of the package.

To validate the model of the MC device, time-domain load-pull measurements [10] were carried out on the 8-cell device without any internal match structure and then compared with simulations of the MC model. In this case, the model used for the package is the one without the internal match structure, to be coherent with the measured sample. Fig. 4k shows the measured impedance grid, whereas Figs. 4l-4o show the comparison between measurements and model predictions at 3.3 GHz, V_{DS0} = 50 V, and I_{DS0} = 24 mA. Output power, drain efficiency and time-domain waveforms of drain voltage and current are reported for all input power levels and loading conditions synthesized during the characterization campaign. As it can be noticed, the global accuracy of the model is excellent; in fact, the model is able to predict the current and voltage waveforms, as well as the output power under both saturated and linear operations.

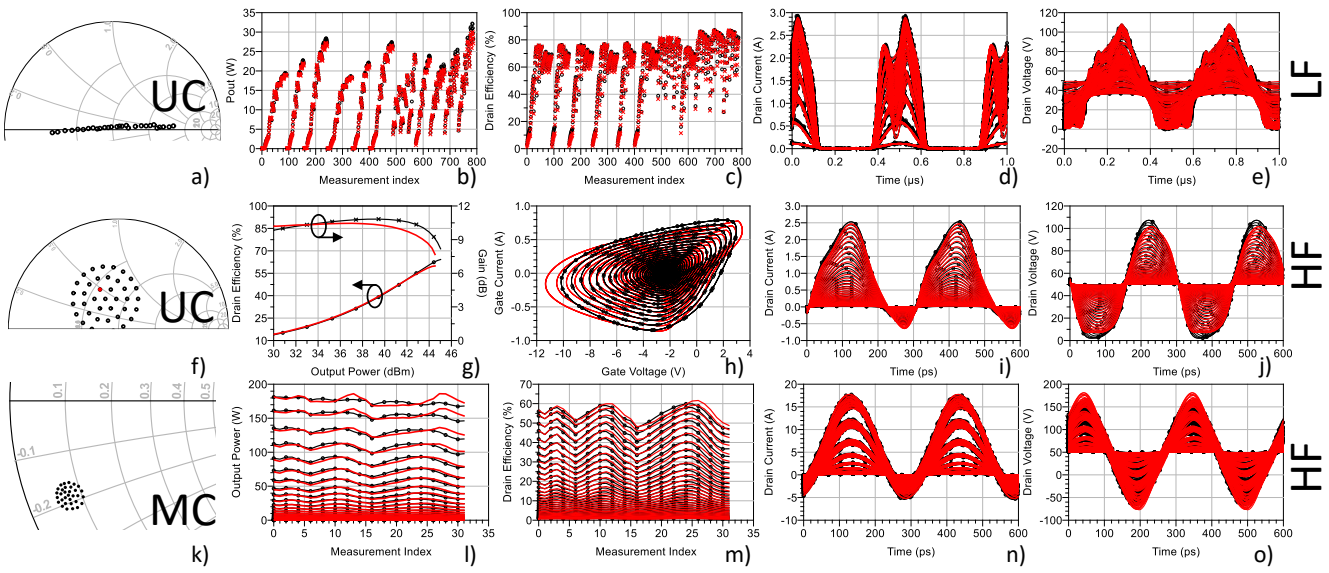

Fig 4. UC LF measured (circled lines) and simulated (continuous lines) (a) impedance grid, (b) output power, (c) drain efficiency, (d) drain current, and (e) drain voltage used in the extraction (index 0 – 450) and in the validation (index 451 – 787) of the current-generator model. UC HF (f) impedance grid, (g) drain efficiency and gain as function of output power, (h) input loci, (i) drain current, (j) drain voltage used for model validation. MC HF (k) impedance grid, (l) output power, (m) drain efficiency, (n) drain current, and (o) drain voltage used for model validation. Reference planes of MC measurements lie at the edge of the PKG.

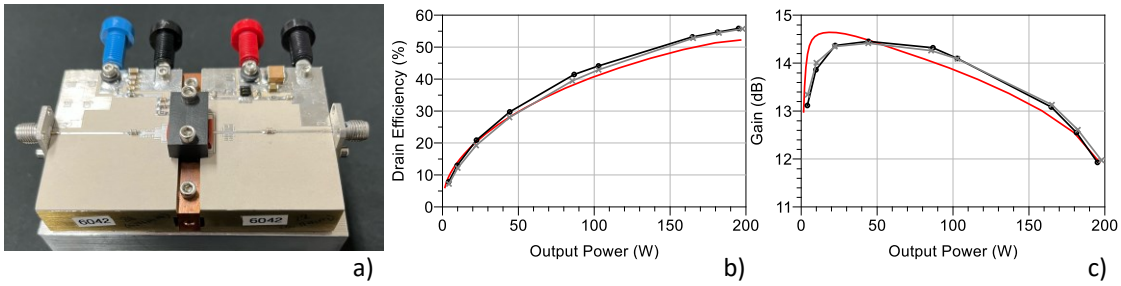

Fig. 5. (a) Picture of the realized S-band HPA. PA measured (circled and crossed lines) and simulated (continuous lines) (b) drain efficiency and (c) gain as function of output power under pulsed condition with 10% duty cycle and 300-µs pulse width. Frequency is 3.3 GHz and bias is 50 V, 24 mA. Reference planes are at the coaxial connectors.

V. Power Amplifier Validation

A HPA was designed with the purpose of validating the nonlinear model of the MC device. It is designed to operate at S-band under class-B operation. One pre-matched multicell device with with 26.4 mm of periphery is used, biased at 50 V and 24 mA, at the central operating frequency of 3.3 GHz.

An evaluation board was designed to create an impedance match for the MC device from 3.1 through 3.5 GHz. The fixture uses high dielectric board material, with a dielectric constant of 10.2 and with 0.025-inch-thick dielectric (0.6 mm). The high dielectric constant enables low impedance distributed matching sections for the 200 W device. Gate and drain bias to the device are provided through printed high impedance lines that are approximately quarter wave in length with a shorting RF capacitor, this to provide a low pass filter and eliminate loading effects from the bias network. Fig. 5a shows a picture of one sample of the realized HPA. Model predictions and measurements performed on two samples of the designed HPA were compared. Figs. 5b and 5c show the results of this comparison for gain and drain efficiency as function of output power. The model shows very good prediction capability since the maximum deviation is 3.5 % for efficiency and 1 dB for gain below 50 W of output power and 0.5 dB above. This excellent agreement confirms the effectiveness of the proposed modeling technique that preserves the same level of accuracy both for the UC and MC devices.

VI. Conclusion

We reported in this paper a modeling technique suitable for very large periphery GaN transistors based on the extraction of a reference size device model (i.e., the UC device) and electromagnetic simulations. We demonstrated that the excellent prediction capabilities of the UC model are transferred to the MC device. The design of a 200-W PA and the comparison of its performance with model predictions definitely assess the effectiveness of the proposed approach.

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REFERENCES

[1] T. Ohki, *et al.*, "An over 20-W/mm S-band InAlGaN/GaN HEMT with SiC/diamond-bonded heat spreader", *IEEE Electron Device Lett.*, vol. 40, pp. 287–290, Feb. 2019.

[2] C. Friesicke, *et al.*, "Packaged AlGaN/GaN HEMT power bars with 900W output power and high PAE at L-band," *Proc. 46th Eur. Microw. Conf.*, 2016, pp. 409–412.

[3] G. F. Formicone, "A highly manufacturable 75–150 VDC GaN-SiC RF technology for radars and particle accelerators," *IEEE Trans. on Semiconductor Manufacturing*, vol. 31, no. 4, pp. 440-446, Nov. 2018.

[4] S. C. Binari, *et al.*, "Trapping effects in wide-bandgap microwave FETs," 2002 *IEEE MTT-S Int. Microw. Symp. Dig.*, 2002, pp. 1823-1826.

[5] A. Raffo, V. Vadalà, D. M. M.-P. Schreurs, G. Crupi, G. Avolio, A. Caddemi, and G. Vannini, "Nonlinear dispersive modeling of electron devices oriented to GaN power amplifier design," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 4, pp. 710–718, April 2010.

[6] G. Avolio, A. Raffo, V. Vadalà, G. Vannini and D. M. M. . -P. Schreurs, "Dynamic-Bias S-Parameters: a new measurement technique for microwave transistors," in *IEEE Trans. Microw. Theory Tech.*, vol. 64, no. 11, pp. 3946-3955, Nov. 2016.

[7] A. Raffo, *et al*., "A new modeling technique for microwave multicell transistors based on EM simulations," in *IEEE Trans. on Microw. Theory and Techn.*, vol. 68, no. 7, pp. 3100-3110, Jul. 2020.

[8] I. Angelov, N. Rorsman, J. Stenarson, M. Garcia, and H. Zirath, "An empirical table-based FET model," *IEEE Trans. Microw. Theory and Techn.*, vol. 47, no. 12, pp. 2350-2357, Dec. 1999.

[9] G. Crupi *et al.*, "Accurate multibias equivalent-circuit extraction for GaN HEMTs," *IEEE Trans. Microw. Theory and Techn*., vol. 54, no. 10, pp. 3616-3622, Oct. 2006.

[10] M. Marchetti, *et al.*, "Active harmonic load–pull with realistic wideband communications signals," *IEEE Trans. Microw. Theory Techn.,* vol. 56, no. 12, pp. 2979-2988, Dec. 2008.