

# Minipac Building Blocks

## Workflow guide

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restricted



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# Working environment

- › Windows environment must not be used, Unix only.
- › Camino subproject "Freeman\_legacy" must not be used for design.
- › Camino subproject "tx\_00" shall be used.
  - Enter Camino environment (Unix):

– `camino mod_00 tx_00 -unit top_tx_00`

- › ADS command help:

– `ads -h` →

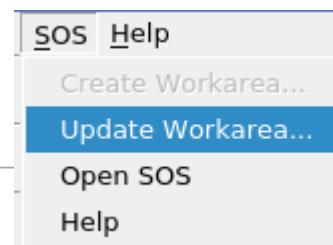
- › Update ClioSoft SOS workarea:

- from Terminal → type `sos` (and click Update in the SOS interface)
- after launching ADS →

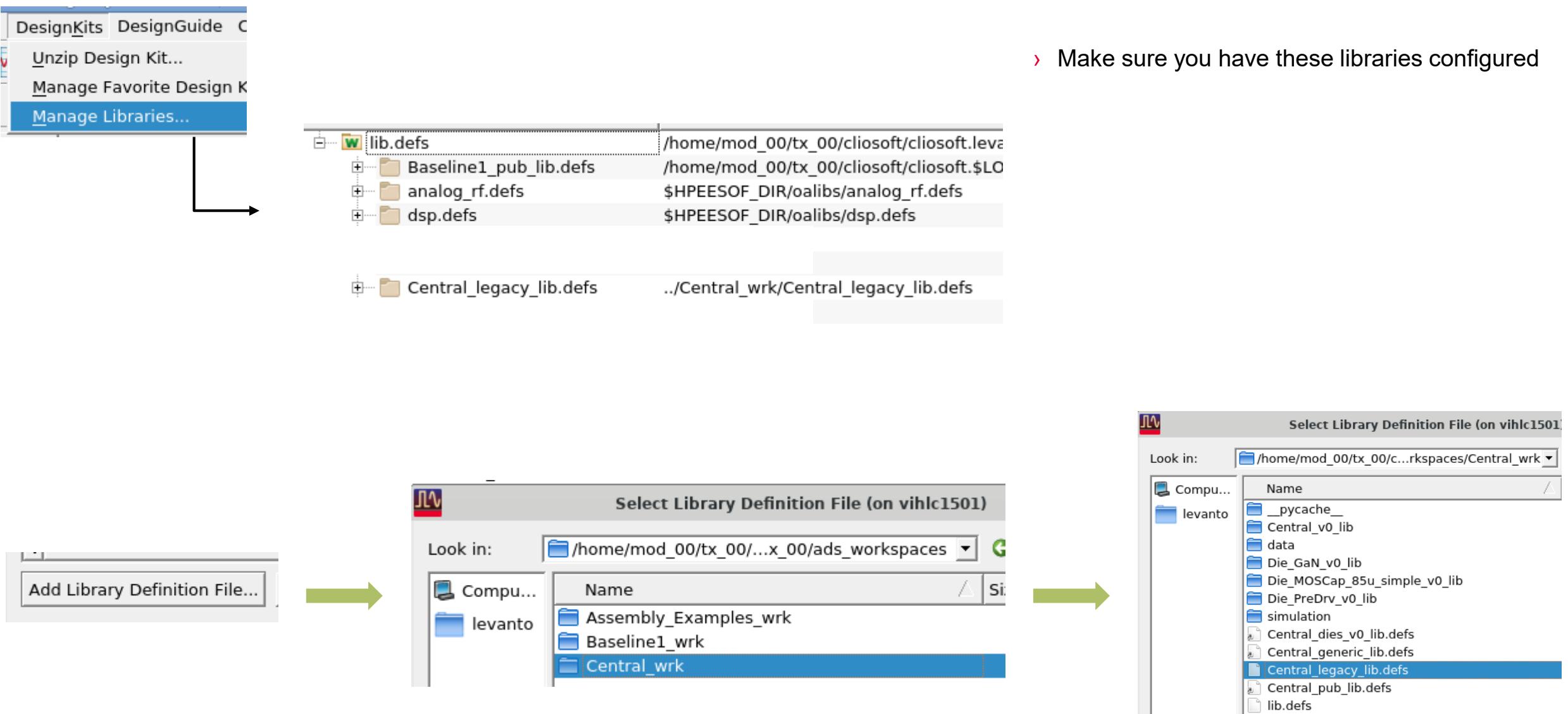
```
levanto@vihlc1767[ads_workspaces/Baseline1_wrk] ads -h
usage: ads [-h] [-v VERSION] [-sos] [-hp] [-ncpu NCPUs] [-ram RAM]

Camino ADS Wrapper

optional arguments:
  -h, --help            show this help message and exit
  -v VERSION, --version VERSION
                        specify ads version. Example: ads -v 2020
  -sos, --update_sos   use this switch to update sos before running ads
  -hp                  option to send ADS to high performance machine. Use
                      with caution
  -ncpu NCPUs          specify number of cores for ADS
  -ram RAM             specify memory requirement for this ADS Session
```



# Add libraries to workspace



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# Resources

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- › Main Minipac activity share folder: [Mini Pac](#)
- › Variants (DOEs) reference: [Excel table](#)
- › Reference catalog for GaN and MOSCap selection: [RFP\\_tech\\_product catalog -PL55.xlsx](#)
- › Reference DRC folder (use for design): [Rgb assy design rule](#)
  
- › Quick check list
  - Keep the Excel up to date.
  - Designer shall complete the design fields properly (ex. MOScap value), in case of doubt raise the question in our Team Meeting.
  - Designer should set the status of the design as **Done** when:
    - Design is checked-in in ADS library
    - Excel file is updated
  - **Communicate by email to others when design is done**

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# ADS libraries overview

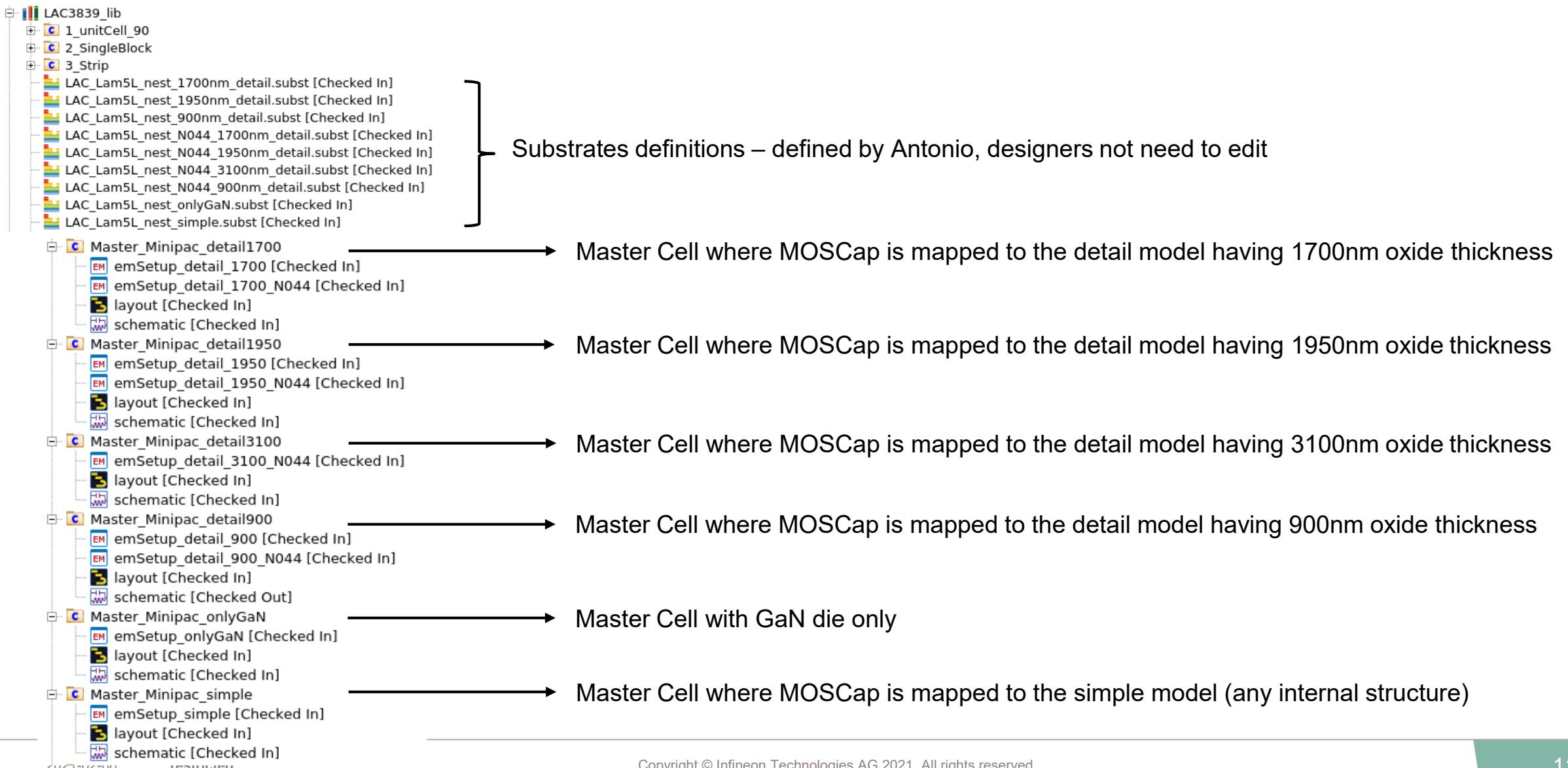
- › **PLP3839\_lib** → library for 2-layers laminate Leiterplatten Hoffmann variant design
- › **LAC3839\_lib** → library for 5-layers laminate ACCESS variant design
  
- › **Central\_v0\_lib** (Read-Only) → contains **RF GaN** and **MOScap** layouts mapped to laminate PDK layerstack for [assembly drawing](#) only
  - Additional MOScap layouts need to be newly created
- › **Die\_GaN\_v0\_lib** (Read-Only) → contains the layouts for **RF GaN** with its own layerstack and its simplified substrate for [design and em simulation](#)
  - If not available, additional RF GaN layouts with em setup and ports need to be newly created
- › **IC\_LD8C\_lib** (Read-Only) → contains the layouts for **MOSCap** with its own layerstack and its simplified substrate for [design and em simulation](#)
  - If not available, additional MOSCap layouts with em setup and ports need to be newly created
  
- › **LF0004\_lib** → master library containing the **LF0004** cell used for PLP3839 2-layers laminate layout only (not for substrate)
- › Master laminate layout for LAC3839 is not a library but a cell in the LAC3839\_lib called **1\_unitCell\_90**
  
- › [Read-Only Libraries](#) overview:
  - **IFX\_RFGaN\_C1\_v1p4p0\_lib** → IFX library for RF GaN schematic only (linked to "freeman\_legacy")
  - **IC\_GaN\_S\_lib** → different RF GaN layouts and schematic for [em simulation](#) (linked to "freeman\_legacy")) + several substrates
  - **ART\_IC\_N\*\_lib** → IFX library for MOScap layout + link to substrate in library IFX\_LD8C50R\_IPD\_v0\_tech
  - **IC\_LD8C\_lib** → different MOScap layout, schematic and EM setup + several substrates

# Libraries summary for Design & Assembly Drawing

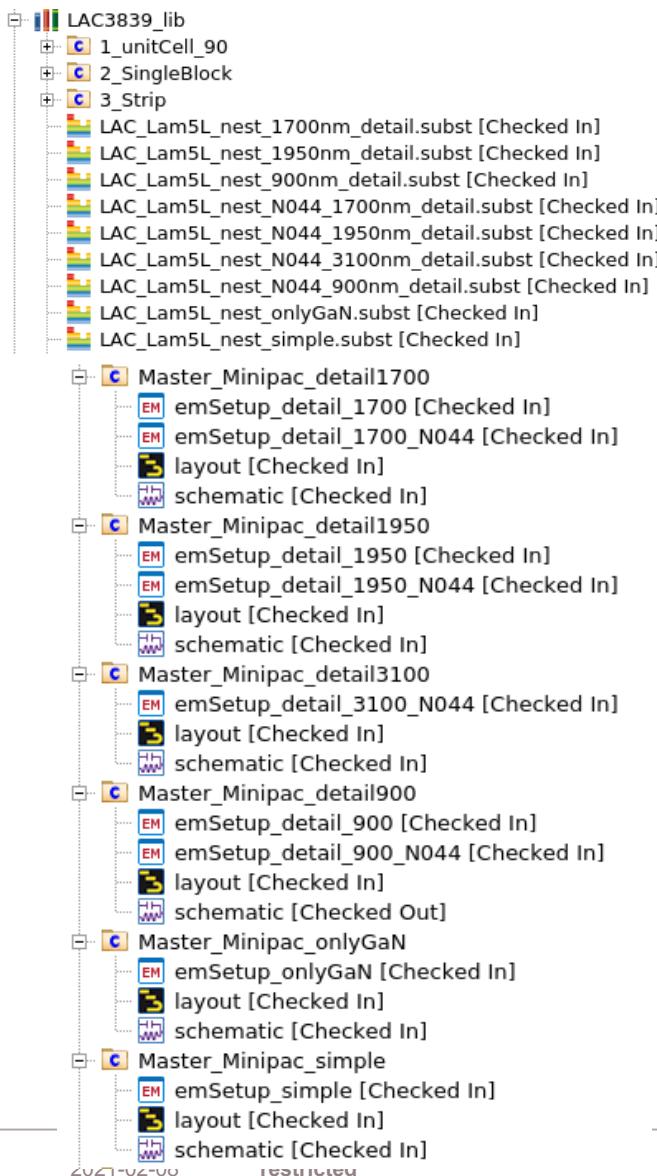
	GaN	MOSCap
Design	Die_GaN_v0_lib	IC_LD8C_lib
Assembly drawing		Central_v0_lib

- › If any layout is missing then it needs to be created, please notify Antonio.

# LAC3839\_lib master structure



# Workflow



1. Copy/paste the entire cell and rename it
  - You will have to rename at the end of the design according to the Excel file naming convention once GaN and MOScap are fixed
2. "schematic" view shall not be renamed -> used to define BW profiles
3. emSetup views are pre-configured for a quicker design
4. Do your design plus DRC check.
5. Once design is completed, copy/paste your layout in the same cell and rename **layout\_Assy** which will be used to generate the assembly drawing.
6. Update Excel file and notify the other colleagues (for design review and assembly drawing generation)
7. *Dimension Lines* will be added by Jorge Teixeira after assembly drawing delivery and before providing to RGB for assembly.



Part of your life. Part of tomorrow.