Behavioral Modeling of GaN FETs: A Load-Line Approach

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***Abstract*—In this paper, a new model formulation is presented that correctly accounts for low-frequency dispersion (i.e., trapping and thermal phenomena) affecting field-effect transistors (FETs). In particular, for the first time a behavioral description is applied only to the intrinsic current generator, enabling the correct measurement-based evaluation of the intrinsic device operation. The model, which is by construction technology independent, has been extensively validated considering a GaN FET. This choice is justified by the large interest around this technology and by the presence of dispersion effects that must be accurately accounted for.**

***Index Terms*—Field-effect transistors (FETs), GaN transistors, microwave amplifiers, nonlinear circuits, nonlinear distortion, semiconductor device modeling.**

I. Introduction

OVER THE last years, a growing interest has been manifested by the microwave community toward behavioral modeling of transistors [1]–[4] despite the wide adoption of traditional compact modeling [5]–[9]. It should be pointed out that behavioral modeling at circuit level has ancient roots [10]–[14] due to the intrinsic advantages related to such a kind of approach in terms of simulation time and convergence robustness. Nevertheless, at transistor level the aforementioned advantages are not so evident. The reason is quite intuitive: behavioral models, in their more common definition, are essentially measurement datasets, and, as a consequence, they work well when the device-under-test (DUT) actual operation can be exhaustively investigated and stored. With the aim of clarifying this aspect, a simple example is represented by the comparison between the admissible load conditions for a power amplifier (PA) and a transistor. PAs are typically designed for working under matching condition, so a characterization under nearly matched operation can be considered exhaustive, whereas for a transistor the loading conditions, both at the fundamental and harmonics, should cover the entire Smith chart to be actually exhaustive [15], [16]. This consideration also impacts the cost of the instrumentation required to extract the model. As a matter of fact, for the transistor case, two multi-harmonic tuners are needed for properly varying the source and load conditions. Also when X-parameters are considered, when the principle of harmonic superposition is applicable, at least two tuners working at the fundamental frequency are necessary for ensuring proper power transfer and for varying the load condition [17]. Therefore, cost and frequency limitations of large-signal setups strongly influence the spread of behavioral transistor models limiting their potential advantages.

Another negative facet related to behavioral models is that circuit designers need to engineer transistor waveforms at the current generator plane (CGP), as all the design methodologies refer to this reference plane [15], [16], [18]. Undeniably, looking at the extrinsic waveforms gives a clear indication about the achievable device performance (e.g., output power, power gain, power-added efficiency (PAE), etc.), nevertheless no information can be deduced about the transistor class of operation since the extrinsic model waveforms are not linkable to any design technique. Moreover, the lack of information at the intrinsic plane (IP) also implies poor scaling capabilities: in fact, parasitic elements, differently from the intrinsic ones, do not scale easily and directly with periphery [19]–[21]. As a consequence, scalable behavioral models require the identification of a suitable description for the extrinsic parasitic network [22], [23] which de facto sounds like a *back to the future* (i.e., compact models).

In conclusion, instrumentation cost and frequency limitation and the missing link with design techniques make behavioral models less attractive than the compact ones.

In this paper, a new transistor model is presented that combines the main advantages of compact and behavioral approaches. The proposed formulation exploits a behavioral description for the intrinsic current generator and a compact description for both the nonlinear capacitances and extrinsic parasitic elements. In this way, by using only general-purpose instrumentation, it is possible to overcome frequency and cost limitations related to microwave nonlinear setups. Moreover, the access to the CGP is preserved, as for any compact model, and, as a consequence, also the link with design techniques.

This paper is organized as follows. Section II briefly reviews the physics of trapping effects in transistors. Section III describes the theoretical model formulation. In Section IV, the model implementation in the computer-aided design (CAD) environment is dealt with. Section V reports the measurement-based procedure for constructing the behavioral model. In Section VI, the model accuracy is evaluated by comparing experimental data with simulation results. Finally, conclusions are drawn in Section VII.

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II. Trapping Phenomena in field-effect transistors (FETs)

When dealing with new transistor technologies, the problem of accurately modeling low-frequency (LF) dispersion is immediately apparent. As a matter of fact, GaN is following the GaAs steps: formulations proposed for GaAs transistors (e.g., [24]) have been used for GaN HEMTs (e.g., [9]), leading to good prediction capability. Nevertheless, LF dispersion in GaN transistors has undeniably posed complex challenges. In order to clarify this aspect, it is convenient to briefly review the fundamentals of trapping phenomena.

In numerical simulation, the Shockley–Read–Hall formulation [25], [26] is included in the continuity equations for assessing the behavior of traps inside the material [27]–[29]. These equations provide a useful insight into the physics of capture and emission phenomena. In (1) and (2), the formulas that describe the capture and emission rates (cr and er, respectively) for electrons (n) and holes (p) are reported

$$\begin{aligned} cr_{n,p} &= d_{n,p}\left\{N_t h_{n,p}\left(E_t\right)\right\}\left(v_{\rm th}\sigma_{n,p}\right) \\ er_{n,p} &= \left[N_t\left(1-h_{n,p}\left(E_t\right)\right)\right]e_{n,p} \end{aligned} \tag{1}$$

where $d_{n,p}$ is the free-carrier density, N_t is the trapping state density, E_t is the trap energy level, $h_{n,p}$ represents the probability (in the most general case of nonequilibrium condition) that traps are empty (n) or occupied by electrons (p), $v_{\rm th}$ is the thermal velocity (which is here assumed equal for electrons and holes for simplicity), $\sigma_{n,p}$ is the capture cross section, and $e_{n,p}$ is the emission probability, which can be expressed as

$$e_{n,p} = v_{\rm th}\sigma_{n,p}n_i{\rm e}^{\left(\pm\frac{E_t-E_i}{kT}\right)} = C_{n,p}T^2{\rm e}^{\left(\pm\frac{E_t-E_{n,p}}{kT}\right)}. \tag{2}$$

In (2), n_i is the intrinsic carrier concentration, T represents the semiconductor temperature, E_i is the intrinsic Fermi level, $C_{n,p}$ is a constant, $E_{n,p}$ is the lower edge of the conduction band (n) or the top edge of the valence band (p), and the sign of the exponential argument is positive in the n case and negative otherwise.

Finally, the net recombination rate through a recombination center can be expressed as

$$\begin{aligned} U &= cr_n - er_n \\ &= cr_p - er_p \\ &= \frac{N_t v_{\rm th}(d_n d_p - n_i^2)}{f(\sigma_{n,p}, d_{n,p}, E_t, E_i, n_i, T)} \end{aligned} \tag{3}$$

where f is a nonlinear function [26].

Equation (1) clearly evidences that emission and capture phenomena behave differently. More precisely, in the cr expression the free-carrier density is present, whereas the intrinsic carrier concentration appears in the er expression. This is a clear sign that the time constants associated with the two phenomena are different. As an example, focusing on an n-type semiconductor $(d_n \gg n_i)$, in the particular case in which $E_t = E_i$, it is possible to further simplify (2) obtaining

$$\frac{cr_n}{er_n} = \left(\frac{h_n\left(E_t\right)}{1-h_n\left(E_t\right)}\right)\frac{d_n}{n_i} \tag{4}$$

which indicates that the electron capture rate could be orders of magnitude faster, and as a consequence, the associate time constants could be orders of magnitude shorter.

Equations (1) and (2) explicitly point out another fundamental aspect of the trapping phenomena, i.e., their dependence on the device thermal state. Focusing on the emission probability (2), it can be noticed, besides the temperature square, that the temperature is present in the exponential argument. Such exponential dependence gives a clear idea of the problem complexity: temperature variation induces a similar effect of moving the trap-state energy level (E_t) in the energy gap [29]–[31]. The strong influence of the thermal state on the trap-occupation state is typically disregarded in model formulations oriented to CAD analysis; nevertheless this approximation is considered as one of the major limitation to the accuracy of advanced FET models (e.g., [32]).

Equation (3) reveals another level of complexity: the net recombination rate is controlled by the disequilibrium term $(d_n d_p - n_i^2)$ that, in typical FET applications, depends on the selected nonlinear dynamic operation. Reasoning on the gate Schottky junction, under dc operation the voltage across the junction defines the extension of the space-charge region, and as a consequence, the profile of the disequilibrium term into the material. The extension of this concept to the nonlinear dynamic case is quite intuitive: the profile is dynamically modulated by the voltage applied to the junction, which in FET operation means by the intrinsic gate–source and gate–drain voltages, or, equivalently, by the gate–source and drain–source voltages. Such a consideration, associated with the previous discussion on time constants, has induced to propose a dependence of the trap occupation state on the average values of the intrinsic voltages [9], [24], [33] and some authors have also hypothesized a dependence on the peak value of the voltages [32], [34]. In fact, the peak values, negative for the gate voltage and positive for the drain one, define the maximum extension of the depletion region beneath the gate, and as a consequence, a *limit* condition for carriers that, once captured, are not able to break free due to the slower time constants related to the emission mechanisms. Nevertheless, from our discussion, the above mentioned dependencies still remain a first order approximation. In fact, due to the temperature influence, the trap occupation state is accurately defined only by considering both the actual electrical and thermal regimes of the device.

III. Proposed Formulation

The theoretical analysis carried out in the previous section has indicated that different time constants are associated with trapping effects. In particular, the available experimental evidence shows that they can be slow (second and millisecond order [31]) or very fast (nanosecond order [32], [34], [35]). It is worth noticing that, if the model is oriented to predict at microwave frequencies the transistor continuous-wave (CW) response (i.e., it is not of interest to model the transistor response under pulsed operation [36]), under a few megahertz operation the full influence of slow and fast trapping effects can be gathered. In particular, while the possibility of catching the slow phenomena has been largely demonstrated [9], [24], [33], it is

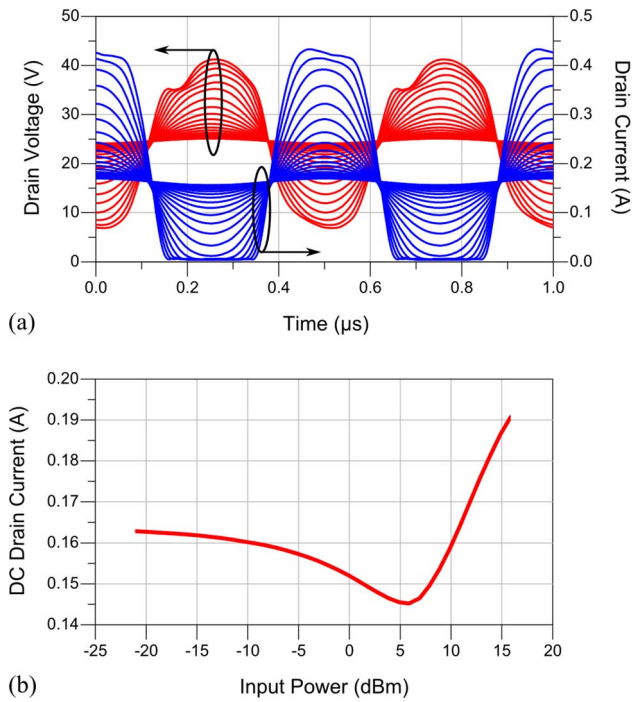

Fig. 1. Measured (a) time-domain drain current and voltage waveforms and (b) average drain current versus input power for a $0.25 \times 600\ \mu\text{m}^2$ GaN HEMT biased in $V_{d,0} = 25$ V, $I_{d,0} = 165$ mA. The load impedance is 75 Ω and the fundamental frequency is 2 MHz.

of interest to investigate the fast trapping effects. It must be observed that, even assuming valid the hypothesis of dependence on the peak gate and drain voltages [32], [34], it is sufficient to reproduce at LF the same operating conditions, in terms of instantaneous gate and drain voltages at the intrinsic-device active area (i.e., the same electric-field profile), for obtaining an accurate characterization of the transistor. Intuitively, once the electrons have been captured, since the emission mechanism is very slow, they remain *frozen* in that particular state at 2 MHz as at 10 GHz. In order to justify this assumption, Fig. 1 shows a power sweep carried out at the fundamental frequency of 2 MHz on a $0.25 \times 600\ \mu\text{m}^2$ GaN HEMT biased in $V_{d,0} = 25$ V, $I_{d,0} = 165$ mA. The drop of the average value of the drain current is well evident. Such a behavior is emphasized in [32] and [34] as the most important experimental evidence of fast trapping phenomena in GaN FETs.

On the basis of the previous considerations, above the cutoff of slow trapping effects, the currents of the transistor at the IP can be expressed in the most general form by

$$\begin{bmatrix} i_g \\ i_d \end{bmatrix} = \begin{bmatrix} f_g\left(v_g, v_d, X_{\Theta,0}, X_{T,0}\right) \\ f_d\left(v_g, v_d, X_{\Theta,0}, X_{T,0}\right) \end{bmatrix} \tag{5}$$

where i_g and i_d are the instantaneous currents at the Schottky junction and at the current generator, respectively, v_g and v_d are the instantaneous values of the voltages at the intrinsic device, and $X_{\Theta,0}$ and $X_{T,0}$ are state variables describing the frozen states of thermal and trapping effects. In particular, since the case temperature (T_c) and the intrinsic voltages completely define the electric and thermal state of the device, $X_{\Theta,0}$ and $X_{T,0}$ can be expressed, without introducing any approximation, as nonlinear functions of the voltage phasors and T_c:

$$\begin{bmatrix} X_{\Theta,0} \\ X_{T,0} \end{bmatrix} = \begin{bmatrix} h_\Theta\left(T_c, V_{g,0}, V_{g,1}, \ldots, V_{g,n}, V_{d,0}, V_{d,1}, \ldots, V_{d,n}\right) \\ h_T\left(T_c, V_{g,0}, V_{g,1}, \ldots, V_{g,n}, V_{d,0}, V_{d,1}, \ldots, V_{d,n}\right) \end{bmatrix} \tag{6}$$

where n is the practically limited number of the spectral components. As a consequence, the device current can be reformulated as follows:

$$\begin{bmatrix} i_g \\ i_d \end{bmatrix} = \begin{bmatrix} p_g\left(T_c, V_{g,0}, V_{g,1}, \ldots, V_{g,n}, V_{d,0}, V_{d,1}, \ldots, V_{d,n}\right) \\ p_d\left(T_c, V_{g,0}, V_{g,1}, \ldots, V_{g,n}, V_{d,0}, V_{d,1}, \ldots, V_{d,n}\right) \end{bmatrix} \tag{7}$$

where the explicit dependence on v_g and v_d has been removed since the instantaneous voltages can be conveniently expressed in terms of their phasors. In the particular case where the case temperature and the bias condition $(V_{g,0}, V_{d,0})$ are fixed, the expressions reduce to

$$\begin{bmatrix} i_g \\ i_d \end{bmatrix} = \begin{bmatrix} q_g\left(V_{g,1}, \ldots, V_{g,n}, V_{d,1}, \ldots, V_{d,n}\right) \\ q_d\left(V_{g,1}, \ldots, V_{g,n}, V_{d,1}, \ldots, V_{d,n}\right) \end{bmatrix}. \tag{8}$$

The number of voltage harmonics to be controlled in (8) depends on the specific application. Nevertheless, when the transistor is used at its proper operating frequencies, there is an intrinsic shorting effect at harmonic frequencies due to the transistor capacitances. As a consequence, when harmonic tuning is not involved, controlling the voltage phasors only at the fundamental frequency in (8) is adequate to guarantee a high level of accuracy. This is an important feature of the proposed approach with respect to the existing ones. In addition, when harmonic tuning has to be performed, the principle of harmonic superposition [17] could be applied to (7) and (8). Such a choice could represent a good solution to limit the amount of data and measurement time. Nevertheless, when the harmonic superposition is not applicable, i.e., the number of voltage harmonics to be controlled in (7) and (8), and consequently, the complexity of constitutive model equations increase, the proposed modeling approach still provides a great advantage with respect to the existing behavioral models. In fact, by performing measurements at few megahertz, it is possible to control up to 60 harmonics, by exploiting a low-cost arbitrary function generator, without the need of expensive harmonic tuners.

Equation (8) accurately describes the behavior of the transistor intrinsic current generator. In order to account for linear and nonlinear reactive elements, it is required to identify a suitable description for the parasitic network [19]–[21] and for the intrinsic nonlinear capacitances [5]–[9]. Both these models can be conveniently identified on the basis of conventional S-parameter measurements.

IV. Model Implementation in CAD Environment

The model topology is reported in Fig. 2. In particular, for the linear parasitic network we chose a lumped component structure, where each element has been identified by using standard S-parameter measurements [19], [20]. The description of the

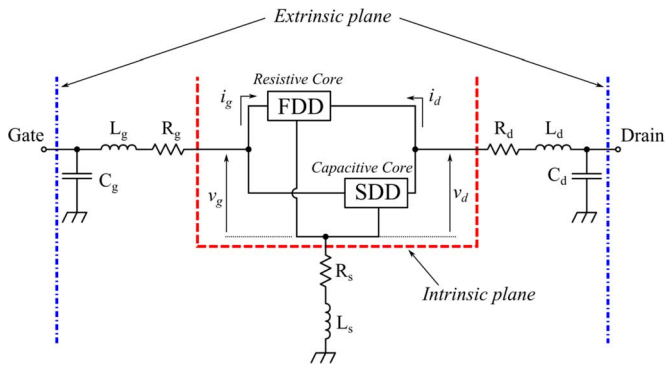

Fig. 2. Topology of the proposed model.

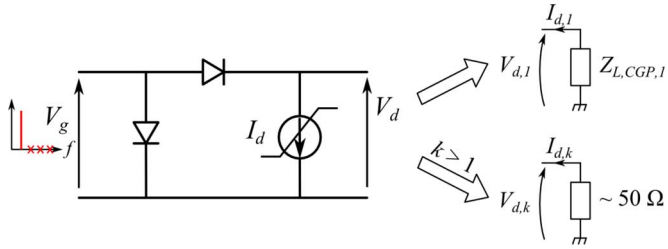

Fig. 3. Approximations related to the resistive core behavior in the considered operation. $Z_{L,\mathrm{CGP},1}$ is the load at the fundamental frequency.

TABLE I
0.25-μm GaN HEMT TECHNOLOGY SPECIFICATIONS

Quantity	*Value*
Breakdown Voltage	-70 V
Pinch-off Voltage	-3 V
I_{dss}	700 mA/mm
Saturated Output Power	5 W/mm

nonlinear capacitances (i.e., the capacitive core) has been implemented, following a quasi-static approach, with lookup tables (LUTs) wherein the intrinsic capacitance values are stored. Bias-dependent capacitance values were calculated by using intrinsic multi-bias Y-parameters [33]. A symbolically defined device (SDD), which allows to define a nonlinear element by using a time-domain formulation, has been used for its implementation. Different implementations could be adopted for parasitic elements and transistor capacitances. For example, a distributed description of the access structures of the device resulting from an electromagnetic simulation might be exploited [21] instead of the lumped solution for the parasitic network, whereas the capacitive core could be implemented by using an analytical formulation [5].

The implementation of the currents, i_g and i_d in Fig. 2, deserves a deeper discussion, bearing in mind that our purpose is to define a relationship as expressed in (8). In Fig. 2, these currents have been associated with the *resistive core* that represents the strictly-algebraic part of the intrinsic device [18]. On the gate side, the current can be described by a conventional formulation of the Schottky junction [26] or by a LUT approach as the one that will be detailed in the following for the drain current. With the aim of preserving a high level of computational efficiency, we chose the first approach. On the drain side, the nonlinearity of the current generator produces voltage harmonic components. However, if no harmonic tuning is needed at microwave frequencies, due to the shorting effect of the capacitances at the harmonic components, the resistive drain current is mainly defined by the load termination at its reference plane at the fundamental frequency. Under this hypothesis, the behavior of the current generator (i.e., the current phasors) can be described, in the space of load impedances, characterizing the dependence on the voltage phasors only at the fundamental frequency. This greatly simplifies the model identification phase since the harmonic terminations can be set to the system characteristic impedance (i.e., 50 Ω), the influence of their variation on the transistor response being negligible. A schematic representation is shown in Fig. 3.

For the implementation of the current generator model, a LUT approach was adopted. Due to the choices previously discussed, the use of a two-port frequency-domain defined device (FDD) is suitable, and each current harmonic component is defined as the value read from the LUT corresponding to the actual intrinsic voltage phasors $V_{g,1}$ and $V_{d,1}$. It is important to point out that the number of the current harmonic components n available in the LUT plays an important role in the FDD definition of the resistive core. Indeed, it is not possible to use the model for harmonic-balance analyses where a number of harmonics greater than n is needed. Anyway, as previously discussed, this does not represent a big issue: because of the LF operation, an exhaustive number of current harmonics can be gathered without any additional cost and complexity of the adopted setup [37].

The description of the model structure that has been given so far is actually technology independent. However, to prove its capabilities and verify its limitations, in this work we focused on a 0.25×600 μm^2 GaN on SiC HEMT since modeling GaN transistors still represents an important challenge. The main foundry specifications for this technology are summarized in Table I.

V. MEASUREMENT PROCEDURE AND DATA PROCESSING

The characterization of the transistor current generator can be obtained by means of CW measurements carried out at 2 MHz, i.e., in a frequency range where, as discussed, the trap and thermal states of the transistor can be considered *frozen*. Indeed, at megahertz frequencies all the reactive elements of the device (i.e., the intrinsic capacitances and the reactive parasitic elements) can be neglected so it is possible to directly characterize the device resistive core.

The exploited setup is depicted in Fig. 4 [37]. It implements an active load–pull measurement system operating in the frequency range [200 kHz–240 MHz]. The DUT is excited with drain and gate incident waves generated by an arbitrary function generator whereas its bias point is imposed by a dc source. A PA may be adopted on the drain signal path when high-power devices have to be characterized. Reflected and incident waves, separated by two directional couplers, are acquired by a four-channel oscilloscope and the resulting data are post-processed by a mathematical procedure to obtain all the electrical quantities at the DUT plane. In the frequency range of operation, all the measurement setup components satisfy linear nondistortion

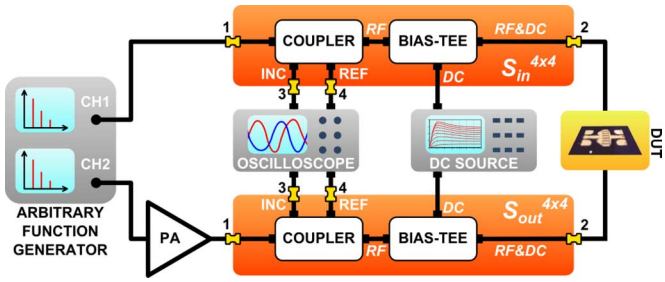

Fig. 4. LF large-signal measurement setup exploited for the acquisition of the data needed for the implementation of the proposed model.

conditions. This greatly simplifies the setup calibration procedure, which practically consists in the experimental characterization of the two four-port networks ($S_{\text{in}}^{4\times4}$ and $S_{\text{out}}^{4\times4}$) shown in Fig. 4.

Such a setup can be used to synthesize a specific load condition at the CGP at both the fundamental frequency and harmonics [38] by properly tuning the incident waves at the gate and drain ports. For example, if just the fundamental impedance ($Z_{L,\text{CGP},1}$) has to be controlled, three variables must be identified for each impedance value: the amplitudes of the incident waves at the DUT gate port, $|A_{g,1}|$, and drain port, $|A_{d,1}|$, and their relative phase, φ.

In Fig. 5, the GaN HEMT device biased in class AB ($V_{d,0} = 25$ V, $I_{d,0} = 100$ mA) has been characterized at 2 MHz by using this technique for a constant input power (i.e., $|A_{g,1}| = 0.55$ V), whereas both $|A_{d,1}|$ and φ have been swept over a proper set of values. Due to high output power levels that the function generator cannot handle, a 30-W PA has been inserted in the drain path. For $|A_{d,1}|$ that goes to zero, the load impedance degenerates into a value determined by the output impedance of the PA. As shown, increasing the value of $|A_{d,1}|$ moves the load impedance toward the boundary of the Smith chart with a "direction" determined by φ. It is evident how this method allows to synthesize every load condition on the Smith chart. It is noteworthy that, by knowing the resistive parasitic elements of the electron device, their contribution can be easily de-embedded, thus these impedances are actually obtained at the CGP.

In order to apply the proposed model formulation, the behavior of the current generator has to be characterized for a sufficient number of load conditions and for different input power levels. To this aim, a dedicated software to automatize the whole measurement procedure has been developed. In Fig. 6, the flowchart that describes its operation is reported. Basically, the incident wave variables at the fundamental frequency are swept over a grid of values defined by the user and the corresponding load impedances are synthesized as long as they lie inside the Smith chart. Measured results are stored as vector frequency-domain data for a number of harmonics high enough to minimize the loss of information (in the present case, 11 spectral components were gathered, including the dc).

Each set of measurement data is acquired by keeping the bias point constant, thus the associated model can be exploited for simulation at the same bias point only. If a multi-bias model is needed, the same procedure can be repeated for each bias condition of interest, thus increasing the dimension of the final LUT.

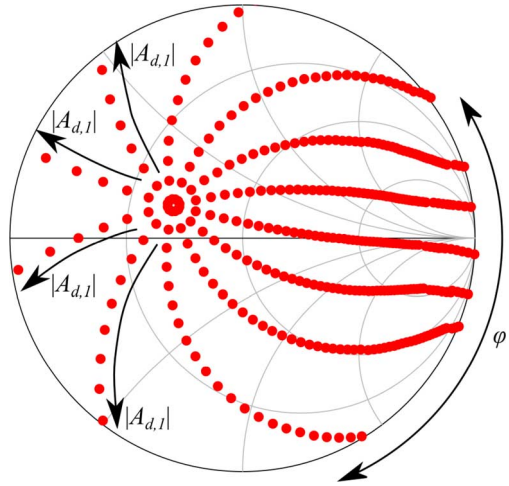

Fig. 5. Example of load impedances synthesized by means of the LF measurement setup. $0 \le \varphi \le 330°$ step 30°, $0.4\ V \le |A_{d,1}| \le |A_{d,1}|^{\max}$, where $|A_{d,1}|^{\max}$ is the maximum value of $|A_{d,1}|$ for which the synthesized impedance lies inside the Smith chart.

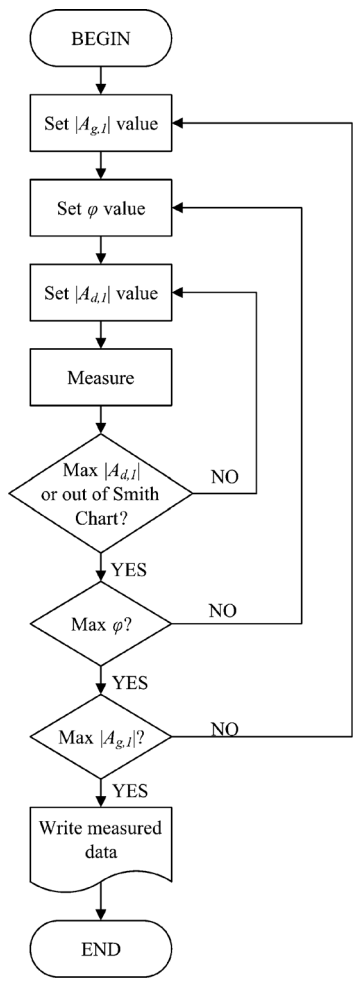

Fig. 6. Flowchart of the measurement procedure implemented to control the LF measurement setup.

Since no additional complexity is introduced from a practical point of view, this eventuality will not be discussed hereafter.

After the LF data related to the current generator model have been collected, they must be processed to define the model in the

CAD environment, i.e., Agilent Technologies' Advanced Design System (ADS). This data processing is strictly related to the model topology and implementation described in Section IV. In particular, the following two operations are needed.

- Collected data have to be redefined as a function of the gate and drain voltage phasors at the IP at the fundamental frequency, i.e., $V_{g,1}$ and $V_{d,1}$.
- Measurement data have to be *extended* with respect to the measured domain.

Each of these steps will be described in the following.

A. Domain Redefinition

According to (8), the current generator model implemented as an FDD needs to be defined with relationships where the voltage phasors at its ports are directly coupled with the corresponding current values. Unfortunately, this is not a straightforward operation because the data achieved with the LF measurements are expressed as dependent on incident wave parameters, i.e., $|A_{g,1}|$, $|A_{d,1}|$, and φ. For this reason, measured data must be redefined by using the voltage phasors as independent variables. The whole operation is even more complicated since the measured voltage phasors at the fundamental frequency do not constitute a rectangular grid in the complex plane because of the measurement procedure itself. As a matter of fact, while the intrinsic gate voltage phasor $V_{g,1}$ remains constant for each input power level (i.e., $|A_{g,1}|$) because, at LF, the gate port of the DUT is equivalent to an open circuit as long as the Schottky junction conduction is prevented, different drain voltage phasors at the fundamental frequency are available because of the different loads that have been synthesized. In Fig. 7, an example for some values of $|V_{g,1}|$ is depicted. It is evident that the measured grids are not suitable for a regular LUT. To solve this problem, an interpolation procedure must be applied. First, the phase of $V_{g,1}$ has been assumed as reference. This operation reduces the information related to $V_{g,1}$, which is stored in the LUT as the first independent variable, at just its magnitude. The second independent variable, $V_{d,1}$, is a complex number, so it has to be split into its real and imaginary parts. Another solution would be to use its magnitude and phase, but it was intentionally excluded because of the continuity issue that affects, by definition, the argument of a complex number.

According to this choice, a new rectangular grid was defined within the whole measured space. To this end, another detail has to be taken into account. For low values of $|V_{g,1}|$, the measured values of $V_{d,1}$ lie inside a small area of the polar plane, i.e., approximately the gray area reported in Fig. 7(a). Thus, a large number of points are *squeezed* inside a small area, resulting very close to each other if compared to the ones obtained for higher values of $|V_{g,1}|$. To avoid a loss of information and guarantee robust convergence capability at low levels of input power, the new grid has to be dense in this area. However, keeping such a large density for higher power levels would lead to a huge number of entries in the LUT, which directly affects its dimension. To keep the latter limited, the step of the grid was adjusted along the axes by using a quadratic rule. The resulting grid is reported in Fig. 7(b). The interpolation was performed over this grid for each level of $|V_{g,1}|$ separately, by using standard procedures (i.e., *triScatteredInterp* [39]) available in the commercial software MATLAB. The result of the interpolation was a regular grid in the new voltage phasor domain. In the extrapolated region, the data need to be further processed according to the following step.

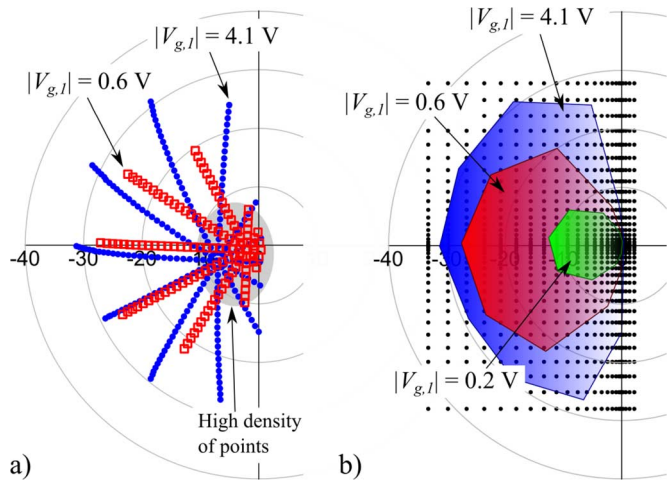

Fig. 7. (a) Measured drain voltage phasors at the fundamental frequency and (b) domain for different amplitudes of the gate voltage phasor at the fundamental frequency. The new grid of the drain voltage phasors for interpolation is shown in black dots in (b).

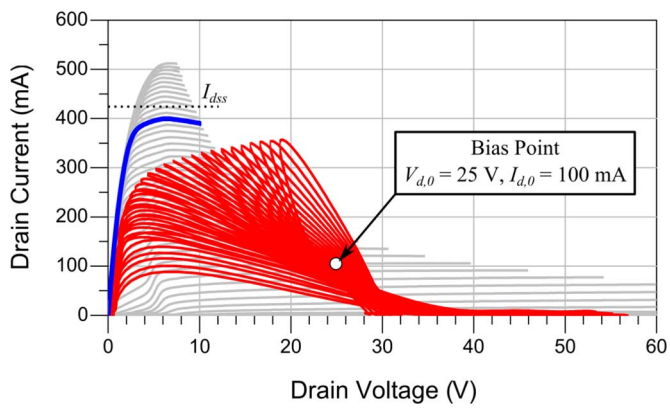

Fig. 8. Example of the load lines synthesized during the LF characterization. The bias point is indicated with a white filled dot, whereas the load lines are shown via the red solid line (in online version). In the background, the dc *I/V* characteristics are depicted and the dc characteristic for $V_{g,0} = -0.2$ V is highlighted with a thick solid line.

B. Data Extension

The choice of the interpolation grid depicted in Fig. 7(b) shows that many points are outside the measured domain, especially for the lowest levels of $|V_{g,1}|$. Obviously, the corresponding current phasors cannot be obtained through interpolation, as no measurement is available. The interpolator returns an invalid numerical value for them, such as NaN (not a number), which is not correctly managed by the simulator. To avoid this problem, an extrapolation procedure has been adopted. For each value of $|V_{g,1}|$, the current phasors outside the measured domain were determined by using suitable routines (i.e., the curve-fitting function *fit* with biharmonic surface interpolation [40]) available in MATLAB. At the end of this procedure, the LUT is suitable for implementing the model of the current generator in the CAD software.

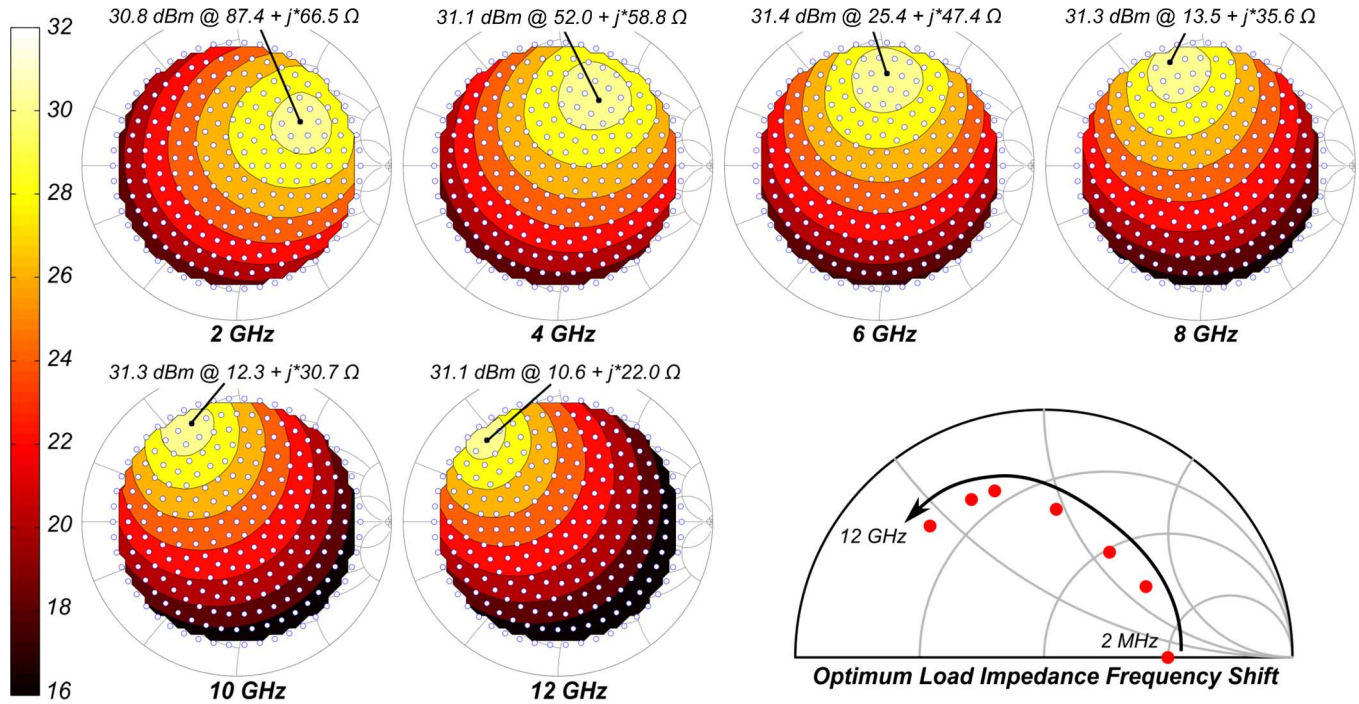

Fig. 9. Simulated output power load–pull contours for 2 dB of gain compression at different frequencies within 2 and 12 GHz. The power difference between the contour curves is 2 dB. The shift of the predicted optimum impedance versus frequency is pointed out. The optimum impedance obtained at low frequency (i.e., 2 MHz) is also shown.

It is worth noticing that the extrapolation of the measured grid is only functional to the model implementation in a CAD environment. In fact, all the operating conditions of interest for the current generator need to be defined in the model LUT by measured or interpolated data.

VI. Experimental Results

A. Model Convergence Capability

According to (8), the intrinsic current generator model has been implemented as an FDD. As well known, the main problems for a LUT-based model in nonlinear analysis are convergence robustness and simulation time. To assess the capabilities of the proposed large-signal behavioral model, it has been implemented for a 0.25×600 μm^2 GaN HEMT under the bias condition $V_{g,0} = -2.2$ V, $V_{d,0} = 25$ V, and $I_{d,0} = 100$ mA ($\approx I_{dss}/4$). First of all, according to the model topology shown in Fig. 2, the device has been characterized in terms of its dc *I/V* characteristics and multi-bias S-parameters up to 40 GHz for modeling the parasitic network and the capacitive core.

The DUT has then been characterized at LF, i.e., 2 MHz, by exploiting the measurement setup described in Section V for input power levels corresponding to different values of $|A_{g,1}|$ between 0.05–2.05 V. A constant step of 0.25 V was considered initially. However, between $|A_{g,1}| = 0.05$ V and $|A_{g,1}| = 0.3$ V, the device behavior changes a lot in terms of output power because of the high LF gain. Thus, for the lower input power levels, a finer step of 0.05 V has been used. The final LUT contains data for 13 input power levels, i.e., 13 levels of $|V_{g,1}|$, which correspond to 19×29 points, respectively, for the real and the imaginary part of $V_{d,1}$ and 11 harmonics, including the dc component, for a total dataset size of about 2.1 MB.

Fig. 8 shows some synthesized load lines. They were measured for a constant value of both $|A_{g,1}|$ and φ, whereas the amplitude of the drain incident wave has been swept. For each load line, the gate voltage is a sinusoidal wave with an amplitude of 2 V at the DUT plane that reaches, at its maximum, the value of -0.2 V. If we look in Fig. 8 at the dc characteristic for $V_{g,0} = -0.2$ V, the effect of dispersive phenomena related to traps and thermal effects on the dynamic behavior of the device is well evident. As deeply discussed in Section II, this behavior, depending on both the thermal and trap occupation state, is very difficult to accurately describe. Nevertheless, the behavioral nature of the proposed model makes such a description simple since it is implemented by directly using the gathered measurements.

To verify the robustness of the model in a nonlinear simulation environment, a large number of operating conditions should be considered. In our case, load–pull simulations were chosen. The model has been tested in a simulation bench created by using Agilent ADS 2008 Update 2. The source impedance was kept constant to 50 Ω, whereas the fundamental load impedance was swept over a grid of 227 values, covering an area of the Smith chart of radius 0.8. Simulations were performed for different operating frequencies from 2 to 12 GHz and no convergence issue has been observed.

Simulation data were analyzed and processed in order to obtain load–pull contours. In Fig. 9, constant output power contours are shown for 2 dB of gain compression for each operating frequency. Their regular shape suggests the model does not produce any discontinuity or numerical problem for the simulator

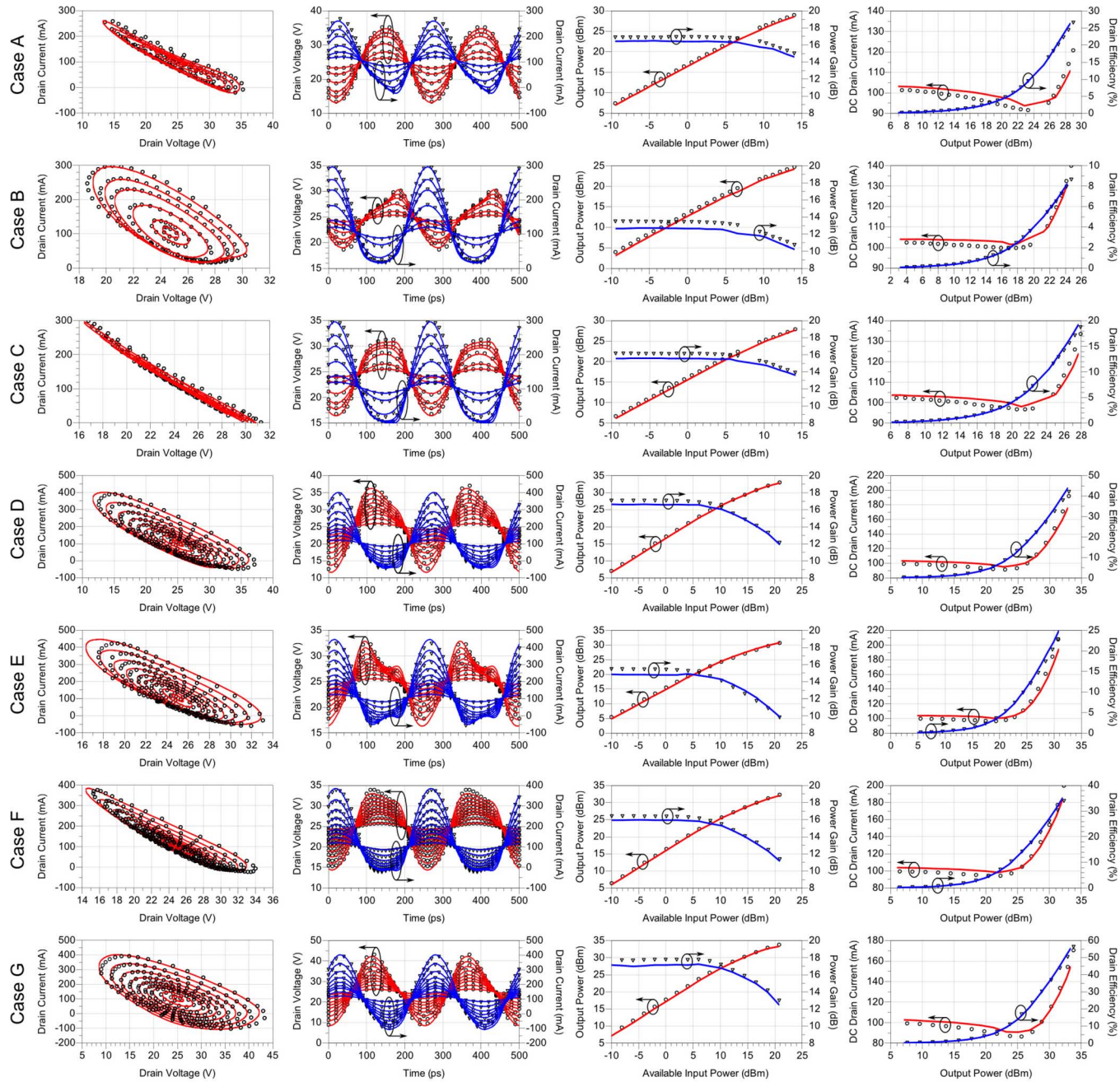

Fig. 10. Comparisons between measurement (symbols) and simulation (solid lines) under large-signal operation at 4 GHz. The bias point is $V_{d,0} = 25$ V and $I_{d,0} = 100$ mA. Fundamental load impedances are: $81.2 + \mathrm{j} * 19.6\ \Omega$ (case A), $25.2 - \mathrm{j} * 24.1\ \Omega$ (case B), $50.0 + \mathrm{j} * 0.0\ \Omega$ (case C), $46.9 + \mathrm{j} * 27.2\ \Omega$ (case D), $24.3 + \mathrm{j} * 15.3\ \Omega$ (case E), $35.0 + \mathrm{j} * 15.6\ \Omega$ (case F), and $46.8 + \mathrm{j} * 48.8\ \Omega$ (case G).

that could be induced by the interpolation over the LUT data. The optimum impedance predicted by the model moves on the Smith chart as function of frequency following a typical trajectory (see Fig. 9). In the figure, the impedance corresponding to the maximum output power at LF (i.e., 2 MHz) for 2 dB of gain compression is also reported for comparison. As expected [16], it lies on the real axis of the Smith chart, which corresponds to a pure resistive impedance.

Regarding the simulation time, it was pretty limited. As an example, at the fundamental frequency of 4 GHz and considering an input power swept between 0–18 dBm with a step of 1 dB, the simulation lasted approximately 140 s on a PC with an Intel Core i7-3770K microprocessor (clock frequency, 3.5 GHz) and 8 GB of DDR3 RAM. Moreover, this simulation time is strongly affected by the LUT implementation of the capacitive core. In practice, for the simulation of the resistive core only, over the same grid of load impedances and for the same number of input power levels, a simulation time of just 16 s was needed.

B. High-Frequency Validation

The model has been validated by exploiting high-frequency measurements performed with a large-signal network analyzer (LSNA) with a total bandwidth of 50 GHz. The device was measured at 4 GHz, and under the same bias condition for which the

model was extracted, different load conditions were synthesized at the fundamental frequency by using a mechanical tuner. Impedances at the harmonic frequencies were not controlled with the aim of validating the proposed approach in the selected operation (i.e., no tuning at harmonics is performed). Moreover, the selected operating frequency has been chosen relatively low in order to test the model in an unfavorable condition for the shorting effect of the intrinsic nonlinear capacitances at the harmonic frequencies. Indeed, being the selected technology oriented to X-band PA design, up to 12 GHz the shorting effect is not yet pronounced.

In Fig. 10, comparisons between model predictions and measurement results are shown. The load impedances cover a set of pretty different values from conditions close to the power matching to strongly mismatched ones. In any case, the model provides a very good fit of the device behavior, in some conditions up to a gain compression level higher than 4 dB.

There is a small difference (fraction of a decibel) between the simulated and measured small-signal gain, whose entity depends on the load impedance value. These discrepancies can be equally attributed to inaccuracy of the model of the intrinsic nonlinear capacitances (extracted by multi-bias S-parameters) and residual uncertainty of the LSNA. As the input power increases, the fitting of the model gets better, overlapping measured data.

The last column in Fig. 10 shows the most interesting results since all the quantities involved (i.e., average value of the drain current, output power, and efficiency) are strictly related to the current generator model. As can be seen, the agreement is excellent. It is important to point out how the shape of the average drain current is well reproduced by the model, including the initial typical drop ascribed in [32] to fast trapping phenomena.

VII. Conclusion

In this paper, an original model formulation for GaN FETs has been proposed. In particular, for the first time a behavioral model has been used for the transistor current generator, adopting a conventional equivalent circuit description for the capacitive core and the parasitic network. Such an approach has the unique feature of merging the benefits of compact descriptions (i.e., correct intrinsic load-line evaluation) and behavioral ones (i.e., characterization of complex phenomena directly by measurements).

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