Scalable Nonlinear FET Model Based on a Distributed Parasitic Network Description

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***Abstract*—Electron device modeling requires accurate descriptions of parasitic passive structures connecting the intrinsic electron device to the external world. In conventional approaches, the parasitic phenomena are described by a network of lumped elements. As an alternative, a distributed description can be conveniently adopted. This choice has been proven very appropriate when dealing with device scaling and very high operating frequencies.**

In this paper, a novel approach to distributed parasitic modeling is adopted for the very first time in association with a nonlinear electron device model. In particular, it is shown how an *equivalent* intrinsic device and a suitably defined distributed parasitic network can be accurately defined and modeled on the basis of standard measurements and easy electromagnetic simulations.

Wide experimental validation based on GaAs pseudomorphic HEMTs is provided, showing accurate prediction capabilities both under small- and large-signal conditions. The proposed model is shown to perform optimally even after periphery scaling.

***Index Terms*—Electromagnetic (EM) analysis, field-effect transistors (FETs), iterative methods, semiconductor device measurements, semiconductor device modeling.**

I. Introduction

MICROWAVE and millimeter-wave communication systems need accurate computer-aided design (CAD) tools in the monolithic microwave integrated circuit (MMIC) design phase. In fact, first-run success and low-cost design constraints are goals only achievable thanks to these tools. In this context, accurate electron device models, which accurately describe the linear and nonlinear behavior up to millimeter-wave frequencies, play a key role. However, full exploitation of a given technology for MMIC design would require the capability of choosing devices with an optimized number and width of fingers. Unfortunately, empirical models usually adopted for circuit design do not explicitly provide a link between technological process parameters (such as the device layout) and the corresponding device electrical response. Conventional modeling approaches based on lumped equivalent circuits may also be inappropriate for the following reasons.

- Distributed effects and coupling phenomena occurring at very high frequencies may strongly affect the transistor performance. Such behavior is not easily described by standard lumped parasitic elements [1]–[3]. Either distributed effects should be taken into account in the device model or rather complicated equivalent circuit structures have to be considered [4]–[18].
- Parameters of lumped equivalent circuits are usually scaled with device size and finger number according to different approaches from very simple linear rules to completely empirical algorithms [19]–[21]. Some of these approaches may not be sufficiently accurate at relatively high operating frequencies, and a large number of measurements on different device structures could be needed in order to obtain a good scalable model. Particular care must be paid in any case to parasitic network modeling and identification.

In this paper, a distributed parasitic network description based on electromagnetic (EM) simulation is adopted and used in conjunction with an empirical nonlinear device model. The proposed approach (see Fig. 1) is based on the partition of the device geometry into a convenient number of elementary intrinsic devices (EIDs) placed along the layout fingers. The EIDs are interconnected by a linear "passive distributed structure," which can be described in terms of a $2N + 2$-port admittance matrix, where N is the total number of EIDs, through accurate EM simulations [14]. Actual device geometries and material stratification, as well as losses in the dielectric and metal electrodes, are taken into account [22].

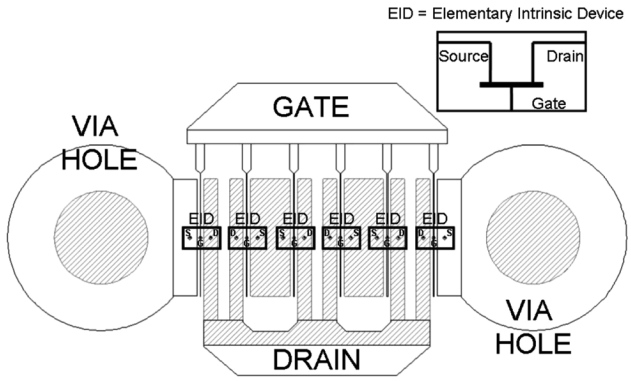

Fig. 1. Device layout example and EM simulator setup using internal ports to define the EIDs.

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Linear distributed electron device modeling has been widely discussed in [14]. Instead, this paper deals with issues related to the exploitation of such a type of approach in the *nonlinear* case. A major problem arising in this context is related to computational efficiency. In fact, it is well known that nonlinear circuit analysis requires iterative evaluations of the model response during harmonic-balance simulations. In the presence of a large number of nonlinear EID models associated with the actual device, dramatic performance worsening, in terms of CPU time and memory occupation required, may occur [23]. This necessarily pushes towards some kind of simplification with respect to a fully distributed approach. In particular, in the following it is shown how the device can be described as an *equivalent* two-port intrinsic nonlinear block connected to a linear *distributed* four-port passive parasitic network.

This kind of *compact* modeling was first introduced in [15], where a preliminary validation under linear multibias conditions was also provided. More extensive validation may be found in [16], where conventional equivalent circuit scalable models are extracted (and compared) on the basis of both distributed and lumped parasitic networks. The linear multibias validation in [16] suggests that the four-port distributed parasitic network description, together with equivalent intrinsic device (EqID) modeling, leads to great improvements in prediction accuracy with respect to conventional approaches, both for reference and scaled devices.

Experimental results clearly prove the validity of the EM-based scalable modeling approach. However, the main assumption of considering *all the EIDs equally fed* could be considered questionable at first sight. In this paper, after briefly recalling the previously presented identification procedure [15] in Section II-A, a completely new and more general procedure is, therefore, proposed in Section II-B. The two different identification procedures are then compared and discussed in Section II-C.

Nonlinear device modeling is dealt with in Section III. In particular, the distributed description of the parasitic network is adopted along with a well known empirical nonlinear model for GaAs-based 0.25-μm pHEMTs. Scalability features of the proposed nonlinear modeling approach are eventually investigated in Section IV.

II. Compact Distributed Parasitic Modeling

The active region of the electron device in Fig. 1 is partitioned in a given number N of two-port EIDs.[1] Every EID is interconnected to each other through a distributed passive $2N+2$-port network, which can be characterized by a admittance matrix $\mathbf{Y}_{\rm EM}$ $[(2N+2)\times(2N+2)]$ obtained on the basis of accurate EM simulations. This accounts for the parasitic effects due to the gate and drain accesses to the active area, along the device fingers and possible transverse couplings between fingers. A schematic representation of this $2N+2$-port parasitic description is shown in Fig. 2, where V_1, V_2, I_1, and I_2 are the phasors of extrinsic gate–source and drain–source voltages and extrinsic gate and drain currents, respectively. Analogously, V_j, V_{j+1} I_j, I_{j+1} $(j=3,5,\ldots,2N+1)$ are the phasors of the EID voltages and currents.

[1]A single EID per finger has been considered for instance in [17], [18].

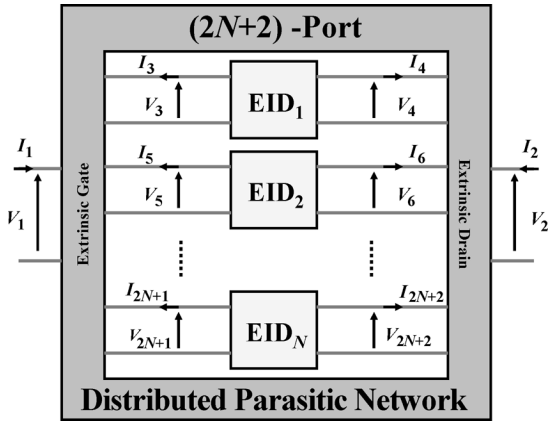

Fig. 2. Distributed parasitic network (gray pattern) directly obtained from the EM simulation of the device passive structure (described by the $\mathbf{Y}_{\rm EM}$ admittance matrix). Voltage and current phasors at the external gate and drain terminals and at the gate and drain EID terminals are also shown.

The distributed $2N+2$-port parasitic network shown in Fig. 2 is adopted in [14] for the definition of a fully distributed linear model of electron devices. In order to develop a similar approach in the more general nonlinear case, a single EqID is considered in the following leading to the corresponding definition of a compact distributed parasitic four-port network, described by the admittance matrix $\mathbf{Y}_C$ $[4\times 4]$.

A. Simplified Identification Approach

A simplified procedure consistent with the EqID concept is proposed in [15]. This is briefly recalled here for subsequent comparisons with the new identification procedure provided in Section II-B.

According to [15], every EID is considered equal to each other (both from a geometrical and electrical point of view) and *equally excited*. The second hypothesis means that both attenuation and delay of signals traveling across the active area are assumed to be negligible. This is quite reasonable in "well-designed" devices since either nonuniform current densities along the fingers or out-of-phase current combinations from different device fingers correspond to suboptimal device performance.

On the basis of these two assumptions, the $2N+2$-port distributed parasitic network in Fig. 2 can be *compacted* into a four-port description of parasitic effects by imposing

$$\begin{aligned}
&\mathrm{V}_1 \doteq V_1\\
&\mathrm{V}_2 \doteq V_2\\
&\mathrm{V}_3 \doteq V_3 = V_5 = \ldots = V_{2N+1}\\
&\mathrm{V}_4 \doteq V_4 = V_6 = \ldots = V_{2N+2}
\end{aligned} \tag{1}$$

and

$$\begin{aligned}
&\mathrm{I}_1 \doteq I_1\\
&\mathrm{I}_2 \doteq I_2\\
&\mathrm{I}_3/N \doteq I_3 = I_5 = \ldots = I_{2N+1}\\
&\mathrm{I}_4/N \doteq I_4 = I_6 = \ldots = I_{2N+2}
\end{aligned} \tag{2}$$

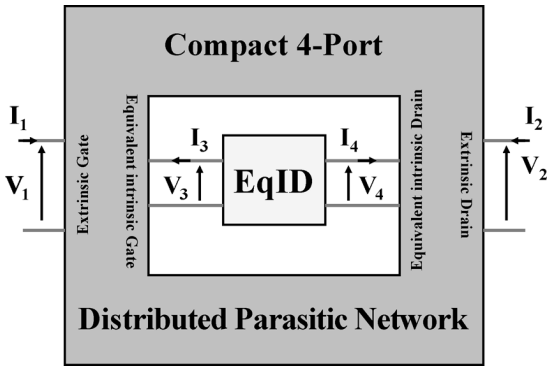

Fig. 3. Electron device model composed by the single EqID and the *compact* four-port's distributed parasitic network identified directly from the EM simulation through (3).

where V_j and I_j $(j = 1,\ldots,4)$ are the phasors of voltages and currents at the ports of the yet unknown compact parasitic network (see Fig. 3).

The admittance matrix $\mathbf{Y}_C$ of the compact distributed parasitic network, can be evaluated on the basis of (1) and (2) after simple algebraic manipulation through (3), shown at the bottom of this page, where y_{ij} $(i,j = 1,\ldots,2N+2)$ are the elements of the $\mathbf{Y}_{\mathrm{EM}}$ matrix.

Multifrequency closed-form deembedding of the parasitic network described by (3) from small-signal device measurements directly leads to the multibias multifrequency linear model of the EqID.

B. Multibias Identification Approach

As discussed above, two assumptions are made in the simplified approach presented in Section II-A. First, every EID is equal to each other; second, every EID is fed by identical excitations. Both hypotheses are questionable at first sight. For instance, internal versus borderline EIDs could be affected differently by EM coupling with surrounding structures, especially at high frequencies, or important delays could be present in the excitations of different EIDs.

A compact distributed description of the parasitic network can be alternatively obtained by means of a more general procedure, where the second assumption is abandoned. In particular, a new procedure is presented here where possible different excitations of every EID are taken into account.

The procedure is based on a "multibias iterative algorithm," whose goal is still to identify a compact four-port distributed parasitic network, as shown in Fig. 3. However, the desired goal now consists of identifying a four-port compact admittance matrix $\mathbf{Y}_C$, which guarantees, at any bias condition, voltage and (scaled) current phasors at the single EqID ports to be coherent (in "a least square sense") with the corresponding quantities at the ports of every EID (out of the N considered in the distributed network in Fig. 2).

As mentioned above, all the EIDs are still assumed to be equal in the generic bias condition. In addition, the unknown admittance matrix $\mathbf{Y}_{\mathrm{EqID}}$ of the EqID is defined to be scaled up by a factor N with respect to the $\mathbf{Y}_{\mathrm{EID}} \doteq \mathbf{Y}_{\mathrm{EID}}^{(d)}$ $(d = 1,\ldots,N_d)$, representing the description of every EID (i.e., $\mathbf{Y}_{\mathrm{EqID}} = N \cdot \mathbf{Y}_{\mathrm{EID}}$). Although the EIDs are considered equal, no *a priori* assumption is made here on the relationships existing between their excitations.

Since the $\mathbf{Y}_C$ matrix describes a four-port network, four linearly independent (complex-valued) excitations should be theoretically applied in order to get a complete characterization. However, according to Fig. 3, internal ports 3 and 4 are unfortunately not accessible in the actual case. Thus, two linearly independent excitations are only applicable through the external device ports 1 and 2 [e.g., (1 V, 0 V), (0 V, 1 V)]. However, excitations of port 3 and 4 can be equivalently obtained by considering the device behavior in (at least two) very different bias conditions (corresponding to very different couples of terminating impedances at ports 3 and 4).

The identification procedure is carried out according to the flowchart shown in Fig. 4.

At the first iteration, a suitable initial estimate for the unknown $\mathbf{Y}_C^{(k)}$, corresponding to index $k = 0$, must be provided. Since the problem is very well conditioned, a rough initial guess can be adopted, such as considering completely negligible parasitics.

Let $f = 1,\ldots,N_f$ be the frequency index, $e = 0,1$ be the external excitation index, $b = 1,\ldots,N_b$ be the bias condition index, and $d = 1,\ldots,N_d$ be the EID location index, where N_f, N_b, and N_d represent the number of frequencies, bias conditions, and EIDs considered, respectively.

The iterative procedure consists in three nested loops: the outer loop (k) involves successive approximations of the unknown matrix $\mathbf{Y}_C$, while the mid and inner loops (f,b) cycle through different frequencies and bias conditions.

$$\mathbf{Y}_C = \begin{pmatrix} y_{11} & y_{12} & \sum_{j=2}^{N+1} y_{1,2j-1} & \sum_{j=2}^{N+1} y_{1,2j} \\ y_{21} & y_{22} & \sum_{j=2}^{N+1} y_{2,2j-1} & \sum_{j=2}^{N+1} y_{2,2j} \\ \sum_{i=2}^{N+1} y_{2i-1,1} & \sum_{i=2}^{N+1} y_{2i-1,2} & \sum_{i=2}^{N+1}\sum_{j=2}^{N+1} y_{2i-1,2j-1} & \sum_{i=2}^{N+1}\sum_{j=2}^{N+1} y_{2i-1,2j} \\ \sum_{i=2}^{N+1} y_{2i,1} & \sum_{i=2}^{N+1} y_{2i,2} & \sum_{i=2}^{N+1}\sum_{j=2}^{N+1} y_{2i,2j-1} & \sum_{i=2}^{N+1}\sum_{j=2}^{N+1} y_{2i,2j} \end{pmatrix} \tag{3}$$

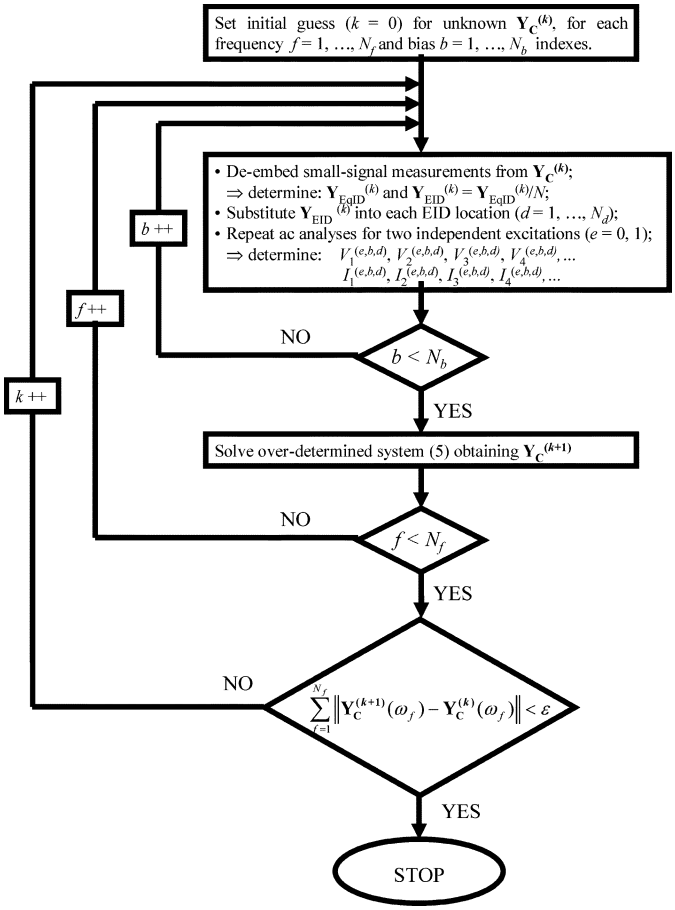

Fig. 4. Flowchart describing the multibias approach to the identification of the compact distributed parasitic network $\mathbf{Y}_C$.

For each k and f index choice, a multibias overdetermined system of equations is build up, whose solution leads to the identification of the compact $\mathbf{Y}_C^{(k+1)}$ matrix to be used in the $(k+1)$th iteration. To this aim, the small-signal admittance measurements of the device, carried out over the selected bias points (index b), are deembedded from $\mathbf{Y}_C^{(k)}$ in order to determine $\mathbf{Y}_{\text{EqID}}^{(k,b)}$ and $\mathbf{Y}_{\text{EID}}^{(k,b)} = \mathbf{Y}_{\text{EqID}}^{(k,b)}/N$, representing the admittance matrices (at frequency index f) of the EqID and of every EID at the (k)th iteration, respectively.

Any obtained $\mathbf{Y}_{\text{EID}}^{(k,b)}$ matrix is then iteratively inserted into every EID location and connected to the $2N+2$-port distributed network of Fig. 2. Each one of the resulting two-port linear networks (one for each b index value) is then simulated twice, in the presence of two linearly independent external excitations (e.g., indices $e = 0, 1$ corresponding to phasors $V_1^{(0,b,d)} = 1$ V, $V_2^{(0,b,d)} = 0$ V and $V_1^{(1,b,d)} = 0$ V, $V_2^{(1,b,d)} = 1$ V, respectively). The resulting voltage and current phasors at the extrinsic device ports and at the ports of each EID are then monitored by means of voltage and current probes. Namely, they are

$$\begin{aligned} &V_1^{(e,b,d)}, V_2^{(e,b,d)}, I_1^{(e,b,d)}, I_2^{(e,b,d)} \\ &V_3^{(e,b,d)}, V_4^{(e,b,d)}, I_3^{(e,b,d)}, I_4^{(e,b,d)}, \\ &V_5^{(e,b,d)}, V_6^{(e,b,d)}, I_5^{(e,b,d)}, I_6^{(e,b,d)} \\ &\cdots \\ &V_{2N+1}^{(e,b,d)}, V_{2N+2}^{(e,b,d)}, I_{2N+1}^{(e,b,d)}, I_{2N+2}^{(e,b,d)} \end{aligned} \tag{4}$$

where the f index is omitted anywhere for the sake of simplicity. Since the goal is to obtain a compact distributed description $\mathbf{Y}_C$ of the extrinsic parasitics, $4 \times 2 \times N_b$ constraints are now imposed for each EID (thus a total of $4 \times 2 \times N_b \times N_d$ equations are written) like

$$\begin{aligned} \mathrm{I}_1^{(e,b,d)} &= \mathrm{Y}_{11}^{(k+1)} \cdot \mathrm{V}_1^{(e,b,d)} + \mathrm{Y}_{12}^{(k+1)} \cdot \mathrm{V}_2^{(e,b,d)} \\ &\quad + \mathrm{Y}_{13}^{(k+1)} \cdot \mathrm{V}_3^{(e,b,d)} + \mathrm{Y}_{14}^{(k+1)} \cdot \mathrm{V}_4^{(e,b,d)} \\ \mathrm{I}_2^{(e,b,d)} &= \mathrm{Y}_{21}^{(k+1)} \cdot \mathrm{V}_1^{(e,b,d)} + \mathrm{Y}_{22}^{(k+1)} \cdot \mathrm{V}_2^{(e,b,d)} \\ &\quad + \mathrm{Y}_{23}^{(k+1)} \cdot \mathrm{V}_3^{(e,b,d)} + \mathrm{Y}_{24}^{(k+1)} \cdot \mathrm{V}_4^{(e,b,d)} \\ \mathrm{I}_3^{(e,b,d)} &= \mathrm{Y}_{31}^{(k+1)} \cdot \mathrm{V}_1^{(e,b,d)} + \mathrm{Y}_{32}^{(k+1)} \cdot \mathrm{V}_2^{(e,b,d)} \\ &\quad + \mathrm{Y}_{33}^{(k+1)} \cdot \mathrm{V}_3^{(e,b,d)} + \mathrm{Y}_{34}^{(k+1)} \cdot \mathrm{V}_4^{(e,b,d)} \\ \mathrm{I}_4^{(e,b,d)} &= \mathrm{Y}_{41}^{(k+1)} \cdot \mathrm{V}_1^{(e,b,d)} + \mathrm{Y}_{42}^{(k+1)} \cdot \mathrm{V}_2^{(e,b,d)} \\ &\quad + \mathrm{Y}_{43}^{(k+1)} \cdot \mathrm{V}_3^{(e,b,d)} + \mathrm{Y}_{44}^{(k+1)} \cdot \mathrm{V}_4^{(e,b,d)} \end{aligned} \tag{5}$$

where $Y_{ij}^{(k+1)}$ $(i, j = 1, \ldots, 4)$ are the admittance parameters of the $\mathbf{Y}_C$ matrix at the $(k+1)$th iteration at the particular frequency corresponding to f, and

$$\begin{aligned} \mathrm{V}_1^{(e,b,d)} &= V_1^{(e,b,d)} \\ \mathrm{V}_2^{(e,b,d)} &= V_2^{(e,b,d)} \\ \mathrm{V}_3^{(e,b,d)} &= V_{2d+1}^{(e,b,d)} \\ \mathrm{V}_4^{(e,b,d)} &= V_{2d+2}^{(e,b,d)} \\ \mathrm{I}_1^{(e,b,d)} &= I_1^{(e,b,d)} \\ \mathrm{I}_2^{(e,b,d)} &= I_2^{(e,b,d)}, \\ \mathrm{I}_3^{(e,b,d)} &= N \cdot I_{2d+1}^{(e,b,d)} \\ \mathrm{I}_4^{(e,b,d)} &= N \cdot I_{2d+2}^{(e,b,d)}. \end{aligned}$$

The solution of the overdetermined system (5) leads to the estimation of $\mathbf{Y}_C^{(k+1)}$ at the frequency index f (i.e., angular frequency ω_f).

The above steps are repeated, cycling through the outer loop (k) until the accuracy between two subsequent estimations of the $\mathbf{Y}_C$ matrix satisfies the final test

$$\sum_{f=1}^{N_f} \left\| \mathrm{Y}_C^{(k+1)}(\omega_f) - \mathrm{Y}_C^{(k)}(\omega_f) \right\| < \varepsilon \tag{6}$$

with ε being a given tolerance.

Despite the poor initial guess of the unknown matrix $\mathbf{Y}_C$, convergence of the iterative multibias procedure to the solution is very fast and sound.

C. Distributed Parasitic Network Identification: Discussion

As discussed above, the method proposed in Section II-A (method A) identifies the compact distributed parasitic network on the basis of the equally fed EIDs approximation, which could seem quite limiting at first glance, while the new multibias iterative method proposed in Section II-B (method B) relaxes such an hypothesis and is clearly more general. Moreover, the identification based on multibias small-signal measurements should be more robust with respect to the direct identification based on EM simulations obtained through method A.

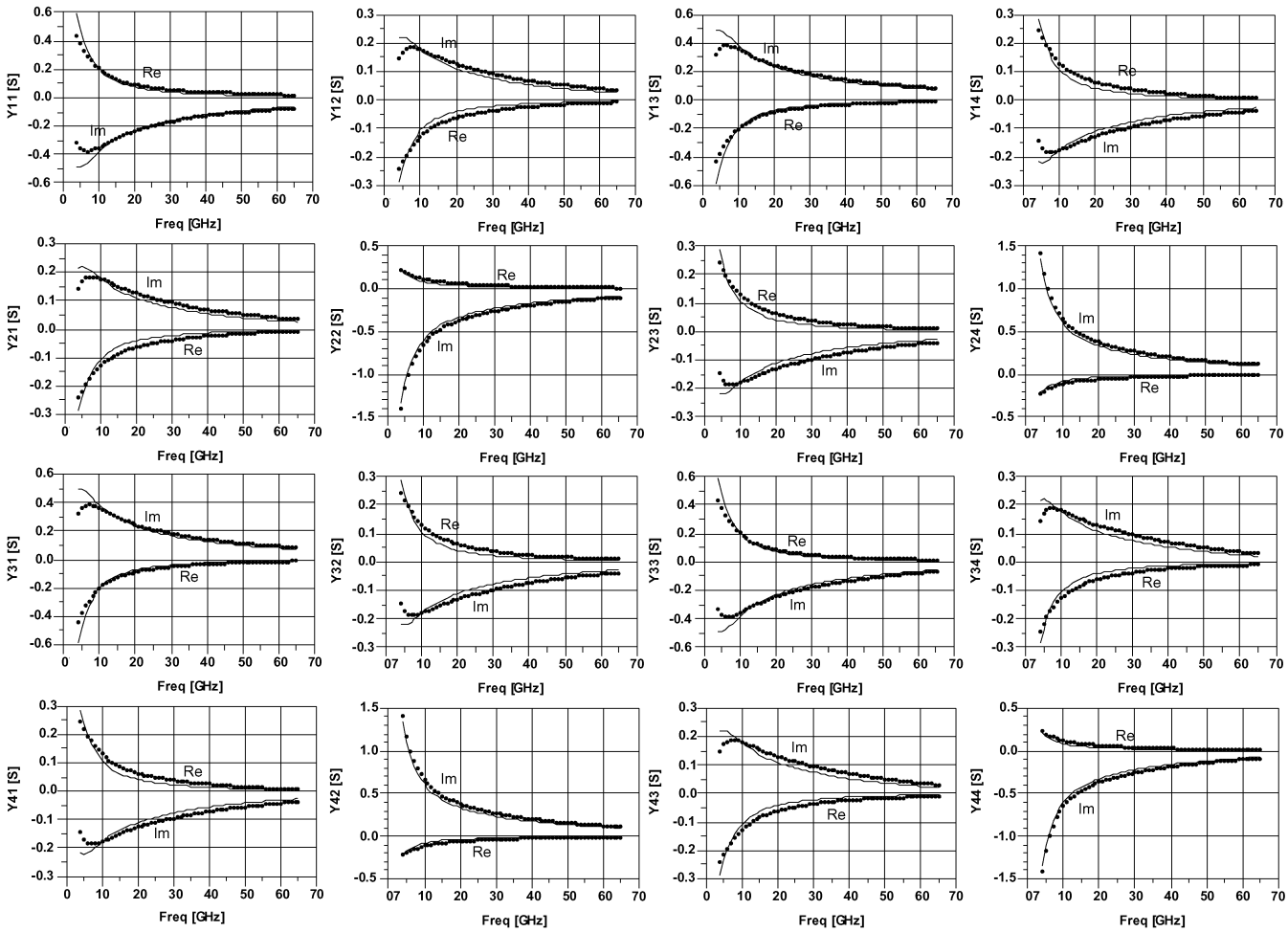

Fig. 5. Comparison of the four-port compact distributed parasitic networks of the 6×50 μm pHEMT in terms of admittance parameters, from 4 to 65 GHz, obtained with the two proposed identification approaches. Lines: method A. Dots: method B.

On the basis of the above considerations, method B can be reasonably used to verify the validity of the simpler method A. In order to carry out the comparison, both approaches are applied to different devices of the same family, namely, a 6×50 μm, a 10×48 μm, and a 12×75 μm GaAs pseudomorphic HEMT (pHEMT) ($L = 0.25$ μm).

Referring, for instance, to the 6×50 μm device, method A is applied starting from a $2N+2$-port distributed parasitic network with $N = 6$, i.e., the EM simulation is carried out by considering only one EID per finger. The validity of such a choice has been verified also in previous papers [17], [18]; in fact, it should be considered that, if an electron device is accurately designed for its operating frequency range, the propagation effects along the structure width, in particular signal attenuation, should not be too relevant, otherwise there will be some parts of the active area not efficiently exploited. In addition, it must be observed that the adoption of more than one EID per finger, when using method A, inherently leads to neglect the parasitic effects along the same finger due to the assumption of EIDs fed by identical signals. Thus, increasing the number of EIDs per finger does not provide higher accuracy in model identification through method A.

Method B is applied starting from a $2N + 2$-port distributed parasitic network with $N = 12$ (that is two EIDs per finger) and selecting 12 different bias points covering all the device operating regions. The choice of two sections of EIDs per finger is done in order to define a least square problem robustly overdetermined with respect to the placement of the EID in the electron device structure. With this choice, the iterative method converges to the required result very fast (after six iterations, the absolute error is less than 10^{-7}).

Fig. 5 shows the comparison between the admittance parameters of the four-port compact distributed parasitic networks identified with the two different methods in the frequency range (4–65 GHz). The lower frequency limit of 4 GHz is imposed by our thru-reflect line (TRL) calibration standards. As can be seen, the simplest method A provides results, which are very similar to those obtained by applying the multibias iterative method B.

In order to better compare the two proposed identification methods, the intrinsic device behavior of the same 6×50 μm GaAs pHEMT is investigated. Fig. 6 shows the comparison between the admittance parameters of the intrinsic devices obtained after deembedding the measured data from the compact parasitic networks identified with the two different approaches.

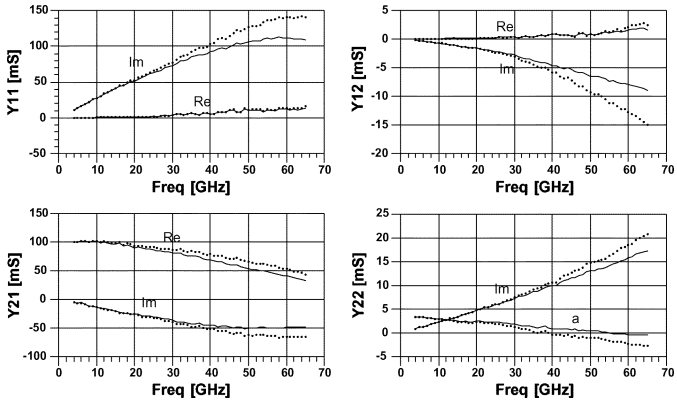

Fig. 6. Comparison of the intrinsic admittance parameters of the $6 \times 50\ \mu$m pHEMT from 4 to 65 GHz, corresponding to $I_{DSS}/2$ bias condition, obtained with the two proposed identification approaches. Lines: method A. Dots: method B.

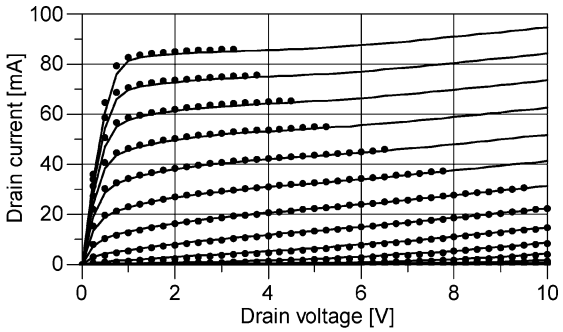

Fig. 7. DC *I/V* output characteristics of the $6 \times 50\ \mu$m pHEMT. The curves are traced for $\mathrm{V_{gs}}$ from -1.4 to 0 V (step 0.1 V) and $\mathrm{V_{ds}}$ from 0 to 10 V (step 0.25 V). Model predictions: lines. Device measurements: dots.

The results, corresponding to the $I_{DSS}/2$ bias condition, show that the intrinsic devices are quite similar.

As a general consideration about the intrinsic admittance parameters shown in Fig. 6, the fair, nearly constant, and linearly increasing behavior of the real and imaginary parts, respectively, can be appreciated. This corresponds to the "short memory" behavior discussed in detail in [24]. The parameters plotted in Fig. 6 suggest the physical soundness of the results, which are coherent with the intrinsic behavior of any electron device (conductive plus displacement current contribution) [27]–[35].

Analogous results are obtained after repeating the same comparisons on the $10 \times 48\ \mu$m and $12 \times 75\ \mu$m GaAs pHEMTs. Application of the two identification methods to devices having extremely large widths, e.g., due to a great number of (or to very long) fingers, could likely provide different results, highlighting the limits of method A. This is proven, however, to not be the case when considering typical widths used in MMIC power amplifier design.

Hence, since the multibias iterative procedure provides the same level of accuracy of the direct approach of Section II-A, it can be deduced that the EM simulation based on a single EID per finger is sufficiently accurate, at least for the overall widths investigated, in order to characterize the electron device parasitic effects, and that the hypothesis of EIDs fed by identical signals is quite reasonable.

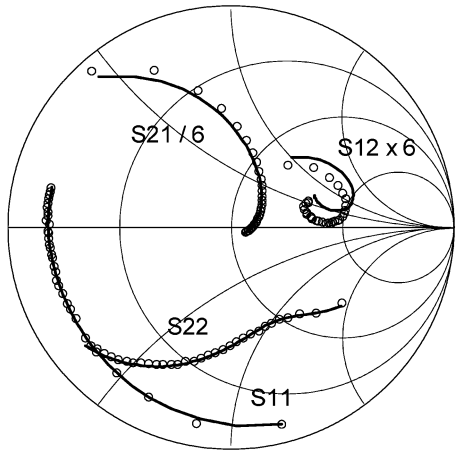

Fig. 8. Extrinsic S-parameters of the $6 \times 50\ \mu$m pHEMT in the bias condition $\mathrm{V_{gs}} = -0.6$ V, $\mathrm{V_{ds}} = 5$ V. Comparison between the model predictions (lines) and device measurements (circles). Frequency from 4 to 65 GHz.

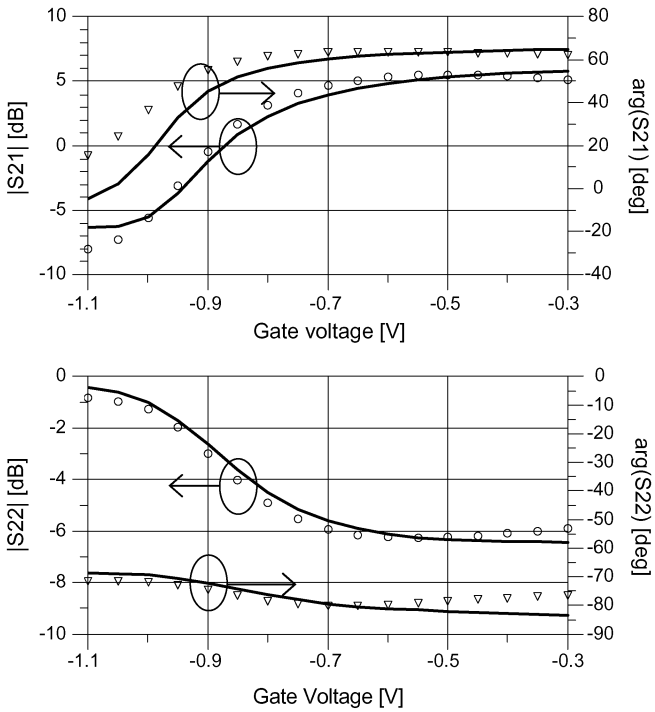

Fig. 9. Extrinsic S-parameters of the $6 \times 50\ \mu$m pHEMT as a function of the gate–source voltage and $\mathrm{V_{d0}} = 5$ V ($\mathrm{freq} = 20$ GHz). Comparison between the model predictions (lines) and the device measurements. Magnitude: circles. Phase: triangles.

Since the identification of the parasitic distributed network through method A is based on EM simulations only, it is inherently free from obvious instrumentation frequency limits involved in method B that also requires S-parameter measurements on the electron device. Moreover, method A is most suitable when a scalable model must be identified. In fact, as will be discussed in the following, a scalable model can be obtained by experimentally characterizing just a single electron device sample and simply performing EM simulations for the different layouts involving a different number and width of fingers.

Since the compact distributed parasitic networks identified by means of the two proposed approaches are almost coincident for

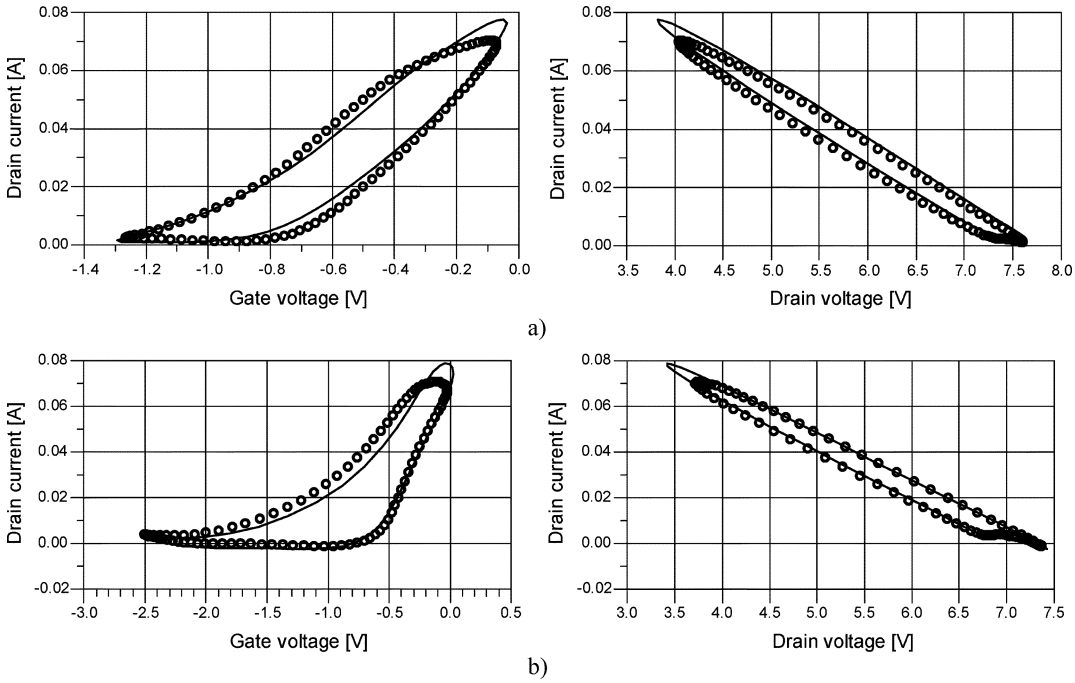

Fig. 10. $6 \times 50\ \mu$m pHEMT dynamic trans-characteristics and output characteristics at 5 GHz, 50-Ω source and load terminations. Comparison between model predictions (lines) and measurements (circles) for the device biased at: (a) $\mathrm{V_{gs}} = -0.6$ V, $\mathrm{V_{ds}} = 6$ V and (b) $\mathrm{V_{gs}} = -1.1$ V, $\mathrm{V_{ds}} = 6$ V.

all the geometries considered, the nonlinear model validation is practically valid for both of them. However, for the sake of completeness, experimental results shown in Section III refers to identification method A.

III. Nonlinear Device Modeling

The proposed identification procedures can be applied to both equivalent circuit and lookup-table-based modeling approaches. As an example, once we identified the pHEMT compact distributed parasitic four-port network, we decided to adopt the nonlinear discrete convolution (NDC) model [24]. In particular, its current–voltage relationships at the intrinsic device ports may be expressed as

$$\begin{aligned} i_1(t) &= F_{LF}^{(1)}\left[\mathbf{v}(t), \mathbf{V_0}, \vartheta_0\right] \\ &\quad + \sum_{p=1}^{N_D} \left(g_{11,p}\left[\mathbf{v}(t)\right] \cdot \left[v_1(t - p\Delta\tau) - v_1(t)\right]\right. \\ &\qquad \left. + g_{12,p}\left[\mathbf{v}(t)\right] \cdot \left[v_2(t - p\Delta\tau) - v_2(t)\right]\right) \\ i_2(t) &= F_{LF}^{(2)}\left[\mathbf{v}(t), \mathbf{V_0}, \vartheta_0\right] \\ &\quad + \sum_{p=1}^{N_D} \left(g_{21,p}\left[\mathbf{v}(t)\right] \cdot \left[v_1(t - p\Delta\tau) - v_1(t)\right]\right. \\ &\qquad \left. + g_{22,p}\left[\mathbf{v}(t)\right] \cdot \left[v_2(t - p\Delta\tau) - v_2(t)\right]\right) \end{aligned} \quad (7)$$

where $\mathbf{v}(t)$ and $\mathbf{V}_0$ represent the vectors of the instantaneous and average port voltages, respectively, and ϑ_0 is the dc value of the channel temperature.

The summation terms represent discretized purely dynamic single-fold convolution integrals between voltage deviations and the *pulse response functions* $g_{ij,p}[\mathbf{v}(t)]$ nonlinearly controlled by the instantaneous applied voltages. These terms account for purely dynamic high-frequency nonlinear phenomena.

The $F_{LF}^{(i)}$ functions instead describe the static and dynamic behavior of the electron device in the frequency range above the

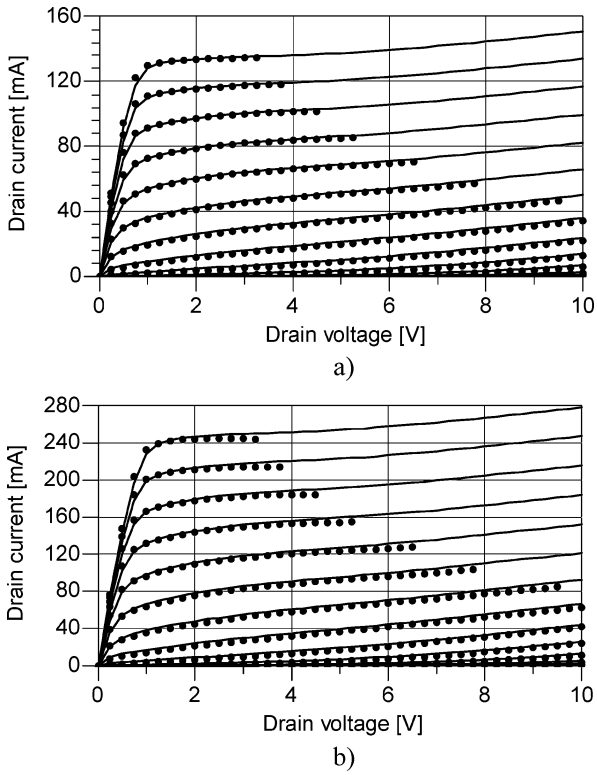

Fig. 11. DC *I/V* output characteristics of the: (a) $10 \times 48\ \mu$m and (b) $12 \times 75\ \mu$m pHEMTs. The curves are traced for $\mathrm{V_{gs}}$ from -1.4 to 0 V (step 0.1 V) and $\mathrm{V_{ds}}$ from 0 to 10 V (step 0.25 V). Scaled model predictions: lines. Device measurements: dots.

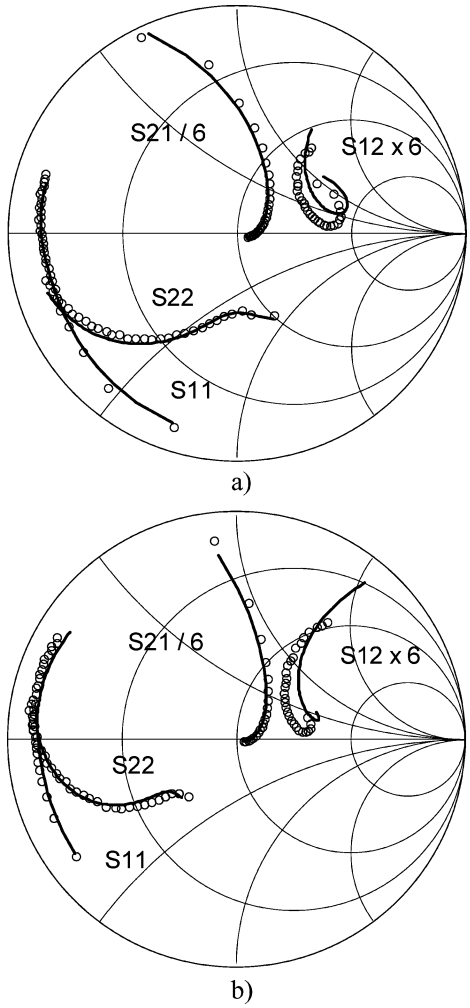

Fig. 12. Extrinsic S-parameters of the: (a) 10 × 48 μm and (b) 12 × 75 μm pHEMTs in the bias condition $\mathrm{V_{gs}} = -0.6$ V, $\mathrm{V_{ds}} = 5$ V. Comparison between the scaled model predictions (lines) and the device measurements (circles). Frequency from 4 to 65 GHz.

cutoff frequency of dispersive phenomena (e.g., above 1 MHz), but low enough to make high-frequency capacitive effects negligible. Since drain current characteristics are affected by dispersive phenomena, a backgating description [25] is adopted as follows:

$$\begin{aligned} F_{LF}^{(1)}\left[\mathbf{v}(t), \mathbf{V_0}, \vartheta_0\right] &= F_{\mathrm{dc}}^{(1)}\left[\mathbf{v}(t)\right] \\ F_{LF}^{(2)}\left[\mathbf{v}(t), \mathbf{V_0}, \vartheta_0\right] &= \left(1 + k \cdot (p_S(t) - P_0)\right) \cdot F_{\mathrm{dc}}^{(2)}\left[\mathbf{v}_m(t)\right] \end{aligned} \tag{8}$$

where

$$\mathbf{v}_m(t) = \mathbf{v}(t) + \begin{bmatrix} \alpha_g & \alpha_d \\ 0 & 0 \end{bmatrix} \cdot \left(\mathbf{v}(t) - \mathbf{V_0}\right). \tag{9}$$

In (8) and (9), $F_{\mathrm{dc}}^{(i)}$ are the static current characteristics, and α_g, α_d, and k are suitable scalar coefficients to be determined. Moreover, P_0 represents the average dissipated power under dynamic conditions and $p_s(t)$ is a "quasi-static" power [25] corresponding to the power that would be dissipated if the applied voltages were "slowly" time-varying quantities.

The method proposed in Section II-A is applied here to identify a scalable nonlinear device model of the 0.25-μm GaAs pHEMT having a total periphery equal to 300 μm (6×50 μm). Method A is chosen because, beside its simplicity, it can be easily implemented in any available commercial CAD tool.

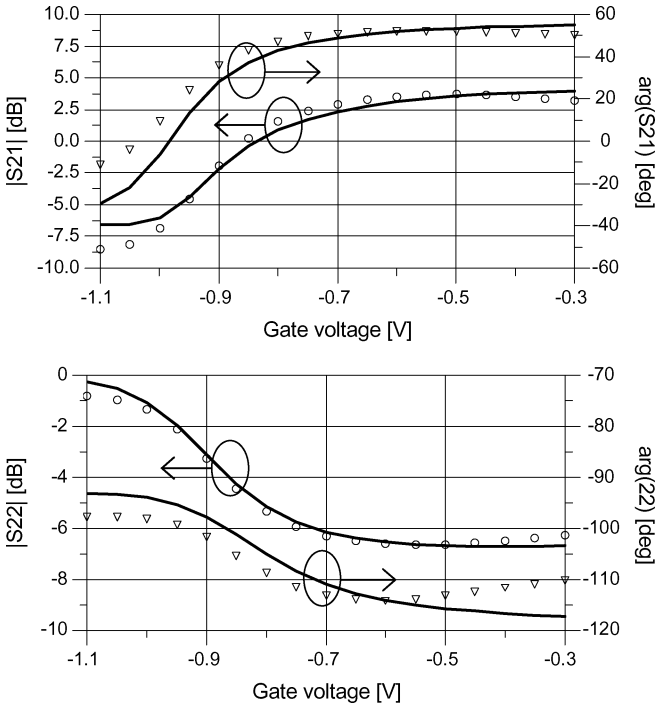

Fig. 13. Extrinsic S-parameters of the 10×48 μm pHEMT as a function of the gate–source voltage and $\mathrm{V_{d0}} = 5$ V ($\mathrm{freq} = 20$ GHz). Comparison between the model predictions (lines) and the device measurements. Magnitude: circles. Phase: triangles.

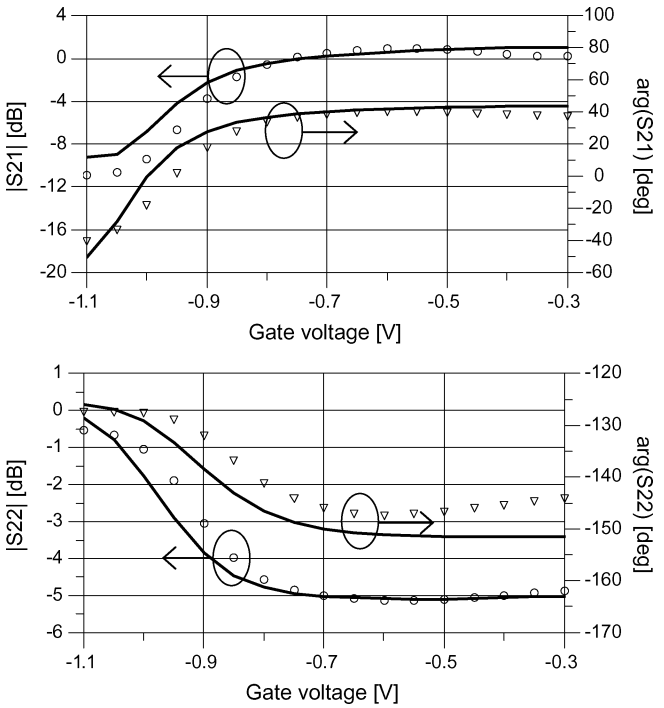

Fig. 14. Extrinsic S-parameters of the 12×75 μm pHEMT as a function of the gate–source voltage and $\mathrm{V_{d0}} = 5$ V ($\mathrm{freq} = 20$ GHz). Comparison between the model predictions (lines) and the device measurements. Magnitude: circles. Phase: triangles.

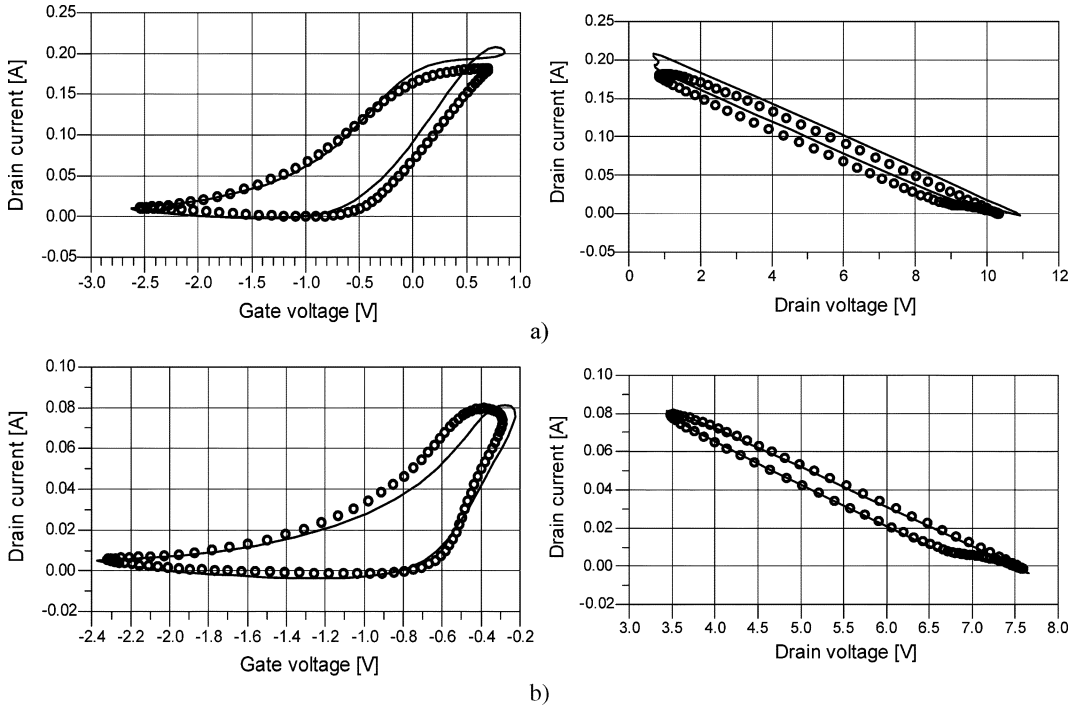

Fig. 15. 10×48 μm pHEMT dynamic trans-characteristics and output characteristics at 5 GHz (50-Ω source and load terminations). Comparison between scaled model predictions (lines) and measurements (circles) for the device biased at: (a) $\mathrm{V_{gs}} = -0.6$ V, $\mathrm{V_{ds}} = 6$ V and (b) $\mathrm{V_{gs}} = -1.1$ V, $\mathrm{V_{ds}} = 6$ V.

Once identified, the pHEMT compact distributed parasitic four-port network, dc, and S-parameters measurements [carried out in the frequency range (4–65 GHz)] have been exploited according to the identification procedure outlined in [24].

The identified compact distributed parasitic network is used in the circuit simulator as a table-based linear network embedded with the selected empirical nonlinear model for the intrinsic device. Such an implementation provides that the computational effort associated to the nonlinear scalable model is practically the same as conventional empirical models.

In Fig. 7, measured extrinsic dc drain current characteristics are compared to model predictions; as expected, the model perfectly fits the measured data.

Figs. 8 and 9 exhibit model prediction versus measurements under small-signal operation. In particular, the good agreement of S-parameters versus frequency obtained in a class-A bias is shown in Fig. 8, while small-signal predictions versus the gate–source voltage at 20 GHz is presented in Fig. 9.

In order to validate the model under nonlinear dynamic operation, we exploited measurements carried out by means of a large-signal network analyzer (LSNA) [26]. This instrument enables simultaneous characterization of the voltage and current waveforms at the device terminals. Thanks to the ability of correlating instantaneous voltages and currents, the source of possible discrepancies between measurements and model predictions can be straightforwardly put in evidence.

In Fig. 10, measurements carried out on the 6×50 μm pHEMT at 5 GHz (50-Ω source and load terminations) are shown. In particular the device is biased here under class-A ($\mathrm{V_{gs}} = -0.6$ V, $\mathrm{V_{ds}} = 6$ V) and class-B ($\mathrm{V_{gs}} = -1.1$ V, $\mathrm{V_{ds}} = 6$ V) operations. The curves refer to the device nonlinear dynamic trans-characteristics and output characteristics. The class-A operation shown corresponds to 2-dB gain compression.

IV. Scalable Nonlinear Device Modeling

As previously mentioned, the intrinsic device obtained by deembedding S-parameter measurements from the parasitic distributed network, shows physically consistent short memory properties, and is very suitable for the identification of a nonlinear device model. To definitely probe this issue, the 6×50 μm pHEMT, described in Section III, has been considered as the "reference device" for the actual technological process. This choice allows testing the nonlinear model scaling capabilities towards geometries having larger peripheries and a different number of gate fingers. In order to scale the 6×50 μm pHEMT nonlinear model to a different device geometry, the linearly scalable intrinsic NDC model is embedded in the compact distributed parasitic four-port network (obtained through a new EM simulation and a new identification procedure through method A) of the given device.

The extrinsic dc *I/V* characteristics for the two scaled devices, namely, the 10×48 μm and 12×75 μm pHEMTs, are shown in Fig. 11. As can be seen, the predicted dc curves for the scaled devices are in excellent agreement with measurements.

The extrinsic S-parameter predictions (4–65 GHz) for the two scaled devices are shown, for typical class-A operation bias conditions, in Fig. 12. Also in this case, the agreement between model prediction and measurements is pretty good.

As an additional validation of the scalable nonlinear model predictions under linear operation, the extrinsic scattering parameters predictions of the scaled 10×48 μm pHEMT are shown as a function of the bias condition at fixed frequency in Fig. 13.

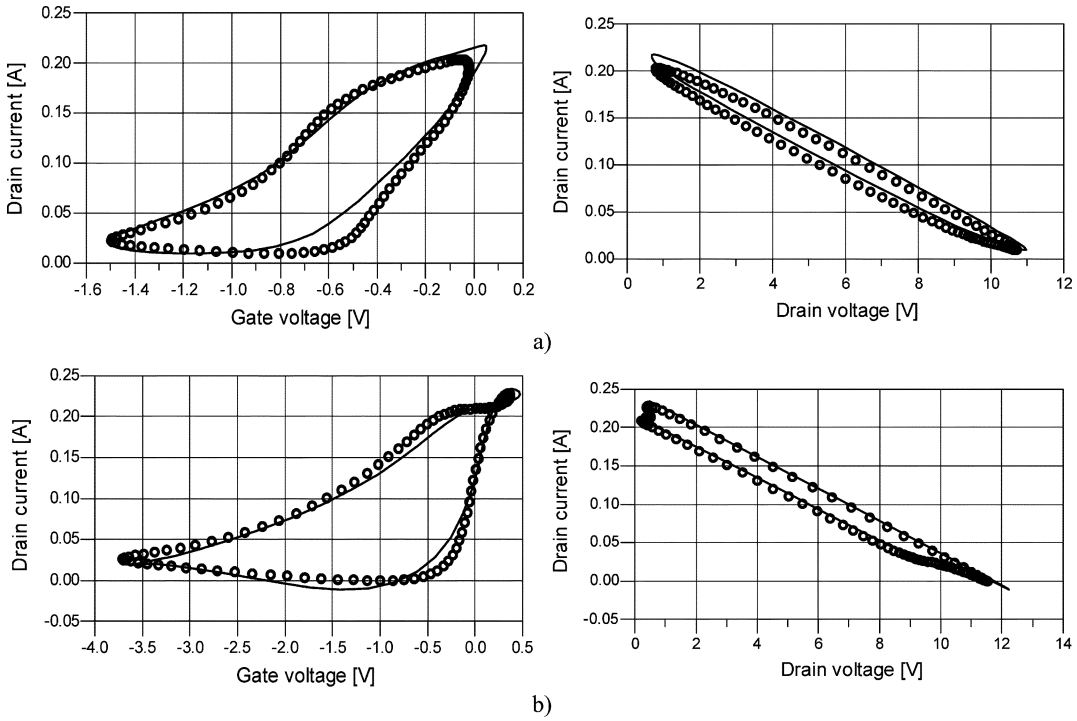

Fig. 16. 12×75 μm pHEMT dynamic trans-characteristics and output characteristics at 5 GHz (50-Ω source and load terminations). Comparison between scaled model predictions (lines) and measurements (circles) for the device biased at: (a) $\mathrm{V_{gs}} = -0.6$ V, $\mathrm{V_{ds}} = 6$ V and (b) $\mathrm{V_{gs}} = -1.1$ V, $\mathrm{V_{ds}} = 6$ V.

Measurements carried out under the same operating conditions are compared to model predictions in Fig. 14 for the 12×75 μm pHEMT.

In Figs. 15 and 16, nonlinear measurements carried out on the 10×48 and 12×75 μm pHEMTs at 5 GHz (50-Ω source and load terminations) are shown; in particular the devices were biased under class-A ($\mathrm{V_{gs}} = -0.6$ V, $\mathrm{V_{ds}} = 6$ V) and class-B ($\mathrm{V_{gs}} = -1.1$ V, $\mathrm{V_{ds}} = 6$ V) operations; the curves refer to the device nonlinear dynamic trans-characteristics and output characteristics.

Fig. 15 clearly shows that the model performances are practically the same when it is scaled with respect to the number of fingers. It should be noted that finger-number scaling is quite critical since the device access structure is dramatically modified. For this pHEMT device, class-A operation refers to 3.5-dB gain compression.

Considering the 12×75 μm device, the "reference device" model is scaled with respect to the two parameters (number and width of fingers). Fig. 16 quantifies the scaled model prediction accuracy. In this case, class-A operation refers to 2-dB gain compression.

To further put in evidence the fair prediction capabilities of the proposed modeling approach, output power predictions at fundamental and harmonic frequencies are compared to measurements for different power levels in Fig. 17. In particular the two figures refer to the 10×48 μm and 12×75 μm devices in class-B conditions, respectively.

In order to provide model validation at more realistic loading conditions and higher frequencies of operation, two-tone measurements have been carried out at 37 GHz (10-MHz tone spacing) for a 10×60 μm pHEMT of the same foundry process, biased for class-A operation. Fig. 18 shows the scaled

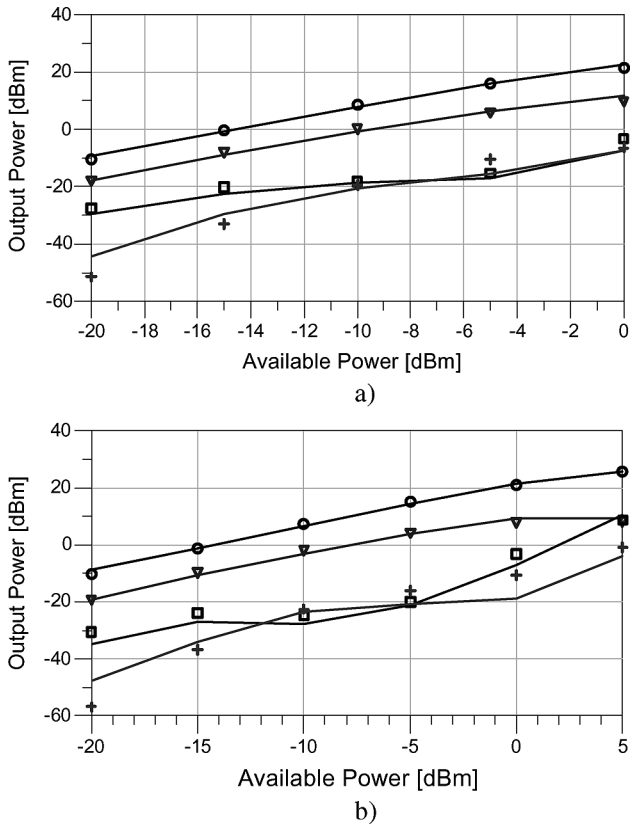

Fig. 17. Output power predictions at fundamental and harmonics (lines) are compared to measurements for different power levels (symbols). In particular, the two figures refer to the class-B bias condition for the: (a) 10×48 μm and (b) 12×75 μm pHEMTs.

10×60 μm pHEMT model predictions compared to the intermodulation distortion (IMD) measurements with two

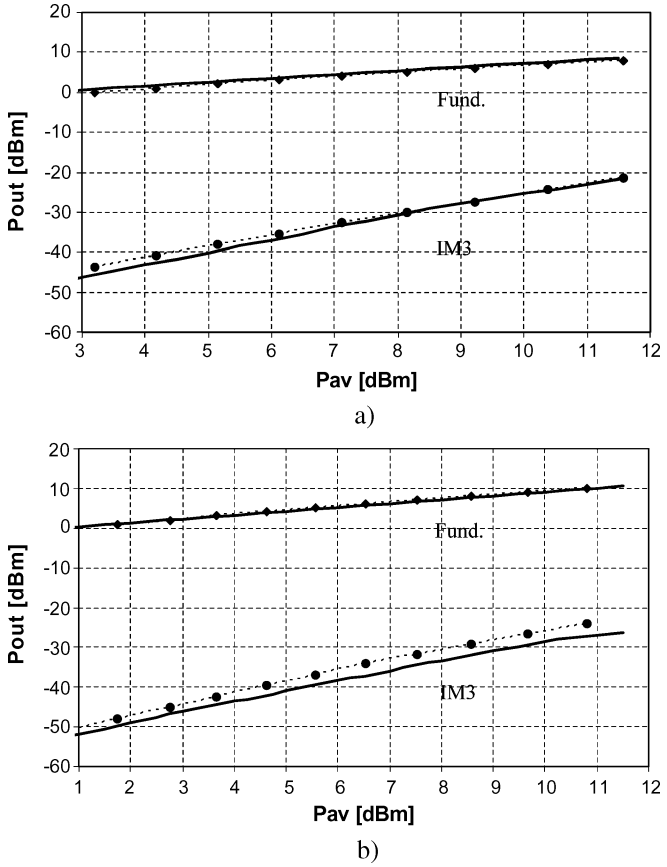

Fig. 18. IMD at 37 GHz (10-MHz tone spacing). Scaled $10 \times 60\ \mu$m pHEMT model prediction (lines) compared to the device measurement (symbols) both for the fundamental tone, as well as for the third-order intermodulation tone. Device biased at $V_{GS} = -0.55$ V, $V_{DS} = 6.5$ V and source impedance $Z_S = 49.547 - j\,9.652$. Load impedance: (a) $Z_L = 30.7 - j\,0.88$ and (b) $Z_L = 14.4 + j\,9.7$.

very different load terminations. The high accuracy achieved in the prediction of IMD makes the model suitable for millimeter-wave high linearity power amplifier design.

It is worth mentioning that model identification, as previously stated, has been carried out here on the basis of a single "reference" electron device. However, the simplicity and closed-form feature of the identification algorithms can be easily extended to account for a larger set of "reference devices" having different peripheries. This approach can definitely be effectively exploited to obtain highly accurate scalable models over a very wide set of devices having remarkable different geometries, as is usually required in advanced general-purpose foundry processes.

V. Conclusion

A distributed nonlinear electron device model has been proposed and different identification procedures have been presented and experimentally validated. The described approach enables a scalable nonlinear electron device model to be identified on the basis of EM device layout simulations and conventional dc and ac measurements carried out on a single "reference device" structure. Such a feature makes the model an extremely powerful and flexible tool not only for design purposes, but also for new device development and/or optimization of the device layout, since electron device performances can be quite accurately predicted without actually manufacturing a given device structure.

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