GaN HEMT Noise Model Based on Electromagnetic Simulations

Andrea Nalli, *Student Member, IEEE*, Antonio Raffo, *Member, IEEE*, Giovanni Crupi, *Senior Member, IEEE*, Sara D'Angelo, Davide Resca, *Member, IEEE*, Francesco Scappaviva, Giuseppe Salvo, *Student Member, IEEE*, Alina Caddemi, *Member, IEEE*, and Giorgio Vannini, *Member, IEEE*

***Abstract*—This paper presents a new approach for the definition and identification of a transistor model suitable for low-noise amplifier (LNA) design. The resulting model is very robust to layout modifications (i.e., source degeneration) providing accurate predictions of device noise-performance and small-signal parameters. Moreover, the described procedure is very robust since it does not require any numerical optimization, with possibly related problems like local minima and unphysical model parameters. The adopted model topology is based on a lumped element parasitic network and a black-box intrinsic device, which are both identified on the basis of full-wave electromagnetic simulations, as well as noise and S-parameter measurements. The procedure has been applied to three GaN HEMTs having different peripheries and a Ku-band LNA has been designed, demonstrating a very good agreement between measurements and predicted results.**

***Index Terms*—Electromagnetic analysis, HEMTs, low-noise amplifiers (LNAs), noise modeling, receivers, semiconductor device modeling.**

I. Introduction

LOW-NOISE amplifiers (LNAs) play a very important role in receiver front-ends, being the most important contributor to the overall system receiving performance.

The GaN HEMT is a promising candidate for robust low-noise applications [1], [2] due to its good noise performance, excellent linearity, and robustness. Additionally, by using GaN HEMTs, the entire transmitter/receiver front-end could be integrated in the same chip, with significant advantages in terms of cost and occupied space. However, the proper identification of a model able to accurately predict GaN HEMT noise performance is not trivial and many studies have been devoted to accomplish this challenging task [3]–[11].

The purpose of this work is to develop a new procedure for the definition and identification of a low-noise transistor model suitable for LNA design. Such a type of application poses tight modeling requirements since a sound physical basis of the transistor parasitic network elements is necessary in order to accurately reproduce noise behavior and properly account for those transistor layout modifications (i.e., inductive source degeneration) needed to optimize the LNA performance.

Source degeneration is widely used in LNA design and it consists of inserting a lossless inductance (or a microstrip line) between the HEMT source and the via-hole to ground. This introduces a series feedback that reduces the transistor available gain, but moves the best input termination for noise closer to the conjugate match termination.

As an example, Fig. 1 shows the noise factor measured with 50-Ω source impedances and the parameter S_{11} for a degenerated 8×50 μm GaN HEMT (degeneration equivalent inductance is 110 pH) predicted by a model where the parasitic network is identified by using the procedure described in this work and a simpler one, based on dc and S-parameter measurements [12]. The different accuracy level is well evident even if without source degeneration the quality of the small-signal response and noise performance predicted by the two models would be exactly the same.

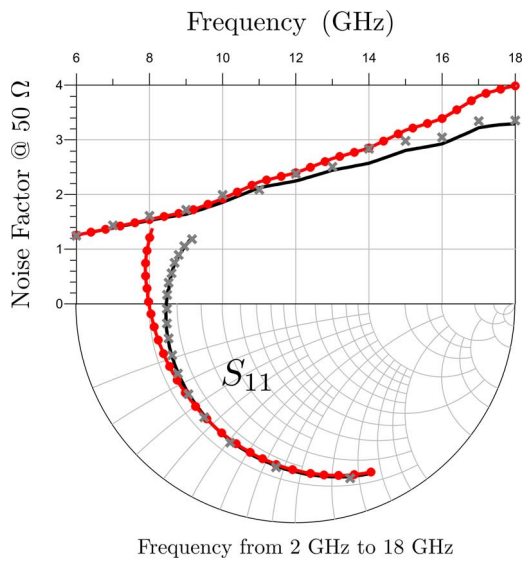

Fig. 1. Prediction of the noise factor with 50-Ω source impedance (*upper*) and S_{11} (*lower*) for a degenerated 8×50 μm GaN HEMT where parasitic layout are correctly taken (black line) and not taken (red line (in online version) with dots) into account; measurements in frequency range of 2–18 GHz are also reported (crosses).

Manuscript received February 28, 2015; accepted June 07, 2015. Date of publication July 09, 2015; date of current version August 04, 2015. This work was supported by the HF Circuits project and by the PON 01_01322 PANREX project with the financial support of the Italian Ministry of Education, University and Research (MIUR).

A. Nalli, A. Raffo, and G. Vannini are with the Engineering Department, University of Ferrara, 44122 Ferrara, Italy (e-mail: antonio.raffo@unife.it).

G. Crupi, G. Salvo, and A. Caddemi are with the DICIEAMA, University of Messina, 98166 Messina, Italy.

S. D'Angelo, D. Resca, and F. Scappaviva are with Microwave Electronics for Communications (MEC) Srl, 40127 Bologna, Italy.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TMTT.2015.2447542

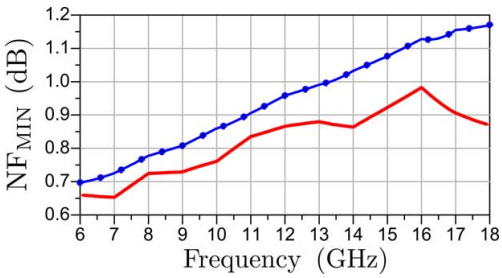

Fig. 2. Minimum noise figure for a 2×50 μm GaN HEMT where noise introduced by the parasitic network is taken (blue line (in online version) with dots in online version) and not taken (red line in online version) into account.

Moreover, the noise contribution of the parasitic network is generally not negligible, as evident in Fig. 2, where the minimum noise figures for a 2×50 μm GaN HEMT with and without parasitic noise contribution[1] are compared.

In this work, a modeling procedure usable by designers without specific modeling knowledge has been developed. To this end, iterative and optimization-based model identification procedures are not a good choice, as they can lead to incorrect and nonphysical results if not carried out by people with in-depth experience in device modeling. As an alternative, a model identification procedure based on linear regression is proposed here. Indeed, linear regression requires only a few interactions by the user (in this case, just the frequency range should be defined) and is clearly more straightforward.

The linear parasitic effects due to the transistor layout are modeled by a lumped-element network, identified by means of an analytical procedure exploiting several full-wave electromagnetic (FW-EM) simulations. On the other hand, the active intrinsic core of the device is modeled by means of black-box noiseless two-ports having input and output correlated noise sources.

Performing FW-EM simulations of the different layout regions of the device allows one to develop a parasitic model where the contributions of each region is well determined; thus, layout parts can be modified (e.g., the via-holes can be removed) preserving the accuracy of the model noise-performance and small-signal response.

As far as the intrinsic core is concerned, a black-box representation is chosen, as it is very easy to be identified and implemented since parameters associated with the intrinsic core are process related and cannot be modified by the designer.

An important benefit of the developed technique is that very simple scaling rules can be straightforwardly applied to the proposed model to get the noise and small-signal performance for differently sized devices.

This paper is organized as follows. In Section II, the analytical parasitic-network modeling and extraction technique are extensively described. Furthermore, the parasitic network responses predicted by the model and the FW-EM simulations are compared, even far beyond the identification frequency range. In Section III, the de-embedding technique used to achieve the small-signal response and noise behavior of the intrinsic-core is fully described. Moreover, simple scaling rules for the intrinsic core are provided and scaled model predictions of noise behavior and S-parameter response are reported. Finally, in Section IV, an LNA designed by exploiting the proposed model is presented and experimental results are reported.

[1]In this second case, the parasitic network temperature was set to 0 K.

II. Modeling and Analytical Identification of the Device Lumped Parasitic Network

A classic transistor device model can be divided into two fundamental parts: the parasitic network and the intrinsic device or "intrinsic core." The latter represents the active area of the device, including the current generator, while the parasitic network takes into account the access structures to the intrinsic device.

Through FW-EM simulations of the device layout, the effects of the parasitic network can be characterized and modeled properly. In this context, coupling phenomena associated with the doped semiconductor substrate are not taken into account, as they have been found generally negligible [13]–[16]. This assumption is further confirmed by the experimental validation provided in Section IV.

The robustness of the transistor model is strongly dependent on the accuracy of the parasitic network description. In this respect, the typical layout of an HEMT device, shown in Fig. 3(a), has been subdivided in the following four different regions [see Fig. 3(b)]:

- regions (I) and (II) enclose gate and drain manifolds, which feed the signal to the fingers;
- region (III) encloses the via-holes, which provide connections to the backplane metallization;
- region (IV) encloses the fingers and the air bridges, which connect the source fingers to the via-hole pads.

A lumped-element network can be associated with each region, as shown in Fig. 3(c). For the manifolds (i.e., regions I and II), whose layout is reported in Fig. 3(d), a resistor R^{GM} (R^{DM}) and an inductor L^{GM} (L^{DM}) (where "M" stands for manifold, "G" for gate and "D" for drain) model the series parasitic effects. Instead, the parasitic capacitive coupling between the manifold and the substrate is modeled by two capacitors: C_1^{GM} (C_1^{DM}) and C_2^{GM} (C_2^{DM}), forming with the other elements the PI-shape network in Fig. 3(e). It is worth noticing that, with the aim of preserving a high computational efficiency, the intrinsic device is modeled by a two-port network. This choice necessary leads to *compact* all the ports, which give access to the intrinsic device [e.g., ports 2–5 in Fig. 3(d)] into a single one. The accuracy of this approximation has been largely demonstrated in [15] and [16] and is confirmed by all the parasitic network lumped descriptions (e.g., [17]), which are inherently based on the same hypothesis. This greatly reduces the complexity of the model and speeds up the model extraction.

The parasitic effects associated with the via-holes (i.e., region III), whose layout is shown in Fig. 3(f), are modeled by a simple series connection of the resistor R^{VH} and the inductor L^{VH}, as reported in Fig. 3(g). Finally, considering region (IV), three capacitors (C^{GS}, C^{DS}, and C^{GD}) model the capacitive coupling between the fingers and between the fingers and the air-bridge, while the series parasitic effects of the fingers and the air-bridge are taken into account by three resistor-inductor series (R^G, L^G

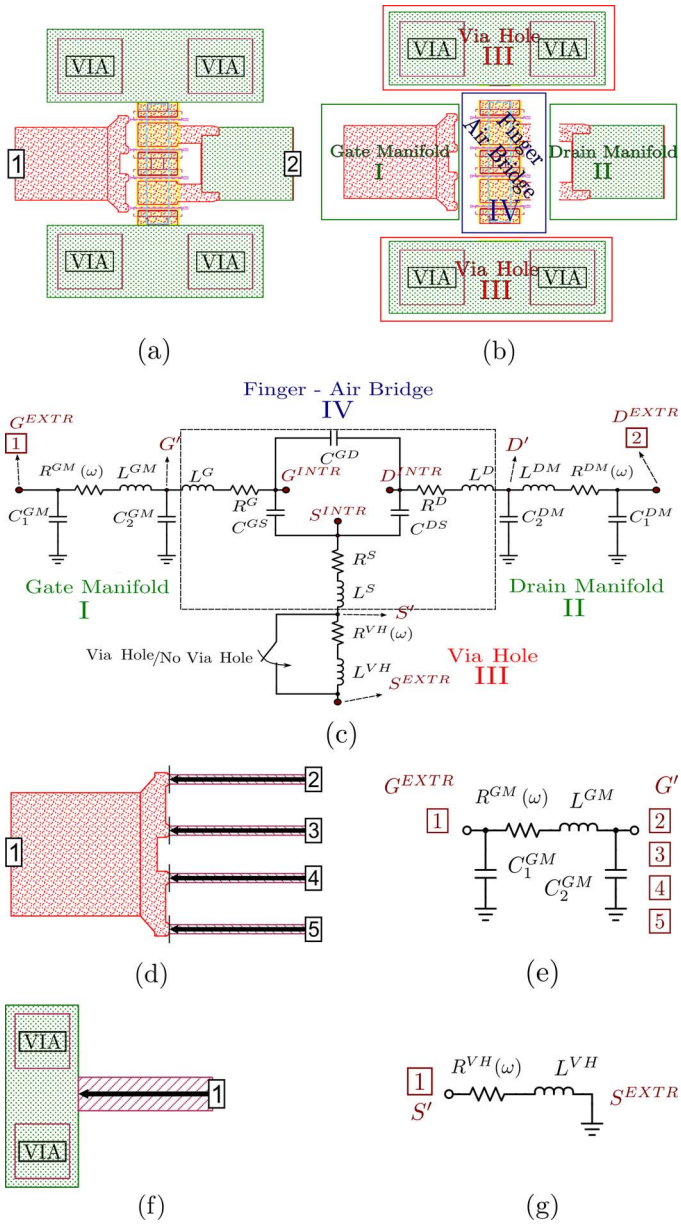

Fig. 3. (a) Transistor layout, (b) associated partitioning for FW-EM simulations, and (c) whole parasitic network of the transistor. (d) Gate manifold and (e) associated lumped element description (identical for the drain manifold). (f) Via-hole and (g) associated lumped element description.

and R^D, L^D and R^S, L^S) forming with the other elements the whole parasitic network reported in Fig. 3(c).

A. Manifold Parameters Extractions

As shown in Fig. 3(e), the manifolds are considered as two-port networks, where one port is at the extrinsic plane of the transistor and the other one connects to the finger region (i.e., gate or drain fingers). The Y matrix associated with the manifold network in Fig. 3(e) is

$$Y^{XM} = \begin{bmatrix} j\omega C_1^{XM} + \frac{1}{j\omega L^{XM} + R^{XM}(\omega)} & -\frac{1}{j\omega L^{XM} + R^{XM}(\omega)} \\ -\frac{1}{j\omega L^{XM} + R^{XM}(\omega)} & j\omega C_2^{XM} + \frac{1}{j\omega L^{XM} + R^{XM}(\omega)} \end{bmatrix} \quad X = G, D. \tag{1}$$

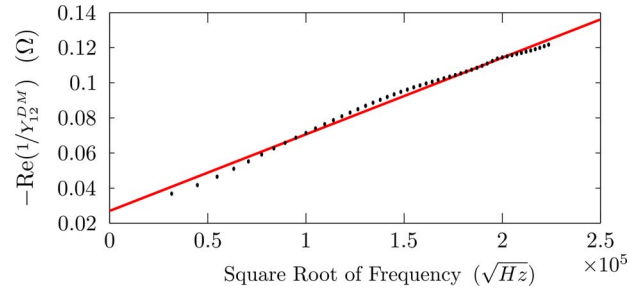

Fig. 4. Resistive coefficient of the drain manifold of a 4×50 μm GaN HEMT versus square root of frequency. FW-EM simulations (dots) are fitted with the formulation reported in (2) (line).

As an example, Fig. 4 shows, for a 4×50 μm GaN HEMT, the real part of $-(Y_{12}^{DM})^{-1}$, corresponding to $R^{DM}(\omega)$, obtained by an FW-EM simulation of region (II). The parameter is clearly linear with the square root of the frequency. This shape is reasonably due to the skin effect, and it is clearly not negligible since the parameter variation is very large. In this respect, the resistors $R^{GM}(\omega)$ and $R^{DM}(\omega)$ are assumed frequency dependent to model such a variation.

In the literature, several types of formulations are available to model the skin effect [18], [19]. In our case, the following simple analytical expression has been empirically found to be suitable:

$$R^{XM}(\omega) = R_{\rm DC}^{XM} + (1+j)R_{\rm RF}^{XM}\sqrt{\omega} \quad X = G, D. \tag{2}$$

All the manifold model parameters can be easily extracted from FW-EM simulations of regions (I) and (II). The elements $R_{\rm DC}^{XM}$ and $R_{\rm RF}^{XM}$ can be determined by a linear regression

$$-{\rm Re}\left(\frac{1}{Y_{12}^{XM}}\right) = R_{\rm DC}^{XM} + R_{\rm RF}^{XM}\sqrt{\omega} \quad X = G, D. \tag{3}$$

Successively, the inductance can be straightforwardly extracted with the following formula:

$$L^{XM} = {\rm mean}\left({\rm Im}\left(-\frac{1}{\omega Y_{12}^{XM}}\right) - \frac{R_{\rm RF}^{XM}}{\sqrt{\omega}}\right) \quad X = G, D \tag{4}$$

where the mean value is calculated over the whole frequency range.

Once obtained, the value of L^{XM} and the elements C_1^{XM} and C_2^{XM} can be determined by

$$C_1^{XM} = {\rm mean}\left(\frac{1}{\omega}{\rm Im}\left(Y_{11}^{XM} - \frac{1}{j\omega L^{XM} + R^{XM}(\omega)}\right)\right) \quad X = G, D \tag{5}$$

$$C_2^{XM} = {\rm mean}\left(\frac{1}{\omega}{\rm Im}\left(Y_{22}^{XM} - \frac{1}{j\omega L^{XM} + R^{XM}(\omega)}\right)\right) \quad X = G, D. \tag{6}$$

Also in this case the mean value is calculated over the whole frequency range.

B. Via-Hole Parameter Extraction

The Z-parameter associated with the via-hole model in Fig. 3(g) is

$$Z^{VH} = R^{VH}(\omega) + j\omega L^{VH} \tag{7}$$

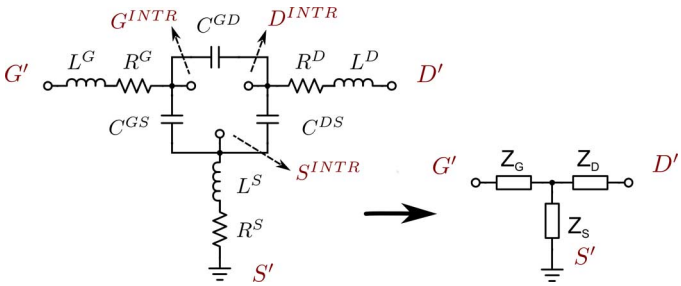

Fig. 5. Finger region parasitic model and associated equivalent representation adopted for parameter extraction.

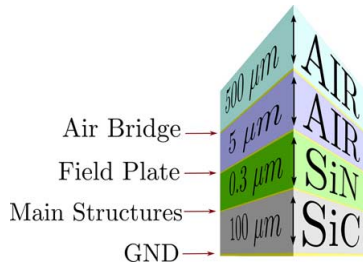

Fig. 6. Dielectric layers used for the FW-EM simulations. Thickness and dielectric types are reported, as well as the structures present between the layers.

where the skin effect is taken into account with

$$R^{VH}(\omega) = R^{VH}_{\rm DC} + (1+j)R^{VH}_{\rm RF}\sqrt{\omega}. \tag{8}$$

Analogously to (2), $R^{VH}_{\rm DC}$ and $R^{VH}_{\rm DC}$ can be extracted by a linear regression of the real part of Z^{VH} on the FW-EM simulation data of region (III),

$$\mathrm{Re}(Z^{VH}) = R^{VH}_{\rm DC} + R^{VH}_{\rm RF}\sqrt{\omega} \tag{9}$$

while L^{VH} can be determined by

$$L^{VH} = \mathrm{mean}\left(\frac{\mathrm{Im}(Z^{VH}) - R^{VH}_{\rm RF}\sqrt{\omega}}{\omega}\right) \tag{10}$$

where the mean value is calculated over the whole frequency range.

C. Finger Region Parameter Extraction

The small-signal response of region (IV) can be extracted from FW-EM simulations of the whole parasitic network by de-embedding the contribution of regions (I)–(III).

The model parameter extraction of this layout region can be more conveniently carried out by exploiting an equivalent "T" representation (see Fig. 5) of the finger region sub-network in Fig. 3(c). The Z matrix associated with this representation can be expressed by

$$Z = \begin{bmatrix} Z^G + Z^S & Z^S \\ Z^S & Z^D + Z^S \end{bmatrix} \tag{11}$$

where

$$Z^X = R^X + j\omega L^X + \frac{1}{j\omega C^X} \quad X = G, D, S. \tag{12}$$

Starting from Z^S , the elements C^S and L^S can be extracted by the linear regression of

$$\omega \cdot \mathrm{Im}(Z^S) = \omega \cdot \mathrm{Im}(Z_{12}) = \omega^2 L^S - \frac{1}{C^S} \tag{13}$$

and R^S can be determined by the regression

$$R^S = \mathrm{mean}\left(\mathrm{Re}\left(Z_{12}\right)\right) \tag{14}$$

where the mean value is calculated over the whole frequency range.

Once the source parasitic parameters are obtained, an identical procedure can be applied to $Z^G = Z_{11} - Z_S$ and $Z^D = Z_{22} - Z_S$ to obtain the gate and drain parasitic parameters.

Finally, a Δ-Y transformation applied to the capacitors allows getting the parasitic elements of the network in Fig. 3(c),

$$\begin{aligned} C^{GS} &= \frac{C^G C^S + C^D C^S + C^G C^D}{C^D} \\ C^{DS} &= \frac{C^G C^S + C^D C^S + C^G C^D}{C^G} \\ C^{GD} &= \frac{C^G C^S + C^D C^S + C^G C^D}{C^S}. \end{aligned} \tag{15}$$

D. Simulation Results

The FW-EM simulations (dc to 50 GHz), needed for the identification of the parasitic network models previously discussed, have been carried out by means of a 3-D planar FW-EM solver (i.e., SONNET by Sonnet Software). The geometry of the metal layer and the physical constants of interest have been determined by the foundry manual. Fig. 3(a), (d), and (f) shows the layouts exploited to perform the FW-EM simulations. The structures described in the foundry design kit (i.e., GDSII files) were slightly simplified in order to improve the simulation speed by reducing the number of dielectric layers to the ones reported in Fig. 6 (e.g., the four simulations needed to extract the lumped parasitic network of a 4×50 μm transistor required less than 2 h by means of an 8-core Intel-Xeon mini-workstation with 32 GB of RAM). As discussed in Section II, in the FW-EM simulations, the manifolds are described as n-port networks [see Fig. 3(d)] and successively reduced to two-port networks by using the formulation reported in [15].

The great advantage of the procedure proposed in this paper is that it can be straightforwardly implemented in any numerical computing environment or by means of a custom program in a high-level language. In our case, a MATLAB script has been developed that automatically extracts the values of the parasitic-network lumped elements starting from the FW-EM simulations.

As a case study, three GaN HEMTs have been considered with a gate length of 0.25 μm and a gate width of 8×50 μm, 4×50 μm (parasitic element values reported in Table I), and 2×50 μm.

As an example, Fig. 7 shows the S-parameters of the extracted parasitic network for the 8×50 μm device. The plot shows only the small-signal parameters of the passive parasitic network of the device without the active part. It is clear that the model not only reproduces perfectly the FW-EM simulations in the extraction range, but the predictions are still very accurate at

TABLE I
PARASITIC ELEMENTS EXTRACTED FOR A 4×50 μm GaN HEMT

GATE MANIFOLD		DRAIN MANIFOLD		VIA HOLE	FINGER		
$L^{GM} = 51\ pH$	$C_1^{GM} = 12\ fF$	$L^{DM} = 42\ pH$	$C_1^{DM} = 18\ fF$	$L^{VH} = 17.9\ pH$	$R^{G} = 327\ m\Omega$	$L^{G} = 0.5\ pH$	$C^{GS} = 82\ fF$
$R_{DC}^{GM} \approx 0\ m\Omega$	$C_2^{GM} = 14\ fF$	$R_{DC}^{DM} = 27\ m\Omega$	$C_2^{DM} = 22\ fF$	$R_{DC}^{VH} = 8.7\ m\Omega$	$R^{D} = 249\ m\Omega$	$L^{D} = 37\ pH$	$C^{DS} = 18\ fF$
$R_{RF}^{GM} = 714\ n\Omega/\sqrt{Hz}$		$R_{RF}^{DM} = 440\ n\Omega/\sqrt{Hz}$		$R_{RF}^{VH} = 384\ n\Omega/\sqrt{Hz}$	$R^{S} = 147\ m\Omega$	$L^{S} = 2.5\ pH$	$C^{GD} = 12\ fF$

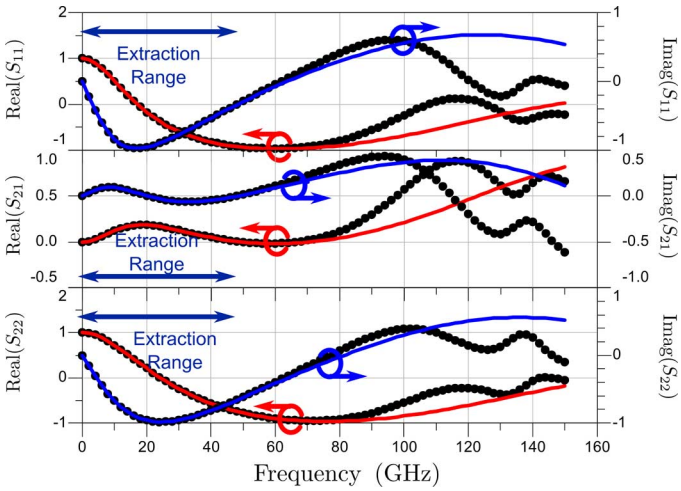

Fig. 7. Real and imaginary parts of S_{11}, S_{22}, and $S_{12} = S_{21}$ for the parasitic network of an 8×50 μm GaN HEMT. FW-EM simulations (dots) and extracted model predictions (lines) are in excellent agreement in the extraction range and in quite good agreement tens of gigahertz beyond it.

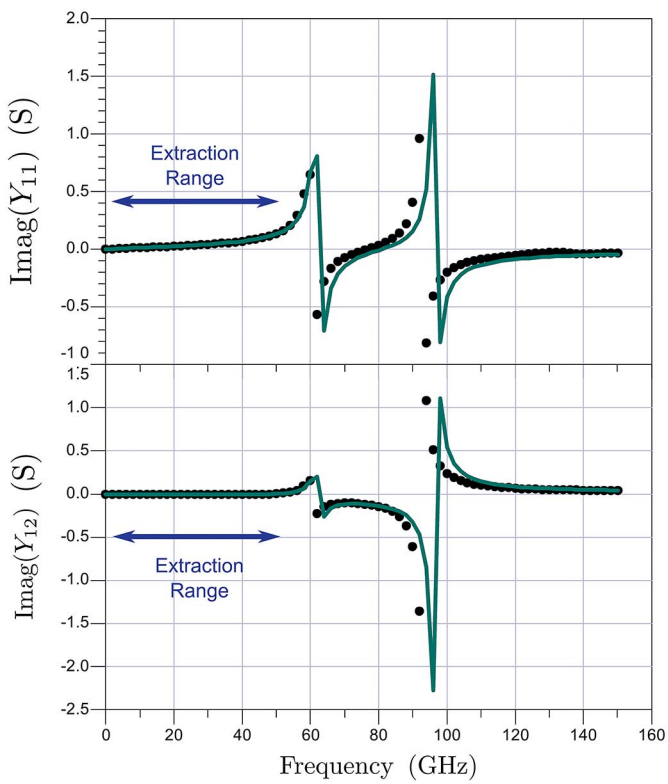

Fig. 8. Imaginary parts of Y_{11} and Y_{12} for the parasitic network of an 8×50 μm GaN HEMT. The extracted model (lines) predicts very accurately the resonance visible in the FW-EM simulations (dots) even far beyond the extraction frequency range.

higher frequencies. This assertion is confirmed in Fig. 8, where the prediction of the Y-parameters is shown. In particular, it has to be emphasized that the developed model shows good accuracy in reproducing the resonance frequencies even if they are well above the extraction frequency range.

E. Source Degenerated Device Predictions

One of the main advantages of the parasitic element identification based on this technique is the accurate definition of the transistor intrinsic planes. As a matter of fact, the small-signal models extracted by dc and S-parameter measurements [12], [17], like conventional foundry models, cannot separate the contribution to the source parasitic elements related to the via-holes from the one associated with the finger region. As a consequence, it is not possible to accurately identify the plane where the source degradation line has to be connected. For such a reason, conventional models are not very accurate for the performance prediction of degenerated devices. Indeed, as an example, the elimination of the source parasitic elements from the transistor equivalent circuit model and its replacement with a source degeneration line necessarily leads to neglect the parasitic contribution related to the source fingers. This assumption is confirmed by the experimental results and is true even when an accurate model of the degeneration line is available. However, the reliable performance prediction of a degenerated device is possible by using the technique proposed in this paper, which exploits accurate EM simulations of the different regions of the transistor layout to provide an accurate definition of the intrinsic planes. In such a case, the simple addition of a suitable degeneration line model provides accurate results.

III. NOISE AND PARASITIC DE-EMBEDDING PROCEDURE

Once the lumped parasitic network elements have been identified, the small-signal and noise intrinsic core model can be extracted by de-embedding the parasitic network contributions.

To this end, the noise correlation matrix $\mathbf{C_A}$ is defined starting from the transistor noise parameters by using the formulation in [20]–[22]

$$\mathbf{C_A^{Extr}} = 2kT\Delta f \cdot \begin{bmatrix} R_N & \frac{F_{\rm MIN}-1}{2} - R_N Y_{\rm OPT}^{*} \\ \frac{F_{\rm MIN}-1}{2} - R_N Y_{\rm OPT} & R_N |Y_{\rm OPT}|^2 \end{bmatrix} \quad (16)$$

where $F_{\rm MIN}$ is the minimum noise factor (also reported in logarithmic scale as $\rm NF_{MIN}$: minimum noise figure), $Y_{\rm OPT}$: the

TABLE II
NOISE CORRELATION MATRIX CONVERSION PARAMETERS

	$\alpha = A$	$\alpha = Y$	$\alpha = Z$
$\beta = A$	$\mathbf{I}$	$\begin{bmatrix} 0 & A_{12} \\ 1 & A_{22} \end{bmatrix}$	$\begin{bmatrix} 1 & -A_{11} \\ 0 & -A_{21} \end{bmatrix}$
$\beta = Y$	$\begin{bmatrix} -Y_{11} & 1 \\ -Y_{21} & 0 \end{bmatrix}$	$\mathbf{I}$	$\mathbf{Y}$
$\beta = Z$	$\begin{bmatrix} 1 & -Z_{11} \\ 0 & -Z_{21} \end{bmatrix}$	$\mathbf{Z}$	$\mathbf{I}$

A, **Y** and **Z** are the matrices representing the small-signal response of the network at the section where the conversion has to take place in ABCD, Y and Z formulation respectively; **I** is the identity matrix.

optimal source termination for noise, R_N: the noise equivalent resistance, k: the Boltzmann constant, T: the reference temperature (290 K), and Δf: the noise bandwidth (i.e., 1 Hz).

A. Noise De-Embedding

The de-embedding of the parasitic element noise contributions is similar to a classic small-signal parameter de-embedding procedure [17]: the contributions of series elements are eliminated by using Z-representations, while the shunt elements are eliminated by means of Y-representations. The formulas used for this de-embedding are [20]–[22]

$$\mathbf{C_Y^D} = \mathbf{C_Y} - 2kT\Delta f \mathrm{Re}(\mathbf{Y}^-) \tag{17}$$

for the shunt elements and

$$\mathbf{C_Z^D} = \mathbf{C_Z} - 2kT\Delta f \mathrm{Re}(\mathbf{Z}^-) \tag{18}$$

for the series elements. In (17) and (18), $\mathbf{C_Y^D}$ and $\mathbf{C_Z^D}$ are the resulting de-embedded noise correlation matrices, $\mathbf{C_Y}$ and $\mathbf{C_Z}$ are the starting noise correlation matrices, while $\mathbf{Y}^-$ and $\mathbf{Z}^-$ are the small-signal parameter matrices associated with the passive network to be de-embedded.

In the noise de-embedding procedure, the noise correlation matrix representation must be converted from Y to Z or $ABCD$, and vice versa. The formula to properly convert those matrices is as follows:

$$\mathbf{C_\beta}'' = \mathbf{T} \times \mathbf{C_\alpha}' \times \mathbf{T}^* \tag{19}$$

where matrix $\mathbf{T}$ depends on the parameters α and β, which indicate, as reported in Table II, the formulation of the starting noise correlation matrix $\mathbf{C}'$ and the converted noise correlation matrix $\mathbf{C}'$, respectively. As an example, the $\mathbf{T}$ matrix that converts a Z noise correlation matrix to an $ABCD$ one is the matrix in column $\alpha = Z$ and row $\beta = A$.

It is clear that the small-signal parameters at each section of the parasitic network are also needed in order to convert the noise correlation matrix representation (e.g., $\mathbf{C_Z}$ to $\mathbf{C_Y}$). Thus, the small-signal parameters $\mathbf{Y^{Extr}}$ also have to be measured

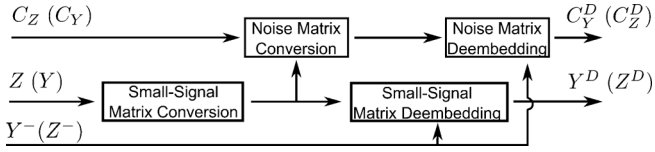

Fig. 9. De-embedding "core-function" flowchart: this function performs matrix representation conversion and de-embeds the noise correlation matrix $\mathbf{C_Z}$ ($\mathbf{C_Y}$), as well as the small-signal parameter matrix $\mathbf{Z}$ ($\mathbf{Y}$) from the matrix $\mathbf{Y}^-$ ($\mathbf{Z}^-$).

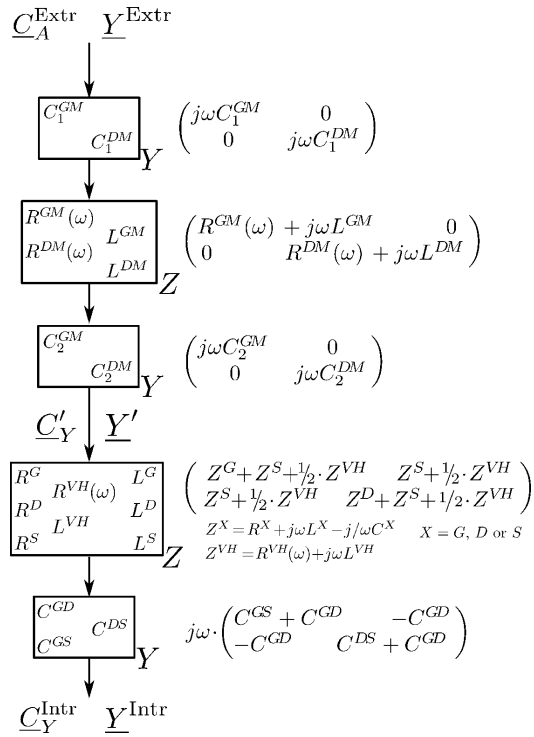

Fig. 10. Noise and small-signal de-embedding procedure flowchart. Each box represent one step of the procedure: the elements to be de-embedded are reported inside the boxes and the corresponding matrices are on the right of the boxes. The formulation used (Y or Z) is also reported at the corner of the boxes.

and a well-known small-signal de-embedding procedure [17] is exploited to achieve the small-signal response of the device at every section where a noise correlation matrix conversion is performed.

Based on the above considerations, the flowchart of the *core-function*, which performs noise de-embedding, small-signal de-embedding, and matrix conversion, is shown in Fig. 9.

The complete de-embedding procedure is composed of five steps, as represented in Fig. 10. The procedure is applied starting from the extrinsic plane of the device going towards the intrinsic core. At each step, the core function in Fig. 9 is applied to de-embed a group of lumped elements (in the Y-formulation for shunt elements or the Z-formulation for series ones). Thus, starting from the extrinsic plane, the first capacitor of the drain and gate manifold is de-embedded using a Y-formulation, successively the procedure de-embeds resistors and inductors of the gate and drain manifolds using a Z-formulation; finally, after de-embedding the last two capacitors, the drain and gate manifold contributions are completely de-embedded.

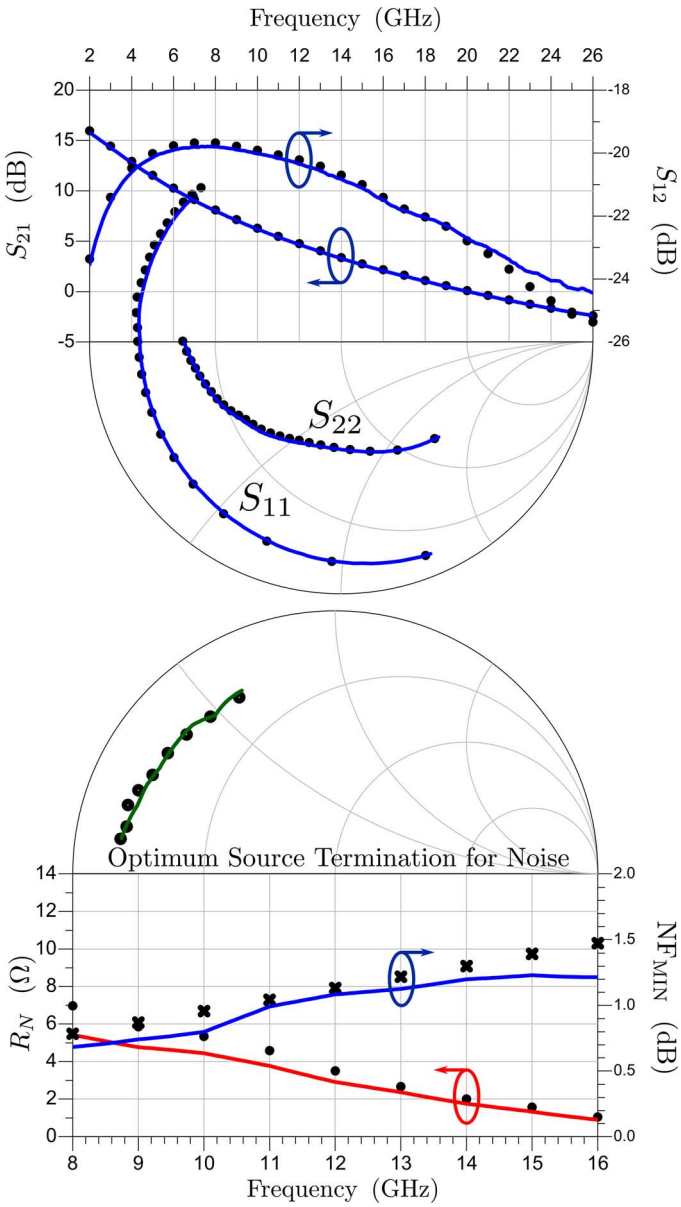

Fig. 11. Small-signal (*upper figure*) and noise parameters (*lower figure*) for the 8×50 μm GaN HEMTs. Measurements (symbols) and simulations (lines) obtained through scaling from the 4×50 μm model are in very good agreement.

The successive step of the procedure is to de-embed the via-hole and the series finger parasitic contributions by using a Z-representation. Once removed, the final contribution of the shunt parasitic capacitances associated with the fingers, the intrinsic noise, and small-signal matrices are achieved. It is worth noting that even the noiseless elements, such as capacitors or inductors, are taken into account in this procedure because they are needed to compute the intrinsic core small-signal model.

It should be observed that very simple scaling rules can be defined at the intrinsic plane of the transistor. In particular, the intrinsic small-signal and noise correlation matrices in the Y-representation of the 2×50 μm and 8×50 μm transistor can be determined, respectively, by dividing and multiplying by 2 the response of the 4×50 μm device. As an example, Fig. 11 shows the predicted small-signal response and noise behavior of the entire 8×50 μm device scaled from the 4×50 μm transistor.

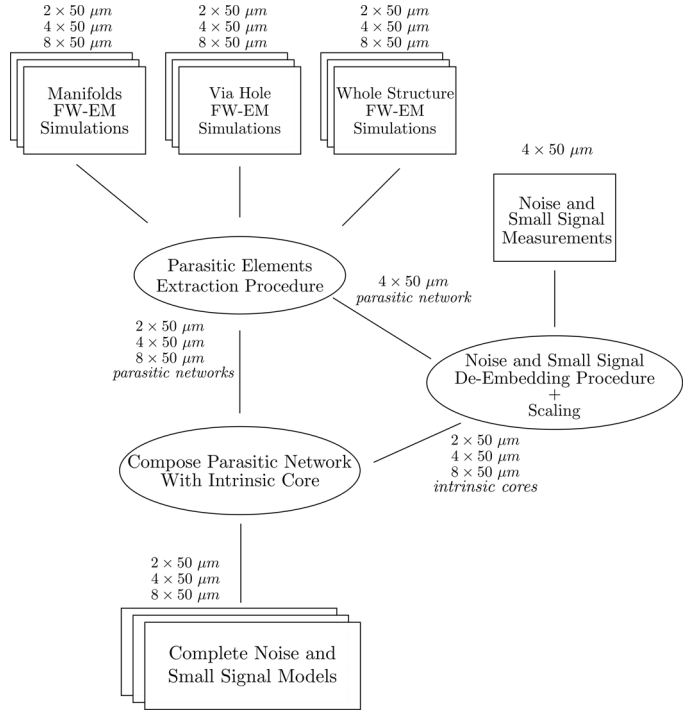

Fig. 12. Extraction flowchart for the low-noise transistor model.

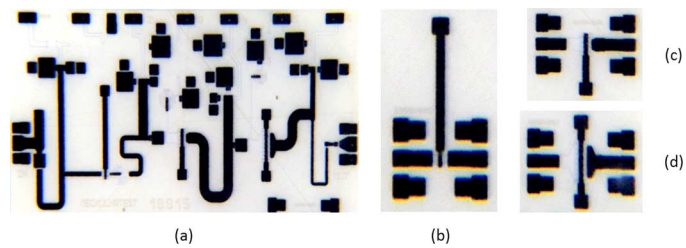

Fig. 13. Photographs of the: (a) developed MMIC LNA, chip size is 4×2 mm^2 and of the: (b) degenerated 2×50 μm, (c) 4×50 μm, and (d) 8×50 μm transistors.

Very good agreement between the model predictions and the measurements is evident.

The scaling procedure and the one described in Section II jointly create a powerful, fast, and simple model identification technique (the model extraction flowchart is shown in Fig. 12), which is able to provide robust low-noise scalable device models for LNA design. To this end, the intrinsic device noise and small-signal parameters can be stored in a Touchstone file, which can be read natively by the most diffused computer-aided design (CAD) tools (i.e., Keysight Advanced Design System). A MATLAB implementation of the described analytical identification procedure and the noise de-embedding technique is available online [23].

B. Experimental Model Identification

The 4×50 μm GaN HEMT (bias: $V_{D0} = 10$ V and $I_{D0} = 100$ mA/mm) noise parameters have been measured at various frequencies by using a source–pull procedure based on noise-figure measurements at different source impedances synthesized by a tuner [24], [25]. S-parameters also have been measured at the same bias condition. The intrinsic noise behavior and small-

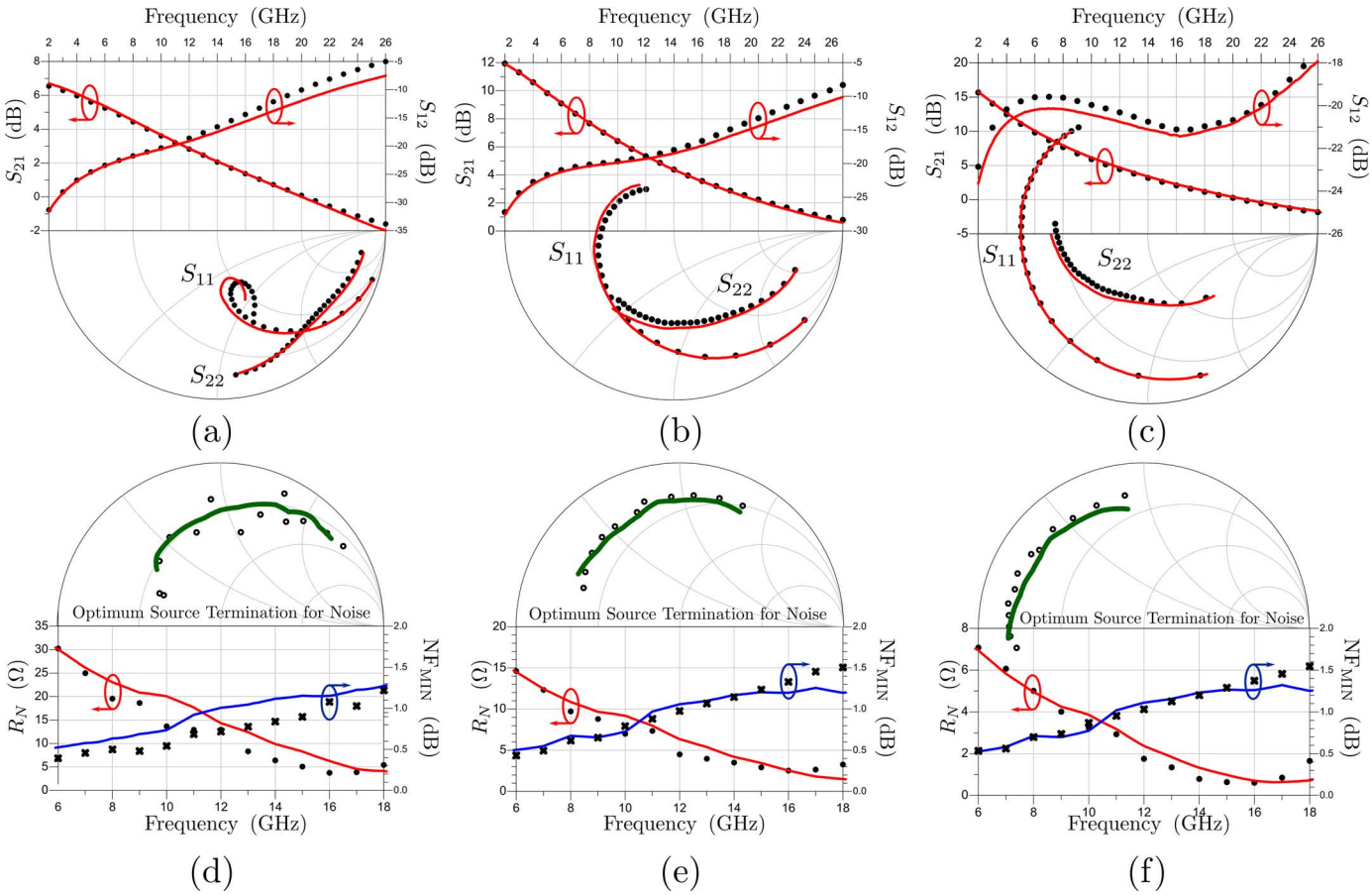

Fig. 14. (a)–(c) Small-signal and (d)–(f) noise parameters of the degenerated: (a) and (d) 2×50 μm, (b) and (e) 4×50 μm, and (c) and (f) 8×50 μm devices. Measurements (symbols) and model predictions (lines) are in good agreement. Bias condition: $V_{D0} = 10$ V and $I_{D0} = 100$ mA/mm.

signal response of the 4×50 μm device have been achieved by exploiting the procedure previously described, and scaled on the 2×50 μm and 8×50 μm devices by simply dividing and multiplying by 2 the response of the 4×50 μm device. Once obtained, the information about the intrinsic core of all the devices of interest, the parasitic lumped network, extracted separately for the 2×50 μm, 4×50 μm, and 8×50 μm devices by FW-EM simulations, has been added to the intrinsic model, in order to obtain the complete device model for the selected bias point. In fact, simple scaling rules, which can be effectively used for the intrinsic transistor, cannot be applied to the parasitic network, due to the complex relationships between the lumped component values and the layout geometry. The choice of using a separated parasitic network descriptions is a clear advantage of the proposed approach since conventional models need to adopt *peculiar* scaling rules, which necessarily degrade performance predictions for the scaled device.

IV. LNA Design

The 0.25-μm AlGaN/GaN on an SiC GH25-10 process of United Monolithic Semiconductors (UMS) (for more information about the technology process, see [26]) has been used to develop an LNA operating in the 12.75–14.8-GHz frequency band. The main design goals were 20 dB of gain and less than 2.0 dB of noise figure. In the preliminary design phase, the foundry model was adopted to determine that a three-stage LNA was needed to fulfill the specifications. In particular, in the first stage, a 2×50 μm transistor minimizes noise, and in addition, is more easily matchable to 50 Ω. In the second stage, a 4×50 μm transistor allows low-loss inter-stage matching, while providing fairly good noise figure and gain. Finally, in order to fulfill output power at 1 dB of gain compression and linearity requirements, a 8×50 μm transistor has been chosen for the third stage. The optimal bias point has been found to be 10 V of drain voltage and 100 mA/mm of drain current for all three stages.

As described in Section III-B, noise and small-signal measurements were carried out on the 4×50 μm GaN HEMT at the selected bias point, and as described in Section II-D, all the FW-EM simulations needed were performed, in order to develop the model by following the procedure outlined in Fig. 12. Once measurements and FW-EM simulations were carried out, model extraction took only a few minutes of work and computation.

By using the developed transistor models, it was possible to accurately study the effects of the source degeneration on the three transistors. In particular, the first transistor source degeneration was designed to get the optimum source impedance for gain (i.e., conjugate match) very close to the optimum impedance for noise. This enables to match the device for the best noise performance with a reasonable mismatch to the optimum source impedance for gain, thus preserving a good LNA input return loss. The second stage source degeneration was designed to have a good tradeoff between noise figure, gain,

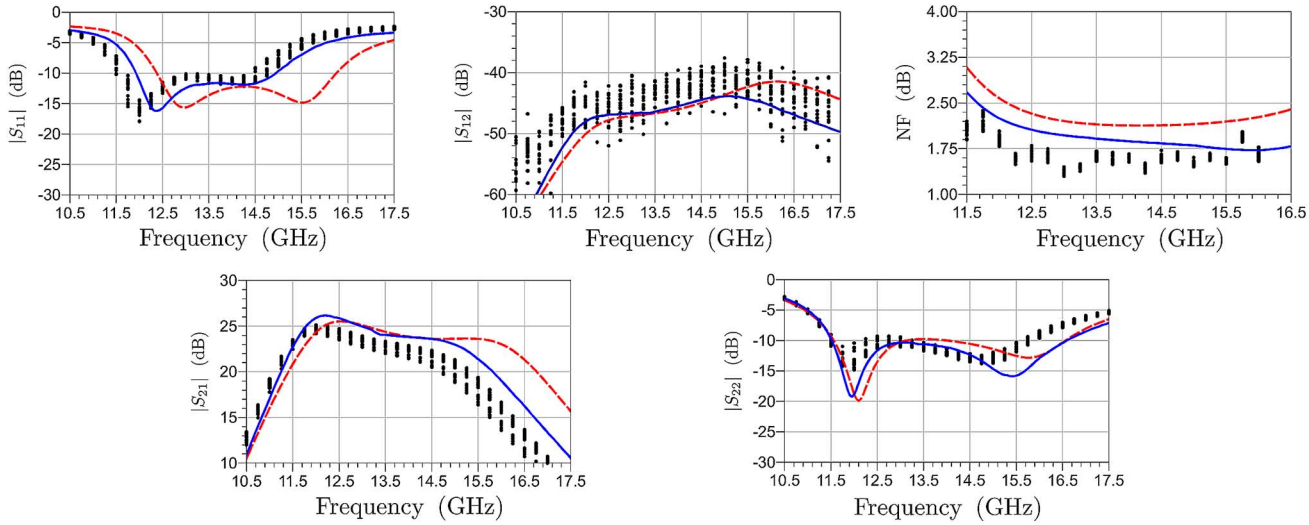

Fig. 15. Small-signal response of the three-stage LNA designed. Predictions with the proposed model (blue continuous lines in online version) and with a small-signal model (red dashed line in online version), extracted by dc and S-parameter measurements [12], are compared with the measurements carried out on 37 samples (circles). The noise figure (NF), which quantifies in logarithmic scale the degradation of the signal-to-noise ratio due to the amplifier, is also reported. The accuracy improvement is well evident.

and stability. A little source degeneration was also exploited in the third stage 8×50 μm transistor for device in-band stabilization.

A lot of care was taken in the matching network design. Since the losses of the input matching network directly add to the LNA noise figure, it was exhaustively optimized to keep losses below 0.2 dB.

The manufactured LNA and the transistor cut-outs (included for model validation purpose), are shown in Fig. 13.

In Fig. 14, a comparison between the measured S-parameters and noise performance of the three degenerated devices and the model predictions are reported; the agreement is very good. It is worth noticing that the predictions are still very good even if the 2×50 μm and the 4×50 μm have a single-side degeneration (i.e., one via-hole is absent) and the device is not symmetrical anymore.

In Fig. 15, the performance of the designed LNA is reported; the simulated predictions are in good agreement with the measurements, carried out on 37 samples, and the gain and noise figure specifications are completely fulfilled in the band of interest. To provide a clearer comparison of the proposed approach with existent ones, the figure also reports, for a degenerated device, predictions of a conventional model extracted on the basis of dc and S-parameter measurements [12]. It should be pointed out that the two models show the same accuracy level when the nondegenerated device is considered; whereas the different level of accuracy in the presence of source degeneration is well evident. As previously discussed, the poor predictions of the conventional model are due to an incorrect identification of the device intrinsic plane. This is clearly independent on the particular model formulation adopted. On the contrary, an EM-based model can identify with high accuracy the intrinsic plane position and provide great accuracy in the performance estimation of a degenerated device. These results confirmed that an approach based on EM simulations is useful not only when the design involves frequencies near the upper limit of the chosen technology [16] (i.e., 20 GHz), but also when nonstandard device configurations have to be used.

V. Conclusion

A new low-noise transistor model and associated identification procedure has been developed, which is based on FW-EM simulations, as well as noise and S-parameter measurements. The proposed technique allows identifying in a short time a robust scalable low-noise model suitable for LNA design. In particular, layout modifications can be accounted for, thus accurately predicting the noise behavior and small-signal response of degenerated devices. Moreover, the described procedure is very robust since it does not require any numerical optimization.

The described procedure has been exploited to identify three low-noise HEMT models starting from a single set of small-signal and noise measurements. Successively, an LNA has been designed by using the extracted models and the excellent quality of the predictions on both the degenerated devices and the LNA has been proven.

References

[1] M. Rudolph *et al.*, "Analysis of the survivability of GaN low-noise amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 1, pp. 37–43, Jan. 2007.

[2] S. Colangeli, A. Bentini, W. Ciccognani, E. Limiti, and A. Nanni, "GaN-based robust low-noise amplifiers," *IEEE Trans. Electron Devices*, vol. 60, no. 10, pp. 3238–3248, Oct. 2013.

[3] S. Nuttinck, E. Gebara, J. Laskar, and M. Harris, "High-frequency noise in AlGaN/GaN HFETs," *IEEE Microw. Wireless Compon. Lett*, vol. 13, no. 4, pp. 149–151, Apr. 2003.

[4] S. Lee, K. J. Webb, V. Tialk, and L. F. Eastman, "Intrinsic noise equivalent-circuit parameters for AlGaN/GaN HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 5, pp. 1567–1577, May 2003.

[5] C. Sanabria, H. Xu, T. Palacios, A. Chakraborty, S. Heikman, U. Mishra, and R. York, "Influence of epitaxial structure in the noise figure of AlGaN/GaN HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 53, no. 2, pp. 762–769, Feb. 2005.

[6] Z. H. Liu, S. Arulkumaran, G. I. Ng, and T. Xu, "Improved microwave noise performance by SiN passivation in AlGaN/GaN HEMTs on Si," *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 6, pp. 383–385, Jun. 2009.

[7] L. Boglione, "Considerations on the $4NT_0/T_m$ ratio and the noise correlation matrix of active and passive two-port networks," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, pp. 4145–4153, Dec. 2013.
[8] M. Rudolph and R. Doerner, "Bias-dependent Pospieszalski noise model for GaN HEMT devices," in *Proc. German Microw. Conf.*, Aachen, Germany, Mar. 2014, pp. 1–4.
[9] M. Rudolph and R. Doerner, "Towards a large-signal noise model for GaN HEMT devices," in *Proc. 8th Eur. Microw. Integr. Circuits Conf.*, Nuremberg, Germany, Oct. 2013, pp. 484–487.
[10] S. Colangeli, A. Bentini, W. Ciccognani, and E. Limiti, "Polynomial noise modeling of silicon-based GaN HEMTs," *Int. J. Numer. Model.*, vol. 27, no. 5–6, pp. 812–821, Sep.–Dec. 2014.
[11] A. Nalli *et al.*, "A scalable HEMT noise model based on FW-EM analyses," in *Proc. 9th Eur. Microw. Integr. Circuits Conf.*, Rome, Italy, Oct. 2014, pp. 1420–1423.
[12] *"GH25-10 User Guide for the DK 2.3,"* United Monolithic Semicond., Villebon-sur-Yvette, France, 2014.
[13] D. Resca, A. Raffo, A. Santarelli, G. Vannini, and F. Filicori, "Scalable equivalent circuit FET model for MMIC design identified through FW-EM analyses," *IEEE Trans. Microw. Theory Techn.*, vol. 57, no. 2, pp. 245–253, Feb. 2009.
[14] S. J. Mahon *et al.*, "LNA design based on an extracted singlegate finger model," in *Proc. IEEE Compound Semicond. Integr. Circuits Symp.*, Monterey, CA, USA, Oct. 2010, pp. 1–4.
[15] D. Resca *et al.*, "Scalable nonlinear FET model based on a distributed parasitic network description," *IEEE Trans. Microw. Theory Techn.*, vol. 56, no. 4, pp. 755–766, Apr. 2008.
[16] D. Resca *et al.*, "A distributed approach for millimetre-wave electron device modelling," in *Proc. 1st Eur. Microw. Integr. Circuits Conf.*, Manchester, U.K., Sep. 2006, pp. 257–260.
[17] G. Dambrine, A. Cappy, F. Heliodore, and E. Playez, "A new method for determining the FET small-signal equivalent circuit," *IEEE Trans. Microw. Theory Techn.*, vol. 7, no. 36, pp. 1151–1159, Jul. 1988.
[18] J. C. Rautio and V. Demir, "Microstrip conductor loss models for electromagnetic analysis," *IEEE Trans. Microw. Theory Techn.*, vol. 51, no. 3, pp. 915–921, Mar. 2003.
[19] F. Schnieder and H. Wolfgang, "Model of thin-film microstrip line for circuit design," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 1, pp. 104–110, Jan. 2001.
[20] R. A. Pucel, W. Struble, R. Hallgren, and U. L. Rohde, "A general noise de-embedding procedure for packaged two-port linear active devices," *IEEE Trans. Microw. Theory Techn.*, vol. 40, no. 11, pp. 2013–2024, Nov. 1992.
[21] S. A. Maas, *Noise in Linear and Nonlinear Circuits*. Norwood, MA, USA: Artech House, 2005.
[22] G. Crupi and D. M. M.-P. Schreurs, *Microwave De-Embedding: From Theory to Applications*. Oxford, U.K.: Academic, 2013.
[23] A. Nalli, "Transistor small-signal and noise model identification procedure," Univ. Degli Studi di Ferrara, Ferrara, Italy, 2015. [Online]. Available: http://endif.unife.it/it/ricerca-1/laboratori-di-ricerca/etlab/download
[24] A. Caddemi, G. Martines, and M. Sannino, "HEMT for low noise microwaves: CAD oriented modeling," *IEEE Trans. Microw. Theory Techn.*, vol. 40, no. 7, pp. 1441–1445, Jul. 1992.
[25] A. Caddemi, G. Crupi, E. Fazio, S. Patanè, and G. Salvo, "Remarks of an extensive investigation on the microwave HEMT behavior under illumination," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 2, pp. 102–104, Feb. 2014.
[26] D. Floriot *et al.*, "GH25-10: New qualified power GaN HEMT process from technology to product overview," in *Proc. 9th Eur. Microw. Integr. Circuits Conf.*, Rome, Italy, Oct. 2014, pp. 225–228.

Andrea Nalli (S'12) was born in Rovigo, Italy, in 1987. He received the M.S. degree (with honors) in engineering and technologies for telecommunications and electronics and Ph.D. degree in information engineering from the University of Ferrara, Ferrara, Italy, in 2011 and 2015, respectively.

Since 2012, he has been with the Engineering Department, University of Ferrara. His research activity is mainly oriented to nonlinear electron device (ED) characterization and modeling for microwave application.

Dr. Nalli was the recipient of a Ph.D. scholarship from the University of Ferrara in 2011.

Antonio Raffo (S'04–M'07) was born in Taranto, Italy, in 1976. He received the M.S. degree in electronic engineering (with honors) and Ph.D. degree in information engineering from the University of Ferrara, Ferrara, Italy, in 2002 and 2006, respectively.

Since 2002, he has been with the Engineering Department, University of Ferrara, where he is currently a Research Associate and teaches courses in semiconductor devices and electronic instrumentation and measurement. He has coauthored over 100 publications in international journals and conferences. His research activity is mainly oriented to nonlinear electron device characterization and modeling and circuit-design techniques for nonlinear microwave and millimeter-wave applications.

Dr. Raffo is a member of the IEEE MTT-11 Technical Committee. He serves as an associate editor for the *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*. He also served as Technical Program chair for the IEEE International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC), Leuven, Belgium, 2014.

Giovanni Crupi (S'04–M'12–SM'13) was born in Lamezia Terme, Italy, in 1978. He received the M.Sc. degree (*cum laude*) in electronic engineering and Ph.D. degree from the University of Messina, Messina, Italy, in 2003 and 2006, respectively.

He is currently an Assistant Professor with the University of Messina, where he teaches "Microwave Electronics" and "Bioengineering." Since 2005, he has been a repeat Visiting Scientist with the University of Leuven (KU Leuven) and with the Interuniversity Microelectronics Center (IMEC), Leuven, Belgium. He has authored or coauthored approximately 100 publications in international journals and conferences and two book chapters. He coedited *Microwave De-embedding: From Theory To Applications* (Academic, 2013). He serves as an associate editor for the *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*. His main research interests include small- and large-signal modeling of advanced microwave devices.

Dr. Crupi serves as the Technical Program Committee chair for the IEEE International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC), Taormina, Italy, 2015. He is a member of the Technical Program Committee of IEEE INMMiC and IEEE TELSIKS. He is also the chair of the IEEE Microwave Theory and Techniques Society (MTT-S) Fellowship program.

Sara D'Angelo received the M.S. degree in electronic engineering from the University of Ferrara, Ferrara, Italy, in 2007, and the Ph.D. degree from the University of Bologna, Bologna, Italy, in 2011. Her doctoral dissertation concerned the electrothermal characterization and nonlinear modeling of GaN transistors for microwave applications.

In September 2011, she joined MEC srl, Bologna, Italy, where she is currently involved with monolithic microwave integrated circuit (MMIC) design, hybrid module design, passive and active device characterization, and modeling.

Davide Resca (S'05–M'09) received the Ph.D. degree from the University of Bologna, Bolgona, Italy.

He is currently a Senior Microwave Design Engineer with MEC srl, Bologna, Italy, which he joined in January 2009, as a MMIC Designer following his post-doctoral studies with the Department of Electronics, Computer Science and Systems (DEIS), University of Bologna. He is responsible for MMIC design, hybrid module design, passive and active device characterization, and modeling. His current research interests are advanced computer-aided design (CAD) techniques for microwave integrated circuit design, electromagnetic (EM) subcircuit advanced modeling, and planar filter synthesis and design.

Francesco Scappaviva received the Laurea degree in electronic engineering and Ph.D. degree in electronic engineering from the University of Bologna, Bologna, Italy, in 2004 and 2009, respectively.

In 2004, he joined the academic spin-off Microwave Electronics for Communication (MEC) srl, Bologna, Italy, as an RF Research Engineer. His research activities are mainly oriented to hybrid and monolithic microwave integrated circuit design and characterization. In 2009, he became Technical Manager with MEC srl, and in 2012, became a member of their Board of Directors. His main research interests are in the field of RF power amplifiers and microwave circuits for space applications and communication systems. Since 2010, he has been involved in the management of industrial and research programs.

Giuseppe Salvo (S'14) is currently working toward the Master's degree in electronic engineering at the University of Messina, Messina, Italy.

He has developed solid experience in the field of linear and noise characterization of discrete and on-wafer microwave devices with the Microwave Electronics Laboratory, University of Messina, where he has worked over the last two years in cooperation with the research staff on a project with the Italian Ministry of Education, University and Research. He serves as an Organizing Committee member for the IEEE International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC), Taormina, Italy, 2015.

Alina Caddemi (M'13) received the Electronic Engineering degree (with honors) and Ph.D. degree from the University of Palermo, Palermo, Italy, in 1982 and in 1987, respectively.

In 1984, she joined the University of Utah, Salt Lake City, UT, USA, as a Visiting Researcher. In 1985, she joined the University of Colorado at Boulder, Boulder, CO, USA, as a Visiting Researcher. From 1990 to 1998, she was with the University of Palermo, as a Research Assistant of microwave electronics. In 1998, she joined the University of Messina, Messina, Italy, where she is currently a Full Professor of electronics. She has authored or coauthored more than 220 papers on international scientific journals and conference proceedings. She is involved with the Reviewer's Board of national and international projects and serves as a reviewer for many international journals. Her research interest is in the field of microwave electronics and mainly concern temperature-dependent linear, nonlinear, and noise characterization techniques; cryogenic measurements and modeling of HEMTs; neural network modeling of devices; computer-aided design (CAD) and realization of hybrid low-noise circuits; and automation and control of microwave linear measurement systems.

Dr. Caddemi is an associate editor for the *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*. She is also on the Editorial Board of *Microwave Review*, a publication of the Serbia and Montenegro IEEE Microwave Theory and Techniques Society (IEEE MTT-S) Chapter and the Serbian National Society for Microwave Technique, Technologies and Systems. She serves as chair for the IEEE International Workshop on Integrated Nonlinear Microwave and Millimetre-wave Circuits (INMMiC), Taormina, Italy, 2015.

Giorgio Vannini (S'87–M'92) received the Laurea degree in electronic engineering and Ph.D. degree in electronic and computer science engineering from the University of Bologna, Bologna, Italy, in 1987 and 1992, respectively.

In 1992, he joined the Department of Electronics, University of Bologna, as a Research Associate. From 1994 to 1998, he was also with the Research Centre on Electronics, Computer Science and Telecommunication Engineering, National Research Council (CSITE), Bologna, Italy, where he was responsible for monolithic microwave integrated circuit (MMIC) testing and the Computer-Aided Design (CAD) Laboratory. In 1998, he joined the University of Ferrara, Ferrara, Italy, as an Associate Professor, where, since 2005, he has been a Full Professor of electronics. He is currently the Head of the Engineering Department, University of Ferrara. During his academic career, he has been a Teacher of applied electronics, electronics for communications, and industrial electronics. He is a cofounder of the academic spin-off Microwave Electronics for Communications (MEC) srl. He has coauthored over 240 papers devoted to electron device (ED) modeling, CAD techniques for MMICs, and nonlinear circuit analysis and design.

Dr. Vannini is a member of the Gallium Arsenide Application Symposium (GAAS) Association.