# Plan for a Greener Radio Unit: Partitioning, PA Architecture, and Advanced Linearization

Christopher Mayer

Analog Devices Inc.


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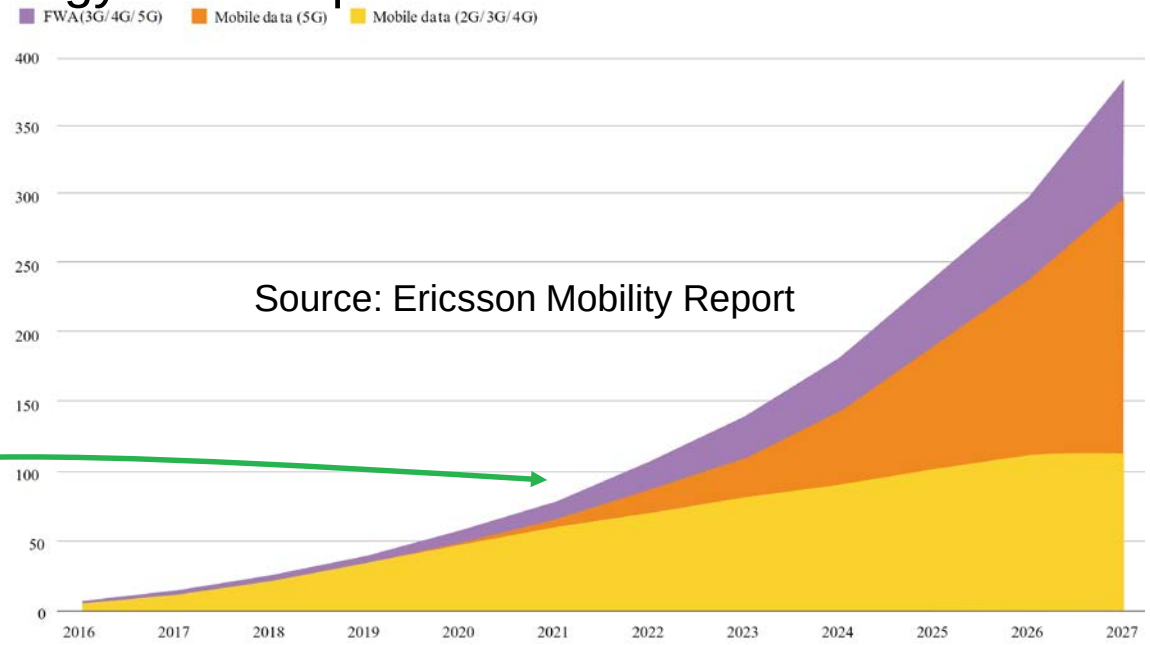
# 5G energy outlook

- Energy costs for Telecoms = 5-6% of opex [McKinsey, 2018]
- Currently 2G-4G networks average 15-20% percent of their overall power consumption in actual data traffic, and the rest “being ready” while idle. [Data Center Dynamics Magazine]
- 5G networks are up to 90% more energy efficient per traffic unit than 4G networks [Nokia & Telefonica]

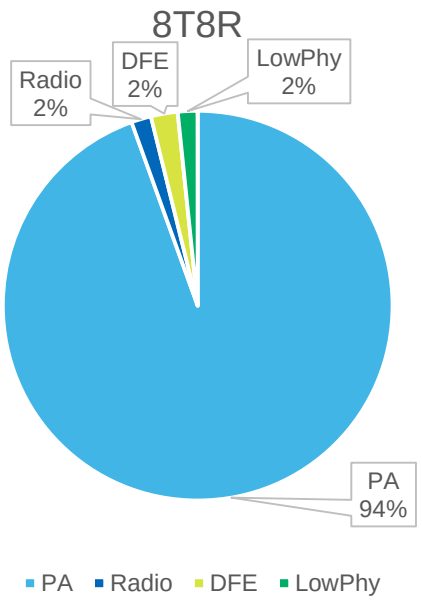
**Great! So what’s the problem?**

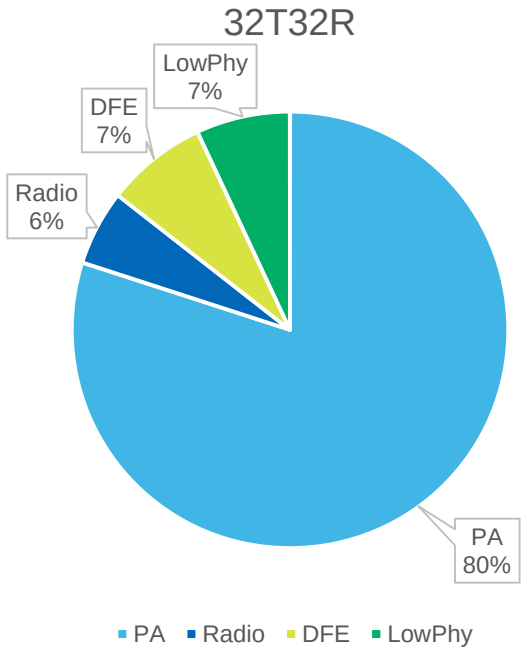
**Data usage is growing at 40-50% yearly!**

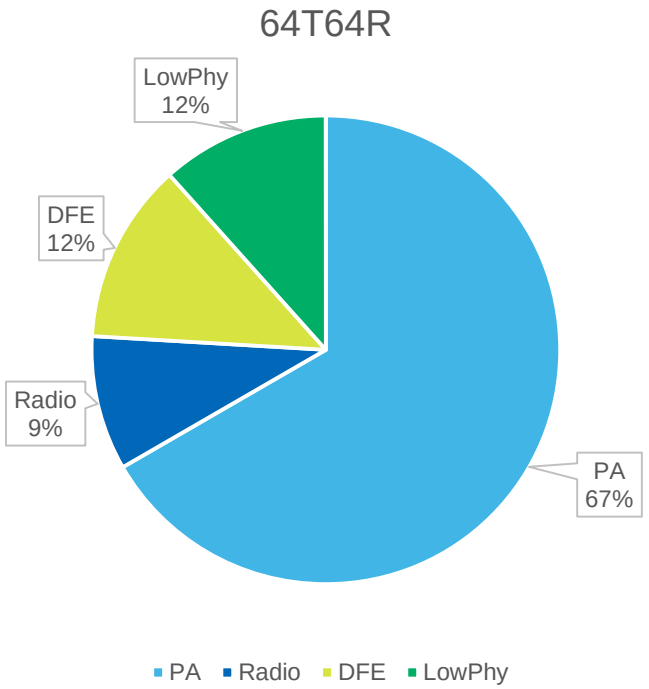



- *5G will double to triple energy consumption for mobile operators, once networks scale.* [MTN]

# RU Power: PA vs. radio vs. DFE vs. LowPhy



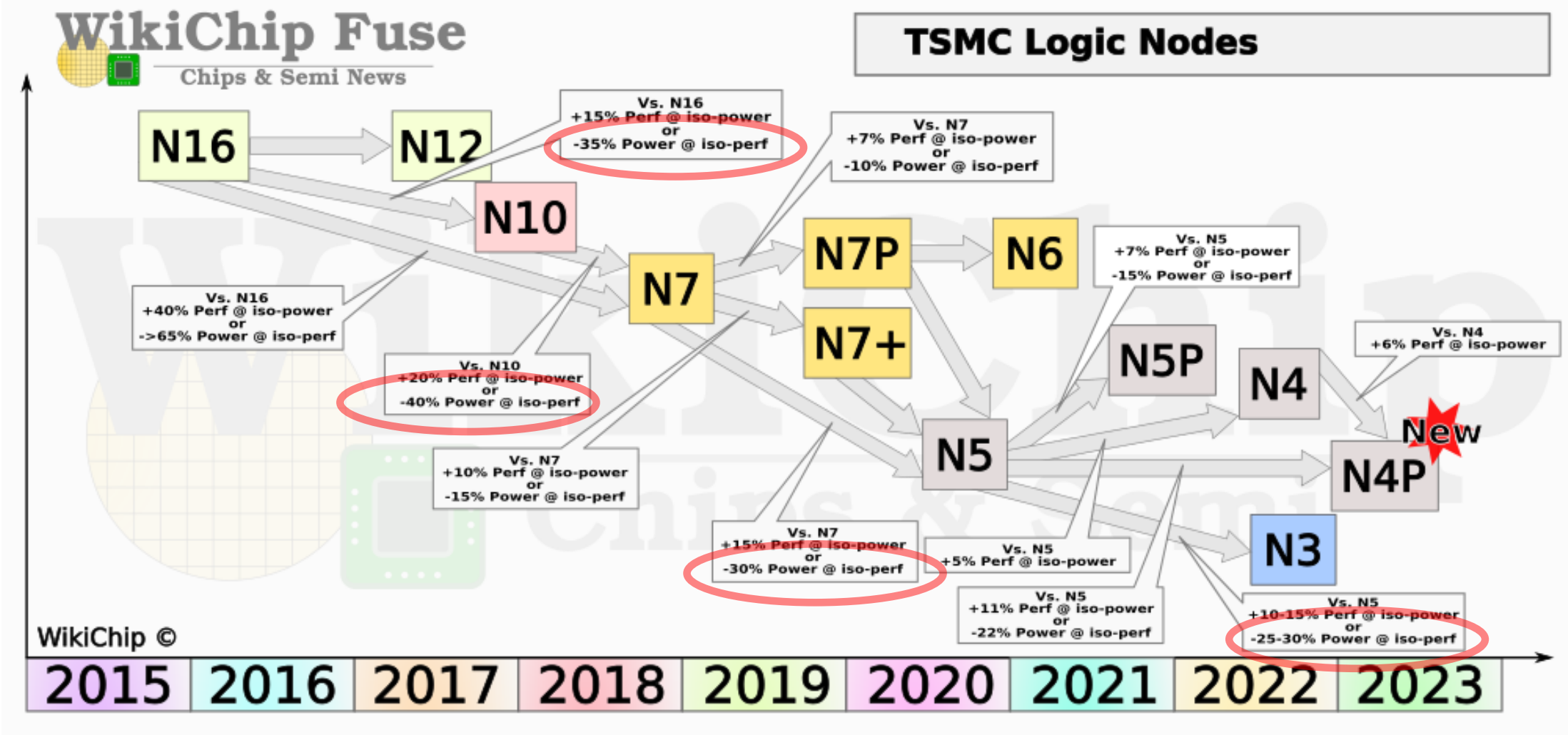

| | |
|---|---|
| 320W TRP (after 2dB post-PA loss) | TDD: 70% TX, 30% RX |
| PA operated at 3dB backoff (i.e. not full cell traffic), resulting in 39% PA efficiency vs. 45% | |

**On all systems, PA power still dominates.**

**DPD and PA technology are the major focus to raise PA efficiency.**

**At lower traffic levels (and idle), radio & digital power needs to scale also.**

# TSMC Process (power reductions @ iso-perf)



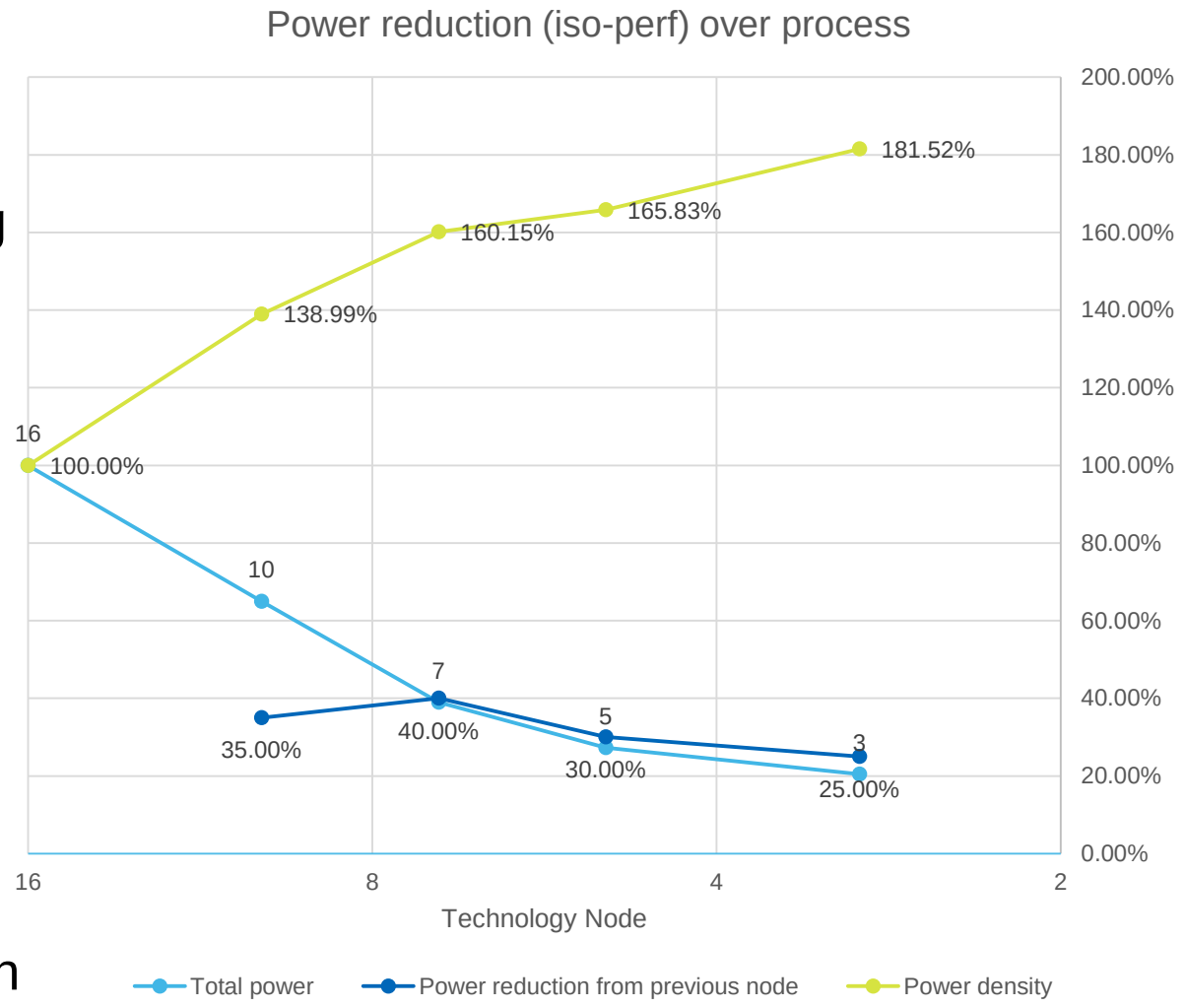
# Digital Power Metrics vs. Process

Trends:

- Voltage scaling is largely over → Modest power improvement (<= 25% / node expected) in future
- Transistor density (digital functions) still increasing linearly, but no longer exponentially
- Power density is increasing
  - Packaging and cooling challenges

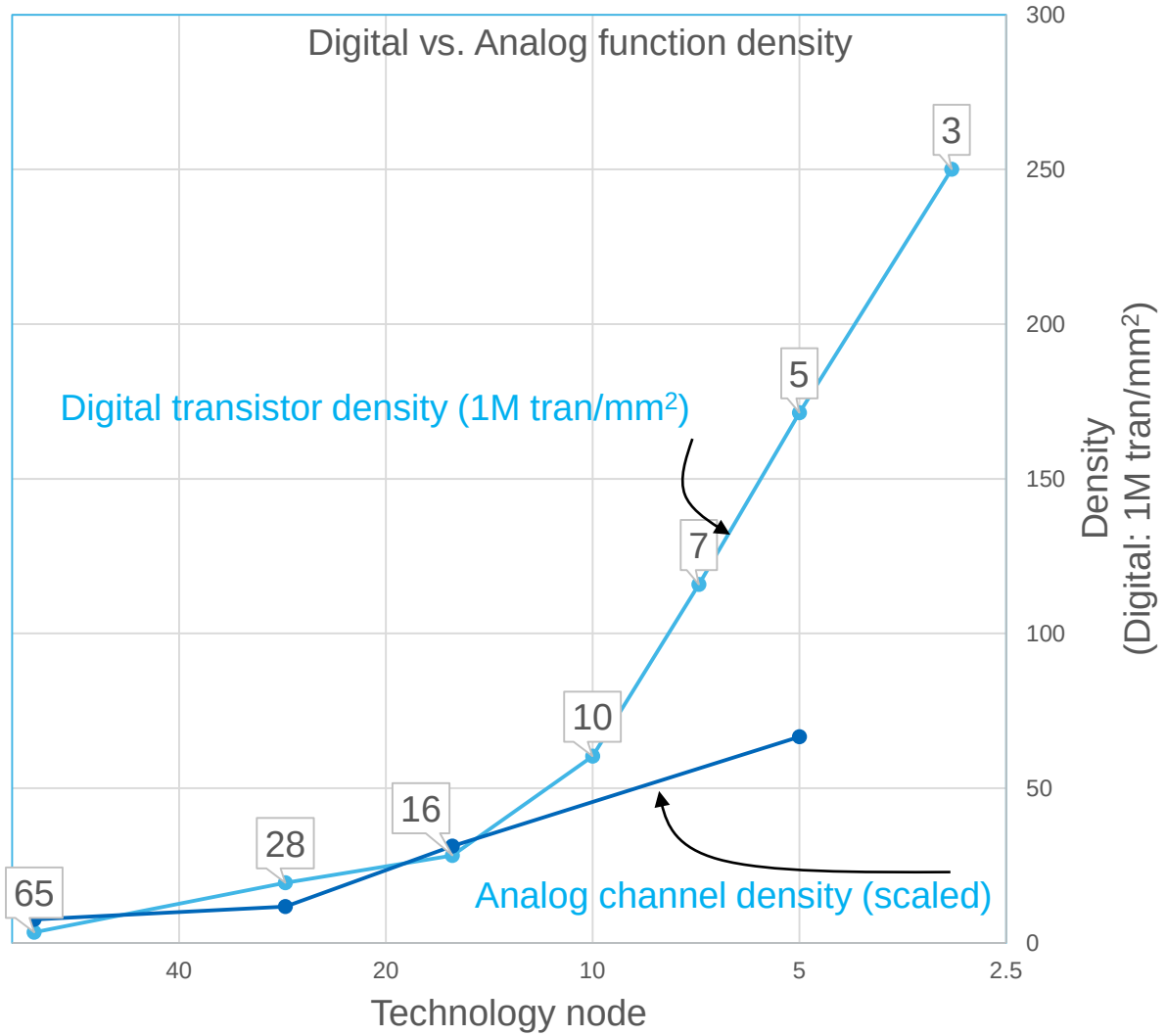
Conclusions:

- The main reason to push to lower nodes is to integrate more logic on a monolithic die
  - Not *better* logic, but *more* logic
- RF isolation and die temperature requirements do **not** point towards increased channel integration



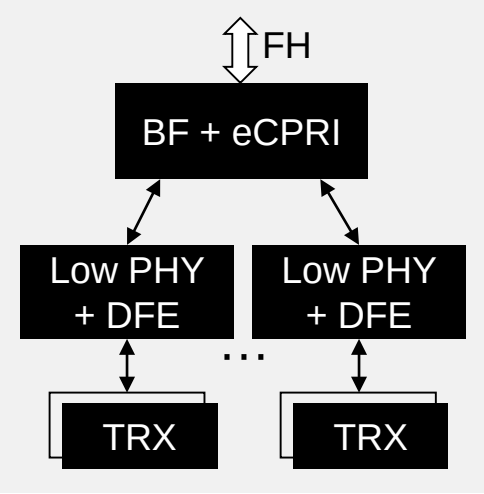
# Transceiver silicon density vs. process node

- Radio transceivers have roughly halved cost and power at each generation, even as bandwidth (OBW and IBW) increased
- This was made possible by architecture and circuit breakthrough developments
- Beyond 16nm, analog circuits no longer scale with digital, regardless of innovation
  - Analog performance can still increase… **but the cost will not be lower**
- Digital Predistortion (DPD) is a tradeoff:
  - DPD benefits from being in the lowest digital process node…
  - But interface bandwidth & power reduce when DPD is integrated with analog/RF



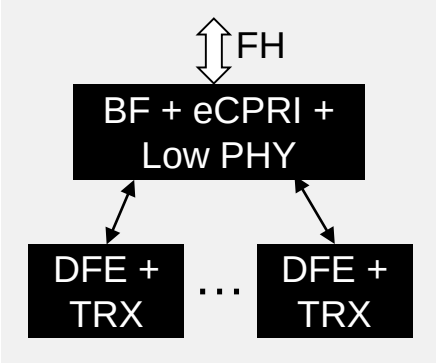
# mMIMO Radio Functional Partitioning

## Partition #1



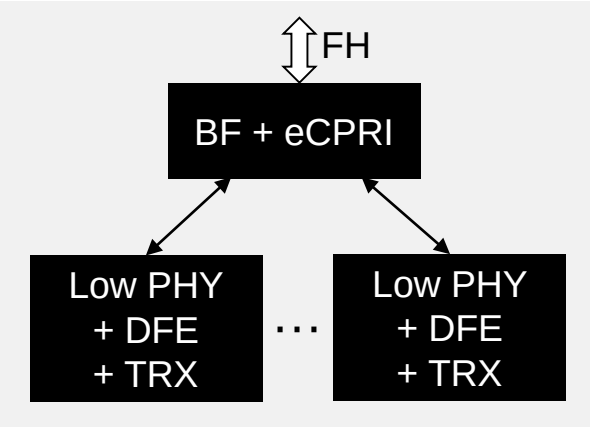

- In production
- Three layers → extra interconnect compared to other options
- Typically, 3 process nodes:
  - BF: 7nm
  - DFE: 14nm or lower
  - TRX: 16nm

## Partition #2




- In production
- Two layers → reduced interconnect.
- Two process nodes:
  - BF: 7nm
  - TRX+DFE: 16nm

## Partition #3




- Optimal architecture?
- Maximum offload of central BF functions → best beamformer.
- Next gen process nodes:
  - BF: 3nm?  2nm?
  - TRX+DFE: 7nm? 5nm?

# DPD Model Evolution

**Generalized Memory Polynomial (GMP)**

- Memory terms → equalization
- Cross terms → frequency dependent compensation
- All-purpose DPD

**Dynamic Deviation Reduction (DDR)**

- Improved frequency dependent compensation
- 3dB-4dB ACLR improvement on some wideband PAs.

**Charge Trap Compensation (CTC)**

- Semi-physical design with long time constants
- Trapped charge model of GaN PAs
- EVM boost for first symbol & low power symbols in dynamic waveforms

**Machine learning DPD optimization**

- ML techniques used to optimize DPD hardware resources
- Basis functions learned by ML (vs. standard orthogonal)
- Power savings (up to 50%) by optimizing away unnecessary terms

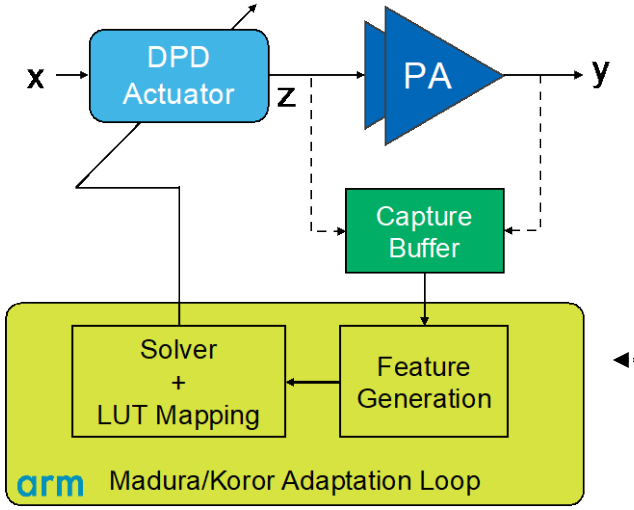
**Physics-inspired DPD**

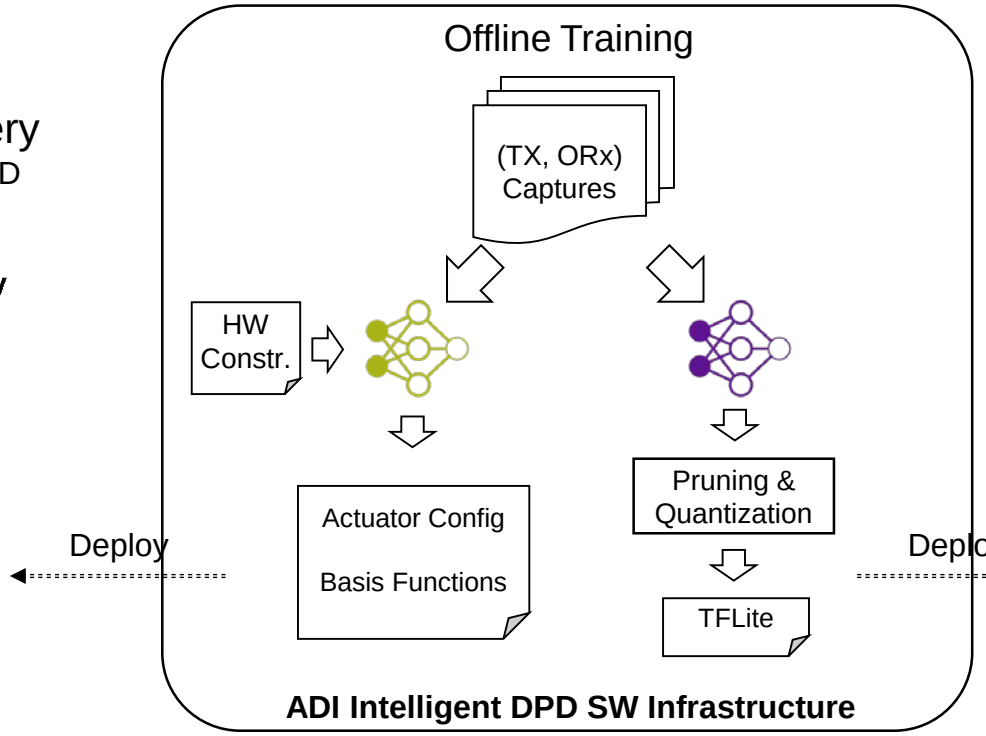
- Compensate effects measured on various high-power PAs
- Physics-inspired model trained with ML techniques
- SEM and ACLR improvements during power level changes at “medium” timescales

# Intelligent DPD

## Hardware-Driven Model Discovery

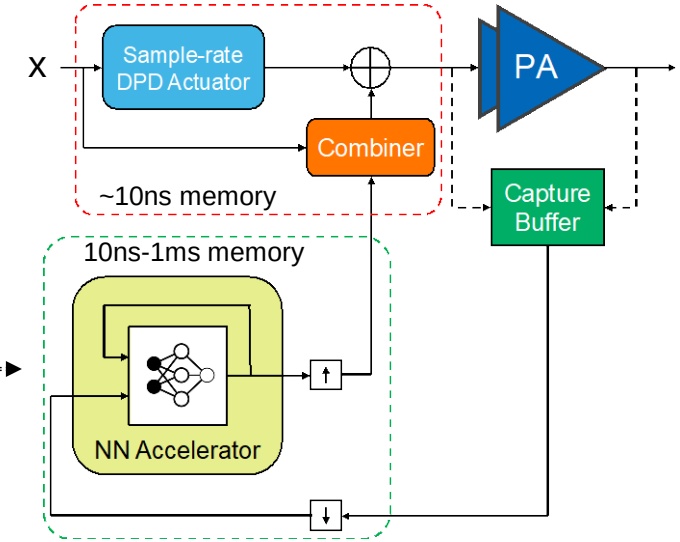
Algorithmically Enhance Sample-Rate DPD




## Neural Network Dynamic Compensation

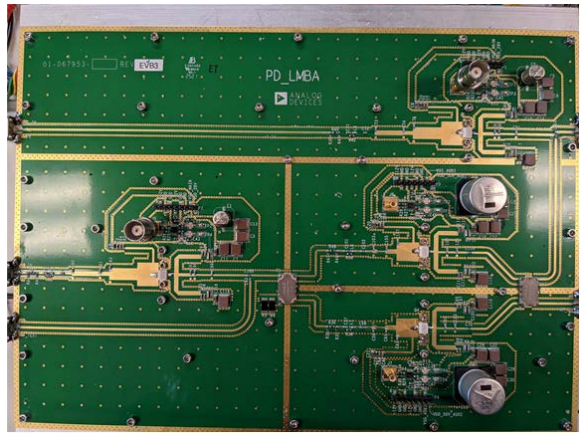
GaN Charge Trapping Correction & More

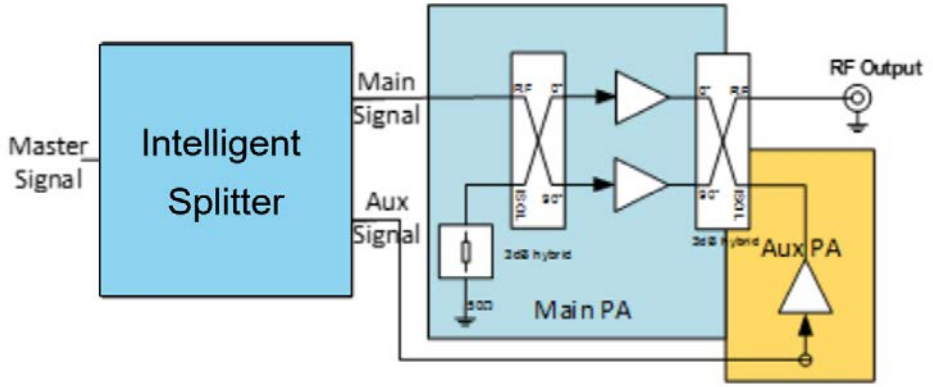


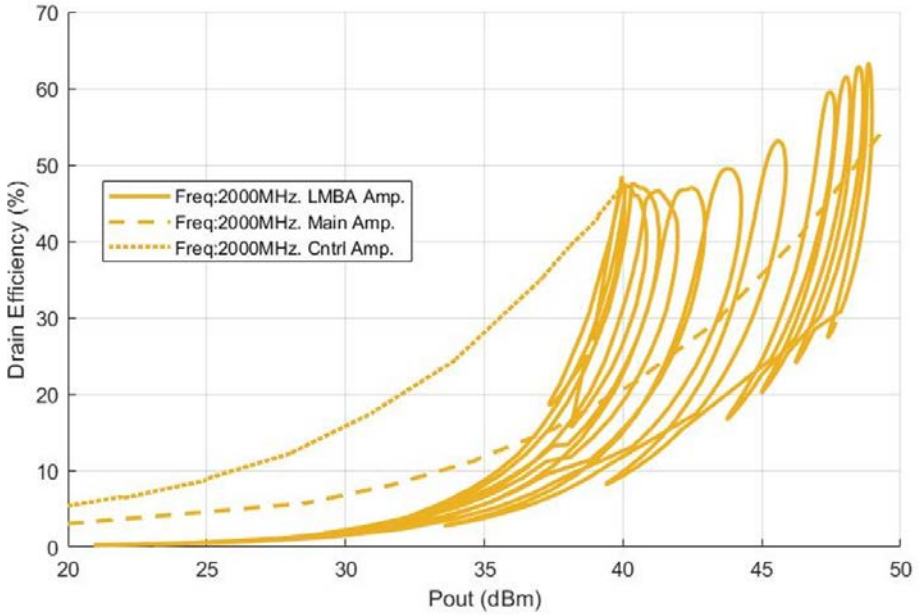

- **Hardware driven model discovery** optimizes use of hardware DPD resources
  - Can be used on current deployed products. Showing up to 50% power reduction
- **Neural Network Dynamic Compensation** is “next gen” DPD.
  - Better than “brute force” – structure designed to target classes of hardware impairments with longer timescales

# Beyond DPD: Alternate PA Architectures
## *Load Modulated Balanced Amplifier*

- Maintaining PA efficiencies at ever increasing bandwidths is a struggle, even for GaN architectures.
- The LMBA employs a **dual path architecture** whereby the aux PA load modulates the main PA
- Requires a second DAC path– but small signal radio has improved to where this is feasible
- Result: Higher efficiency over the PA's entire power range *even with large bandwidths*

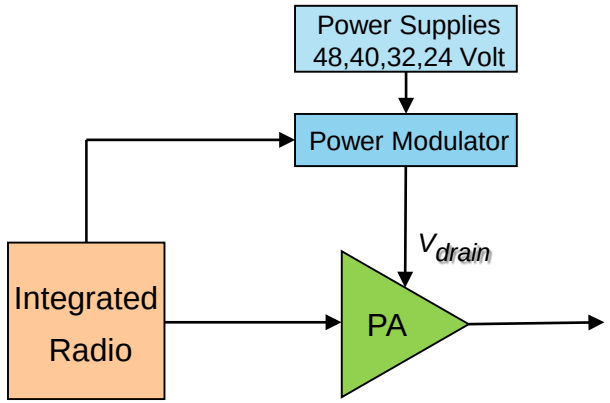


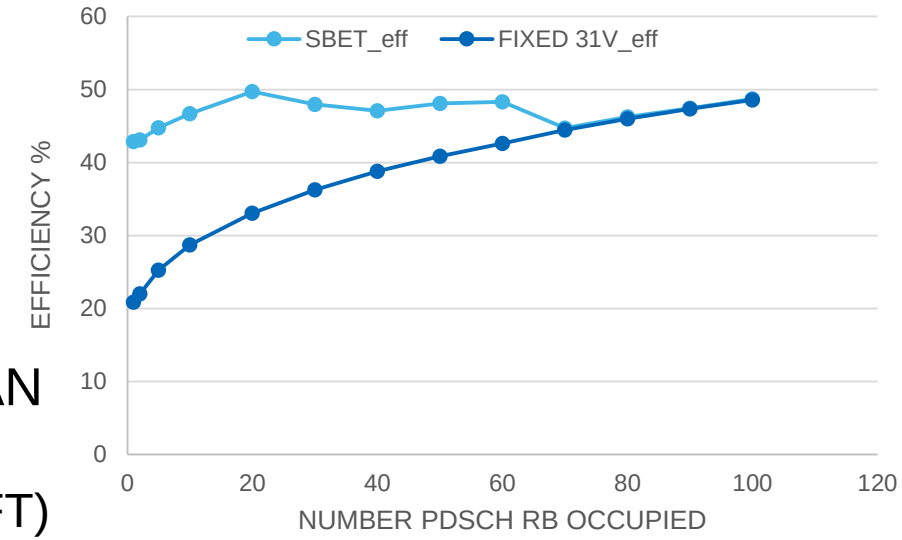



# Beyond DPD: Alternate PA Architectures
## *Symbol Based Envelope Tracking*

- Traditional Envelope Tracking requires a very fast modulator (or very sparse bandwidth)



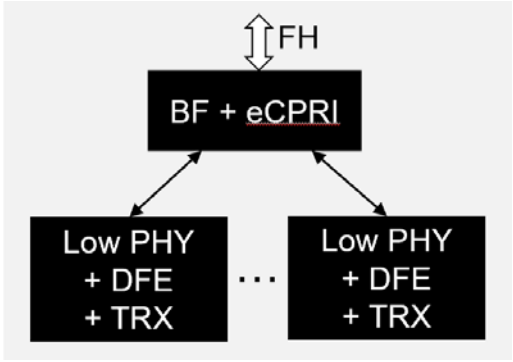

- Symbol based ET changes the PA DC drain voltage on symbol boundaries only
  - Reaps most of the power savings of Envelope Tracking
  - Moderates the power costs of the switching power modulator



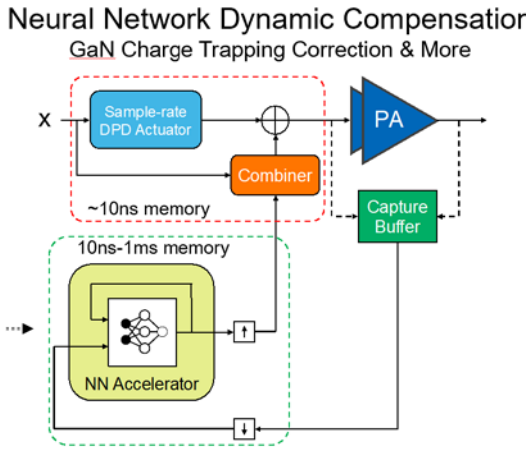

- Average basestation RMS power levels are ~ 33%
  - Biasing the PA to match the envelope preserves efficiency regardless of traffic level
- Symbol based ET is enabled by integration in the Open RAN 7.2 Split
  - Symbol RMS power computed in frequency domain (before IFFT) and fed forward to generate the dynamic control signals

# Plan for a Greener RU – Conclusions

- Partition matters
  - Minimize number of layers and interfaces
  - Combine digital with analog in best process node which supports analog RF
  - Perform beamforming (big digital) in most advanced process node




- Digital Predistortion matters
  - Knowledge of PA physics leads to most effective DPD systems
  - Machine learning and Neural Net are gaining traction in DPD systems




- Alternate PA technologies are just around the corner
  - "Dual path" PA drive architecture are now possible with lower cost / lower power small signal radio
  - LMBA is a promising wideband amplifier class
  - Symbol based envelope tracking raises efficiency across all power levels