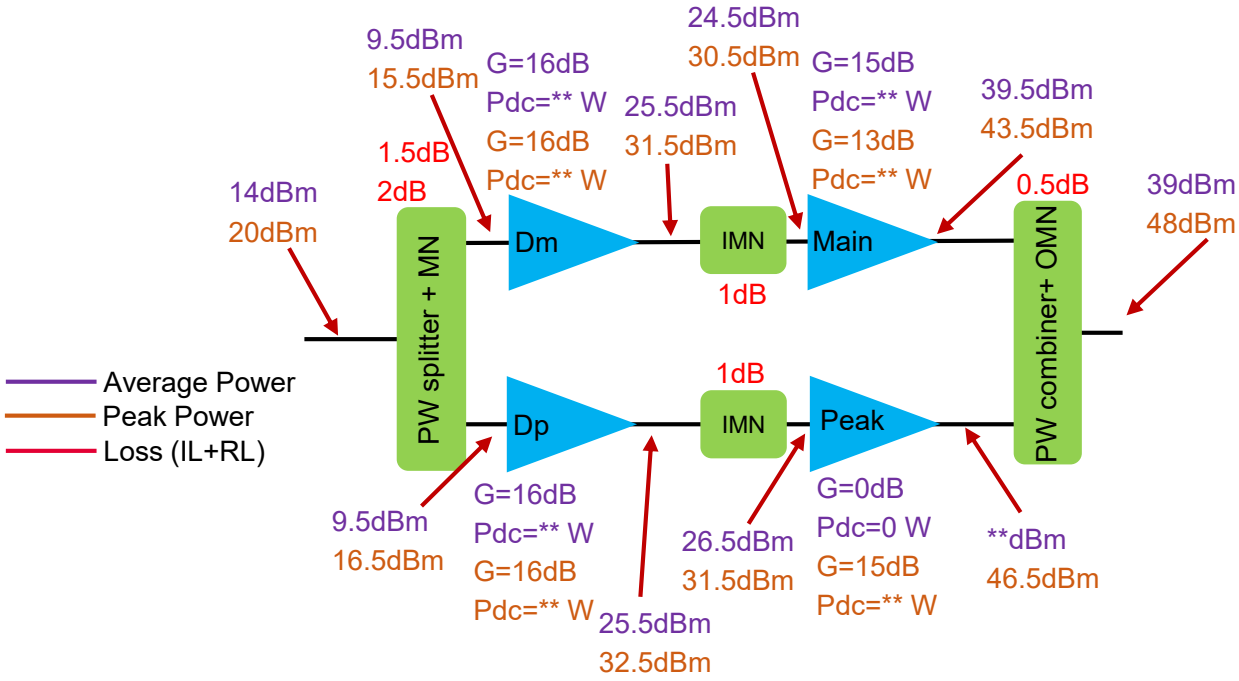
Mini-Pac Design Updates

Theepak Shoundrabalan
19.04.2022

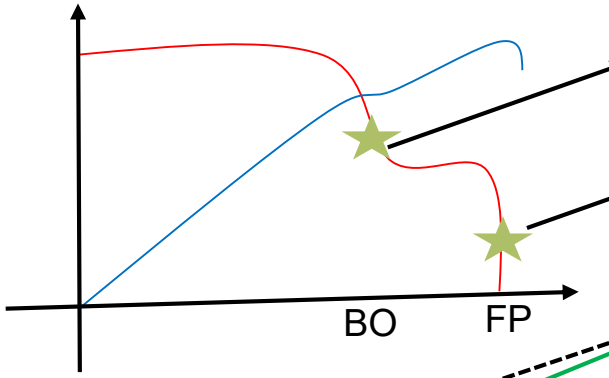
Content

- Dual driver Architecture-Draft
- Main, Peak and Driver Design criteria.
- Proposed Builds
- The current builds designed
- The expected performance
- Lessons learned
- Measurement result ,DOE1_3

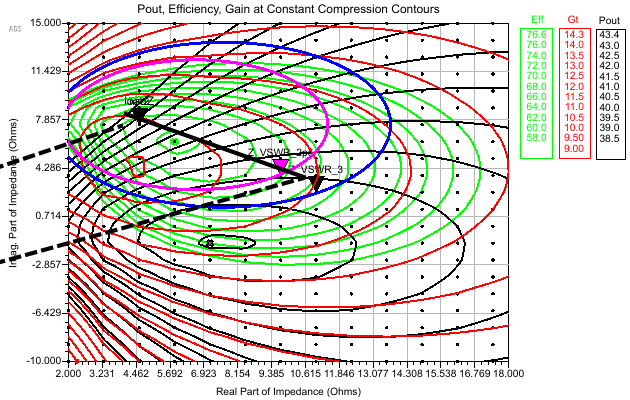
From: Dual driver Architecture-Draft (Alireza)

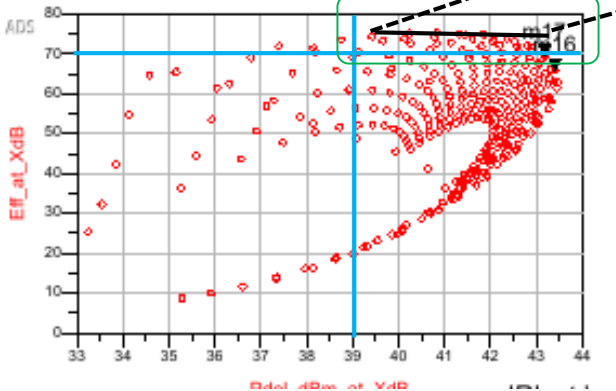


Main (From Pre-match Design Selection : Alireza)



The point with best gain (input Z)



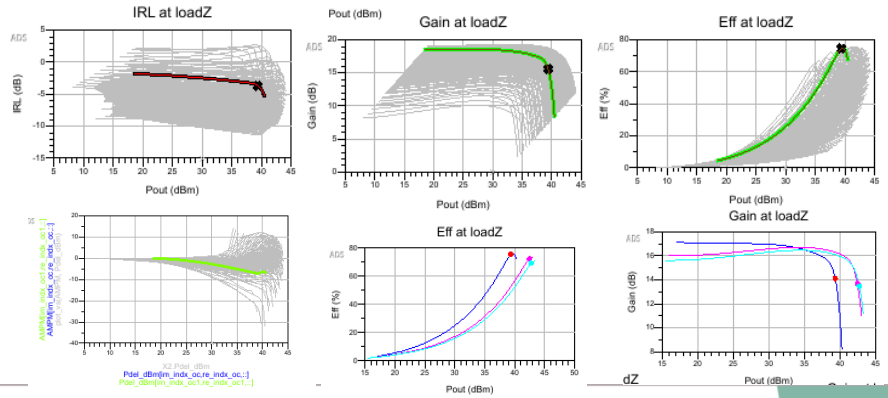


Zin➔

Gian➔

Eff➔

Pout➔



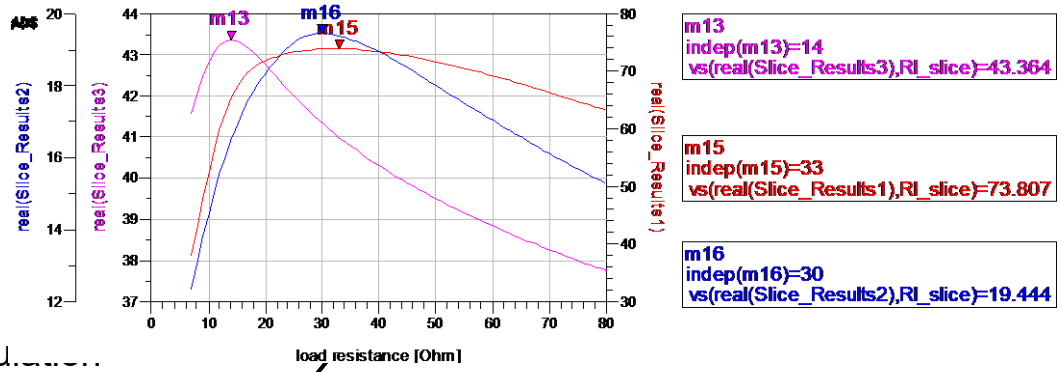
Plot @ 2dB GC

Impact of Source Impedance on Gain Performance under load modulation

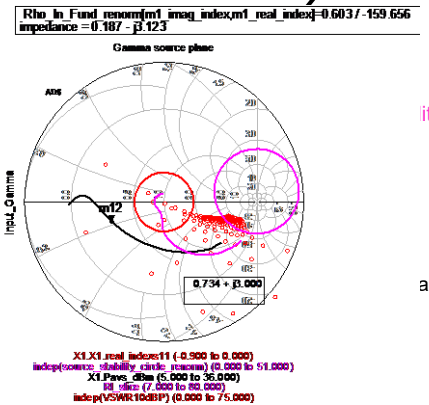
Christian Schuberth (IFAT PSS DCV RFS RF RFD)

6.4.2020

Transducer Gain
Drain Efficiency
Output Power



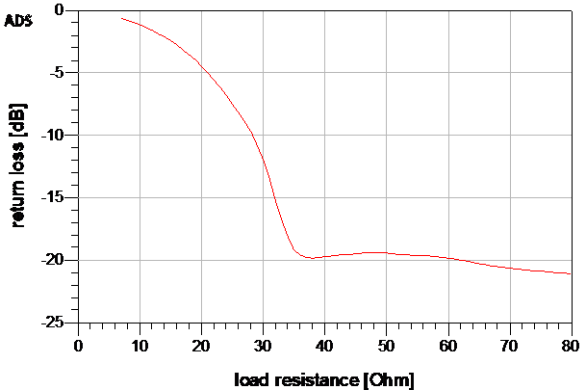
Source Impedance: 0.734+j3 (@3.4GHz)
Intrinsic Load reference plane: Load modu…



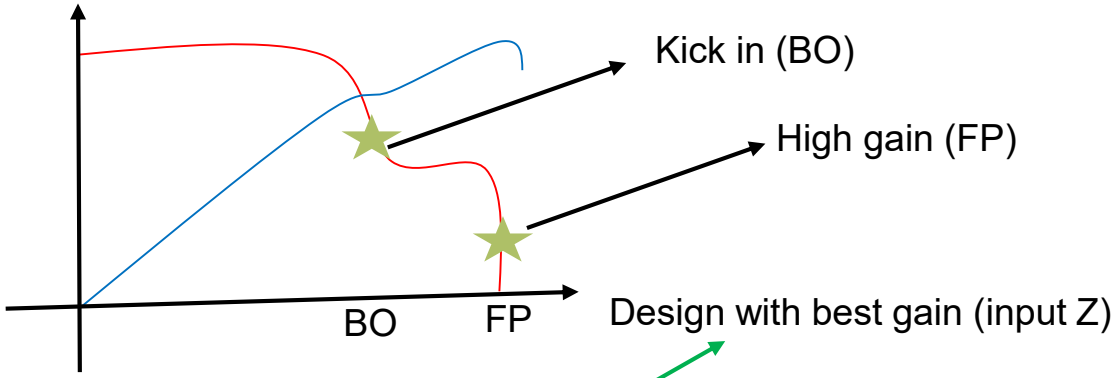
10dB R…

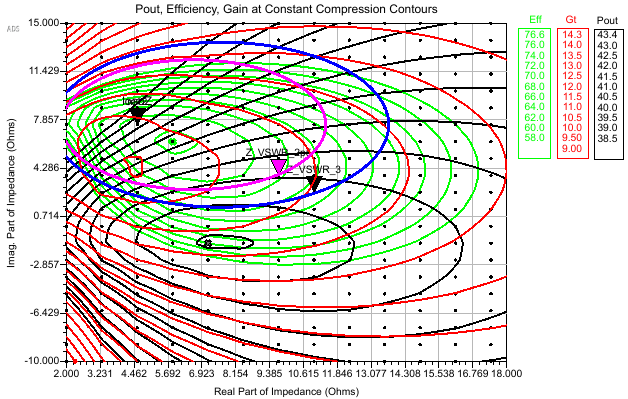
…ity

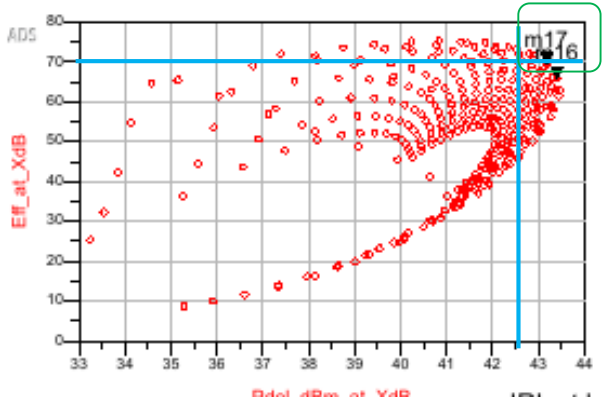
…ance: @ 3dB comp
@ various Loa



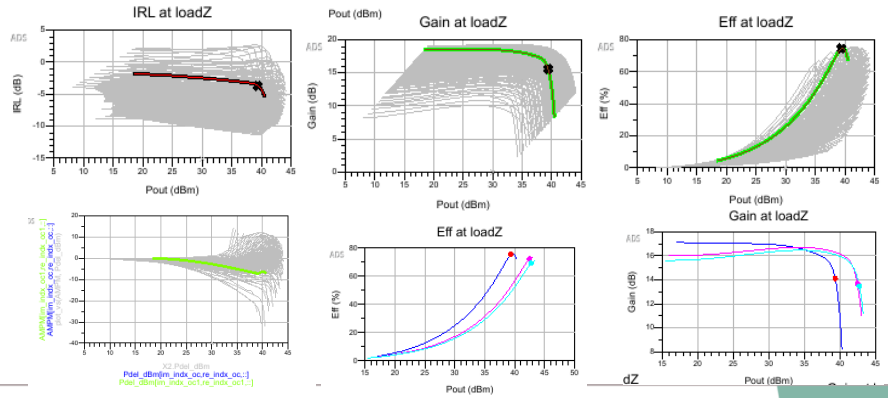
Peak (From Pre-match Design Selection : Alireza)





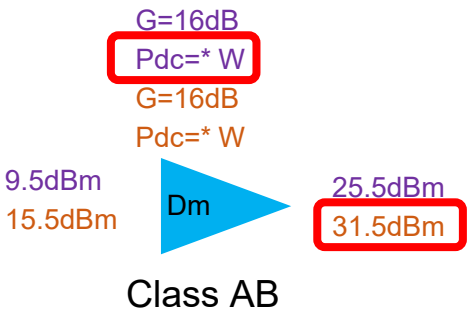


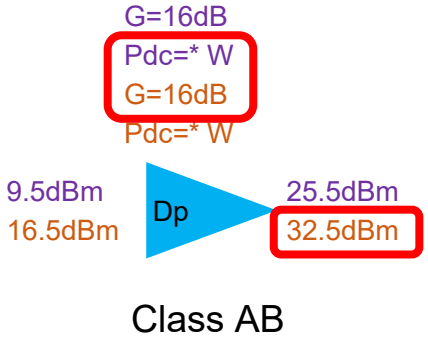
Zin➔
Gian➔
Eff➔
Pout➔



Plot @ FP

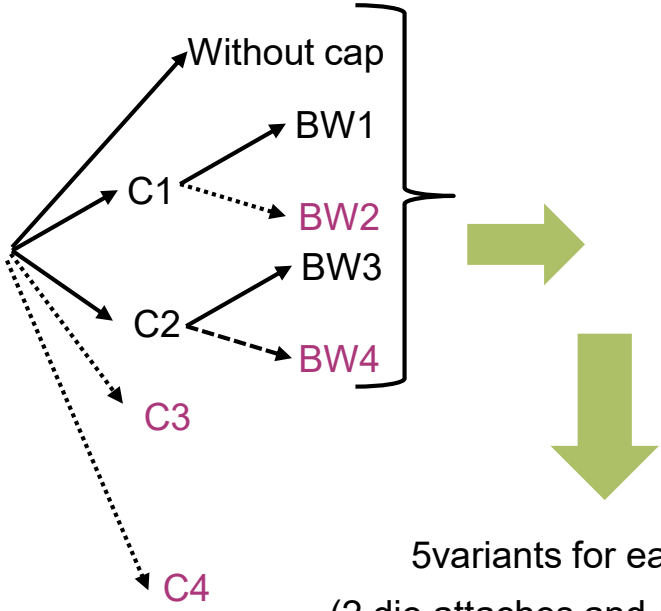
Driver (From Pre-match Design Selection : Alireza)





Proposed Builds

Main	Peak	Driver
DOE1, 5.76 (24*240um)	DOE5, 10.1 (42*240um)	DOE7, 2.4 (6*400um)
DOE2, 5.76 (36*160um)	DOE6, 12 (30*400um)	DOE8, 1.92(8*240um)
DOE3, 4.8 (30*160um)	DOE9, 11.52 (36*320um)	DOE11, 3.84 (12*320um)
DOE4, 5.12 (16*320um)	DOE10, 10.24 (32*320 um)	DOE12, 3.84 (16*240um)
DOE13, 6.40 (20*320um)		
DOE14,4.8 (12*400um)		



5variants for each device size

(2 die attaches and 4 bond-wire shapes)

Current Build (\\mucsdv534.infineon.com\RFS\PG_WI\50_TX_MODULE\40_Innovation_Projects\01_Study_TX_module_baseline\05_Module\Mini Pac\Mini Pac build_tracking)

Assembly build order	Design Status (Theepak/Bhagath)	Drawing status (Antonio/Filippo)	ADS Library	ADS Cell Name	Oxide Thickness [nm]	Assembly build order	Variant (DOE)	Laser Marking for Sample	RF GaN device geometry	RF GaN device name	RF GaN device wafer	Availability date	Quantity of available RF	Required quantity of RF G	Required availability date	Moscap value	MOScap device name	Wafer number (Cap)
1	done	done	PLP3839_lib	P19_Direct_BW1a2a	-	1	DOE1_1	D1-1S1... D1-1S20	5.76 (24*240um)	P19	T9502a_2			30 +30	04.02.2022	-	-	-
1	done	done	PLP3839_lib	P19_N9500Bv6_BW3a4a5a	1700	1	DOE1_2	D1-2S1... D1-2S20	5.76 (24*240um)	P19	T9502a_2			30 +30	04.02.2022	5,5 => 5,57	N9500B_V6	RU105508.03 wfr#14
1	done	done	PLP3839_lib	P19_N9500Bv6_BW3a6a5a	1700	1	DOE1_3	D1-3S1... D1-3S20	5.76 (24*240um)	P19	T9502a_2			30 +30	04.02.2022	5,5 => 5,57	N9500B_V6	RU105508.03 wfr#14
1	done	done	PLP3839_lib	P19_N9500Bv5_BW3a7a5a	900	1	DOE1_4	D1-4S1... D1-4S20	5.76 (24*240um)	P19	T9502a_2			30 +30	04.02.2022	10,19 => 10,27	N9500B_V5	RU105508.02 wfr#16
1	done	done	PLP3839_lib	P19_N9500Bv5_BW3a8a5a	900	1	DOE1_5	D1-5S1... D1-5S20	5.76 (24*240um)	P19	T9502a_2			30 +30	04.02.2022	10,19 => 10,27	N9500B_V5	RU105508.02 wfr#16
1	done	done	PLP3839_lib	P6_Direct_BW1b2b	-	1	DOE2_1	D2-1S1... D2-1S20	5.76 (36*160um)	P6	R9505A	*150		30 +30	04.02.2022	-	-	- -
1	done	done	PLP3839_lib	P6_N9501Bv1_BW3b4b5b	3100	1	DOE2_2	D2-2S1... D2-2S20	5.76 (36*160um)	P6	R9505A	*150		30 +30	04.02.2022	5.59 pF	N9501B_V1	RU105508.04 wfr#04
1	done	done	PLP3839_lib	P6_N9501Bv1_BW3b6b5b	3100	1	DOE2_3	D2-3S1... D2-3S20	5.76 (36*160um)	P6	R9505A	*150		30 +30	04.02.2022	5.59 pF	N9501B_V1	RU105508.04 wfr#04
1	done	done	PLP3839_lib	P6_N9501Bv4_BW3b7b5b	1300	1	DOE2_4	D2-4S1... D2-4S20	5.76 (36*160um)	P6	R9505A	*150		30 +30	04.02.2022	10,22 => 10,30	N9501B_V4	RU105508.04 wfr#10
1	done	done	PLP3839_lib	P6_N9501Bv4_BW3b8b5b	1300	1	DOE2_5	D2-5S1... D2-5S20	5.76 (36*160um)	P6	R9505A	*150		30 +30	04.02.2022	10,22 => 10,30	N9501B_V4	RU105508.04 wfr#10
2	done	done	PLP3839_lib	P3_Direct_BW1c2c__DOE3_1	-	2	DOE3_1	D3-1S1... D3-1S20	4.8 (30*160um)	P3	R9505A	*164		30 +30	21.02.2022	Without	-	- -
2	done	done	PLP3839_lib	P3_N9500Bv6_BW3c4c5c__DOE3_2	1700	2	DOE3_2	D3-2S1... D3-2S20	4.8 (30*160um)	P3	R9505A	*164		30 +30	21.02.2022	5,5 => 5,57	N9500B_V6	RU105508.03 wfr#20 (low loss substrate)
2	done	done	PLP3839_lib	P3_N9500Bv6_BW3c6c5c__DOE3_3	1700	2	DOE3_3	D3-3S1... D3-3S20	4.8 (30*160um)	P3	R9505A	*164		30 +30	21.02.2022	5,5 => 5,57	N9500B_V6	RU105508.03 wfr#20 (low loss substrate)
2	done	done	PLP3839_lib	P3_N9500Bv2_BW3c7c5c__DOE3_4	1700	2	DOE3_4	D3-4S1... D3-4S20	4.8 (30*160um)	P3	R9505A	*164		30 +30	21.02.2022	6,17 => 6,23	N9500B_V2	RU105508.03 wfr#20 (low loss substrate)
2	done	done	PLP3839_lib	P3_N9500Bv2_BW3c8c5c__DOE3_5	1700	2	DOE3_5	D3-5S1... D3-5S20	4.8 (30*160um)	P3	R9505A	*164		30 +30	21.02.2022	6,17 => 6,23	N9500B_V2	RU105508.03 wfr#20 (low loss substrate)
2	done	done	PLP3839_lib	P14_Direct_BW1d2d__DOE4_1	-	2	DOE4_1	D4-1S1... D4-1S20	5.12 (16*320um)	P14	R9505A	*150		30 +30	21.02.2022	Without		
2	done	done	PLP3839_lib	P14_N9500Bv6_BW3d4d5d__DOE4_2	1700	2	DOE4_2	D4-2S1... D4-2S20	5.12 (16*320um)	P14	R9505A	*150		30 +30	21.02.2022	5,5 => 5,57	N9500B_V6	RU105508.03 wfr#20 (low loss substrate)
2	done	done	PLP3839_lib	P14_N9500Bv6_BW3d6d5d__DOE4_3	1700	2	DOE4_3	D4-3S1... D4-3S20	5.12 (16*320um)	P14	R9505A	*150		30 +30	21.02.2022	5,5 => 5,57	N9500B_V6	RU105508.03 wfr#20 (low loss substrate)
2	done	done	PLP3839_lib	P14_N9501Bv5_BW7d8d5d__DOE4_4	1950	2	DOE4_4	D4-4S1... D4-4S20	5.12 (16*320um)	P14	R9505A	*150		30 +30	21.02.2022	6,5 => 6,58	N9501B_V5	RU105508.05 wfr#22 (low loss substrate)
2	done	done	PLP3839_lib	P14_N9501Bv5_BW7d9d5d__DOE4_5	1950	2	DOE4_5	D4-5S1... D4-5S20	5.12 (16*320um)	P14	R9505A	*150		30 +30	21.02.2022	6,5 => 6,58	N9501B_V5	RU105508.05 wfr#22 (low loss substrate)

Current Build (\\mucsdv534.infineon.com\RFS\PG_WI\50_TX_MODULE\40_Innovation_Projects\01_Study_TX_module_baseline\05_Module\Mini Pac\Mini Pac build_tracking)

	A	B	C	D	E	F	G	H	I	J	K	L	S	T	U	V	W	X	Y
1	Assembly build order	Design Status (Theepak/Bhagath)	Drawing status (Antonio/Filippo)	ADS Library	ADS Cell Name	Oxide Thickness [nm]	Assembly build order	Variant (DOE)	Laser Marking for Sample	RF GaN device geometry	RF GaN device name	RF GaN device wafer	Availability date	Quantity of available RF	Required quantity of RF G	Required availability date	Moscap value	MOScap device name	Wafer number (Cap)
23	2b	-	done	PLP3839_lib	N9500Bv2__DOEm_2	1700	2b	DOEm_2	01M-2 B0001, B0002, ...							21.02.2022	6,17 => 6,23	N9500B_V2	RU105508.03 wfr#20 (low loss substrate)
24	2b	-	done	PLP3839_lib	N9501Bv5__DOEm_3	1950	2b	DOEm_3	01M-3 A0001, A0002, ...							21.02.2022	6,5 => 6,58	N9501B_V5	RU105508.05 wfr#22 (low loss substrate)
25	2b	-	done	PLP3839_lib	N9500Bv5__DOEm_4	900	2b	DOEm_4	01M-4 C0001, C0002, ...							21.02.2022	10,19 => 10,27	N9500B_V5	RU105508.02 wfr#19 (low loss substrate)
26	2b	-	done	PLP3839_lib	N9501Bv1__DOEm_5	3100	2b	DOEm_5	01M-5 B0001, B0002, ...							21.02.2022	5.59 pF	N9501B_V1	RU105508.06 wfr#04
27	2b	-	done	PLP3839_lib	N9501Bv4__DOEm_6	1300	2b	DOEm_6	01M-6 C0001, C0002, ...							21.02.2022	10,22 => 10,30	N9501B_V4	RU105508.04 wfr#21 (low loss substrate)
28	3	done	done	LAC3839_lib	P76_Direct_BW1e2e_DOE5_1		3	DOE5_1		10.1(42*240um)	P76	T9503A_1	30.01.2022	*400	30	Available in Rgb	Without	-	-
29	3	done	done	LAC3839_lib	P76_N9501B_V5_BW3e4e5e_DOE5_	1950	3	DOE5_2		10.1(42*240um)	P76	T9503A_1	30.01.2022	*400	30	Available in Rgb	6,5 => 6,58	N9501B_V5	RU105508.05 wfr#22 (low loss substrate)
30	3	done	done	LAC3839_lib	P76_N9501B_V5_BW3e6e5e_DOE5_	1950	3	DOE5_3		10.1(42*240um)	P76	T9503A_1	30.01.2022	*400	30	Available in Rgb	6,5 => 6,58	N9501B_V5	RU105508.05 wfr#22 (low loss substrate)
31	3	done	done	LAC3839_lib	P76_N9501B_V8_BW7e8e5e_DOE5_	3100	3	DOE5_4		10.1(42*240um)	P76	T9503A_1	30.01.2022	*400	30	Available in Rgb	3,53	N9501B_V8	
32	3	done	done	LAC3839_lib	P76_N9501B_V8_BW7e9e5e_DOE5_	3100	3	DOE5_5		10.1(42*240um)	P76	T9503A_1	30.01.2022	*400	30	Available in Rgb	3,53	N9501B_V8	
33	3	done	done	LAC3839_lib	T9505A_1_Direct_BW1e2e_DOE6_1		3	DOE6_1		12 (30*400um)	T9505A_1	T9505A_1		*300	30	Available in Rgb	Without		
34	3	done	done	LAC3839_lib	T9505A_1_N9501B_V5_BW3e4e5e_D	1950	3	DOE6_2		12 (30*400um)	T9505A_1	T9505A_1		*300	30	Available in Rgb	6,5 => 6,58	N9501B_V5	RU105508.05 wfr#22 (low loss substrate)
35	3	done	done	LAC3839_lib	T9505A_1_N9501B_V8_BW3e4e5e_D	1300	3	DOE6_3		12 (30*400um)	T9505A_1	T9505A_1		*300	30	Available in Rgb	8,09 => 8,19	N9501B_V8	
36	3	done	done	LAC3839_lib	T9505A_1_N9501B_V8_BW6e4e7e_D	1300	3	DOE6_4		12 (30*400um)	T9505A_1	T9505A_1		*300	30	Available in Rgb	8,09 => 8,19	N9501B_V8	
37	3	done	done	LAC3839_lib	T9505A_1_N9501B_V4_BW6e4e7e_D	1300	3	DOE6_5		12 (30*400um)	T9505A_1	T9505A_1		*300	30	Available in Rgb	10,22 => 10,3	N9501B_V8	
38	4			LAC3839_lib			4	DOE7_1		2.4 (6*400um)	T9507B_2	T9507B	25.02.2022		30	04.03.2022	Without		
39	4			LAC3839_lib			4	DOE7_2		2.4 (6*400um)	T9507B_2	T9507B	25.02.2022		30	04.03.2022			
40	4			LAC3839_lib			4	DOE7_3		2.4 (6*400um)	T9507B_2	T9507B	25.02.2022		30	04.03.2022			
41	4			LAC3839_lib			4	DOE7_4		2.4 (6*400um)	T9507B_2	T9507B	25.02.2022		30	04.03.2022			
42	4			LAC3839_lib			4	DOE7_5		2.4 (6*400um)	T9507B_2	T9507B	25.02.2022		30	04.03.2022			
43	4			LAC3839_lib			4	DOE8_1		~~1.92 (8*240um)~~ 1.92 (8*240um)	~~P47_8F~~ T9501R_2x1P92	~~R9507A~~ T9501R	25.02.2022		30	04.03.2022	Without		
44	4			LAC3839_lib			4	DOE8_2		~~1.92 (8*240um)~~ 1.92 (8*240um)	~~P47_8F~~ T9501R_2x1P92	~~R9507A~~ T9501R	25.02.2022		30	04.03.2022			
45	4			LAC3839_lib			4	DOE8_3		~~1.92 (8*240um)~~ 1.92 (8*240um)	~~P47_8F~~ T9501R_2x1P92	~~R9507A~~ T9501R	25.02.2022		30	04.03.2022			
46	4			LAC3839_lib			4	DOE8_4		~~1.92 (8*240um)~~ 1.92 (8*240um)	~~P47_8F~~ T9501R_2x1P92	~~R9507A~~ T9501R	25.02.2022		30	04.03.2022			
47	4			LAC3839_lib			4	DOE8_5		~~1.92 (8*240um)~~ 1.92 (8*240um)	~~P47_8F~~ T9501R_2x1P92	~~R9507A~~ T9501R	25.02.2022		30	04.03.2022			

Expected Performance (DOE1-5.76mm(24*240um) PLP3839 (From YK Presentation)

	cap	Max. Eff	Gt	Max. Power
Direct		62,92	16,21	43,6
Option1	4,82pF	73,33	14,77	43,64
	5,29 →5,36pF	72,66	14,91	43,66
	5,5 →5,57pF	72,81	14,8	43,66
	6,17 →6,23pF	73,34	14,7	43,65
	9,55 →9,63pF	74,86	14,28	43,61
	10,19 →10,27pF	51,97	13,08	42,8
Option2 (PD3-A)		76,83	14,23	43,88

- Option 1
- Die : T9502a_2, P19
- MOSCap : N9500B_V6 series
- Minipack : PLP3839
- Recommend to use N9500B_V6, with ox=1700.

- Option 2
- Die : T9502a_2, P19
- MOSCap : N9500B_v5 (oxide thickness = 900nm)
- Minipack : PLP3839
- Target :
  - Check PD3 simulation and design
  - Check prematching 2nd harmonic Source tuning circuit performance.
    - PD3 prematching circuit is focus to design 2nd harmonic source tuning.
    - During LP, can compare external 2nd harmonic tuning and no harmonic tuning.
    - From this data, we can judge effectiveness of internal 2nd harmonic tuning circuit.

Expected Performance (DOE2-5.76mm(36*160um)) PLP3839 (From YK Presentation)

	cap	Max. Eff	Gt	Max. Power
Direct		62,92	16,21	43,6
Option1	4,82pF	73,33	14,77	43,64
	5,29 →5,36pF	72,66	14,91	43,66
	5,5 →5,57pF	72,81	14,8	43,66
	6,17 →6,23pF	73,34	14,7	43,65
	9,55 →9,63pF	74,86	14,28	43,61
	10,19 →10,27pF	51,97	13,08	42,8
Option2 (PD3-A)		76,83	14,23	43,88

- Option 1
- Die : R9505A, P6
- MOSCap : N9501B series
- Minipack : PLP3839
- Recommend to use N9501B_V1, with ox=3100.

- Option 2
- Die : R9505A, P6
- MOSCap : N9501B_v4 (oxide thickness = 1300nm)
- Minipack : PLP3839

Expected Performance (DOE3-4.8mm(30*160um)) (From Theepak)

DOE	Cap (pF)	Gain Main dB	PAE Main	Drain Eff Main	Pdel Main dBm	PAE LU	PAE Main	PAE Main BO	PAE LU BO	Zin ohm	
3_1	-	12	60	64	43	59	60.5	53	50	0.6	4.86
3_2	5.57	10.7	63.2	69	42.4	61	63.2	56.8	51.8	0.6	6.6
3_3	5.57	10.1	65.3	72.4	42.5	62.8	65.3	56.5	50.7	1.4	6.6
3_4	6.23	11.4	66.6	72	42.6	64.6	66.7	57.9	53.3	0.8	6.9
3_5	6.23	9.5	62.2	70	42.3	60	62.3	56.2	50.1	1.2	7

- Option 1
- Die : R9505A, P3
- MOSCap : N9500B series
- Minipack : PLP3839
- Recommend to use N9500B_V6, with ox=1700:5.57pf

- Option 2
- Die : R9505A, P3
- MOSCap : N9500B series
- Minipack : PLP3839
- Recommend to use N9500B_V2, with ox=1700:6.23pf

Eqn G_Drv_dBm_BO=14.5
Eqn DE_Drv_BO=17
Eqn Main_IMN_Loss_BO=3.3
Eqn G_Drv_dB = 13.8
Eqn Main_IMN_Loss=3.3
Eqn DE_drv=46
Eqn Main_OMN_Loss=0.3
Eqn Pin_Drv_dBm=Pin_Main_dBm-G_Drv_dB
Eqn Pin_Drv_Watts=dbmtow(Pin_Drv_dBm)
Eqn Pdc_Drv=((Pin_Main_Watts-Pin_Drv_Watts)/DE_drv)*100

Expected Performance (DOE4-5.12mm(16*320um)) (From YK Presentation)

	cap	Max. Eff	Gt	Max. Power
Option1	5.57pf	75.4	10.4	43.7
Option2	6.58pF	77.3	9.43	43.6

- Option 1
- Die : R9505A, P14
- MOSCap : N9500B series
- Minipack : PLP3839
- Recommend to use N9500B_V6, with ox=1700:5.57pf

- Option 2
- Die : R9505A, P14
- MOSCap : N9501B series
- Minipack : PLP3839
- Recommend to use N9501B_V5, with ox=1950:6.58pf

Expected Performance (DOE5-10.1mm(42*240um)) (From Theepak)

DOE	Cap (pF)	Zout (ohm)		Pout(dBm)	Eff	Gt (dB)	Zin(ohm)	
5_1	-	4	j2.3	45	68.7	18.7	0.38	j2.6
5_2 N044	6.5	3.09	j0.8	46.23	73	17.4	0.33	j2.79
5_3 N044	6.5	3.09	j0.8	46	74.63	14.59	0.83	j3.12
5_4	3.55	3.71	j1.6	45.9	74	16.6	0.45	j2.87
5_5	3.55	3.71	j1.6	45.8	75	16	0.57	j3.37

- Option 1
- Die : T9503A_1, P76
- MOSCap : N9501B series
- Minipack : LAC3839
- Recommend to use N9501B_V5, with ox=1950:6.58pf

- Option 2
- Die : T9503A_1, P76
- MOSCap : N9501B series
- Minipack : LAC3839
- Recommend to use N9501B_V8, with ox=3100:3.53pf

Expected Performance (DOE6-12mm(30*400um)) (From Bhagath)

DOE	Cap (pF)	Zout (ohm)		Pout(dBm)	Eff	Gt (dB)	Zin(ohm)	
6_1	-	3.6	-j 0.8	46.78	68	16.8	0.32	j 2.6
6_2 N044	6.5	2.9	-j 0.9	46.9	69	15.7	0.36	j 2.6
6_3 N044	8.09	2.7	-j 0.9	46.81	69	15.5	0.38	j 2.6
6_4 N044	8.09	2.9	j 0.3	46.68	72	16.1	0.42	j 2.9
6_5 N044	10.3	2.7	j 0.3	46.63	72	15.7	0.45	j 2.9

- Option 1
- Die : T9505A_1
- MOSCap : N9501B series
- Minipack : LAC3839
- Recommend to use N9501B_V5, with ox=1950:6.58pf

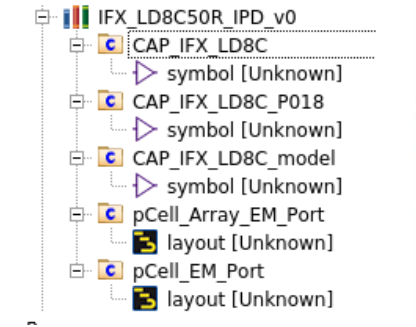
- Option 2
- Die : T9505A_1
- MOSCap : N9501B series
- Minipack : LAC3839
- Recommend to use N9501B_V8, with ox=1300:8.19pf

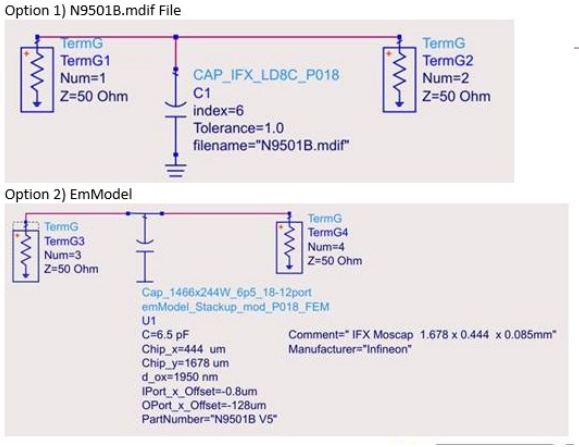
- Die : T9505A_1
- MOSCap : N9501B series
- Minipack : LAC3839
- Recommend to use N9501B_V4, with ox=1300:10.23pf

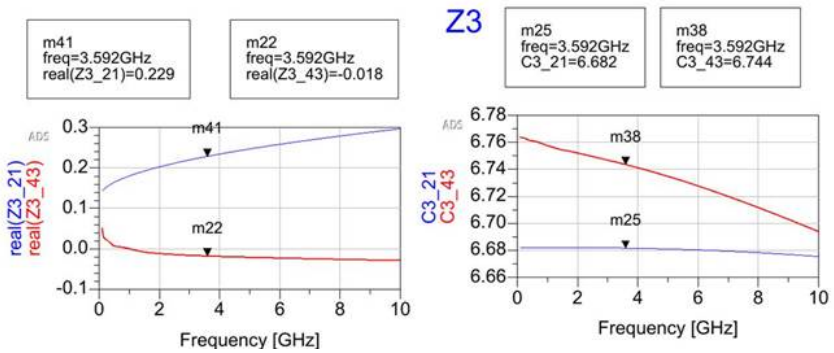
Builds Designed

	Environment Designed	Measured	Remarks
DOE1-2	Freeman Legacy, Laminate	PCB	Have to be simulated in PCB to compare with Measurement.
DOE3-4	PLP3839	Laminate	Have to be simulated in Laminate to compare with Measurement.
DOE5-6	LAC3839	Laminate	Availabe in Simulation To compare the Measurement
DOE7-8	LAC3839	Laminate	Will Be ready in April Last week

IFX_LD8C50R_IPD_V0 (Substrate Used) : Lesson Learned







- CAP_IDX_LD8C_model is a fully parametric equivalent circuit model using the material properties and geometry of the cap to calculate the equivalent capacitor and ESR.
- CAP_IFX_LD8C_PO18 uses an text file and an index to get the parameters which are feed to the parametric model CAP_IDX_LD8C_model.It uses the substrate thickness of 85um and the resistivity of the P018 substrate defined in the default schematic of the library. (IFX_LD8C_IPD_StackupA_Si_P018 and IFX_LD8C_IPD_Si_P018_rho)
- CAP_IFX_LD8C uses an text file and an index to get the parameters which are feed to the parametric model CAP_IDX_LD8C_model.It uses the substrate thickness of 60um and the resistivity of the N044 substrate defined in the default schematic of the library.(IFX_LD8C_IPD_StackupA_Si IFX_LD8C_IPD_Si_N044_rho)

N9501B.mdif File of IC_Ld8c lib(Lesson Learned)

(/home/mod_00/Freeman_legacy/cliosoft/cliosoft.shoundrabala.default/units/top_Freeman_legacy/oa/IC_LD8C/circuit/data/)

› Original N9501.mdif File

Open | N9501B.mdif ... /home/mod_00/Fre... | Save

```
BEGIN DSCRDATA
% INDEX L       W       Ls      Ws      d
1       1446    328     1678    444     1300
2       1446    304     1678    444     1300
3       1446    281     1678    444     1300
4       1446    261     1678    444     1950
5       1446    261     1678    444     1300
6       1446    244     1678    444     1950
7       1446    244     1678    444     1300
8       1446    233     1678    444     1950
9       1446    221     1678    444     1950
10      1446    207     1678    444     1950

END DSCRDATA
```

Plain Text | Tab Width: 8 | Ln 13, Col 1 | INS

› Updated N9501B.mdif File of IC_Ld8c lib

```
BEGIN DSCRDATA
% INDEX L       W       Ls      Ws      d
1       1446    328     1678    444     1300
2       1446    304     1678    444     1300
3       1446    281     1678    444     1300
4       1446    261     1678    444     1950
5       1446    261     1678    444     1300
6       1446    244     1678    444     1950
7       1446    244     1678    444     1300
8       1446    233     1678    444     1950
9       1446    221     1678    444     1950
10      1446    207     1678    444     1950
11      1466    281     1770    536     3100
12      1466    261     1770    536     3100
13      1466    244     1770    536     3100
14      1466    233     1770    536     3100
15      1466    221     1770    536     3100
16      1466    207     1770    536     3100

END DSCRDATA
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```
BEGIN DSCRDATA
% INDEX Cap
1       12.83
2       11.87
3       10.97
4       6.97
5       10.22
6       6.50
7       9.53
8       6.22
9       5.89
10      5.52
11      4.78
12      4.46
13      4.16
14      3.98
15      3.77
16      3.53

END DSCRDATA
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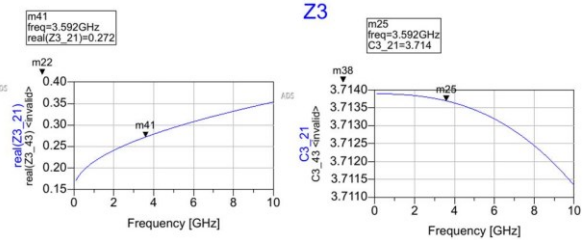
› Index No : 16 Cross check

› 3.53pf (3.714pf)



› Values to be added

	Tech	Mask Code	reticle kind	D9 released basetyp	Die X (um)	Die Y (um)	die area	aspect ratio	Si Thickness [µm]	Substrate	Substrate Name	suitable for 30V & 50V	cap value [pF]	Oxide [nm]	SiN [nm]	RF Top plate X [um]	RF Top plate Y [um]	RF top plate area [mm²]	BS metal
51	LD8C	N9501B_V3	shared	-	1770	536	0,95	3,30	85	N_3.5mOhmcm	L001-L004	x	4,78	3100	150	1466	281	0,41	Ag
52	LD8C	N9501B_V4	shared	-	1770	536	0,95	3,30	85	N_3.5mOhmcm	L001-L004	x	4,46	3100	150	1466	261	0,38	Ag
53	LD8C	N9501B_V5	shared	-	1770	536	0,95	3,30	85	N_3.5mOhmcm	L001-L004	x	4,16	3100	150	1466	244	0,36	Ag
54	LD8C	N9501B_V6	shared	-	1770	536	0,95	3,30	85	N_3.5mOhmcm	L001-L004	x	3,98	3100	150	1466	233	0,34	Ag
55	LD8C	N9501B_V7	shared	-	1770	536	0,95	3,30	85	N_3.5mOhmcm	L001-L004	x	3,77	3100	150	1466	221	0,32	Ag
56	LD8C	N9501B_V8	shared	-	1770	536	0,95	3,30	85	N_3.5mOhmcm	L001-L004	x	3,53	3100	150	1466	207	0,30	Ag

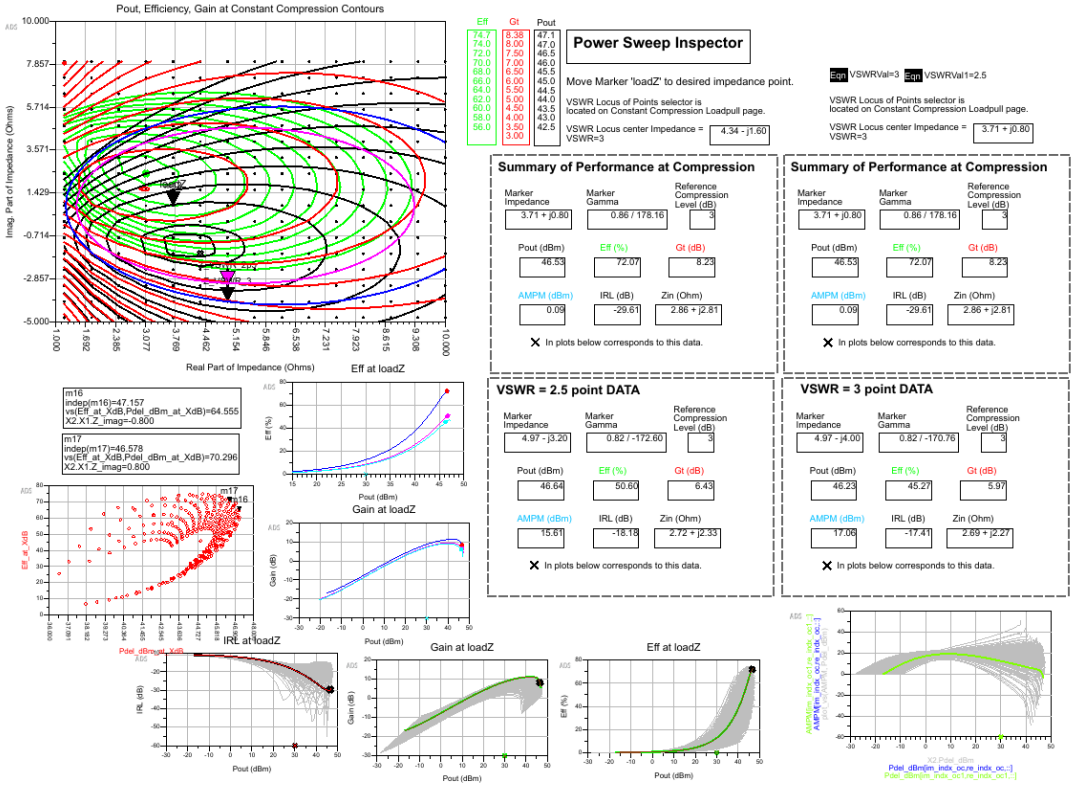
Detailed EM Simulation (DOE5_2) (Lesson Learned)

- Simplified EM settings are not capturing the Moscap properly.
- Gain dropped by 19dB.
- To get the Right Value, Em settings have to be slightly modified.
- More Simulaion time.

C=6.50pF
Detailed
Class C

Moscap-detail

Simplified EM settings (Wrong) Not capturing Moscap sometimes



Updating the Libraries: 60um to 85um Substrate IFX_LD8C50R_IPD_V0 (Lesson Learned)

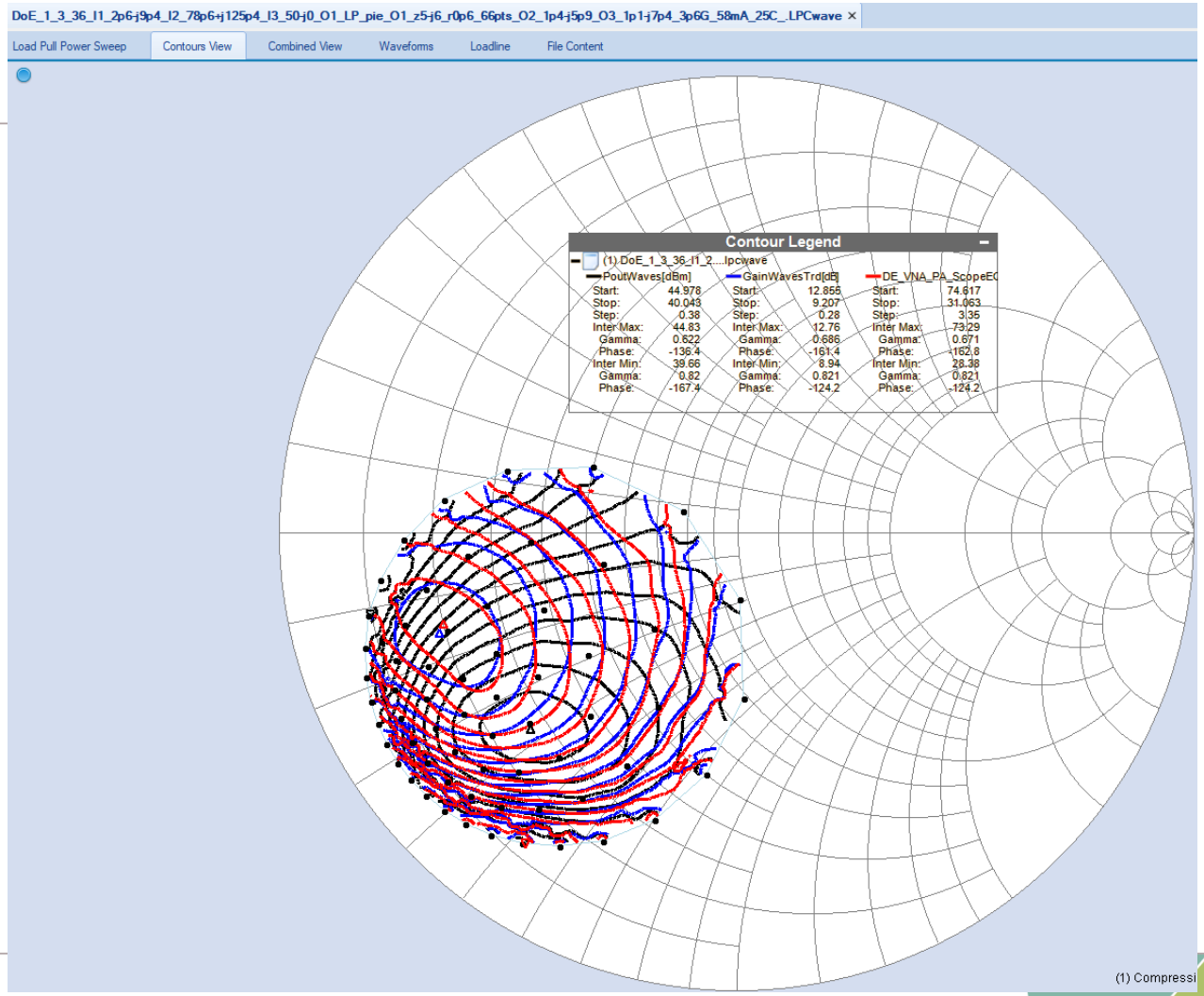
- IFX_LD8C_IPD_StackupA_Si IFX_LD8C_IPD_Si_N044_rho
- DOE5, P76_240_10P1mm, Compression = 3, Class C , 60um Vs 85um Substrate change for N044 of 6.5pF
- Gain Countour is Changing

DOE	Cap (pF)	Zout (ohm)		Pout(dBm)	Eff	Gt (dB)	Zin(ohm)	
5_2 N044_60um	6.5	3.71	j0.8	46.5	69	16.34	0.44	j2.96
5_2 N044_85um	6.5	3.09	j0.8	46.23	73	17.4	0.33	j2.79
5_3 N044_60um	6.5	3.71	j0.8	46.32	68.8	17.52	0.48	j3.48
5_3 N044_85um	6.5	3.09	j0.8	46	74.63	14.59	0.83	j3.12

Measurement DOE 1_3 3.6GHz

Simulation

cap	Max. Eff	Gt	Max. Power
5,29 →5,36pF	72,66	14,91	43,66



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