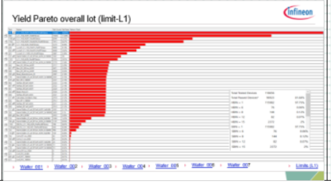
Lunch meeting CW2422

Timeline →	January	February	March	April	May	June
↓ Activity						
1. Training	• **Data analysis:** CEDA, Chronos • **Data extraction:** eSquare, Espresso • **Six Sigma foundation**		 			
2. POM data analysis		• **DOE lot R9653** • Limits & Pareto analysis				

3. PE matrix & flow			• **Build one single matrix that maps**
			  • Identifier
			  • Test type
			  • Binning
			  • Plot type
			  • Functionality
						

4. Automotation			• **Identify similarities** • Automate analysis • Use Rstudio + Shiny • Quick first report			
5. Confluence page		 	 		• **Mini KPI's similar to PE tools** • Track & link dataset with report, revison control • Roles & responsibilities	
6. ANN exploration						• **Build ANN model ?** • Use analysis matrix & flow • Study requests & analysis patterns

Back-up slides

3. Analysis matrix

Dimension 1	Dimension 2	Dimension 3	Dimension 4
Identifier	**Test parameter**	**Functionality**	**Plot type**
Lot	Test type	Filtering	Scatter
wafer	Limits	Grouping	Cumulative
X-Y position	Binning	Correlation	Wafer map
Site		splitting	Pareto
Tester			

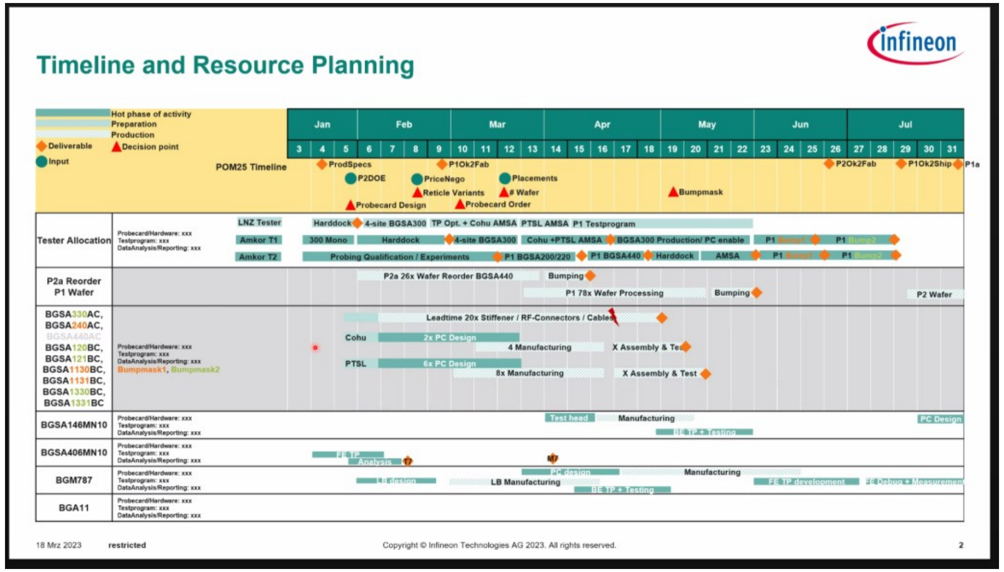
Identifier (Lot/wafer..)_1	Limits & Binning			Scope	Conclusion
a. Filter b. Group c. Correlate d. Plot type	**1**	**8**		**Yield**	**Limits exploration**
Test type					
400 (Leakage)	a & d				
401					
500 (RON)					Contact issue

Analysis identifier	Analysis order	Objective	Conclusion	Next step
R9653_1	213	Cpk = 1.68	Yiel loss not acceptable	Explore limits
R9653_2				
.				
.				
R9653_N				

- Link to further analysis with a flow that can be traced back to PE marix.
- Track objective, scope, observations and conclusions for a particular dataset.
- Maximize the re-use of analysis & reports from your peers related to a particular dataset.
- Once there is more data on analysis flow that can be linked back to PE matrix, then identification of logical similarities is possible.
  - This helps in defining the most used functionalities, plots, and probably their order of use & needed post processing.....
  - Use this information to automate using data science tools (Rstudio) and build a web based app (Python).

4. Automation

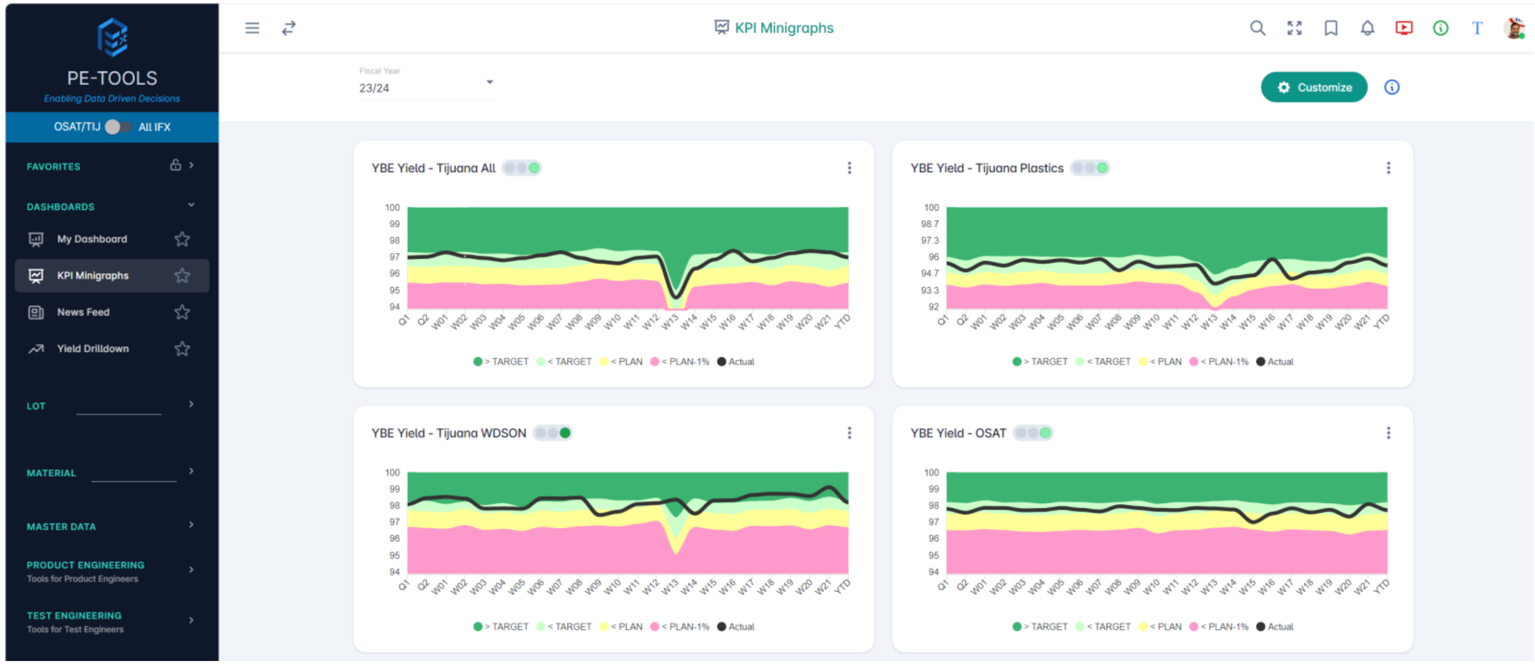
› Why automation ?



Example Shiny Apps

- Big line-up of upcoming devices & analysis requests.
- Huge pressue in terms of TTM & low FTE
- Product requirements might be different but analysis flow is expected to be similar.
- Seek to identify and automate 60-70% of the PE activity & flow
- Pick best practices/services from existing tools and put together using Rstudio/Python.
- Build a web based app to publish, re-use & quick glance of first results with one click.
- Further analysis & discussion doesn't need to be start from scratch.

5. Confluence page



- Mini KPI’s for a quick glance.
- Publish all preliminary, in-depth analysis & link it to PE matrix & flow
- Easy to follow and align on the further discussion due to revision control.
- Works better when sharing reports.
- A common place for PE’s to interact and discuss and share about their work (for re-use)
- Easy to find role and responsibilty of the particular dataset when published
- Helps the PE community to converge on analysis and reporting formats

2. DOE lot R9653

Limit setting -1 (L1)

Type	Test	Explanation	Low	High	Unit
Oscillator Freq.	310	Fixed specification of the parameter (constraints given by digital design)	40	55	#
Coff	805	+-20% limits - tighter limits would be possible, but measurement stability has to be taken into account	143	195	fF
	811		224	276	
	817		243	295	
Continuity	100-104	Filter out short and opens to check proper contact or dramatic fails, do not bother for double distributions	-900	-100	mV
Delta Pre Post Stress All Off	1104	Potentially influenced by settling time. Observed current delta seems not to be explainable by drift due to RF stress. Limits to be widened until further clarification is available. Potential solution: Additional current consumption test with bypassed storage cap. Test results should be verified by CV. Test is a customer requirement!	-0,5	10	µA
Delta Pre Post Stress All On	1103	Potentially influenced by settling time. Observed current delta seems not to be explainable by drift due to RF stress. Limits to be widened until further clarification is available. Potential solution: Additional current consumption test with bypassed storage cap. Test results should be verified by CV. Test is a customer requirement!	-0,5	4	µA
Off-Harmonics	702, 718	Wide limits +-10dB proposed because test will presumably show strong variations of mean values upon test hardware modifcations (probecard, ...). Limits could be potentially tightened in the future.	-74	-54	dBm
	703, 719		-72	-52	
	710		-84	-64	
	711		-79	-59	
On-Harmonics	706	Wide limits +-10dB proposed because test is depending stronly on cleaning cycle. To be discussed if test is really necessary or if improvements are possible	-77	-57	dBm
	707, 722, 723		-74	-54	
	714		-68	-48	
	715		-72	-52	
Current cons. active mode all off	400, 402, 1100, 1102	Upper limit = 30µA: assumed customer specification (to be confirmed)	11	30	µA
Current cons. Active mode all on	401, 1101	Upper limit = 23µA: derived from all of current consumption limit, All off mode adder subtracted (GIDL current x charge pump eff.)	8	23	µA
Current cons. Low power mode	200, 202	Upper limit = 13µA/17µA: derived from correlation with active mode all on current consumption	2	13	µA
	201		2	17	
DC Ron RF Ports	500, 502	+/- 15% limits to ensure key performance parameter stability. Frequent cleaning cycle needed to ensure stable measurements. Not sustainable in mass production. Expected yield loss in mass production if cleaning cycles are reduced and problem can't be resolved	1,3	1,8	Ω
	501		1,25	1,7	
S-Parameter Ron RF Ports	802	Large test variation observed with inexplicable wafer signature. Test maturity not sufficient to ensure key parameter stability. Currently wide limits proposed. However test is a customer requirement	1,5	4,5	Ω
	808		1,2	3,2	
	814		0,9	3,9	
Voffset	900-907	Should mainly filter out outliers, therefore wide test limits.	-4	0	mV

Yield Pareto overall lot (limit-L1)

Test	Name	Fail Count	Fail Rate	Failure Chart
402	I_C1_1V8_AOFF_PostAON_PreRFStress	17638	14.87%	
400	I_C1_1V8_AOFF_PreRFStress	14035	11.84%	
1100	I_C1_1V8_AOFF_PostRFStress	8544	7.21%	
1102	I_C1_1V8_AOFF_PostAON_PostRFStress	7915	6.67%	
401	I_C1_1V8_AON_PreRFStress	5270	4.44%	
200	I_LowP_C1_1V8_PreVH_PreRFStress	4908	4.14%	
202	I_LowP_C1_1V8_PostVH_PreRFStress	4648	3.92%	
201	I_LowP_C1_1V95_VH_PreRFStress	3987	3.36%	
723	Harm33dBm_f3_ref_RF3on_AON_fo1880M	3561	3%	
1101	I_C1_1V8_AON_PostRFStress	3335	2.81%	
707	Harm33dBm_f3_ref_RF1on_AON_fo1880M	2778	2.34%	
502	Ron_DC_RF3on_AOFF	2717	2.29%	
501	Ron_DC_RF2on_AOFF	2671	2.25%	
500	Ron_DC_RF1on_AOFF	2638	2.22%	
300	Read_Manufacturer_ID	2587	2.18%	
719	Harm33dBm_f3_ref_RF3off_AOFF_fo1880M	2551	2.15%	
814	Ron_RF3_1880M	2537	2.14%	
902	Voffset_RF3off_AOFF	2535	2.14%	
907	Voffset_RF3off_AON	2532	2.14%	
901	Voffset_RF2off_AOFF	2529	2.13%	
302	Read_Prod_ID	2526	2.13%	
906	Voffset_RF2off_AON	2521	2.13%	
311	Calculate_Oscillator_freq	2518	2.12%	
802	Ron_RF1_1880M	2512	2.12%	
905	Voffset_RF1off_AON	2511	2.12%	
900	Voffset_RF1off_AOFF	2510	2.12%	
711	Harm35dBm_f3_ref_RF2off_AOFF_fo824M	2501	2.11%	
703	Harm33dBm_f3_ref_RF1off_AOFF_fo1880M	2493	2.1%	
808	Ron_RF2_824M	2433	2.05%	
715	Harm35dBm_f3_ref_RF2on_AON_fo824M	1504	1.27%	
706	Harm33dBm_f2_ref_RF1on_AON_fo1880M	1107	0.93%	
1103	DELTA_I_C1_1V8_AON_PrePostRFStress	798	0.67%	
1104	DELTA_I_C1_1V8_AFF_PrePostRFStress	636	0.54%	
722	Harm33dBm_f2_ref_RF3on_AON_fo1880M	446	0.38%	
714	Harm35dBm_f2_ref_RF2on_AON_fo824M	109	0.09%	
102	Cont_RF1_to_GND	83	0.07%	
100	Cont_C1_to_GND	40	0.03%	
710	Harm35dBm_f2_ref_RF2off_AOFF_fo824M	24	0.02%	
702	Harm33dBm_f2_ref_RF1off_AOFF_fo1880M	19	0.02%	
718	Harm33dBm_f2_ref_RF3off_AOFF_fo1880M	19	0.02%	
104	Cont_RF3_to_GND	9	0.01%	
811	Coff_RF2_824M	8	0.01%	
805	Coff_RF1_1880M	7	0.01%	
817	Coff_RF3_1880M	7	0.01%	

Total Tested Devices	118656	
Total Passed Devices*	96923	81.68%
HBIN = 1	115982	97.75%
HBIN = 6	76	0.06%
HBIN = 8	144	0.12%
HBIN = 12	82	0.07%
HBIN = 15	2372	2%
SBIN = 1	115982	97.75%
SBIN = 6	76	0.06%
SBIN = 8	144	0.12%
SBIN = 12	82	0.07%
SBIN = 15	2372	2%

› Wafer_001 › Wafer_002 › Wafer_003 › Wafer_004 › Wafer_005 › Wafer_006 › Wafer_007 › Limits (L1)

Yield pareto (L1) – wafer 001

Test	Name	Fail Count	Fail Rate	Failure Chart
707	Harm33dBm_f3_ref_RF1on_AON_fo1880M	62	0.69%	
723	Harm33dBm_f3_ref_RF3on_AON_fo1880M	43	0.48%	
1104	DELTA_I_C1_1V8_AFF_PrePostRFStress	39	0.43%	
1103	DELTA_I_C1_1V8_AON_PrePostRFStress	39	0.43%	
715	Harm35dBm_f3_ref_RF2on_AON_fo824M	12	0.13%	
706	Harm33dBm_f2_ref_RF1on_AON_fo1880M	10	0.11%	
719	Harm33dBm_f3_ref_RF3off_AOFF_fo1880M	9	0.1%	
400	I_C1_1V8_AOFF_PreRFStress	9	0.1%	
401	I_C1_1V8_AON_PreRFStress	9	0.1%	
502	Ron_DC_RF3on_AOFF	9	0.1%	
1101	I_C1_1V8_AON_PostRFStress	9	0.1%	
1100	I_C1_1V8_AOFF_PostRFStress	8	0.09%	
1102	I_C1_1V8_AOFF_PostAON_PostRFStress	8	0.09%	
402	I_C1_1V8_AOFF_PostAON_PreRFStress	8	0.09%	
311	Calculate_Oscillator_freq	7	0.08%	
302	Read_Prod_ID	7	0.08%	
902	Voffset_RF3off_AOFF	7	0.08%	
814	Ron_RF3_1880M	7	0.08%	
907	Voffset_RF3off_AON	7	0.08%	
300	Read_Manufacturer_ID	7	0.08%	
500	Ron_DC_RF1on_AOFF	6	0.07%	
905	Voffset_RF1off_AON	6	0.07%	
703	Harm33dBm_f3_ref_RF1off_AOFF_fo1880M	6	0.07%	
900	Voffset_RF1off_AOFF	6	0.07%	
802	Ron_RF1_1880M	6	0.07%	
722	Harm33dBm_f2_ref_RF3on_AON_fo1880M	6	0.07%	
808	Ron_RF2_824M	6	0.07%	
501	Ron_DC_RF2on_AOFF	6	0.07%	
906	Voffset_RF2off_AON	6	0.07%	
901	Voffset_RF2off_AOFF	6	0.07%	
711	Harm35dBm_f3_ref_RF2off_AOFF_fo824M	6	0.07%	
102	Cont_RF1_to_GND	4	0.04%	
100	Cont_C1_to_GND	3	0.03%	
200	I_LowP_C1_1V8_PreVH_PreRFStress	2	0.02%	
201	I_LowP_C1_1V95_VH_PreRFStress	2	0.02%	
202	I_LowP_C1_1V8_PostVH_PreRFStress	2	0.02%	
718	Harm33dBm_f2_ref_RF3off_AOFF_fo1880M	1	0.01%	

Total Tested Devices	9005	
Total Passed Devices*	8804	97.77%
HBIN = 1	8991	99.84%
HBIN = 6	5	0.06%
HBIN = 8	4	0.04%
HBIN = 15	5	0.06%
SBIN = 1	8991	99.84%
SBIN = 6	5	0.06%
SBIN = 8	4	0.04%
SBIN = 15	5	0.06%

Yield pareto (L1) – wafer 002

Test	Name	Fail Count	Fail Rate	Failure Chart
200	I_LowP_C1_1V8_PreVH_PreRFStress	379	6.17%	
202	I_LowP_C1_1V8_PostVH_PreRFStress	373	6.07%	
201	I_LowP_C1_1V95_VH_PreRFStress	361	5.88%	
401	I_C1_1V8_AON_PreRFStress	359	5.84%	
1101	I_C1_1V8_AON_PostRFStress	264	4.3%	
402	I_C1_1V8_AOFF_PostAON_PreRFStress	241	3.92%	
400	I_C1_1V8_AOFF_PreRFStress	238	3.87%	
1100	I_C1_1V8_AOFF_PostRFStress	196	3.19%	
1102	I_C1_1V8_AOFF_PostAON_PostRFStress	190	3.09%	
1103	DELTA_I_C1_1V8_AON_PrePostRFStress	151	2.46%	
723	Harm33dBm_f3_ref_RF3on_AON_fo1880M	143	2.33%	
715	Harm35dBm_f3_ref_RF2on_AON_fo824M	141	2.29%	
501	Ron_DC_RF2on_AOFF	123	2%	
502	Ron_DC_RF3on_AOFF	108	1.76%	
500	Ron_DC_RF1on_AOFF	107	1.74%	
722	Harm33dBm_f2_ref_RF3on_AON_fo1880M	79	1.29%	
1104	DELTA_I_C1_1V8_AFF_PrePostRFStress	76	1.24%	
300	Read_Manufacturer_ID	68	1.11%	
311	Calculate_Oscillator_freq	68	1.11%	
707	Harm33dBm_f3_ref_RF1on_AON_fo1880M	67	1.09%	
302	Read_Prod_ID	65	1.06%	
802	Ron_RF1_1880M	63	1.03%	
814	Ron_RF3_1880M	63	1.03%	
719	Harm33dBm_f3_ref_RF3off_AOFF_fo1880M	62	1.01%	
906	Voffset_RF2off_AON	61	0.99%	
905	Voffset_RF1off_AON	61	0.99%	
901	Voffset_RF2off_AOFF	61	0.99%	
703	Harm33dBm_f3_ref_RF1off_AOFF_fo1880M	61	0.99%	
900	Voffset_RF1off_AOFF	61	0.99%	
902	Voffset_RF3off_AOFF	60	0.98%	
907	Voffset_RF3off_AON	60	0.98%	
808	Ron_RF2_824M	59	0.96%	
711	Harm35dBm_f3_ref_RF2off_AOFF_fo824M	56	0.91%	
714	Harm35dBm_f2_ref_RF2on_AON_fo824M	26	0.42%	
710	Harm35dBm_f2_ref_RF2off_AOFF_fo824M	19	0.31%	
706	Harm33dBm_f2_ref_RF1on_AON_fo1880M	12	0.2%	
102	Cont_RF1_to_GND	12	0.2%	
104	Cont_RF3_to_GND	8	0.13%	
805	Coff_RF1_1880M	7	0.11%	
718	Harm33dBm_f2_ref_RF3off_AOFF_fo1880M	7	0.11%	
817	Coff_RF3_1880M	7	0.11%	
811	Coff_RF2_824M	6	0.1%	
103	Cont_RF2_to_GND	6	0.1%	
702	Harm33dBm_f2_ref_RF1off_AOFF_fo1880M	3	0.05%	
100	Cont_C1_to_GND	2	0.03%	

Total Tested Devices	6147	
Total Passed Devices*	5484	89.21%
HBIN = 1	6077	98.86%
HBIN = 6	3	0.05%
HBIN = 8	15	0.24%
HBIN = 12	35	0.57%
HBIN = 15	17	0.28%
SBIN = 1	6077	98.86%
SBIN = 6	3	0.05%
SBIN = 8	15	0.24%
SBIN = 12	35	0.57%
SBIN = 15	17	0.28%

Yield pareto (L1) – wafer 003

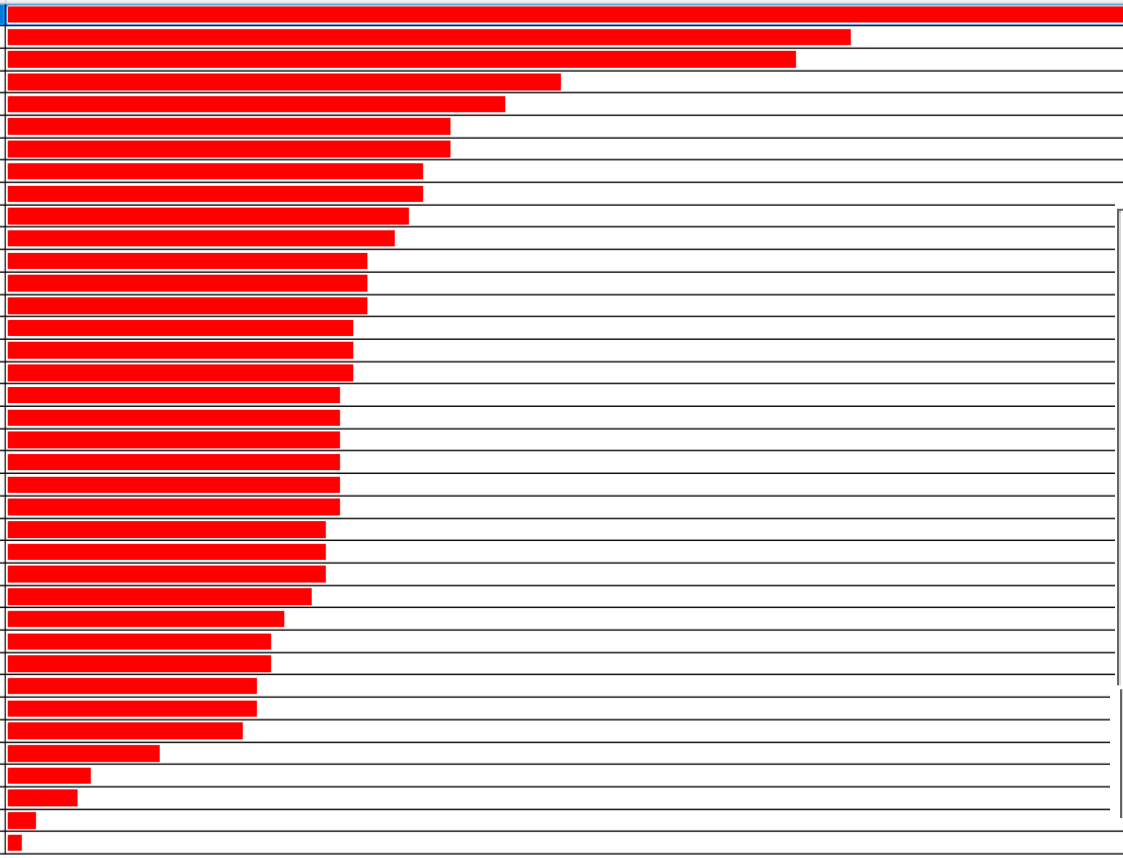
Test	Name	Fail Count	Fail Rate	Failure Chart
715	Harm35dBm_f3_ref_RF2on_AON_fo824M	162	1.8%	
723	Harm33dBm_f3_ref_RF3on_AON_fo1880M	79	0.88%	
1104	DELTA_I_C1_1V8_AFF_PrePostRFStress	57	0.63%	
1103	DELTA_I_C1_1V8_AON_PrePostRFStress	42	0.47%	
707	Harm33dBm_f3_ref_RF1on_AON_fo1880M	34	0.38%	
722	Harm33dBm_f2_ref_RF3on_AON_fo1880M	27	0.3%	
401	I_C1_1V8_AON_PreRFStress	20	0.22%	
402	I_C1_1V8_AOFF_PostAON_PreRFStress	20	0.22%	
1101	I_C1_1V8_AON_PostRFStress	20	0.22%	
400	I_C1_1V8_AOFF_PreRFStress	19	0.21%	
1102	I_C1_1V8_AOFF_PostAON_PostRFStress	17	0.19%	
302	Read_Prod_ID	17	0.19%	
719	Harm33dBm_f3_ref_RF3off_AOFF_fo1880M	17	0.19%	
1100	I_C1_1V8_AOFF_PostRFStress	16	0.18%	
814	Ron_RF3_1880M	16	0.18%	
502	Ron_DC_RF3on_AOFF	16	0.18%	
501	Ron_DC_RF2on_AOFF	15	0.17%	
901	Voffset_RF2off_AOFF	15	0.17%	
902	Voffset_RF3off_AOFF	15	0.17%	
906	Voffset_RF2off_AON	15	0.17%	
311	Calculate_Oscillator_freq	14	0.16%	
802	Ron_RF1_1880M	14	0.16%	
300	Read_Manufacturer_ID	14	0.16%	
900	Voffset_RF1off_AOFF	14	0.16%	
905	Voffset_RF1off_AON	14	0.16%	
907	Voffset_RF3off_AON	14	0.16%	
500	Ron_DC_RF1on_AOFF	14	0.16%	
808	Ron_RF2_824M	14	0.16%	
711	Harm35dBm_f3_ref_RF2off_AOFF_fo824M	14	0.16%	
703	Harm33dBm_f3_ref_RF1off_AOFF_fo1880M	13	0.14%	
706	Harm33dBm_f2_ref_RF1on_AON_fo1880M	8	0.09%	
100	Cont_C1_to_GND	5	0.06%	
102	Cont_RF1_to_GND	5	0.06%	
201	I_LowP_C1_1V95_VH_PreRFStress	3	0.03%	
202	I_LowP_C1_1V8_PostVH_PreRFStress	3	0.03%	
200	I_LowP_C1_1V8_PreVH_PreRFStress	3	0.03%	
710	Harm35dBm_f2_ref_RF2off_AOFF_fo824M	2	0.02%	
714	Harm35dBm_f2_ref_RF2on_AON_fo824M	2	0.02%	
101	Cont_C2_to_GND	1	0.01%	

Total Tested Devices	9005	
Total Passed Devices*	8642	95.97%
HBIN = 1	8977	99.69%
HBIN = 6	8	0.09%
HBIN = 8	9	0.1%
HBIN = 15	11	0.12%
SBIN = 1	8977	99.69%
SBIN = 6	8	0.09%
SBIN = 8	9	0.1%
SBIN = 15	11	0.12%

Yield pareto (L1) – wafer 004

Test	Name	Fail Count	Fail Rate
715	Harm35dBm_f3_ref_RF2on_AON_fo824M	140	1.56%
1103	DELTA_I_C1_1V8_AON_PrePostRFStress	61	0.68%
723	Harm33dBm_f3_ref_RF3on_AON_fo1880M	57	0.63%
707	Harm33dBm_f3_ref_RF1on_AON_fo1880M	40	0.44%
1104	DELTA_I_C1_1V8_AFF_PrePostRFStress	36	0.4%
1101	I_C1_1V8_AON_PostRFStress	32	0.36%
401	I_C1_1V8_AON_PreRFStress	32	0.36%
1102	I_C1_1V8_AOFF_PostAON_PostRFStress	30	0.33%
402	I_C1_1V8_AOFF_PostAON_PreRFStress	30	0.33%
400	I_C1_1V8_AOFF_PreRFStress	29	0.32%
1100	I_C1_1V8_AOFF_PostRFStress	28	0.31%
502	Ron_DC_RF3on_AOFF	26	0.29%
719	Harm33dBm_f3_ref_RF3off_AOFF_fo1880M	26	0.29%
500	Ron_DC_RF1on_AOFF	26	0.29%
902	Voffset_RF3off_AOFF	25	0.28%
501	Ron_DC_RF2on_AOFF	25	0.28%
814	Ron_RF3_1880M	25	0.28%
907	Voffset_RF3off_AON	24	0.27%
905	Voffset_RF1off_AON	24	0.27%
906	Voffset_RF2off_AON	24	0.27%
901	Voffset_RF2off_AOFF	24	0.27%
808	Ron_RF2_824M	24	0.27%
302	Read_Prod_ID	24	0.27%
300	Read_Manufacturer_ID	23	0.26%
900	Voffset_RF1off_AOFF	23	0.26%
802	Ron_RF1_1880M	23	0.26%
311	Calculate_Oscillator_freq	22	0.24%
711	Harm35dBm_f3_ref_RF2off_AOFF_fo824M	20	0.22%
722	Harm33dBm_f2_ref_RF3on_AON_fo1880M	19	0.21%
703	Harm33dBm_f3_ref_RF1off_AOFF_fo1880M	19	0.21%
202	I_LowP_C1_1V8_PostVH_PreRFStress	18	0.2%
201	I_LowP_C1_1V95_VH_PreRFStress	18	0.2%
200	I_LowP_C1_1V8_PreVH_PreRFStress	17	0.19%
706	Harm33dBm_f2_ref_RF1on_AON_fo1880M	11	0.12%
714	Harm35dBm_f2_ref_RF2on_AON_fo824M	6	0.07%
102	Cont_RF1_to_GND	5	0.06%
100	Cont_C1_to_GND	2	0.02%
718	Harm33dBm_f2_ref_RF3off_AOFF_fo1880M	1	0.01%

Failure Chart



Total Tested Devices	9005	
Total Passed Devices*	8687	96.47%
HBIN = 1	8971	99.62%
HBIN = 6	6	0.07%
HBIN = 8	16	0.18%
HBIN = 15	12	0.13%
SBIN = 1	8971	99.62%
SBIN = 6	6	0.07%
SBIN = 8	16	0.18%
SBIN = 15	12	0.13%

Yield pareto (L1) – wafer 005

Test	Name	Fail Count	Fail Rate	Failure Chart
723	Harm33dBm_f3_ref_RF3on_AON_fo1880M	50	0.8%	
715	Harm35dBm_f3_ref_RF2on_AON_fo824M	44	0.7%	
1103	DELTA_I_C1_1V8_AON_PrePostRFStress	40	0.64%	
707	Harm33dBm_f3_ref_RF1on_AON_fo1880M	36	0.57%	
1104	DELTA_I_C1_1V8_AFF_PrePostRFStress	33	0.53%	
502	Ron_DC_RF3on_AOFF	26	0.42%	
501	Ron_DC_RF2on_AOFF	24	0.38%	
500	Ron_DC_RF1on_AOFF	24	0.38%	
302	Read_Prod_ID	23	0.37%	
1100	I_C1_1V8_AOFF_PostRFStress	23	0.37%	
901	Voffset_RF2off_AOFF	22	0.35%	
1102	I_C1_1V8_AOFF_PostAON_PostRFStress	22	0.35%	
311	Calculate_Oscillator_freq	22	0.35%	
300	Read_Manufacturer_ID	22	0.35%	
401	I_C1_1V8_AON_PreRFStress	22	0.35%	
400	I_C1_1V8_AOFF_PreRFStress	22	0.35%	
402	I_C1_1V8_AOFF_PostAON_PreRFStress	22	0.35%	
703	Harm33dBm_f3_ref_RF1off_AOFF_fo1880M	22	0.35%	
900	Voffset_RF1off_AOFF	22	0.35%	
905	Voffset_RF1off_AON	22	0.35%	
719	Harm33dBm_f3_ref_RF3off_AOFF_fo1880M	22	0.35%	
802	Ron_RF1_1880M	22	0.35%	
907	Voffset_RF3off_AON	22	0.35%	
1101	I_C1_1V8_AON_PostRFStress	22	0.35%	
902	Voffset_RF3off_AOFF	22	0.35%	
814	Ron_RF3_1880M	22	0.35%	
711	Harm35dBm_f3_ref_RF2off_AOFF_fo824M	22	0.35%	
906	Voffset_RF2off_AON	22	0.35%	
808	Ron_RF2_824M	19	0.3%	
722	Harm33dBm_f2_ref_RF3on_AON_fo1880M	14	0.22%	
706	Harm33dBm_f2_ref_RF1on_AON_fo1880M	3	0.05%	
100	Cont_C1_to_GND	2	0.03%	
102	Cont_RF1_to_GND	2	0.03%	

Total Tested Devices	6263	
Total Passed Devices*	6092	97.27%
HBIN = 1	6239	99.62%
HBIN = 6	2	0.03%
HBIN = 15	22	0.35%
SBIN = 1	6239	99.62%
SBIN = 6	2	0.03%
SBIN = 15	22	0.35%

Yield pareto (L1) – wafer 006

Test	Name	Fail Count	Fail Rate	Failure Chart
500	Ron_DC_RF1on_AOFF	72	1%	
501	Ron_DC_RF2on_AOFF	58	0.81%	
723	Harm33dBm_f3_ref_RF3on_AON_fo1880M	52	0.72%	
1103	DELTA_I_C1_1V8_AON_PrePostRFStress	43	0.6%	
502	Ron_DC_RF3on_AOFF	41	0.57%	
1104	DELTA_I_C1_1V8_AFF_PrePostRFStress	30	0.42%	
707	Harm33dBm_f3_ref_RF1on_AON_fo1880M	16	0.22%	
715	Harm35dBm_f3_ref_RF2on_AON_fo824M	15	0.21%	
1102	I_C1_1V8_AOFF_PostAON_PostRFStress	10	0.14%	
1101	I_C1_1V8_AON_PostRFStress	8	0.11%	
400	I_C1_1V8_AOFF_PreRFStress	8	0.11%	
722	Harm33dBm_f2_ref_RF3on_AON_fo1880M	8	0.11%	
906	Voffset_RF2off_AON	8	0.11%	
402	I_C1_1V8_AOFF_PostAON_PreRFStress	8	0.11%	
401	I_C1_1V8_AON_PreRFStress	8	0.11%	
901	Voffset_RF2off_AOFF	8	0.11%	
1100	I_C1_1V8_AOFF_PostRFStress	8	0.11%	
808	Ron_RF2_824M	8	0.11%	
711	Harm35dBm_f3_ref_RF2off_AOFF_fo824M	8	0.11%	
907	Voffset_RF3off_AON	7	0.1%	
902	Voffset_RF3off_AOFF	7	0.1%	
719	Harm33dBm_f3_ref_RF3off_AOFF_fo1880M	7	0.1%	
814	Ron_RF3_1880M	7	0.1%	
300	Read_Manufacturer_ID	7	0.1%	
302	Read_Prod_ID	7	0.1%	
311	Calculate_Oscillator_freq	7	0.1%	
905	Voffset_RF1off_AON	6	0.08%	
802	Ron_RF1_1880M	6	0.08%	
900	Voffset_RF1off_AOFF	6	0.08%	
703	Harm33dBm_f3_ref_RF1off_AOFF_fo1880M	6	0.08%	
102	Cont_RF1_to_GND	4	0.06%	
706	Harm33dBm_f2_ref_RF1on_AON_fo1880M	3	0.04%	
714	Harm35dBm_f2_ref_RF2on_AON_fo824M	2	0.03%	
100	Cont_C1_to_GND	2	0.03%	
710	Harm35dBm_f2_ref_RF2off_AOFF_fo824M	1	0.01%	
811	Coff_RF2_824M	1	0.01%	

Total Tested Devices	7190	
Total Passed Devices*	6955	96.73%
HBIN = 1	7177	99.82%
HBIN = 6	4	0.06%
HBIN = 8	2	0.03%
HBIN = 15	7	0.1%
SBIN = 1	7177	99.82%
SBIN = 6	4	0.06%
SBIN = 8	2	0.03%
SBIN = 15	7	0.1%

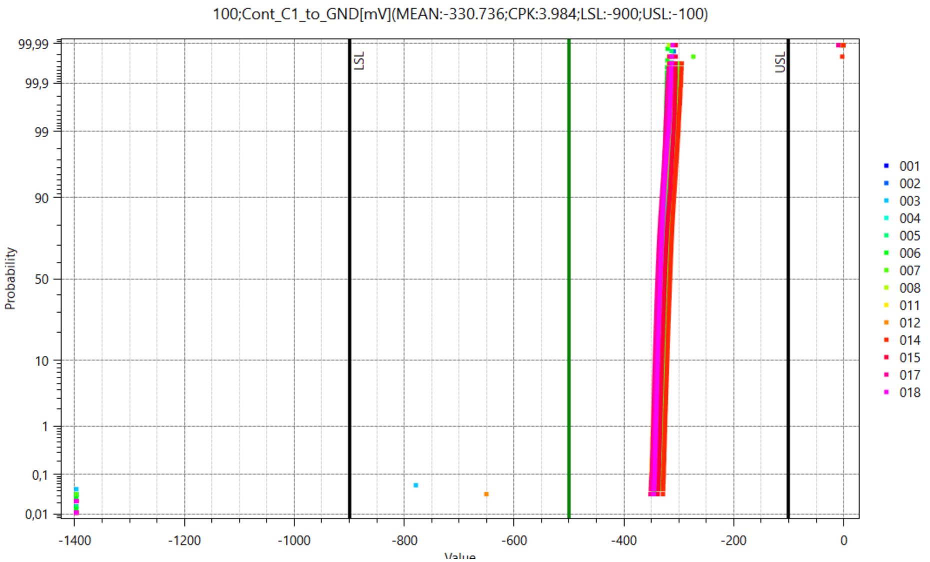
Yield pareto (L1) – wafer 007

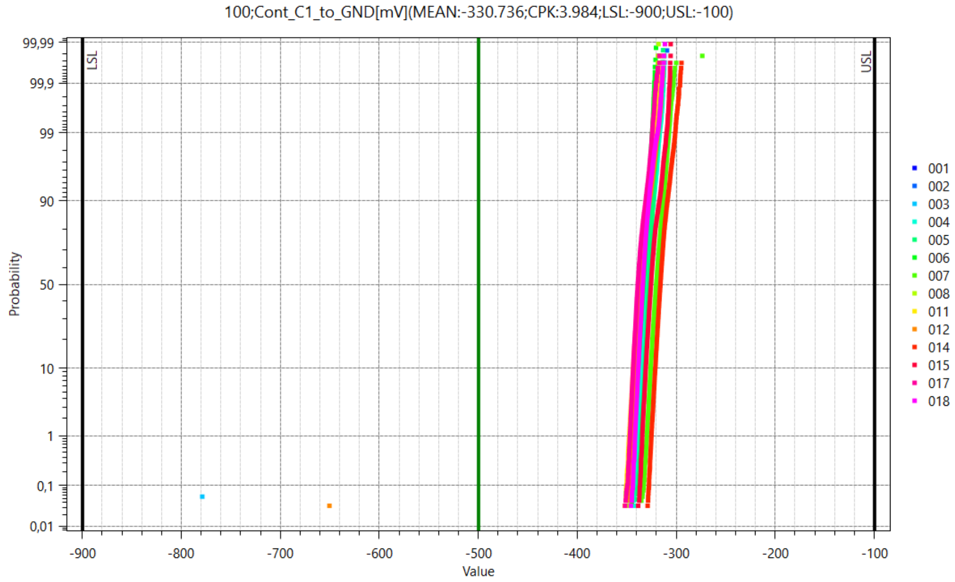
Test	Name	Fail Count	Fail Rate	Failure Chart
402	I_C1_1V8_AOFF_PostAON_PreRFStress	7424	82.47%	
400	I_C1_1V8_AOFF_PreRFStress	5493	61.02%	
1100	I_C1_1V8_AOFF_PostRFStress	2680	29.77%	
1102	I_C1_1V8_AOFF_PostAON_PostRFStress	2363	26.25%	
200	I_LowP_C1_1V8_PreVH_PreRFStress	1176	13.06%	
202	I_LowP_C1_1V8_PostVH_PreRFStress	1119	12.43%	
401	I_C1_1V8_AON_PreRFStress	937	10.41%	
1101	I_C1_1V8_AON_PostRFStress	257	2.85%	
723	Harm33dBm_f3_ref_RF3on_AON_fo1880M	120	1.33%	
715	Harm35dBm_f3_ref_RF2on_AON_fo824M	90	1%	
1103	DELTA_I_C1_1V8_AON_PrePostRFStress	59	0.66%	
1104	DELTA_I_C1_1V8_AFF_PrePostRFStress	49	0.54%	
707	Harm33dBm_f3_ref_RF1on_AON_fo1880M	31	0.34%	
722	Harm33dBm_f2_ref_RF3on_AON_fo1880M	25	0.28%	
302	Read_Prod_ID	5	0.06%	
906	Voffset_RF2off_AON	4	0.04%	
711	Harm35dBm_f3_ref_RF2off_AOFF_fo824M	4	0.04%	
500	Ron_DC_RF1on_AOFF	4	0.04%	
703	Harm33dBm_f3_ref_RF1off_AOFF_fo1880M	4	0.04%	
900	Voffset_RF1off_AOFF	4	0.04%	
901	Voffset_RF2off_AOFF	4	0.04%	
300	Read_Manufacturer_ID	4	0.04%	
905	Voffset_RF1off_AON	4	0.04%	
311	Calculate_Oscillator_freq	4	0.04%	
802	Ron_RF1_1880M	4	0.04%	
501	Ron_DC_RF2on_AOFF	4	0.04%	
502	Ron_DC_RF3on_AOFF	4	0.04%	
100	Cont_C1_to_GND	4	0.04%	
102	Cont_RF1_to_GND	4	0.04%	
719	Harm33dBm_f3_ref_RF3off_AOFF_fo1880M	3	0.03%	
907	Voffset_RF3off_AON	3	0.03%	
808	Ron_RF2_824M	3	0.03%	
902	Voffset_RF3off_AOFF	3	0.03%	
814	Ron_RF3_1880M	3	0.03%	
706	Harm33dBm_f2_ref_RF1on_AON_fo1880M	1	0.01%	
101	Cont_C2_to_GND	1	0.01%	

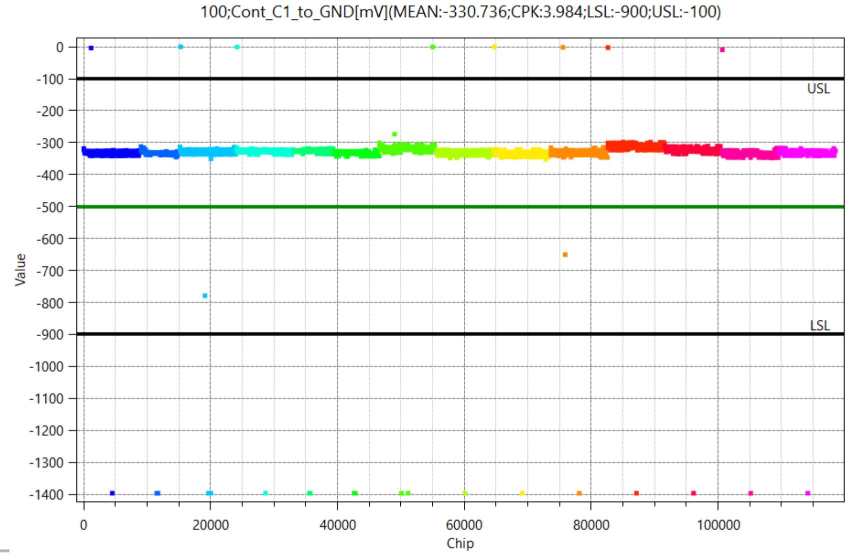
Total Tested Devices	9006	
Total Passed Devices*	1510	16.77%
HBIN = 1	8995	99.88%
HBIN = 6	4	0.04%
HBIN = 8	4	0.04%
HBIN = 12	1	0.01%
HBIN = 15	2	0.02%
SBIN = 1	8995	99.88%
SBIN = 6	4	0.04%
SBIN = 8	4	0.04%
SBIN = 12	1	0.01%
SBIN = 15	2	0.02%

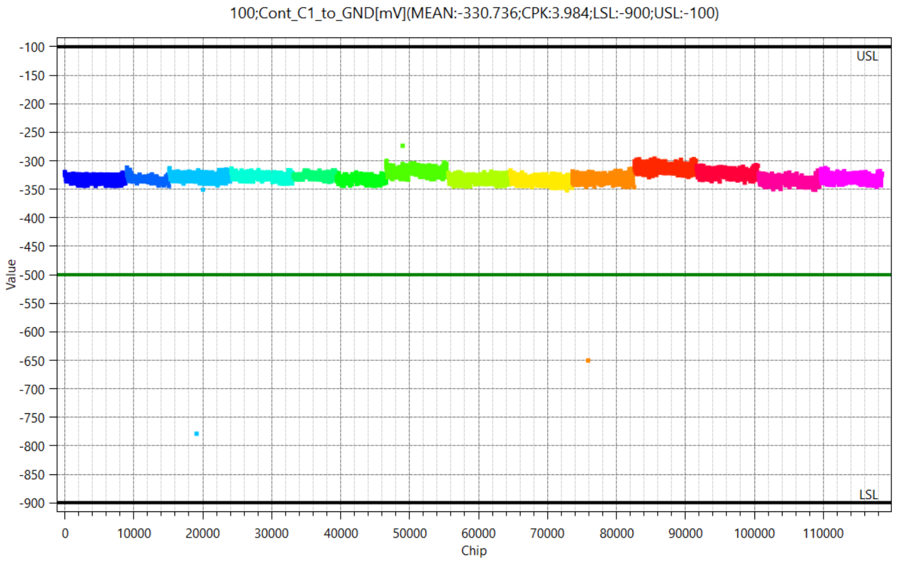
Overall Lot

100: Cont_C1_to_GND

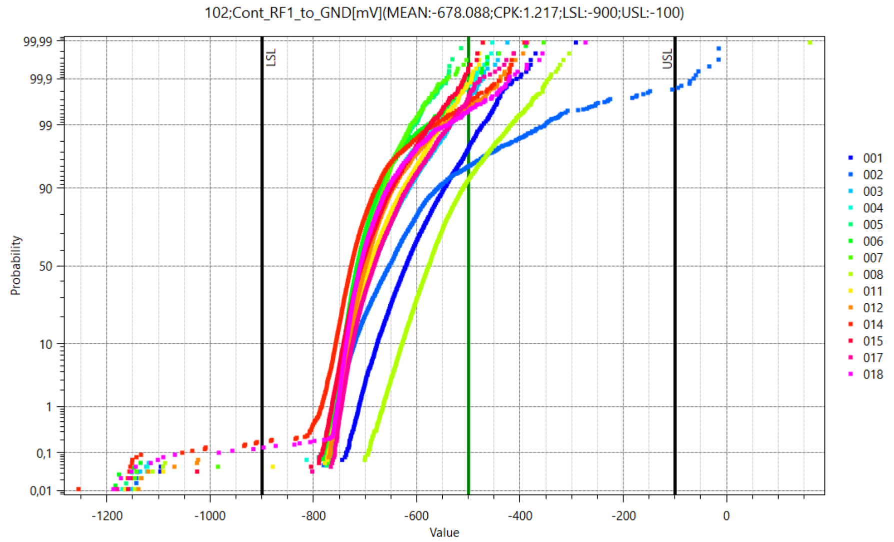


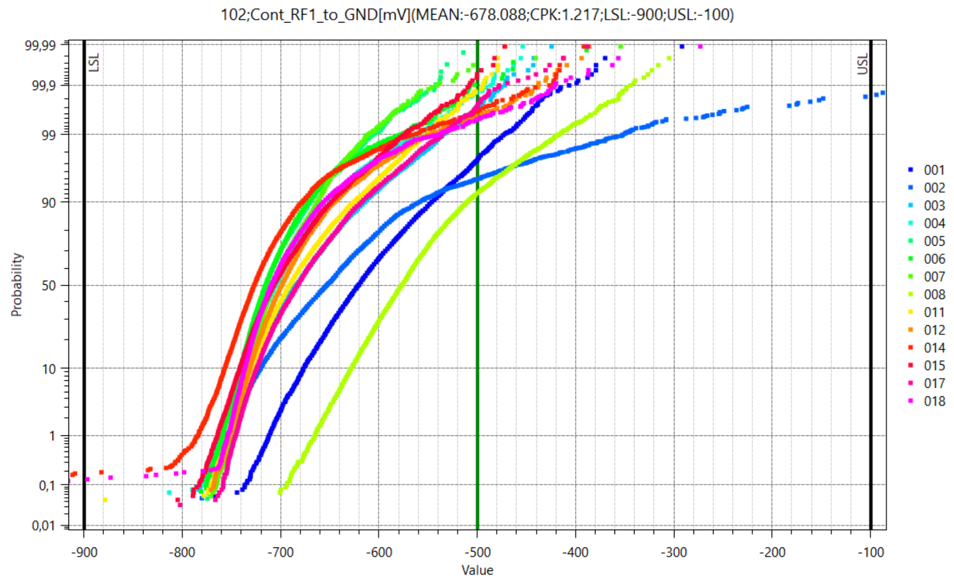


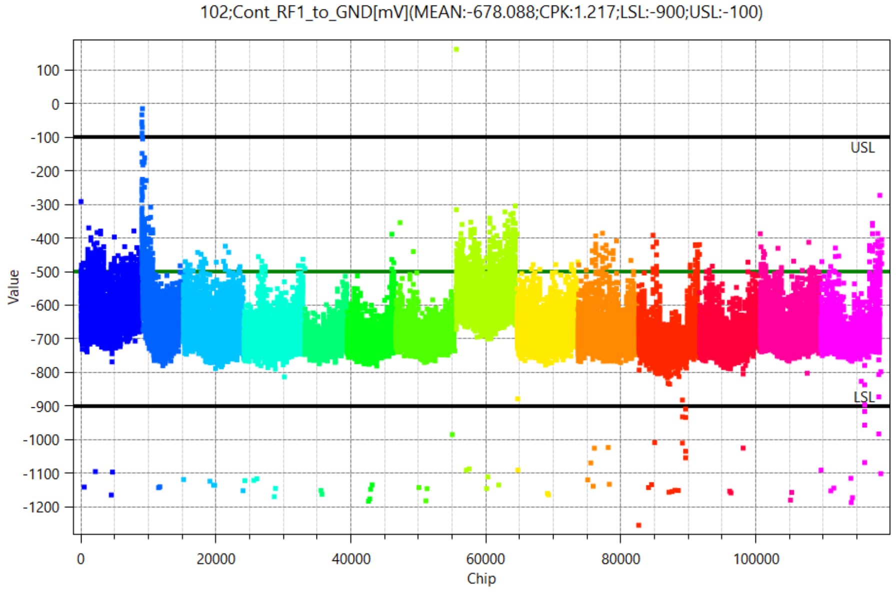


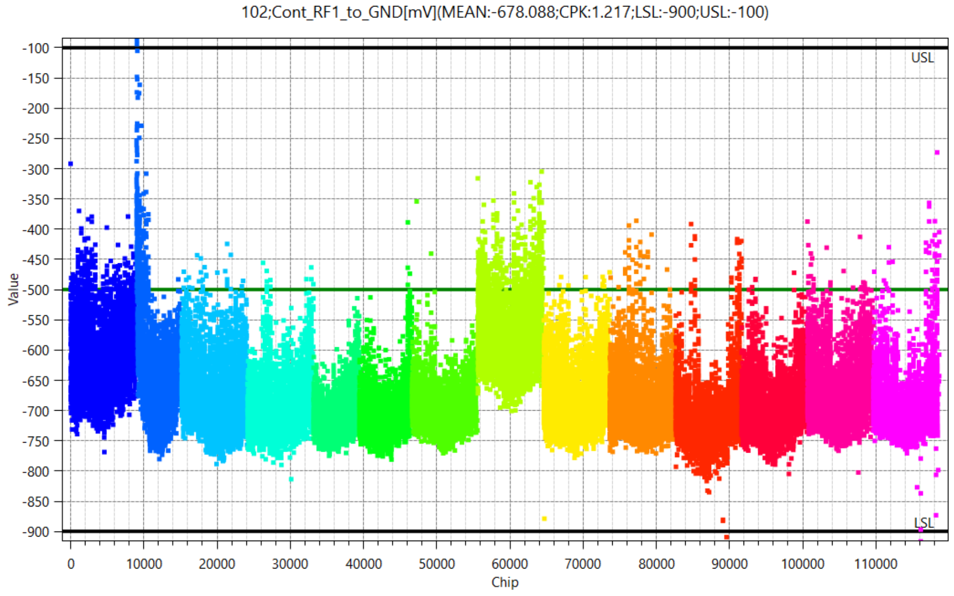


102: Cont_RF1_to_GND

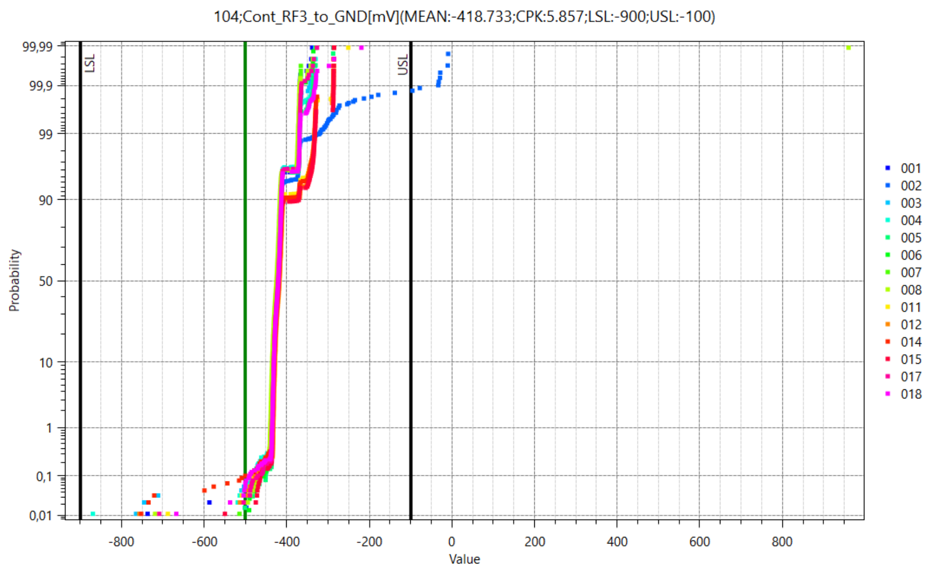


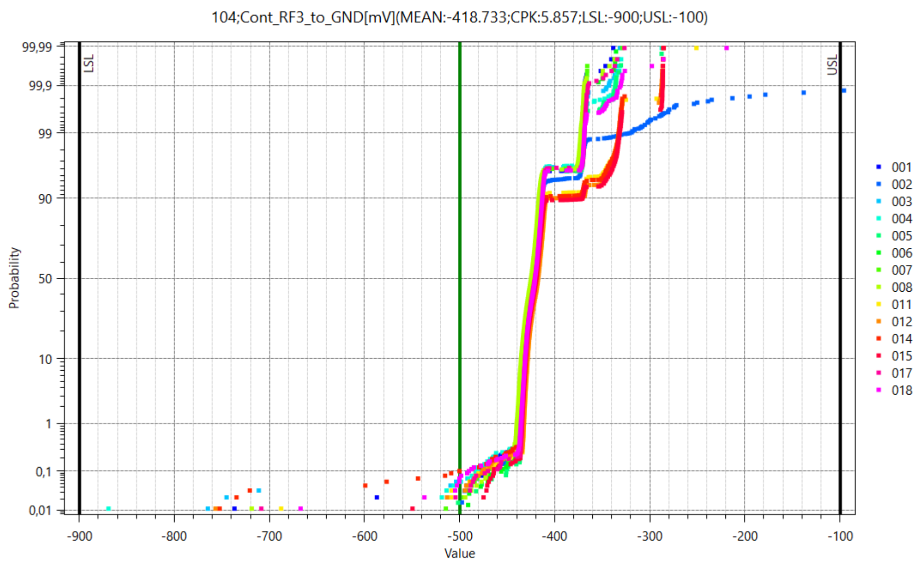


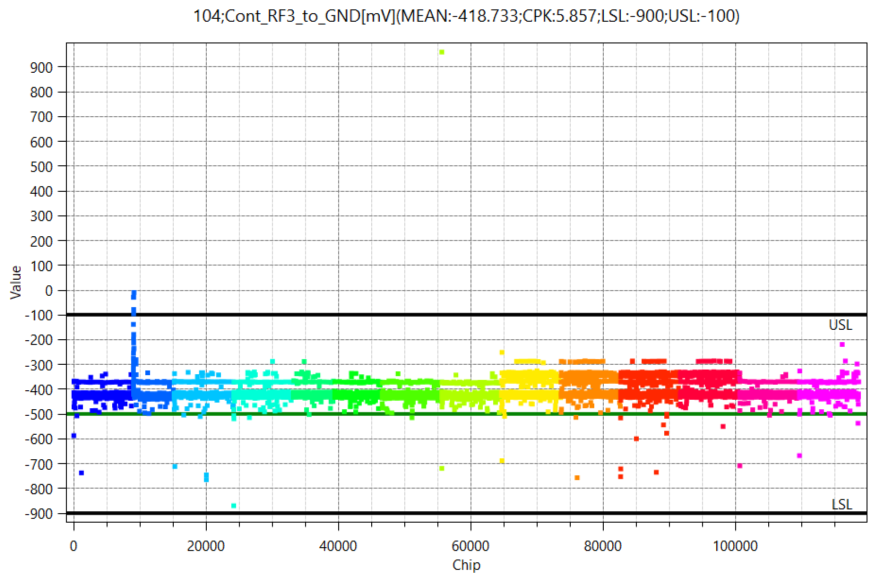


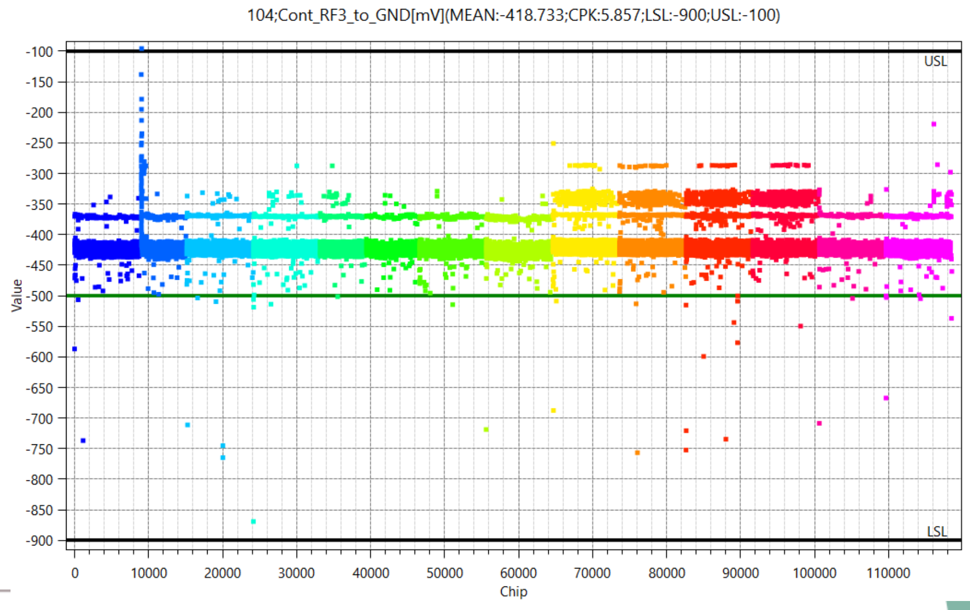


104: Cont_RF3_to_GND

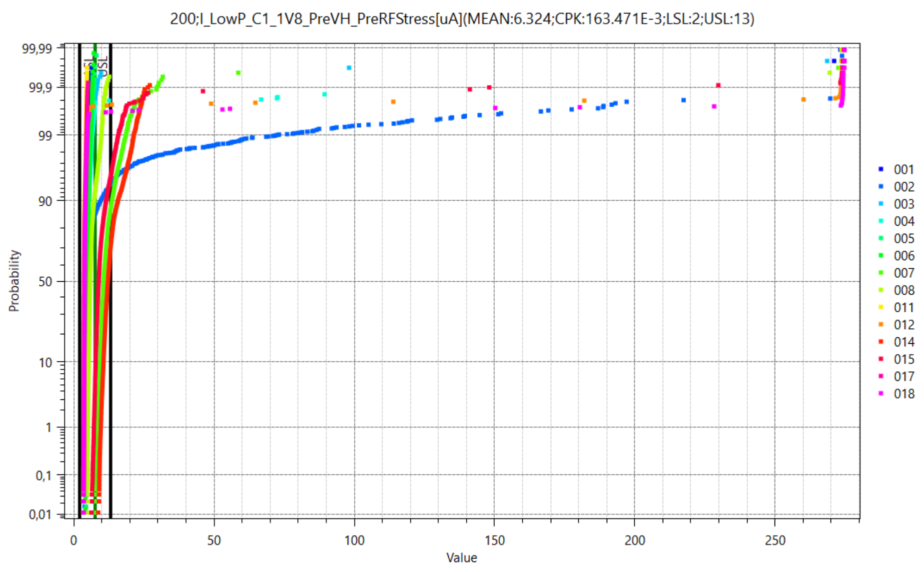


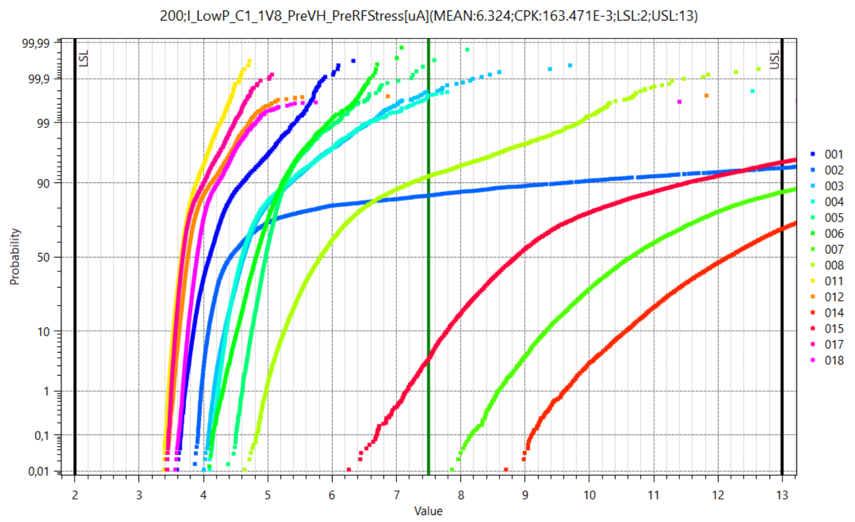


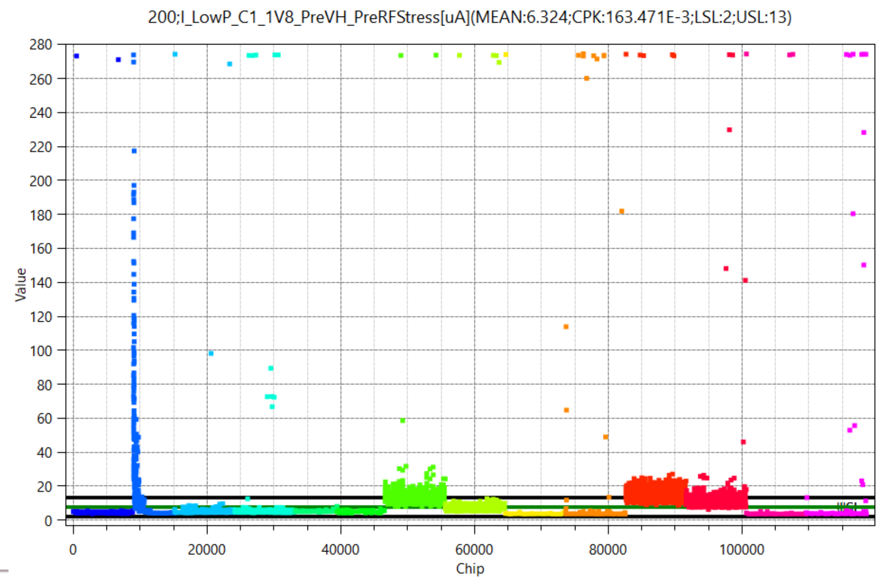


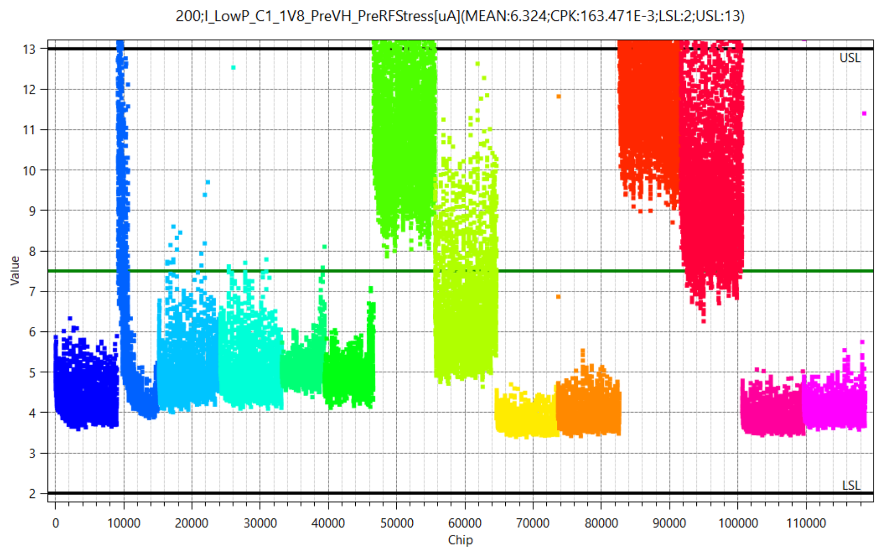


200: I_LowP_C1_1V8_PreVH_PreRFStress

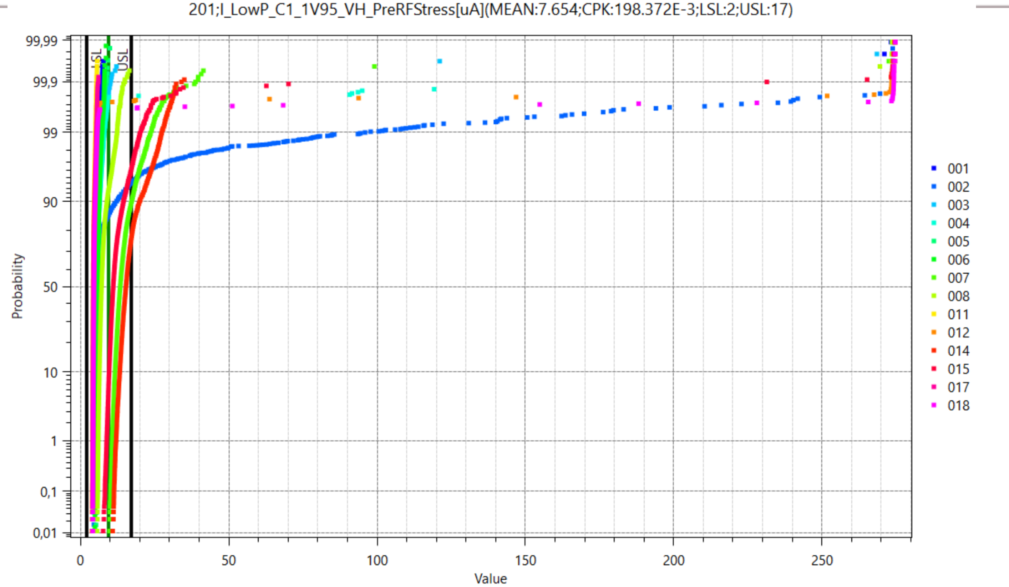


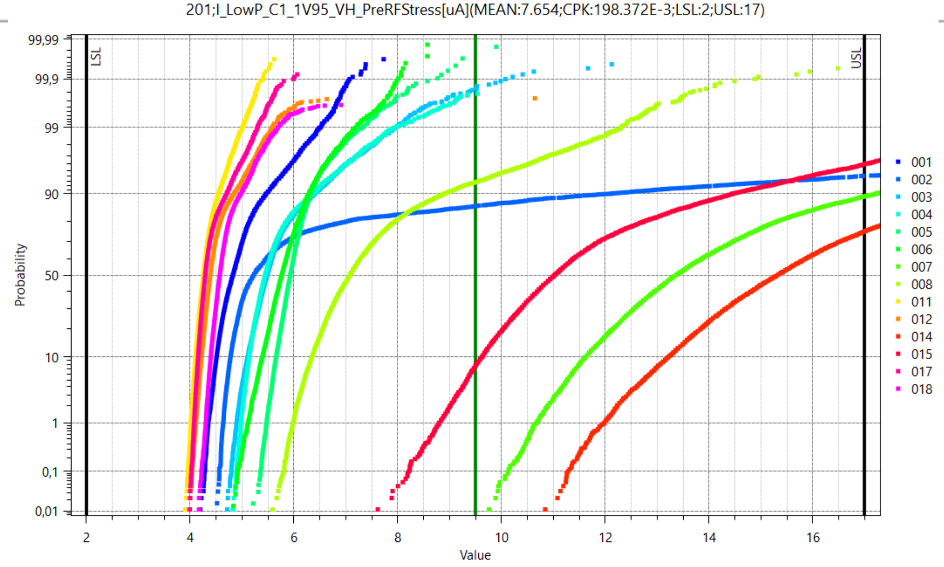


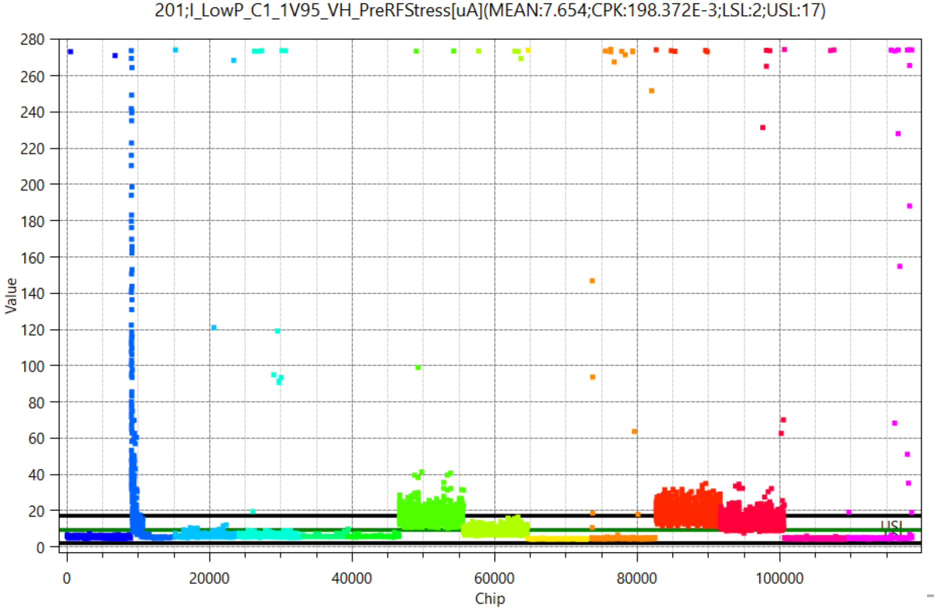


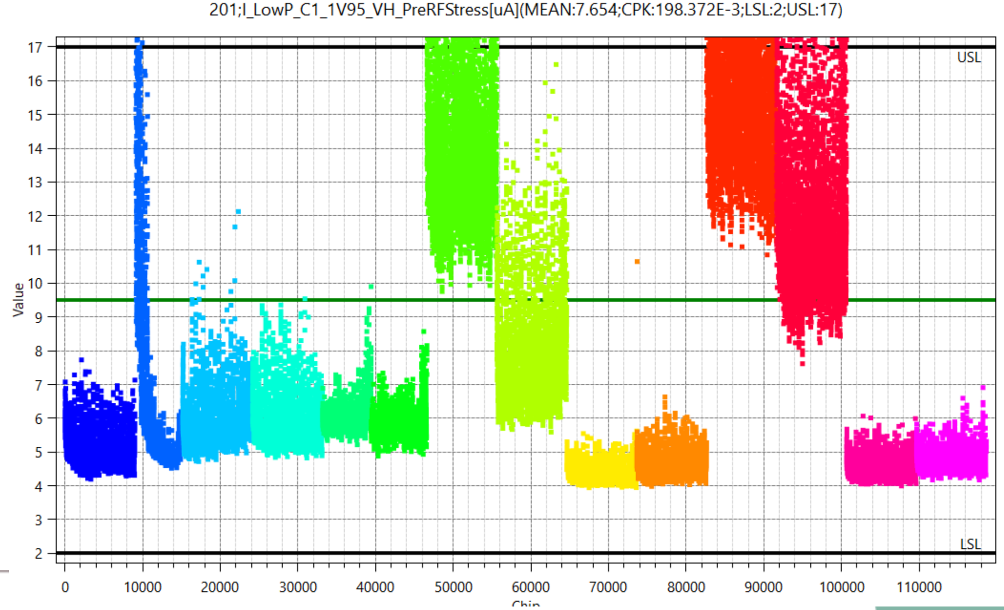


201: I_LowP_C1_1V95_VH_PreRFStress

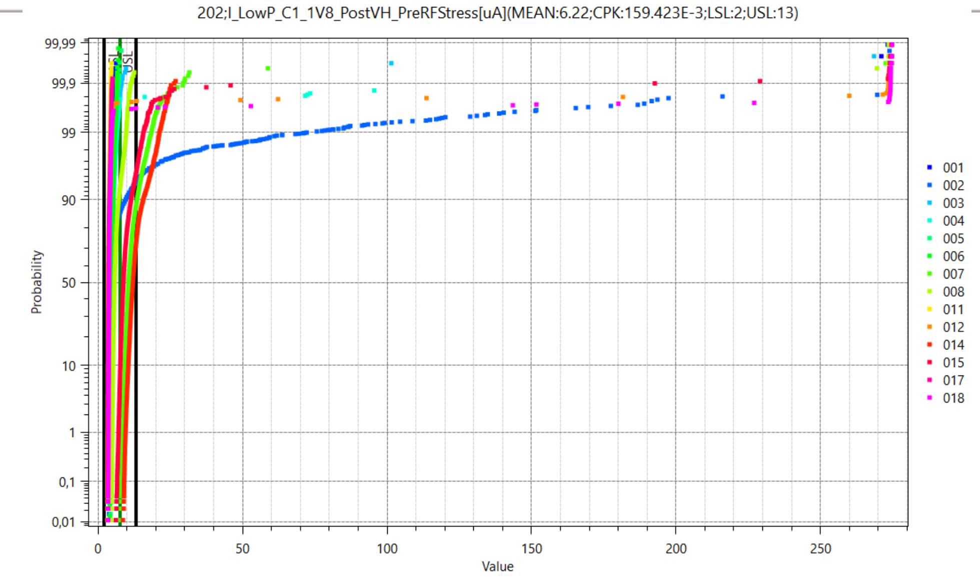


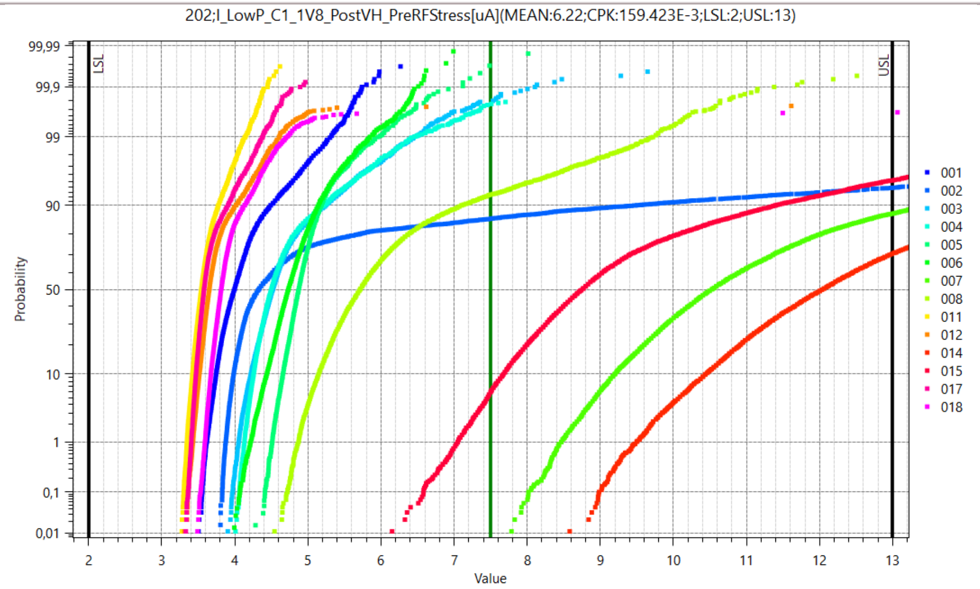


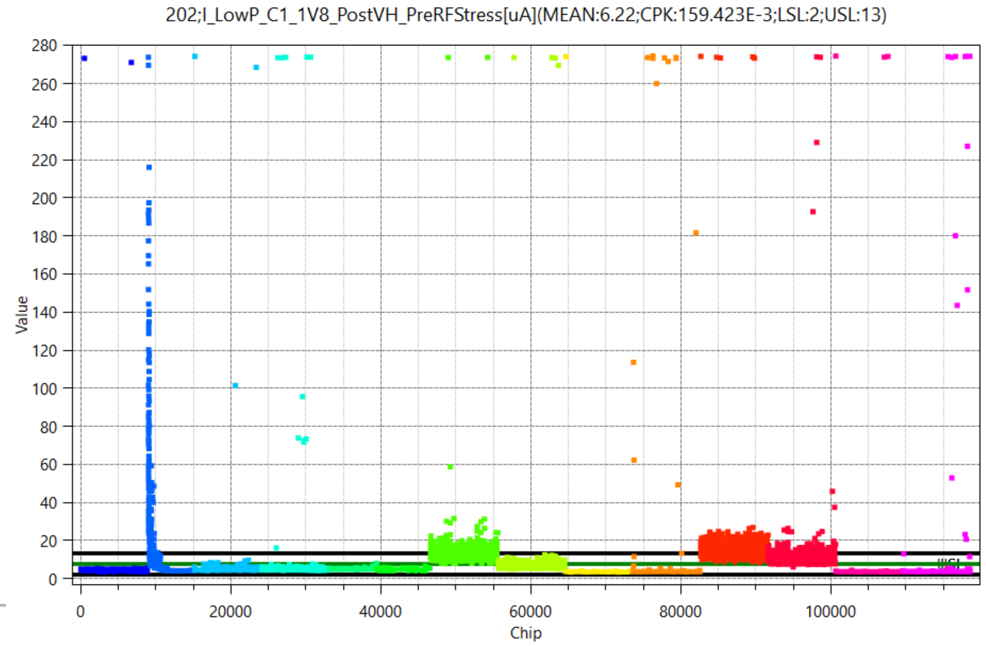


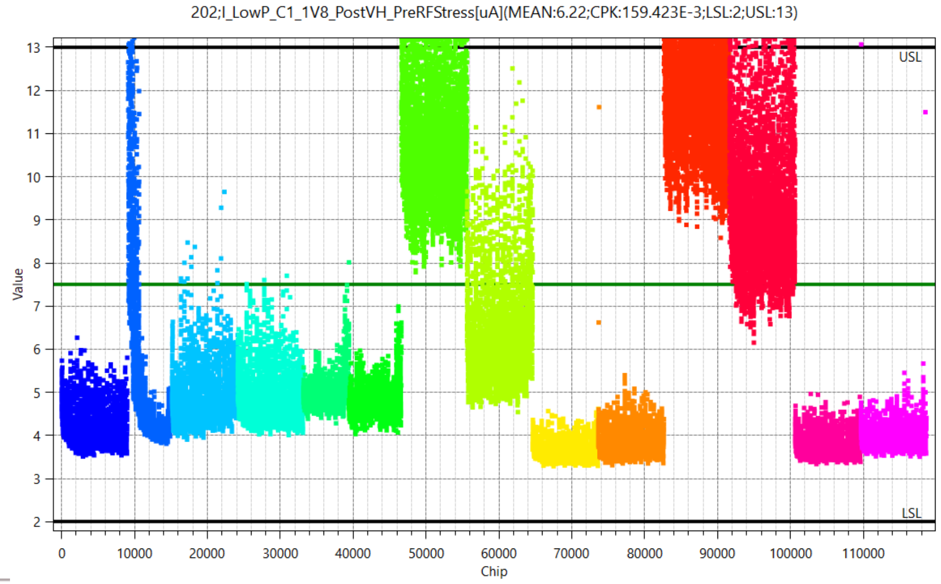


202: I_LowP_C1_1V8_PostVH_PreRFStress

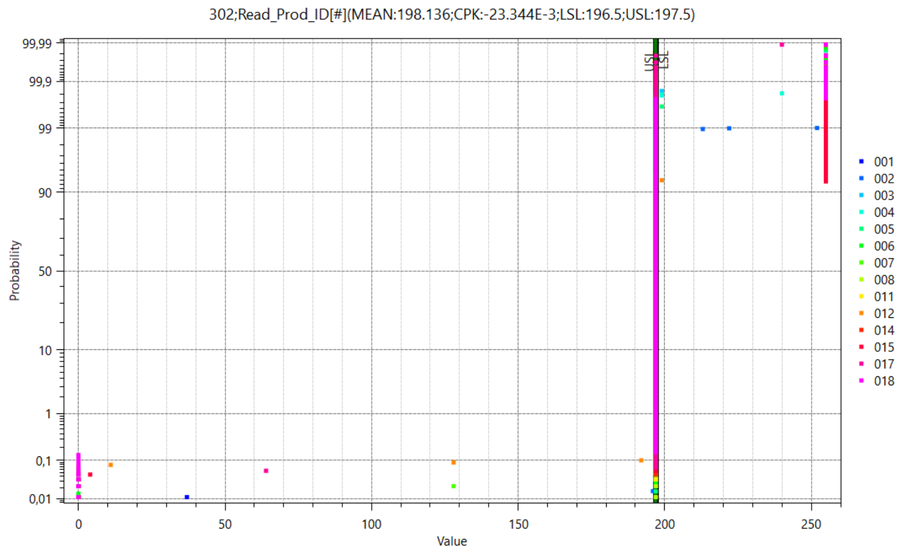


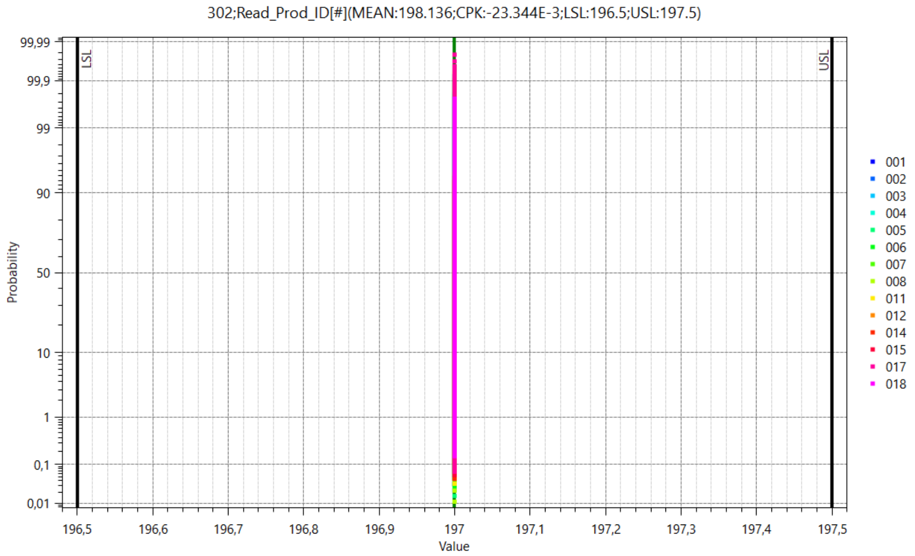


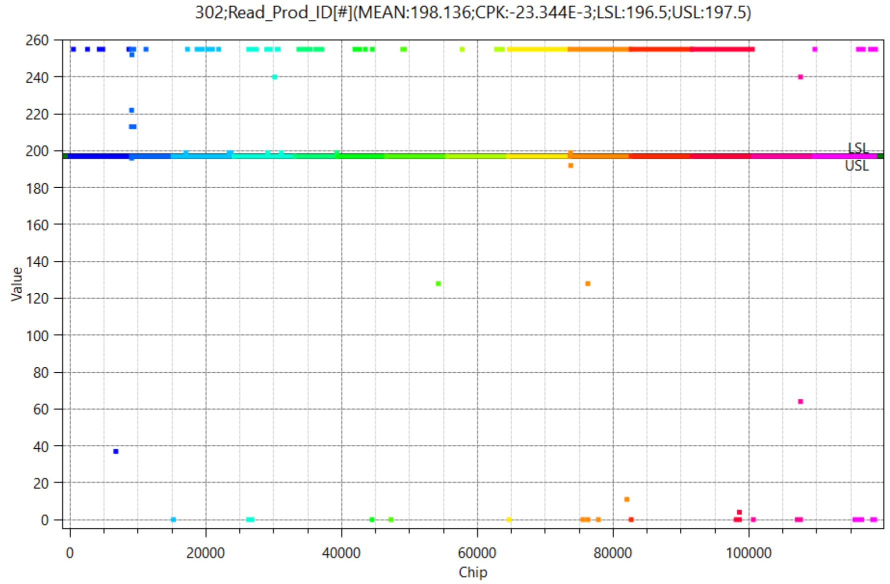


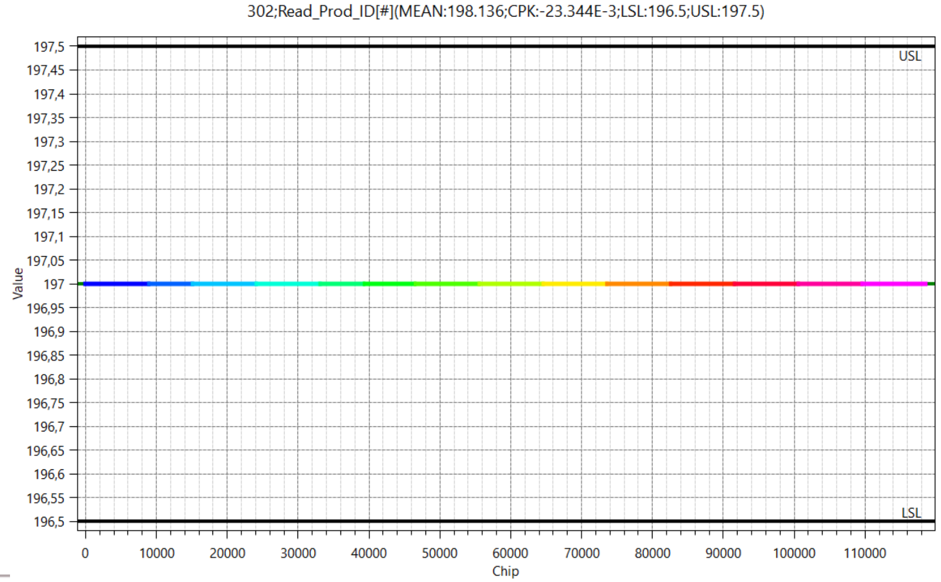


302: Read_Prod_ID

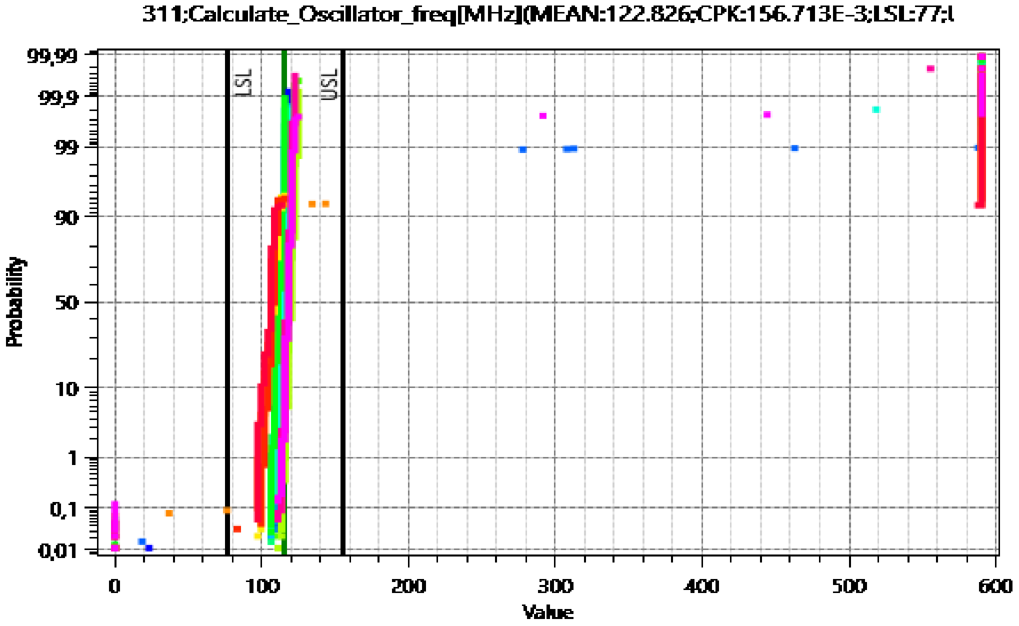


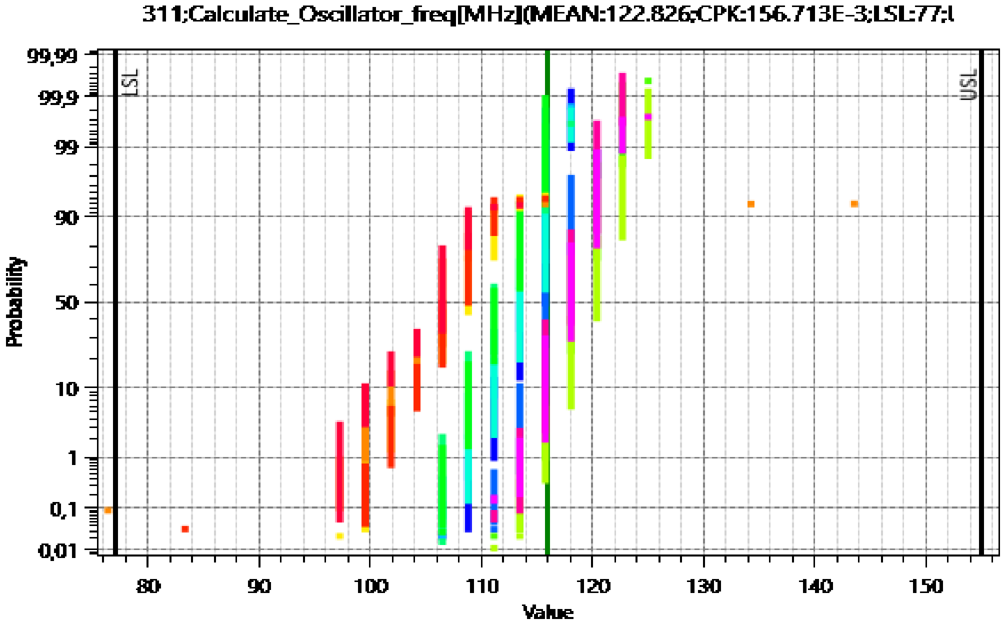


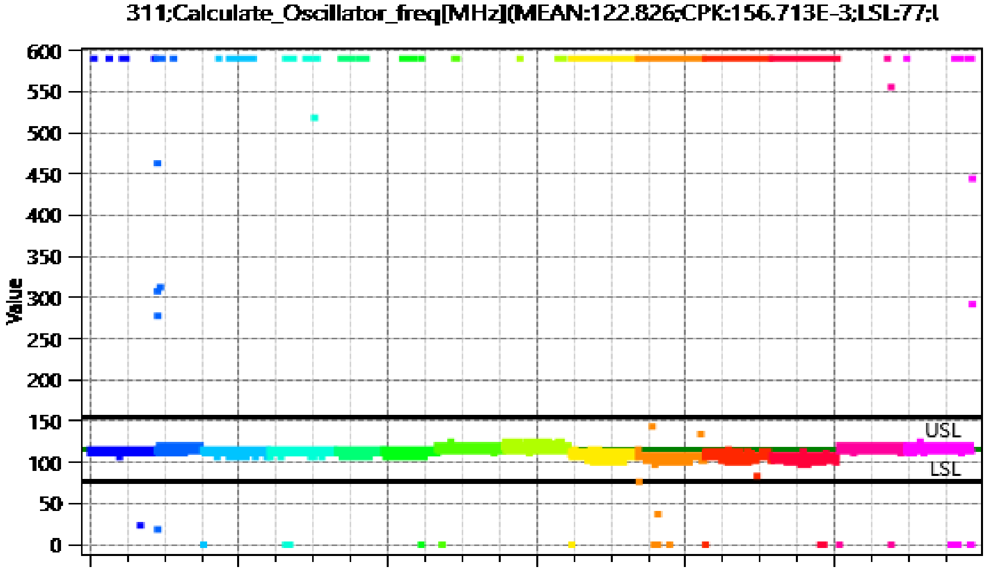


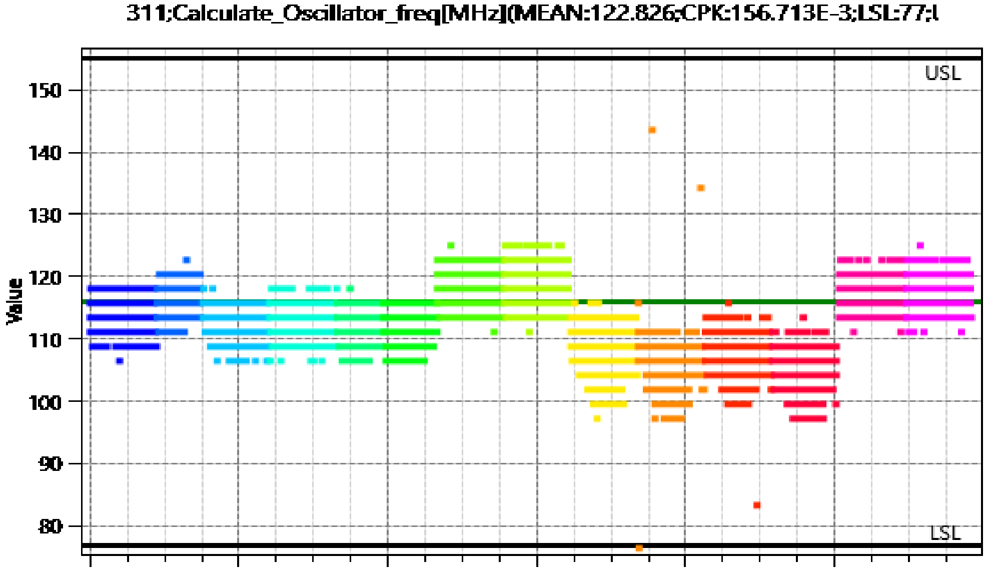


311: Calculate_Oscillator_freq

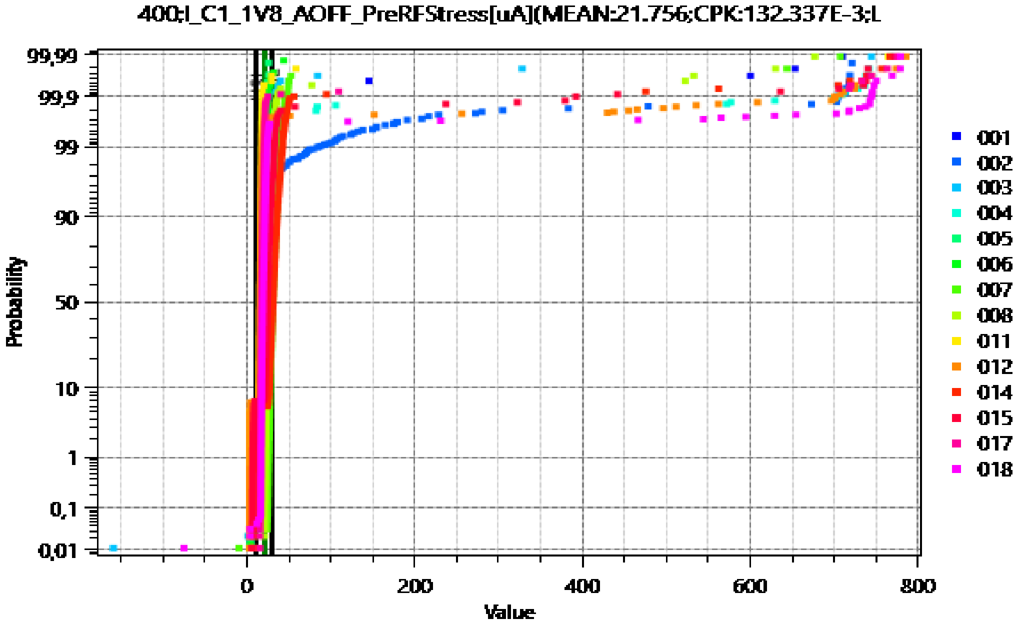


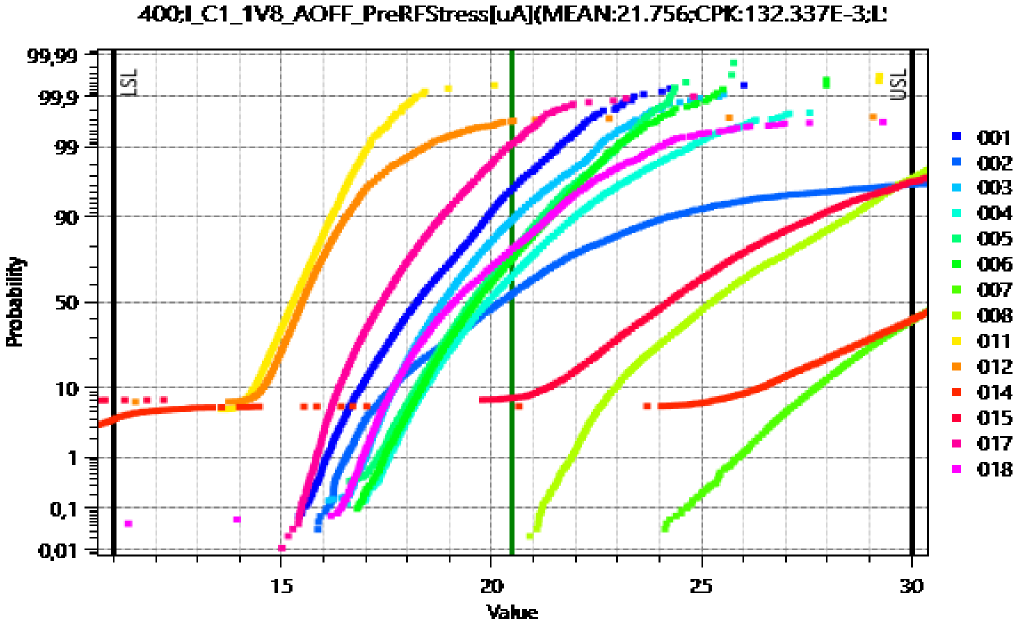


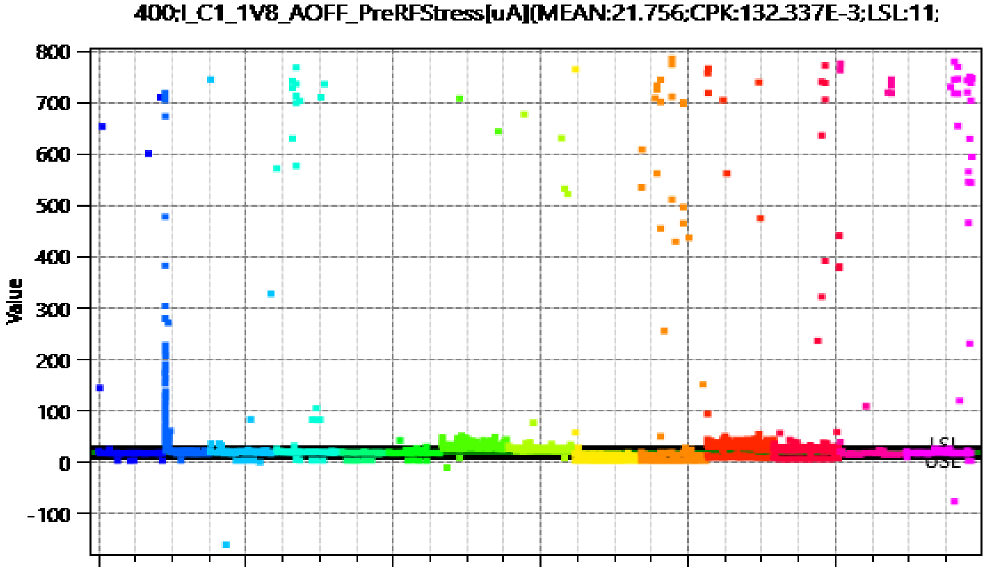


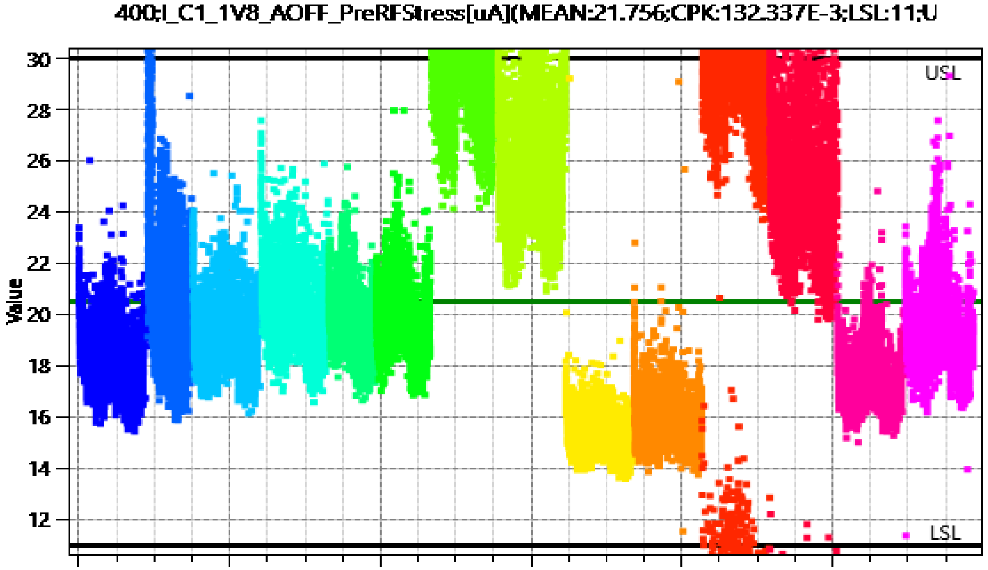


400: I_C1_1V8_AOFF_PreRFStress

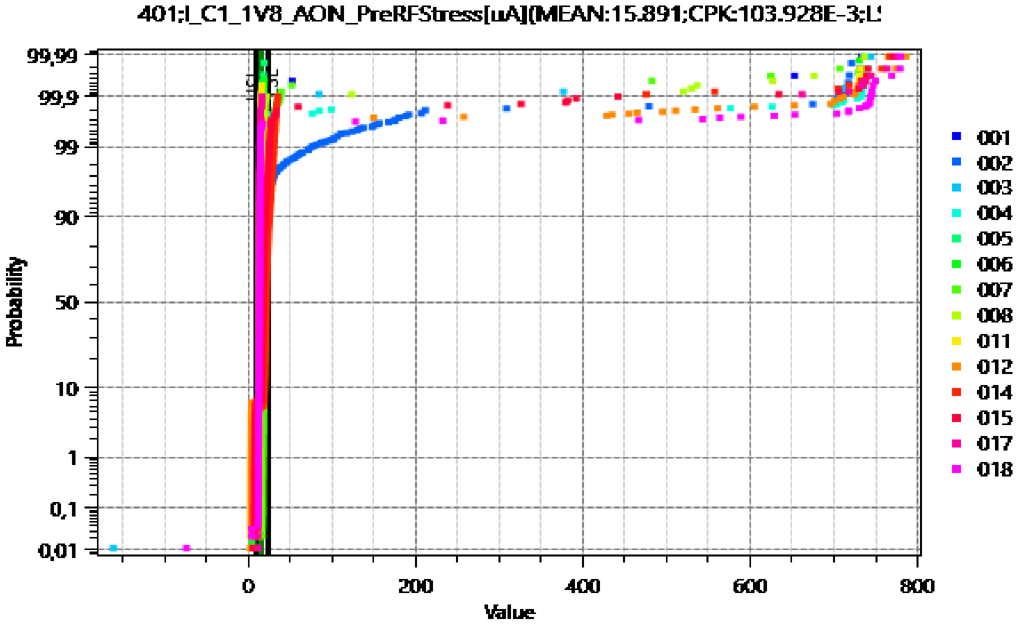


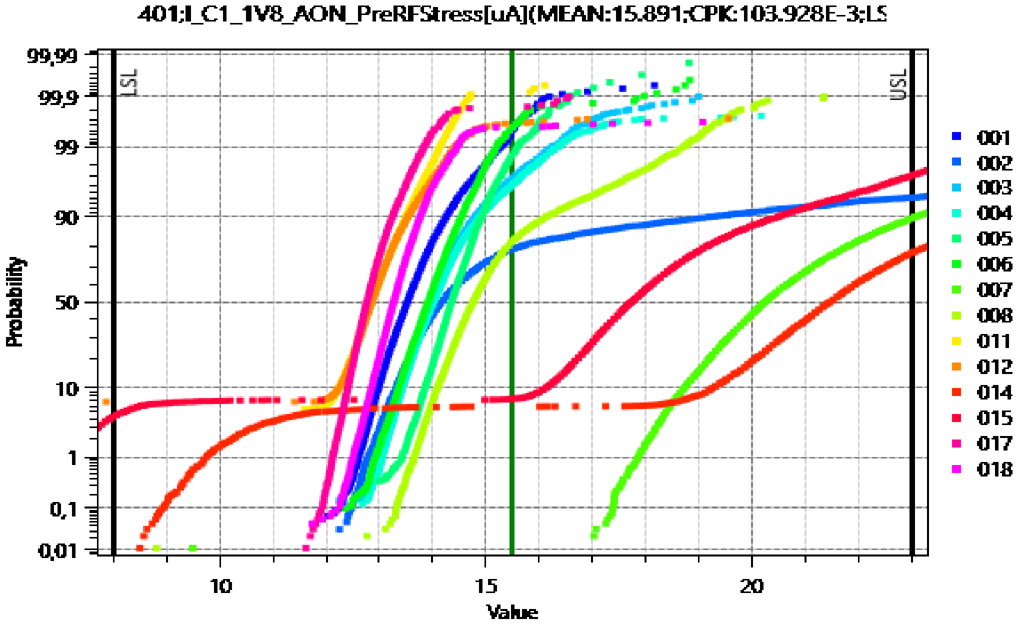


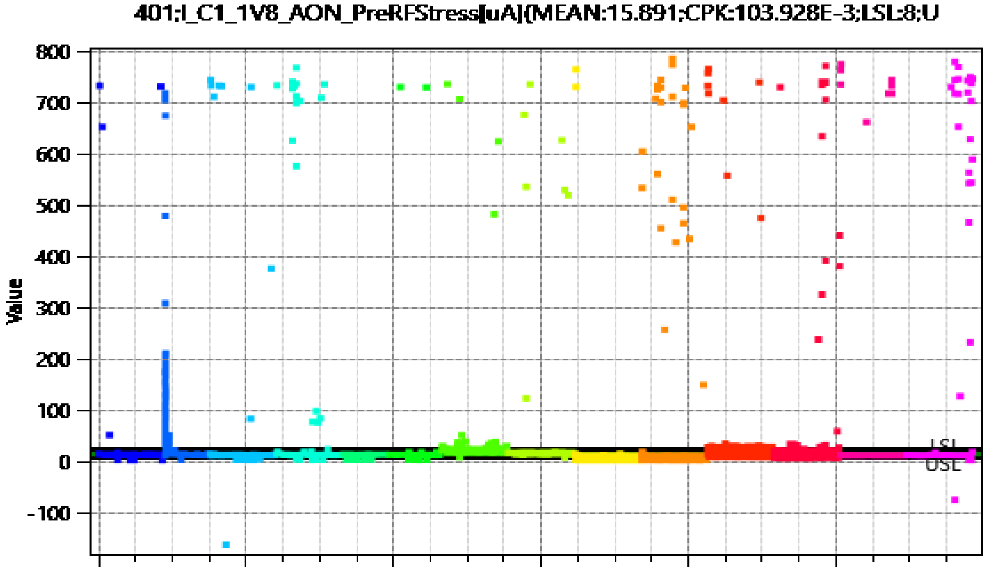


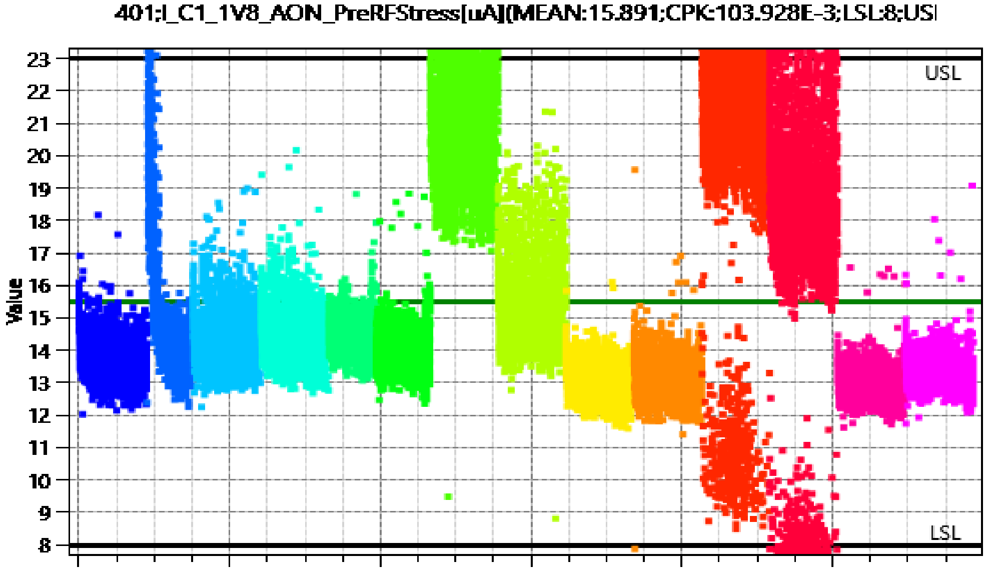


401: I_C1_1V8_AON_PreRFStress

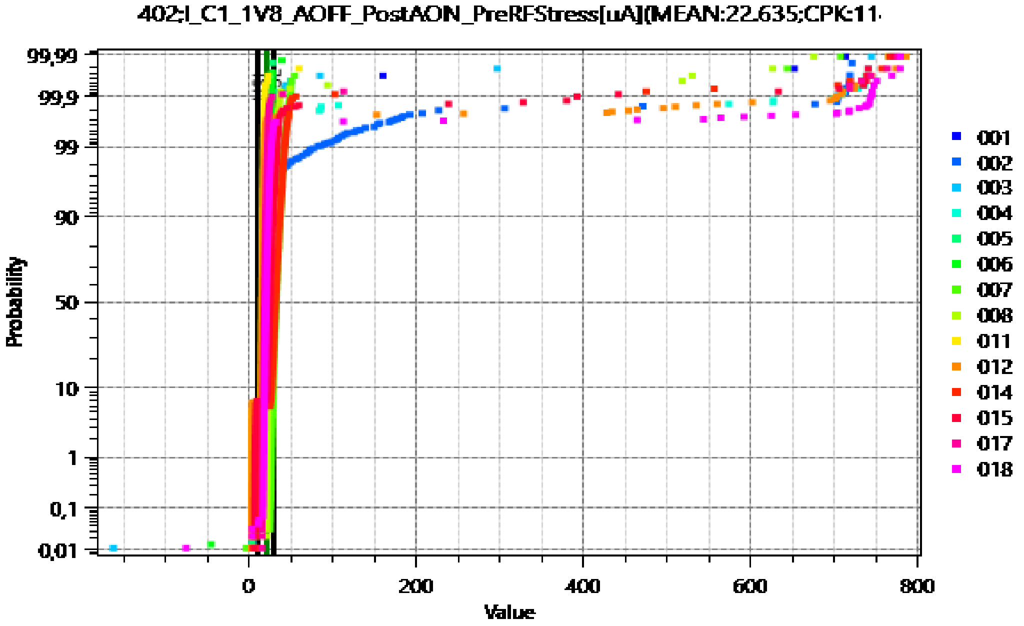


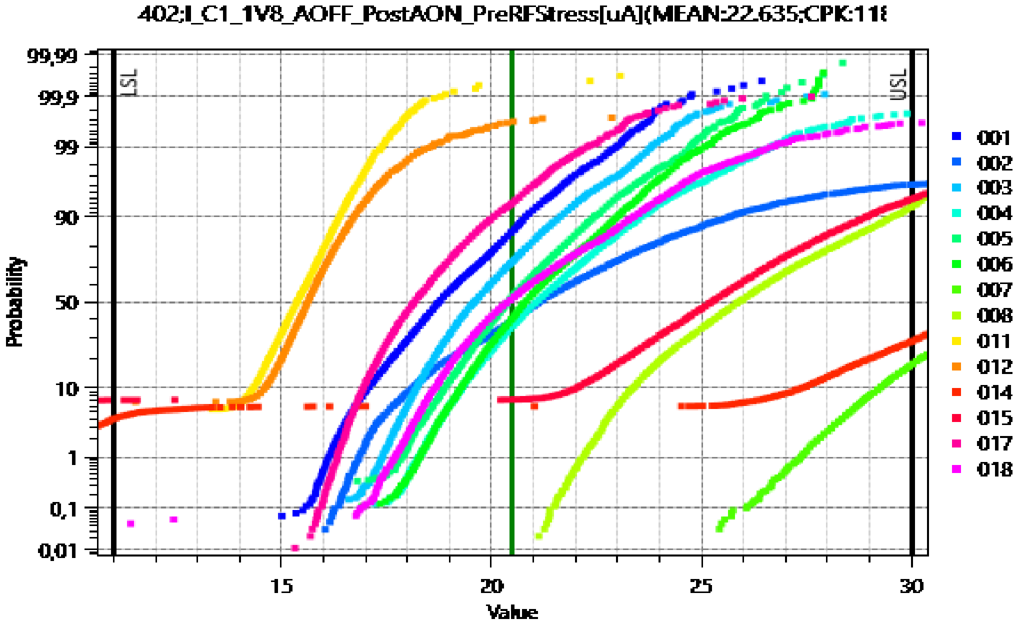


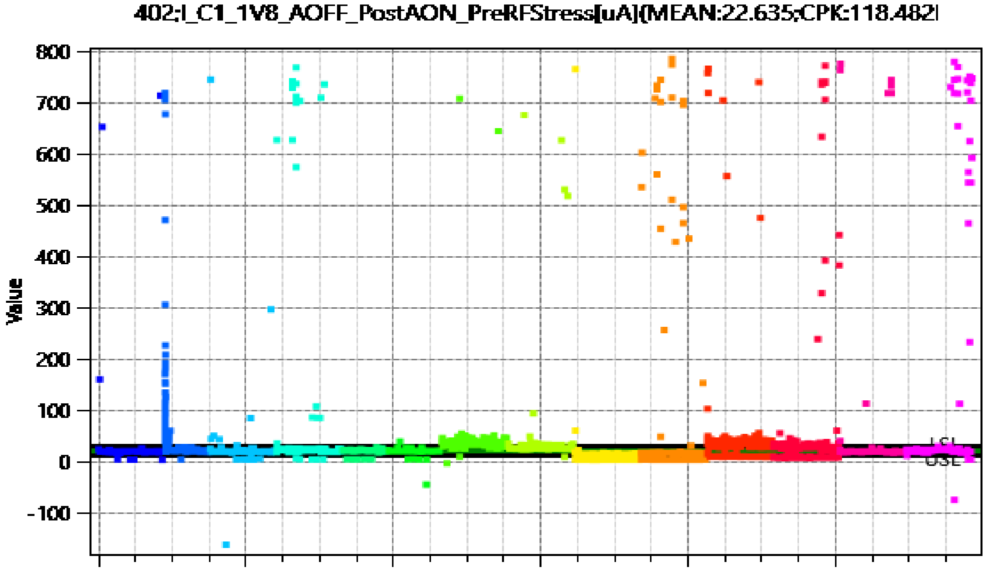


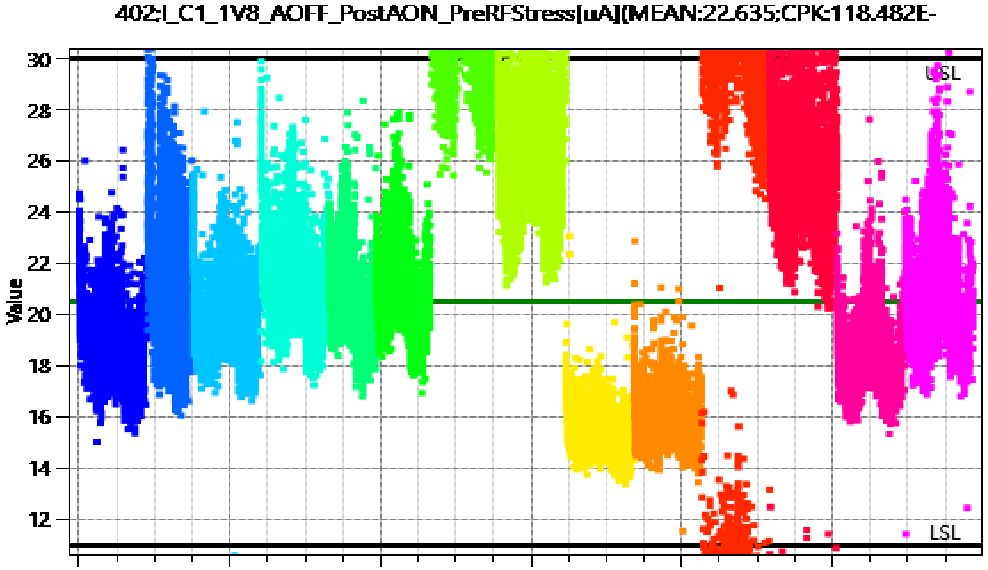


402: I_C1_1V8_AOFF_PostAON_PreRFStress

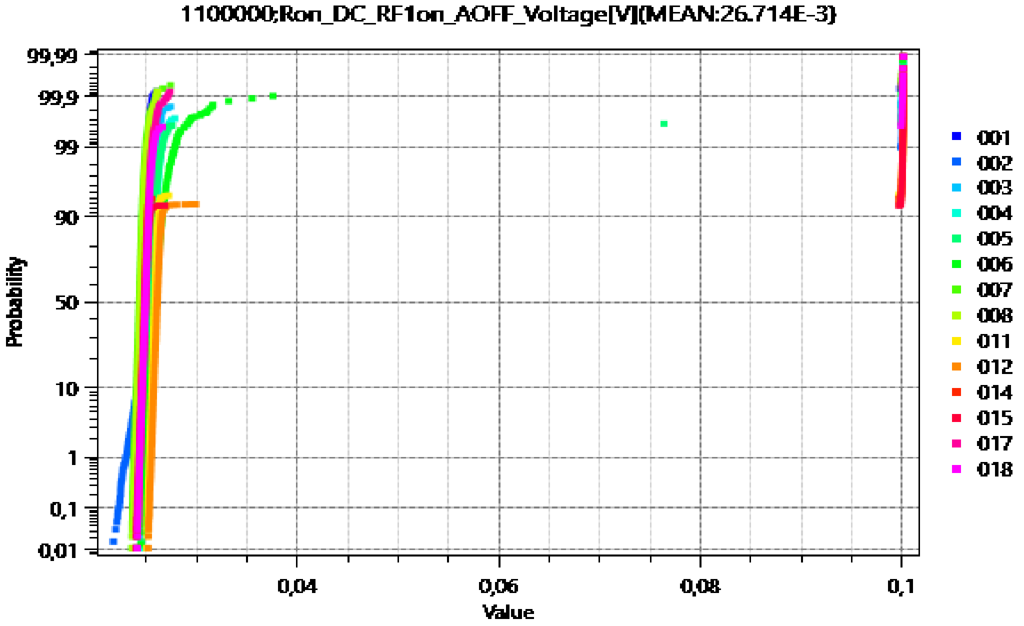


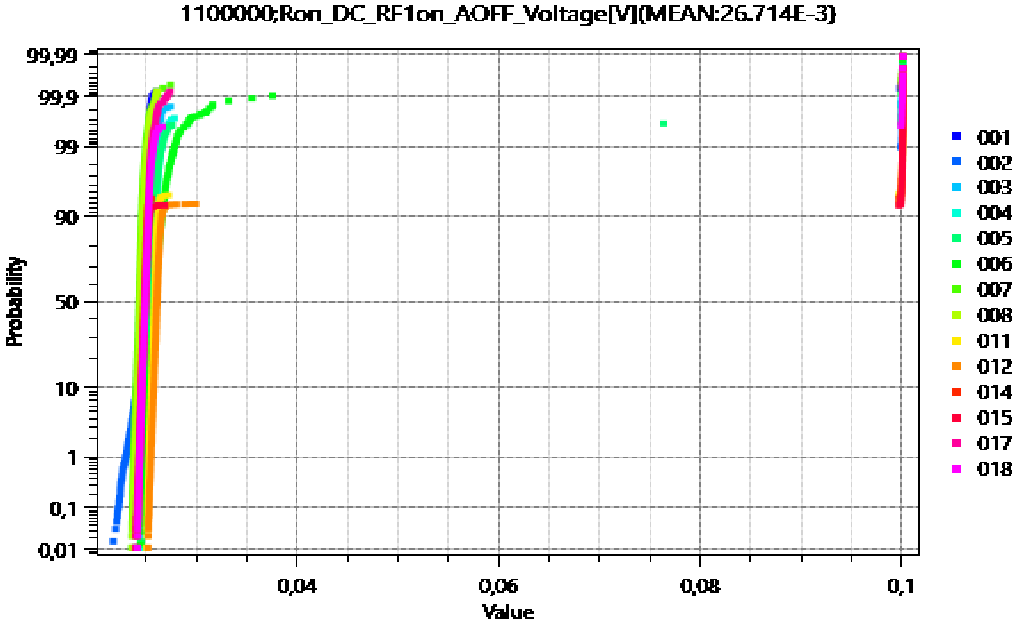


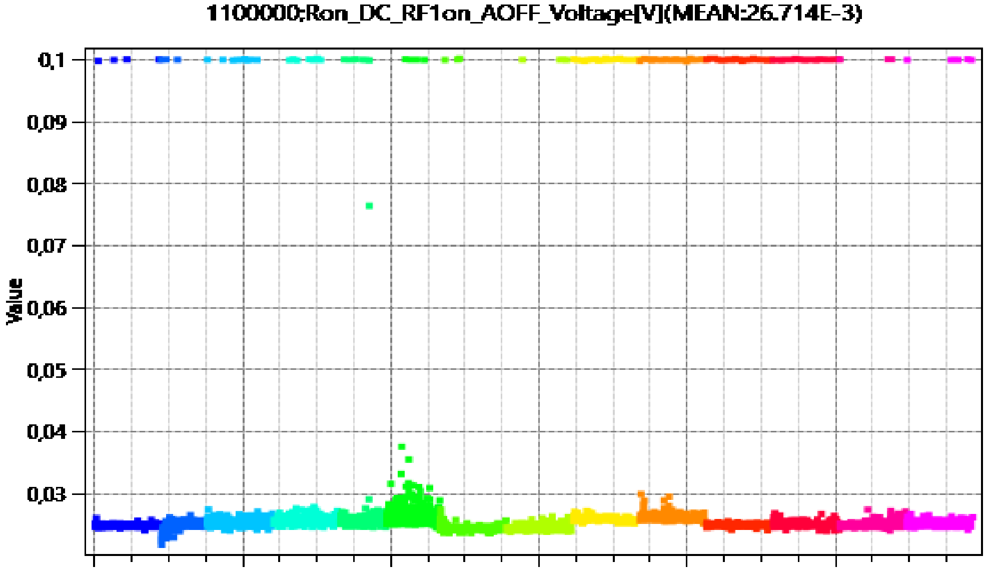


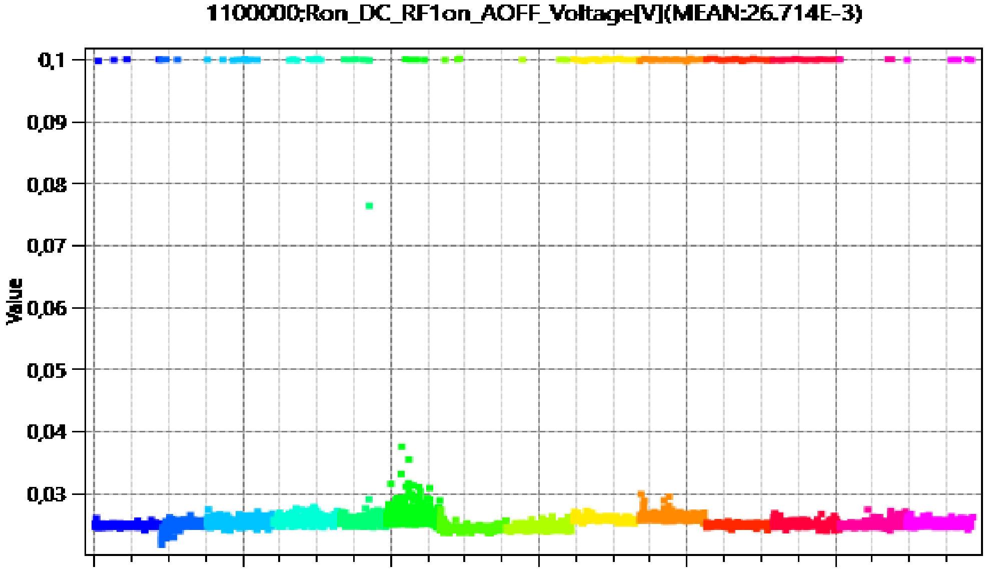


1100000: Ron_DC_RF1on_AOFF_Voltage

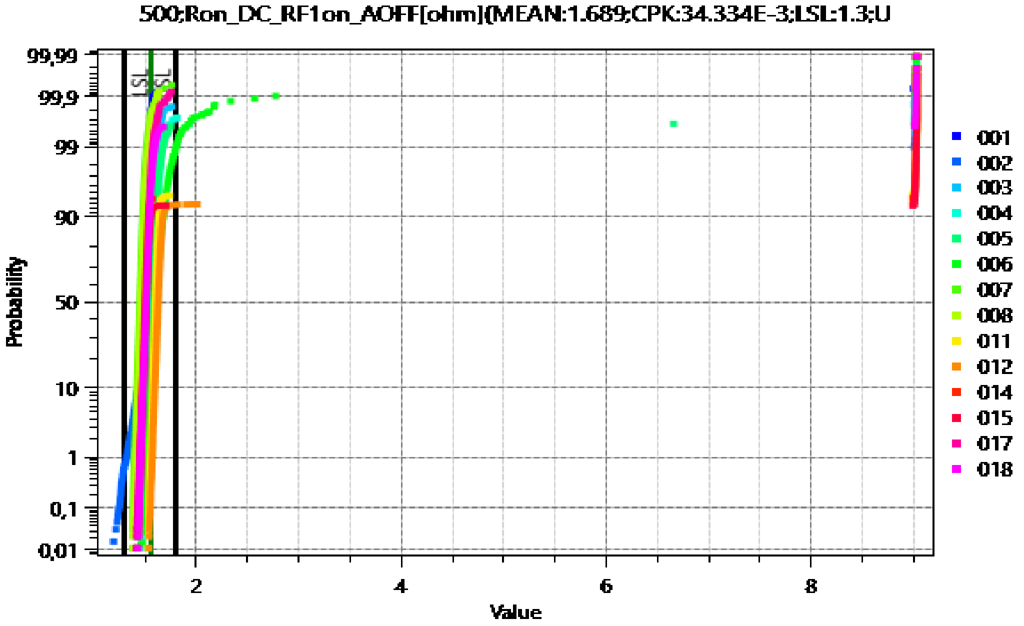


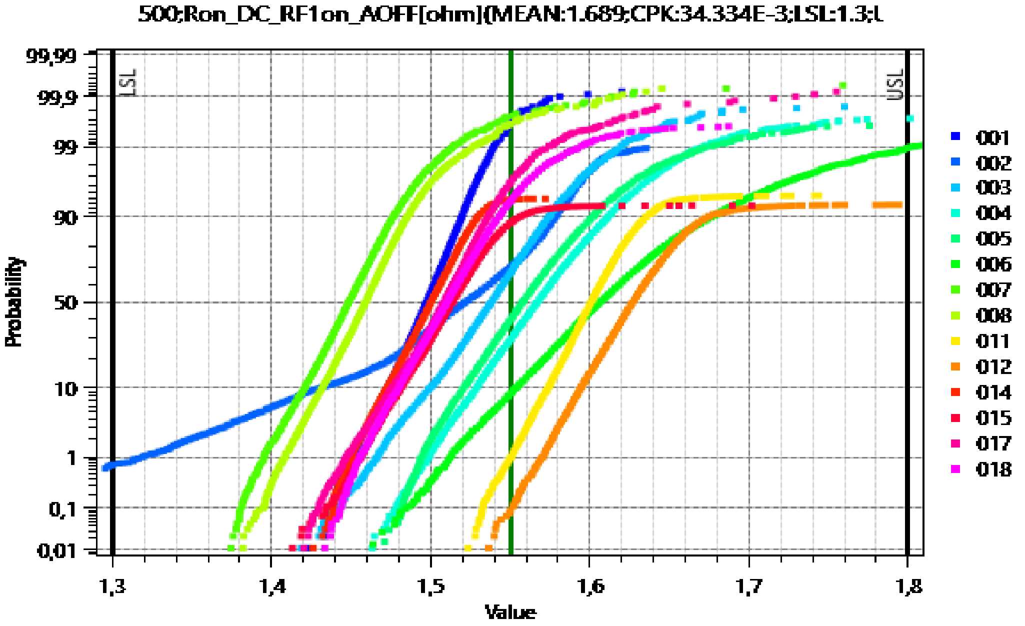


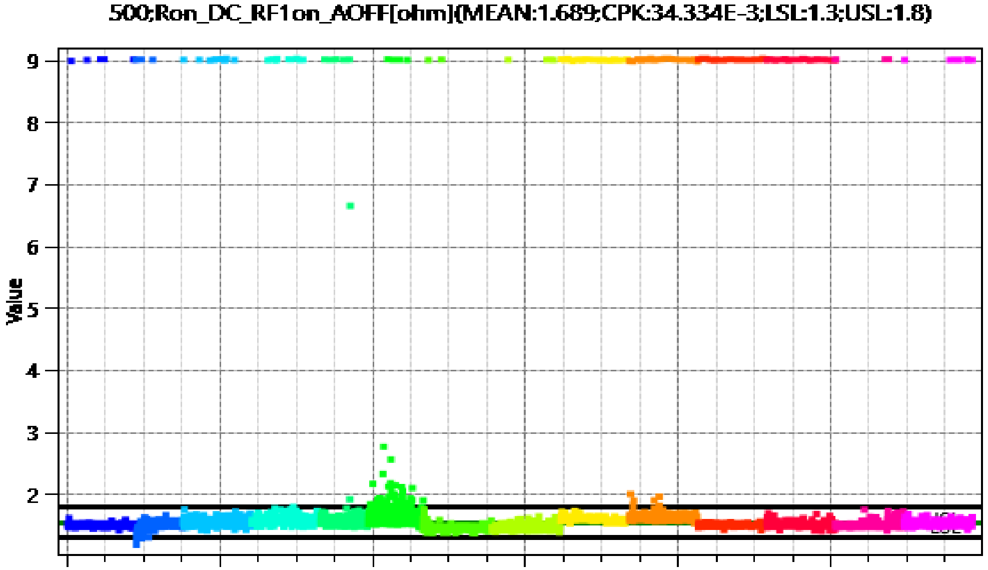


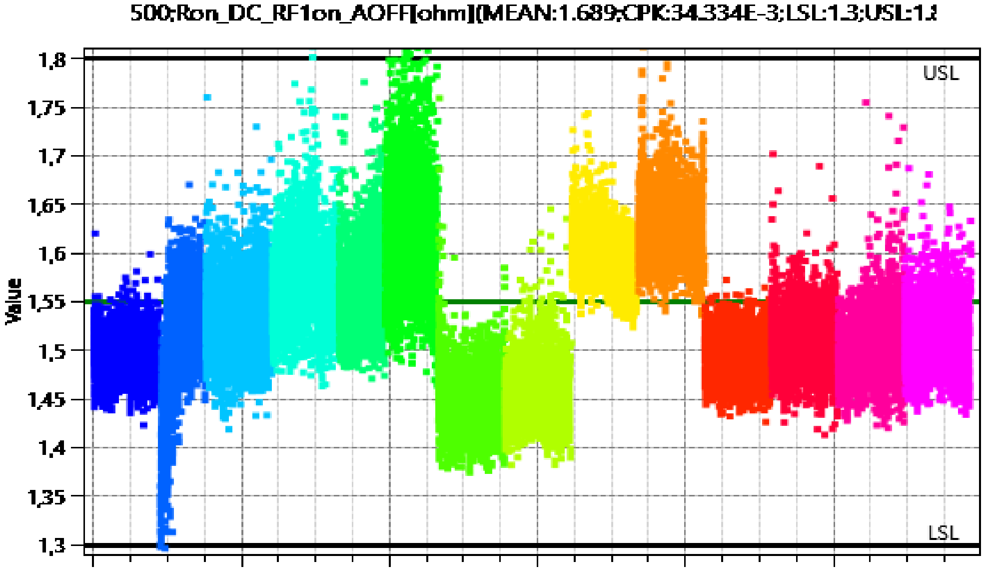


500: Ron_DC_RF1on_AOFF

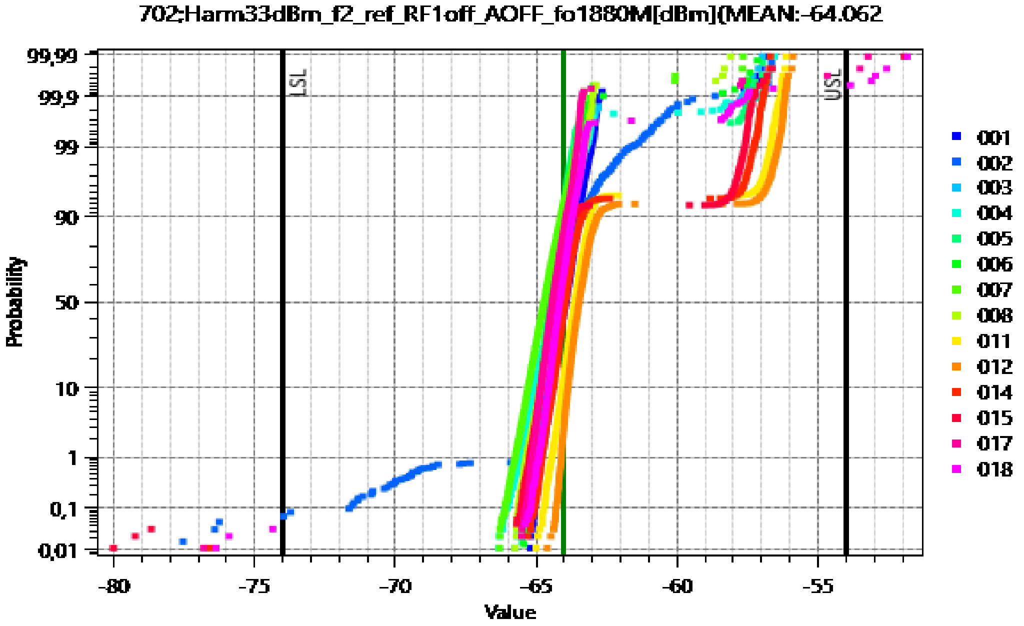


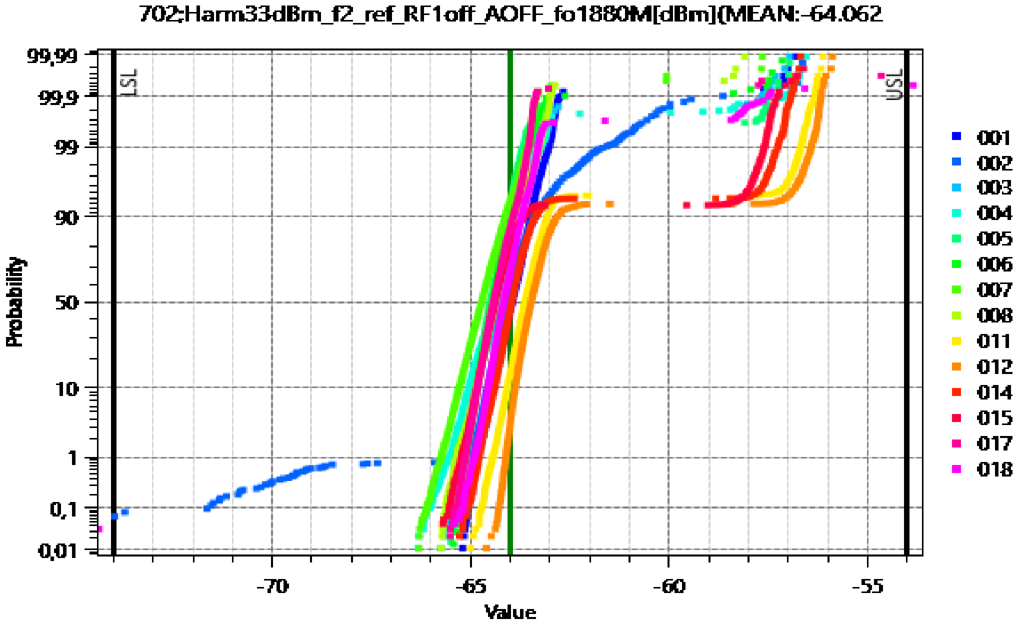


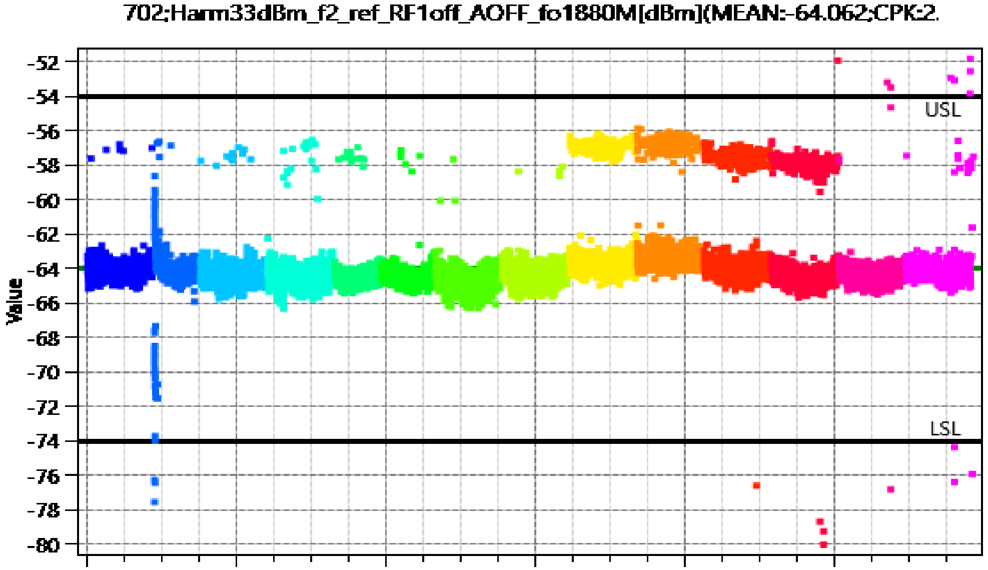


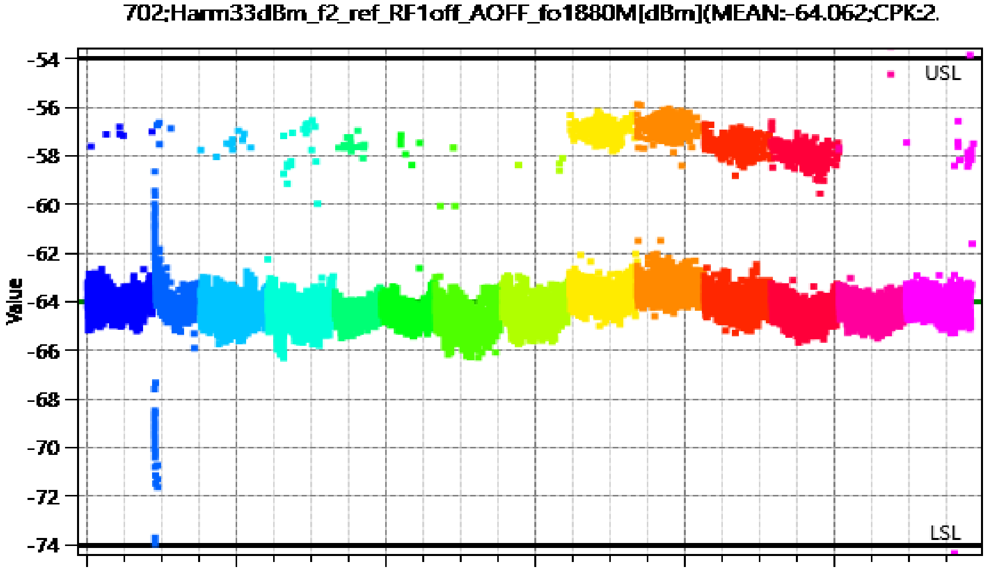


702: Harm33dBm_f2_ref_RF1off_AOFF_fo1880M

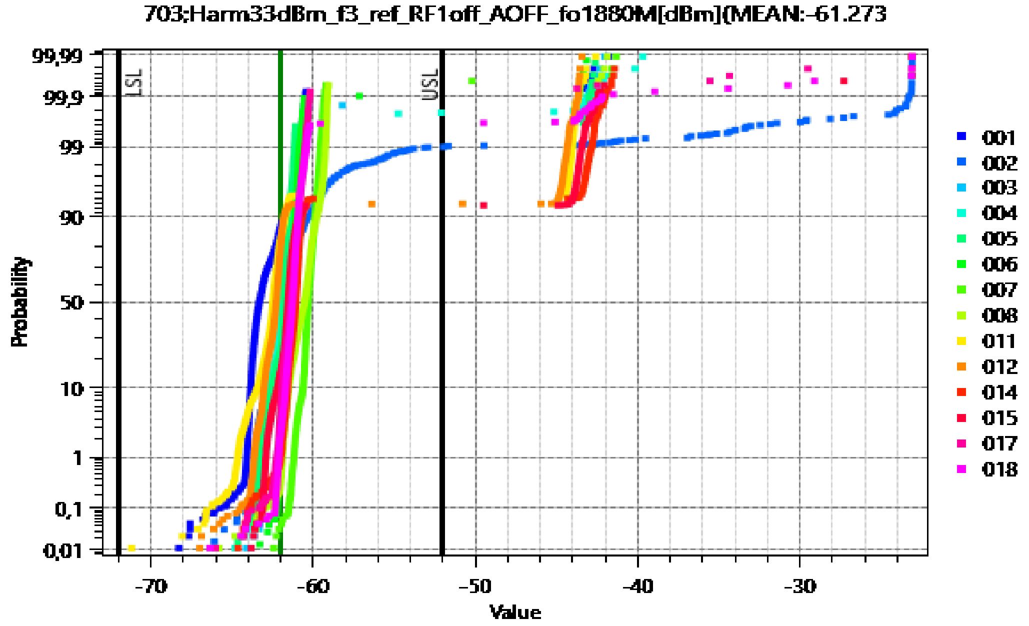


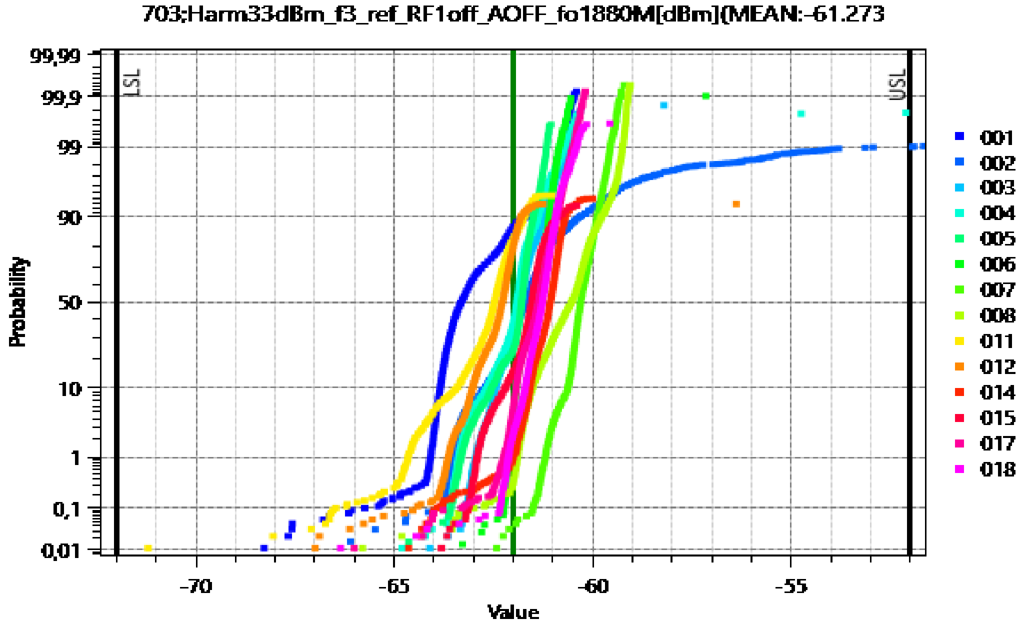


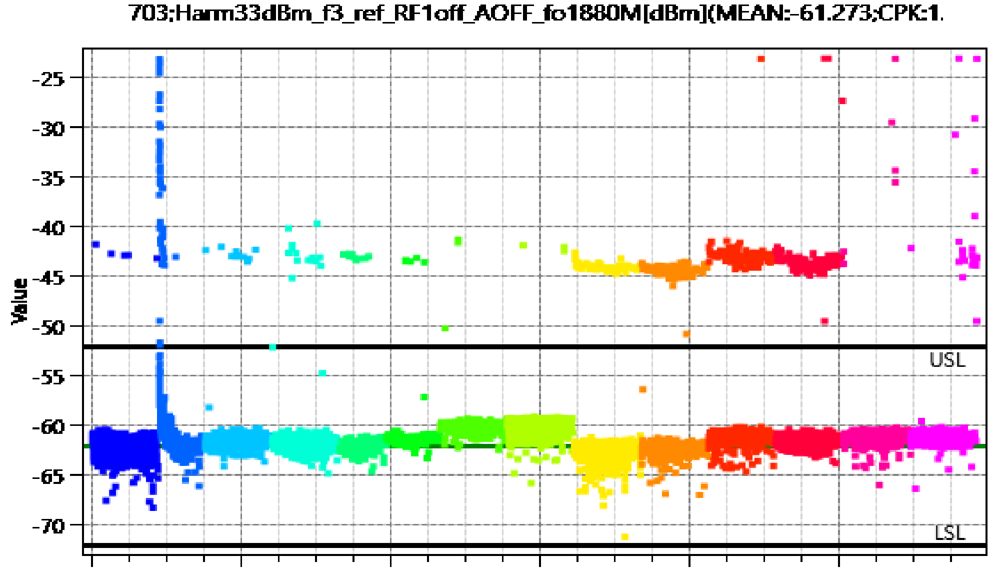


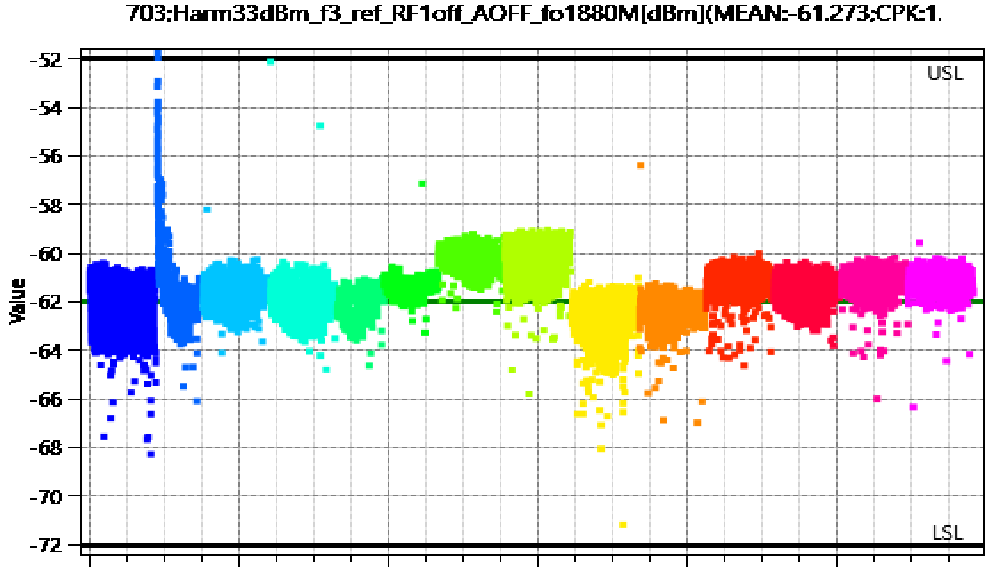


703: Harm33dBm_f3_ref_RF1off_AOFF_fo1880M

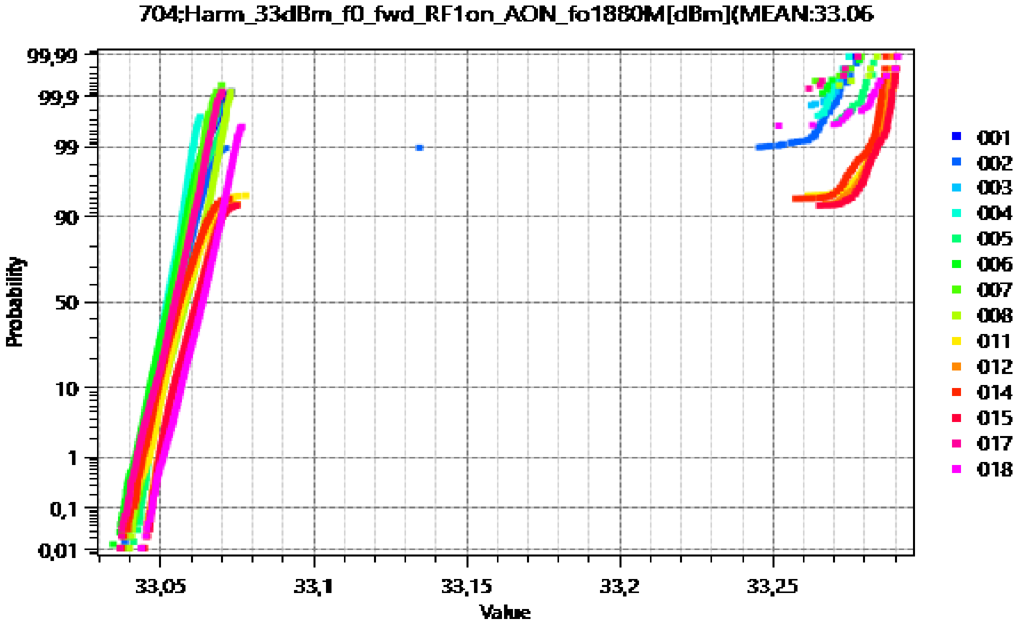


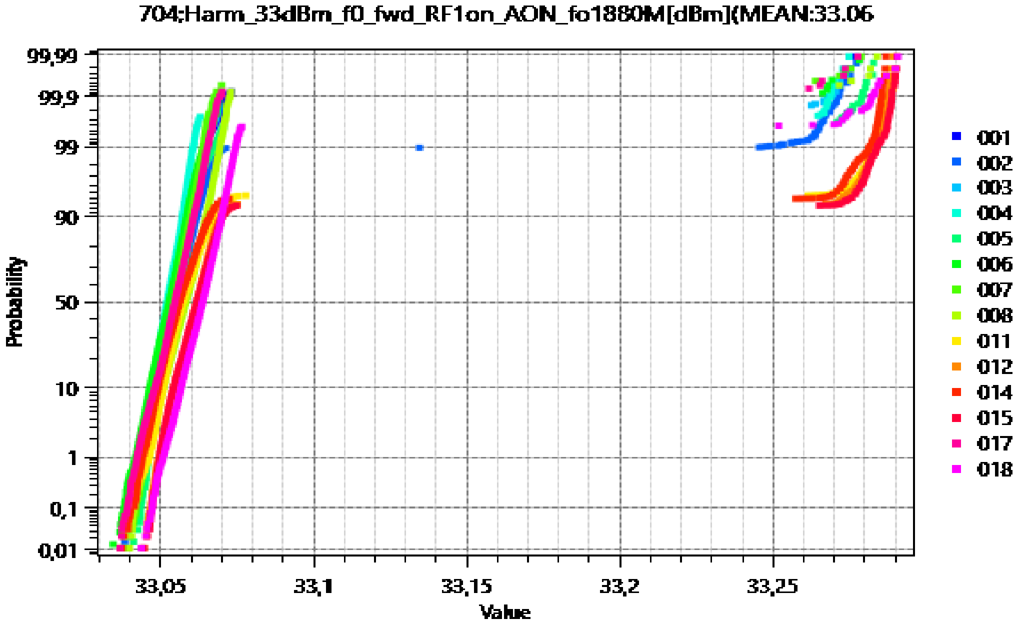


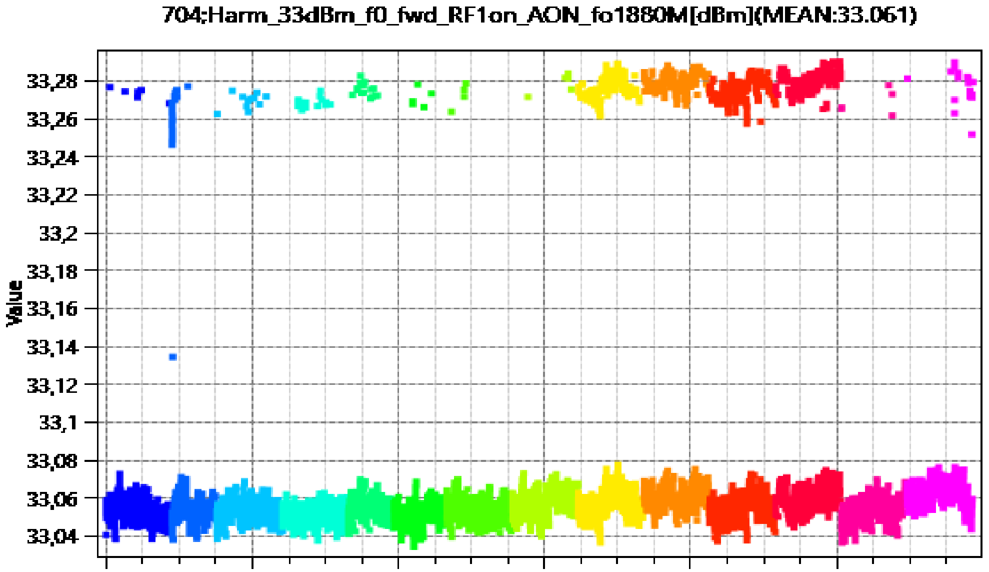


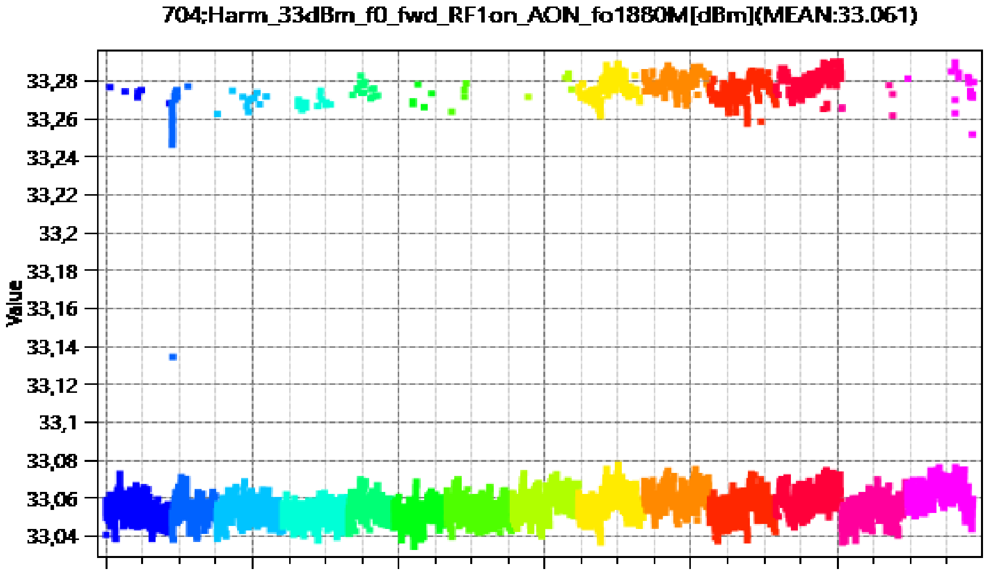


704: Harm_33dBm_f0_fwd_RF1on_AON_fo1880M

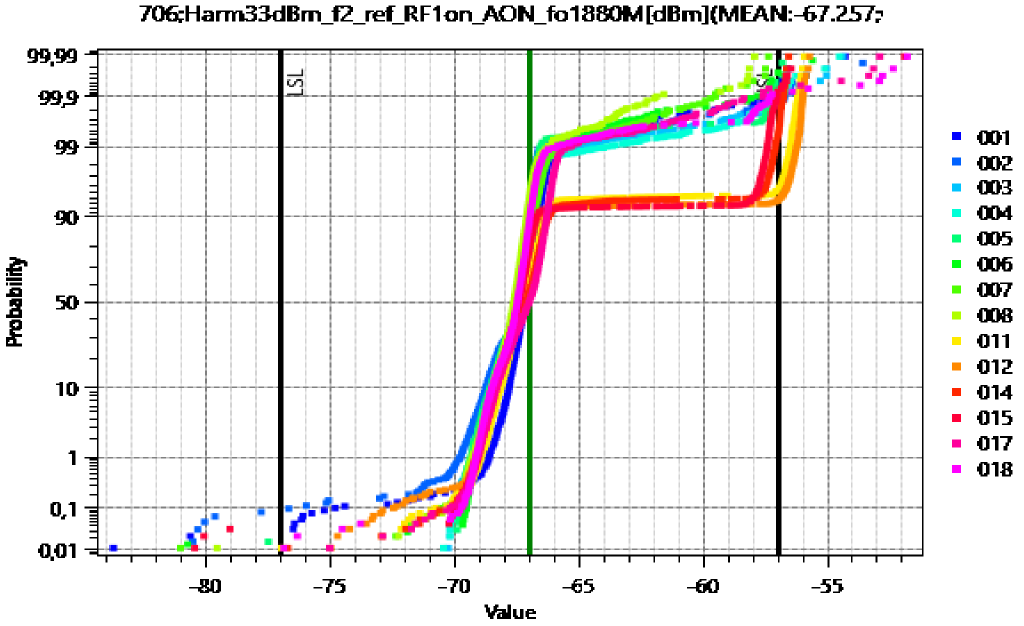


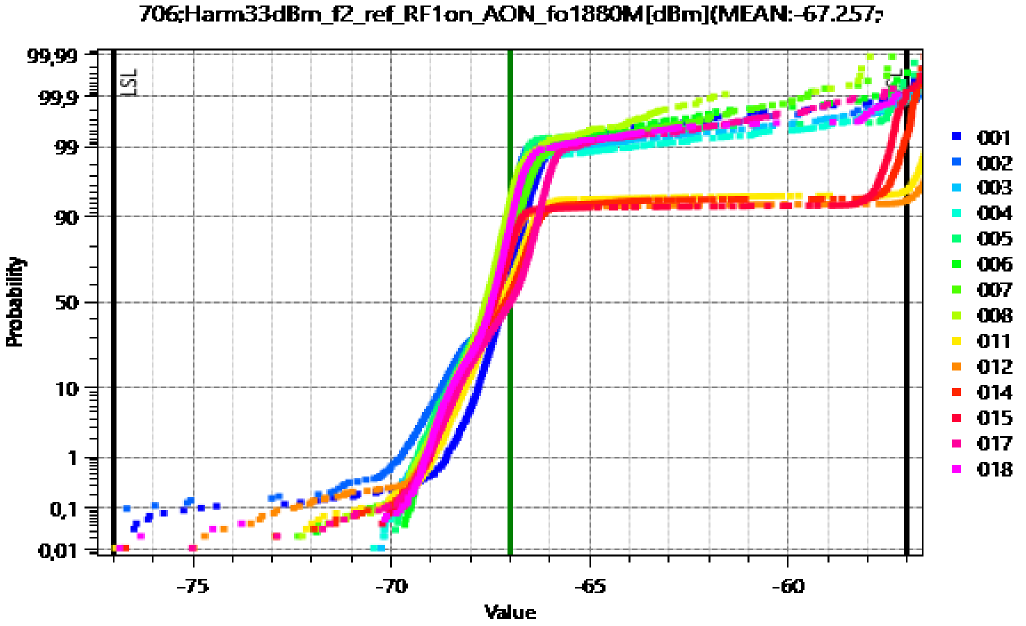


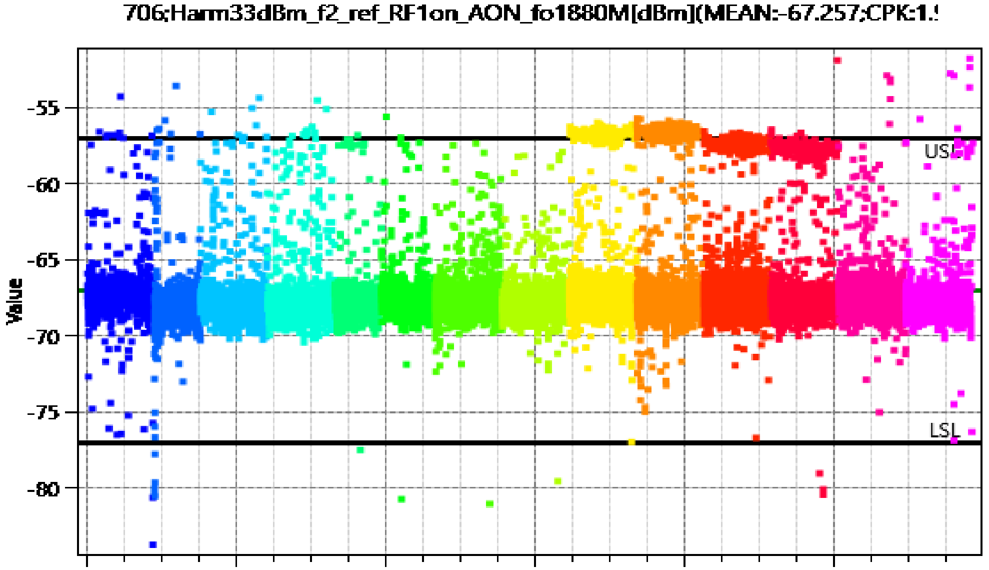


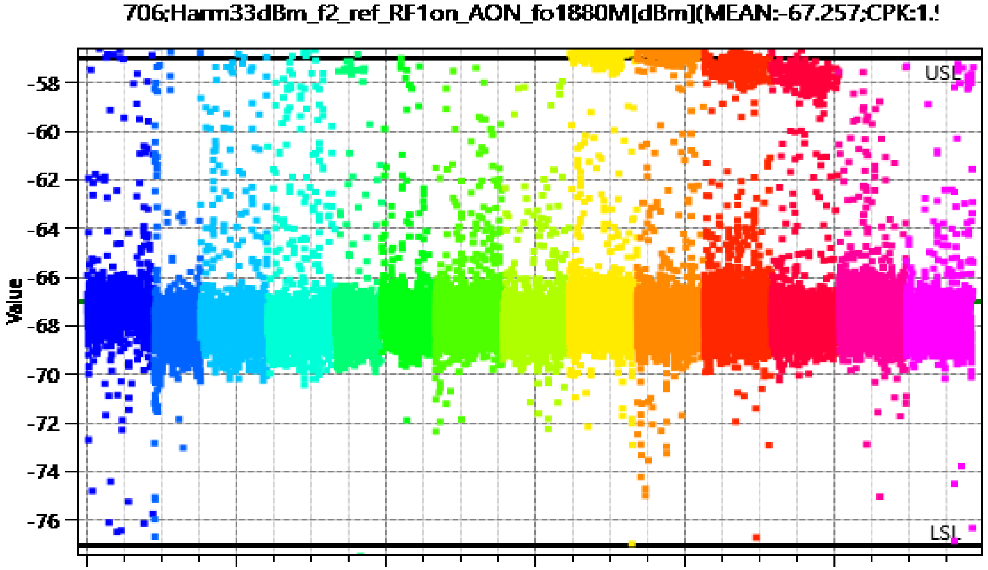


706: Harm33dBm_f2_ref_RF1on_AON_fo1880M

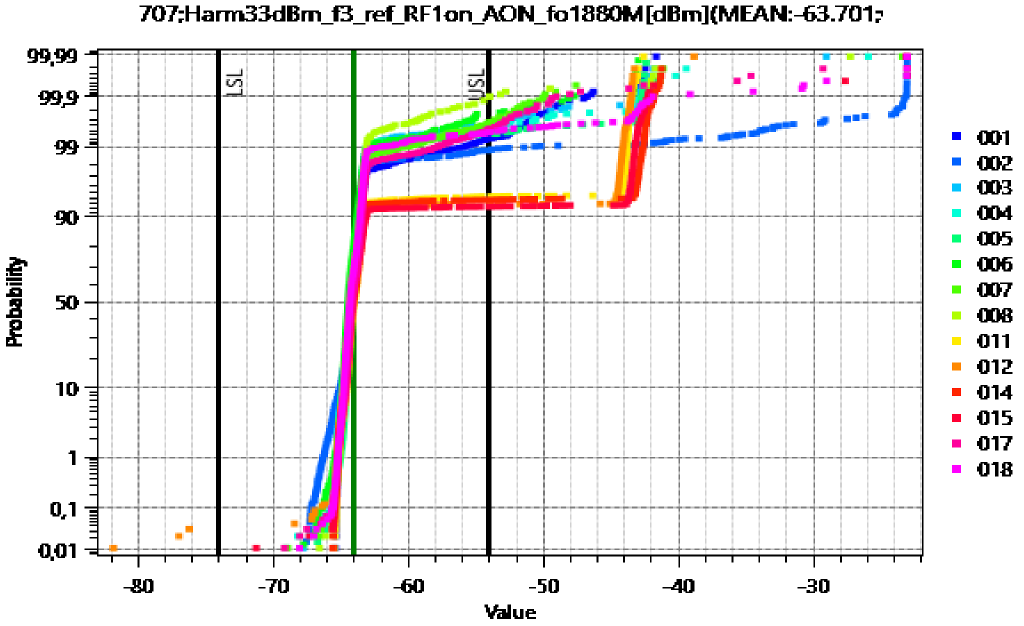


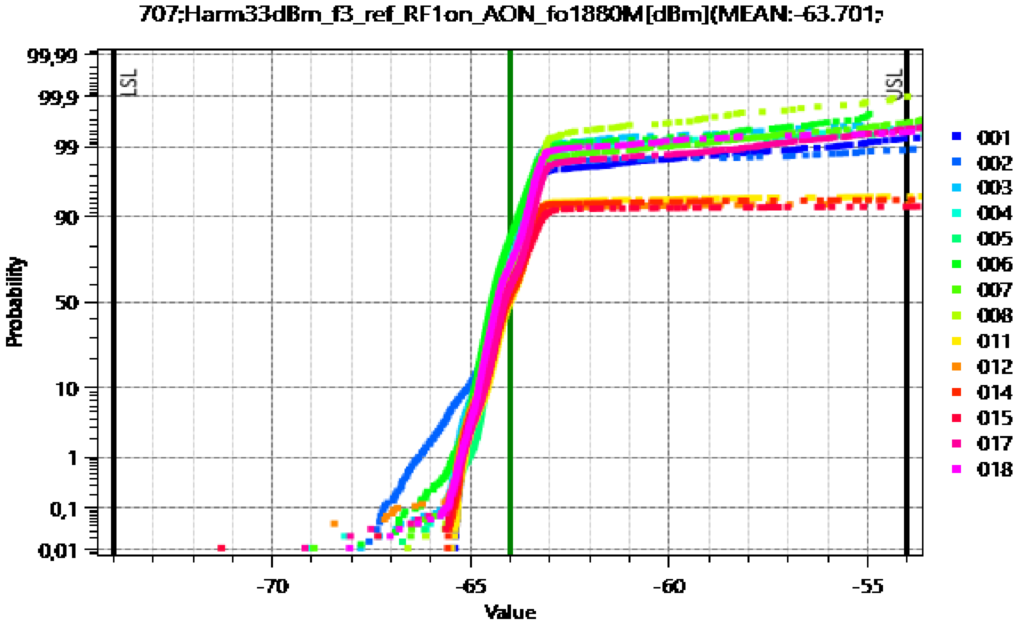


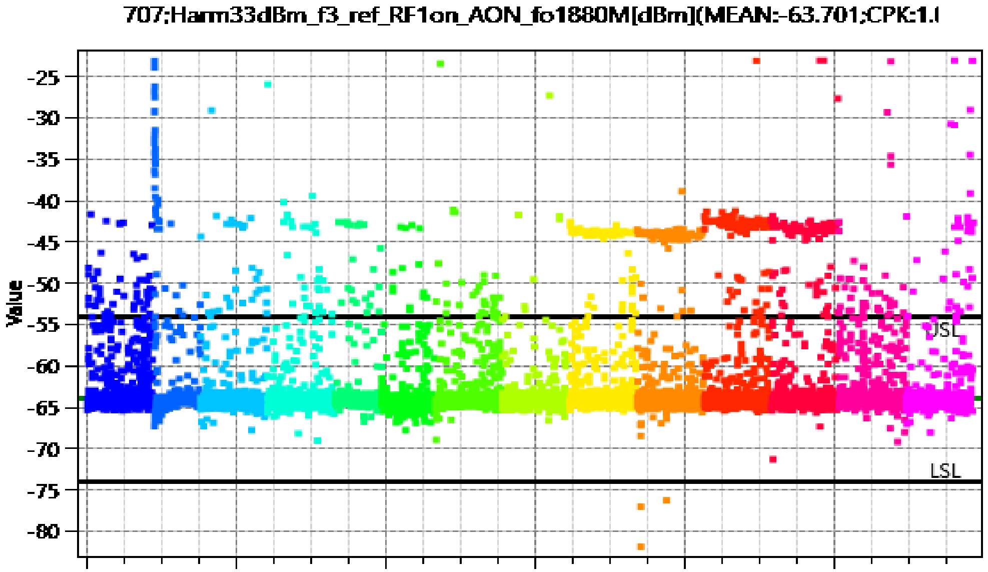


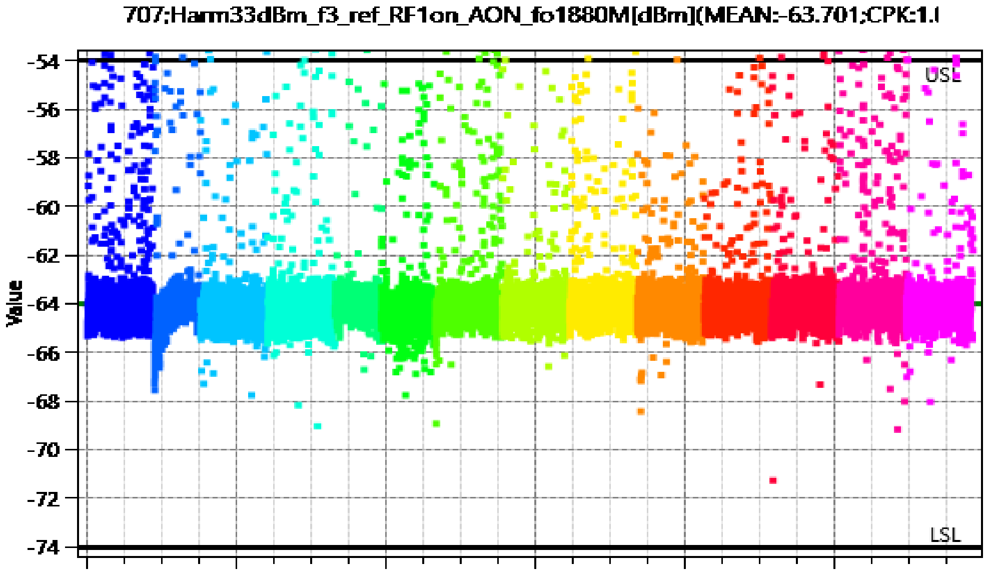


707: Harm33dBm_f3_ref_RF1on_AON_fo1880M

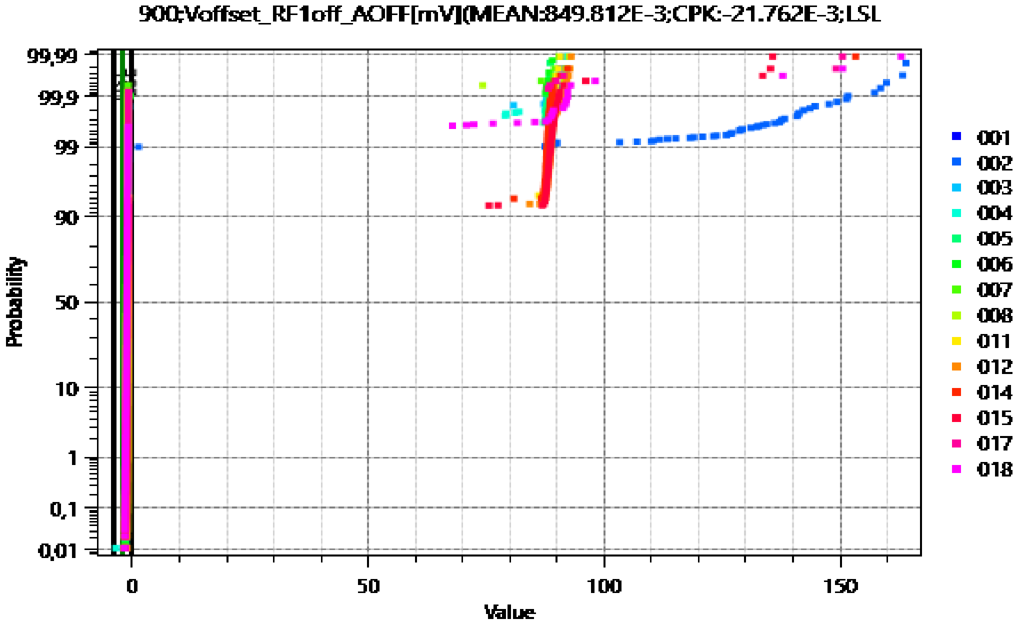


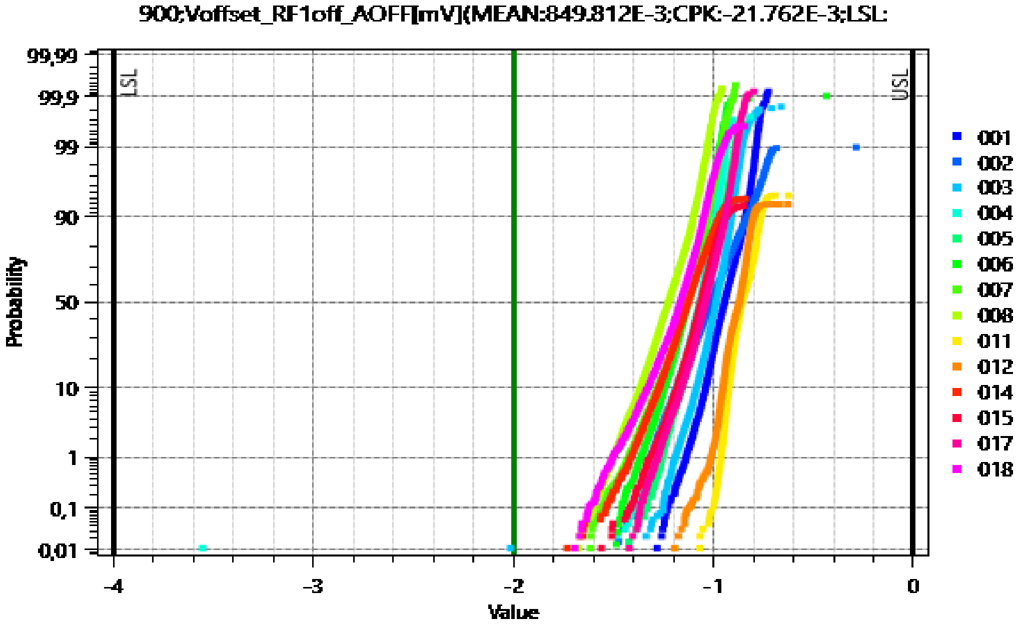


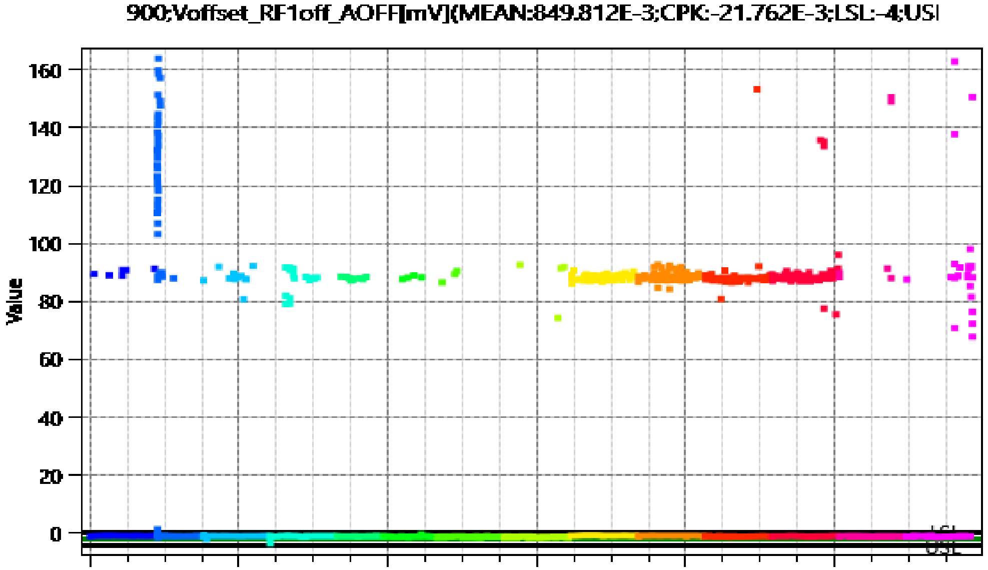


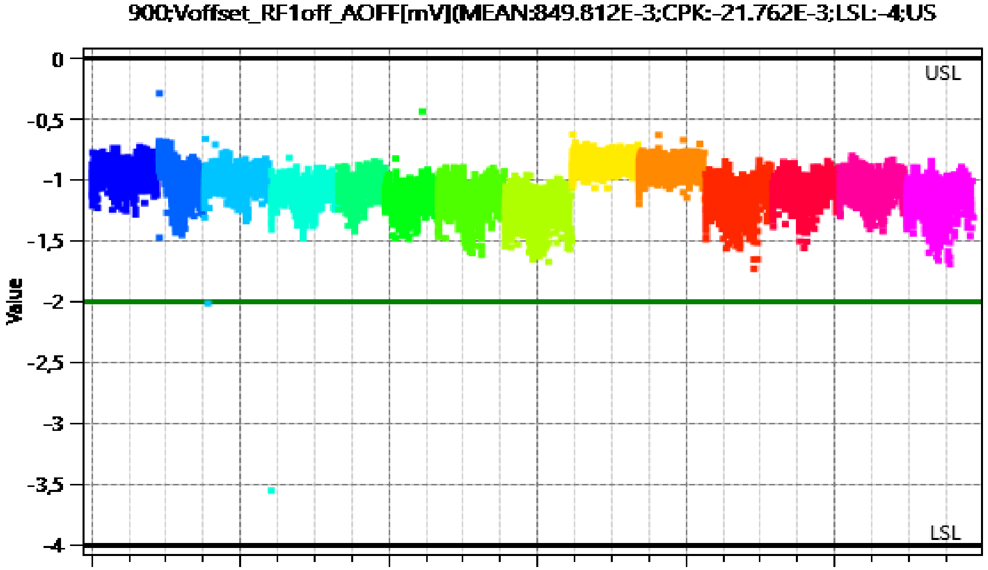


900: Voffset_RF1off_AOFF

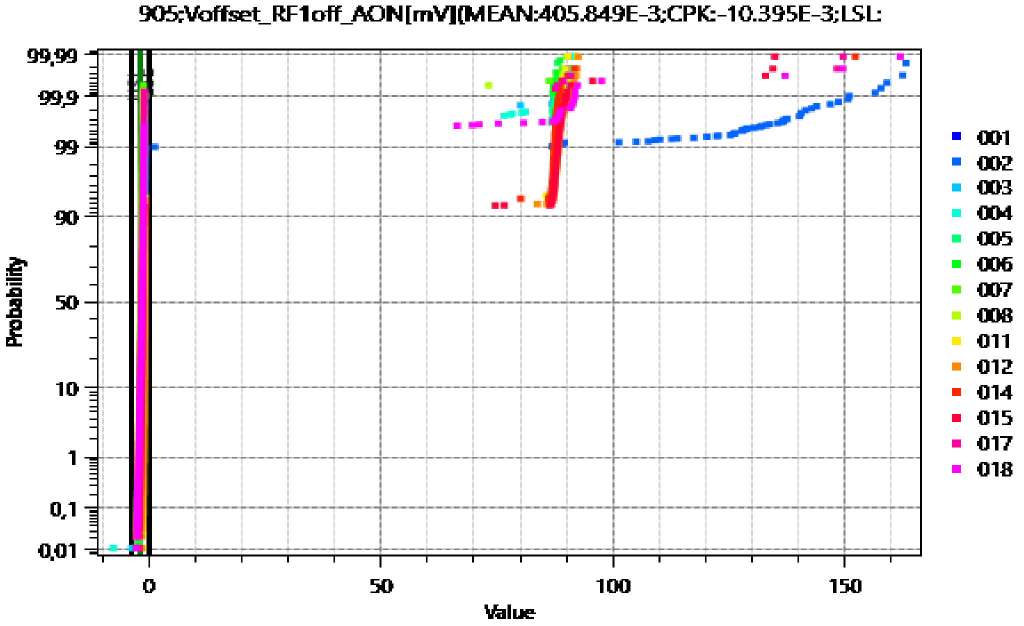


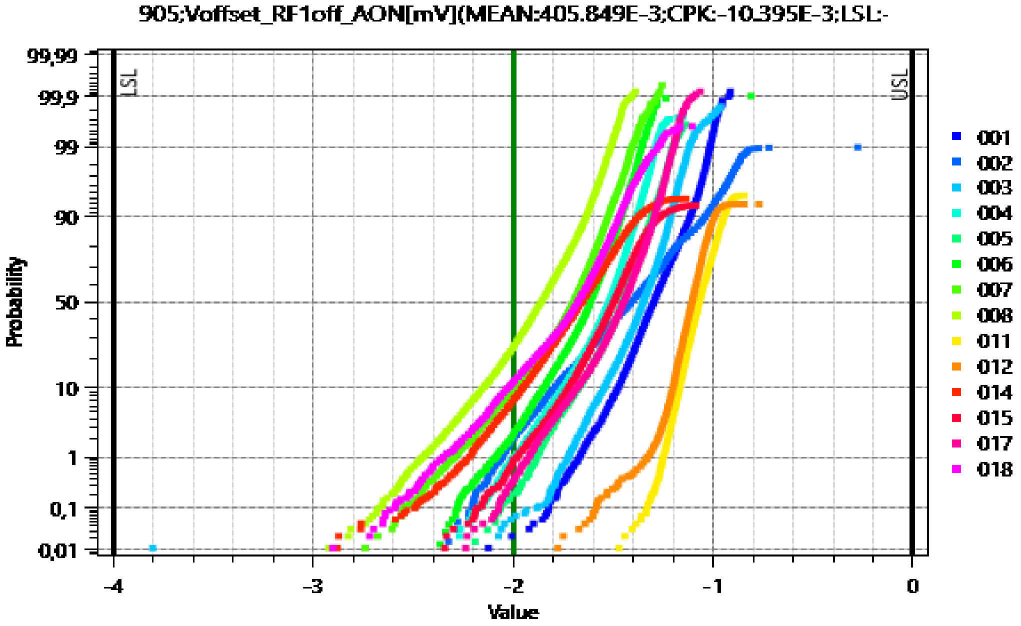


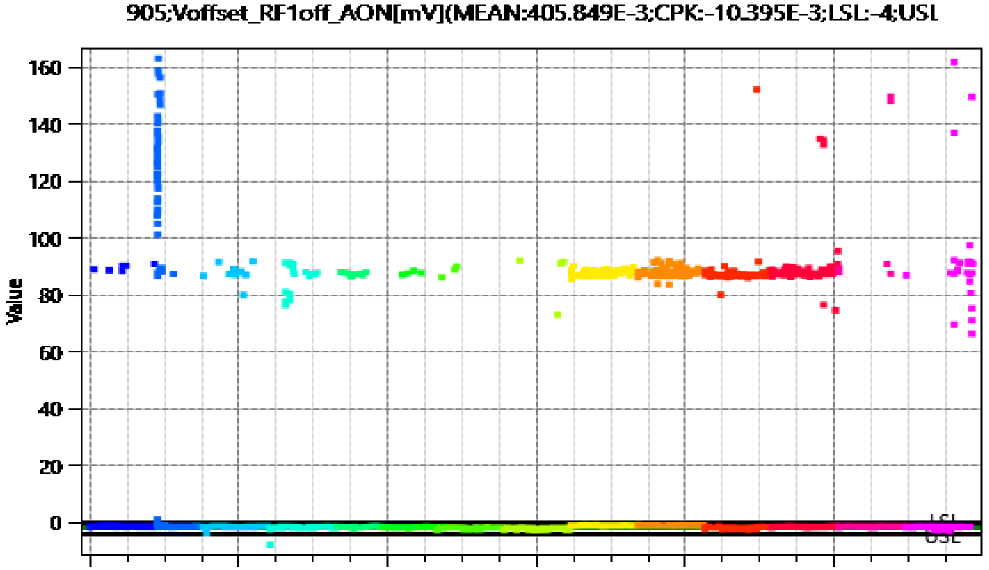


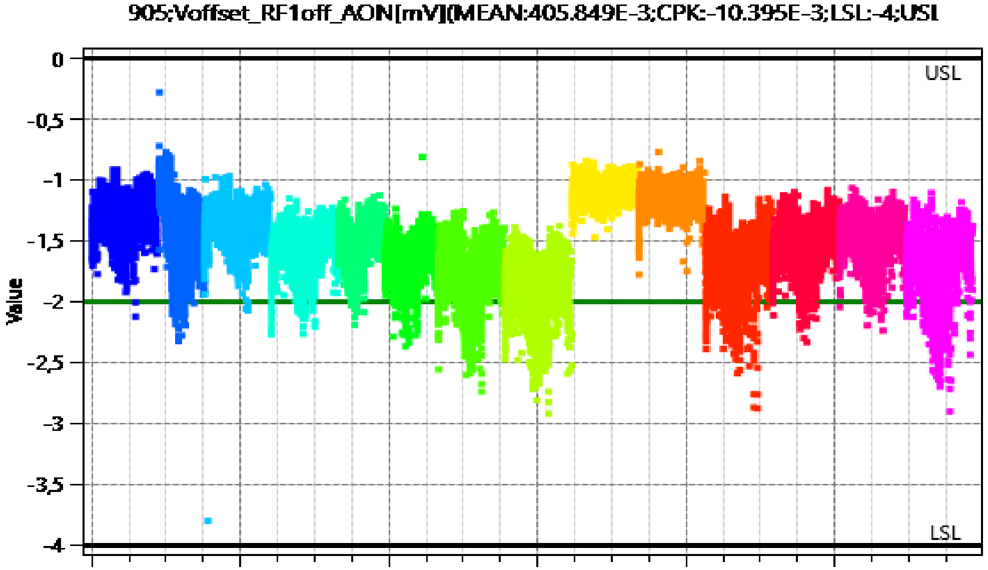


905: Voffset_RF1off_AON

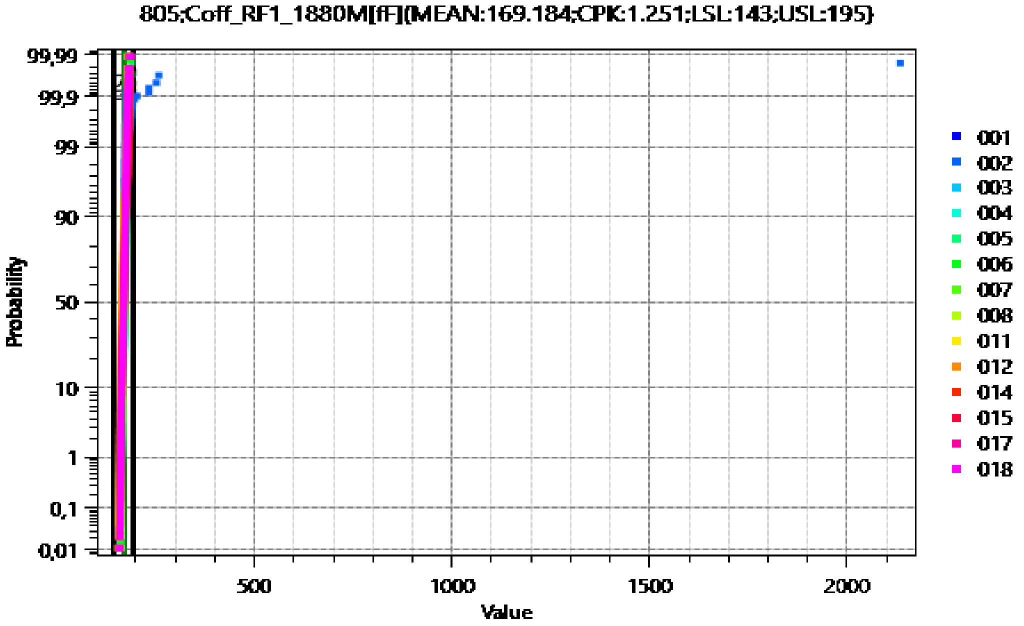


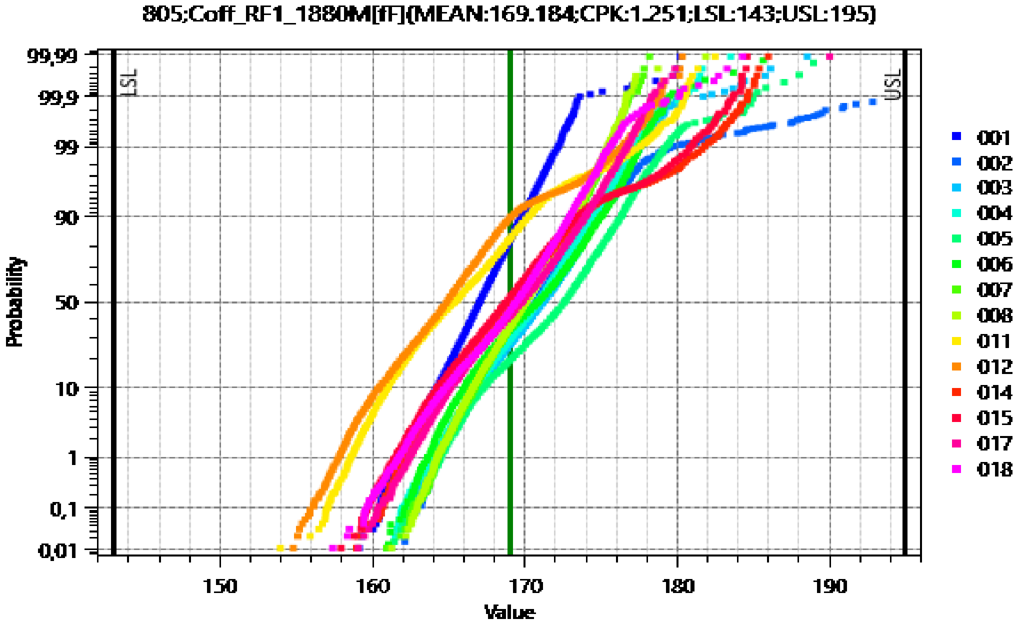


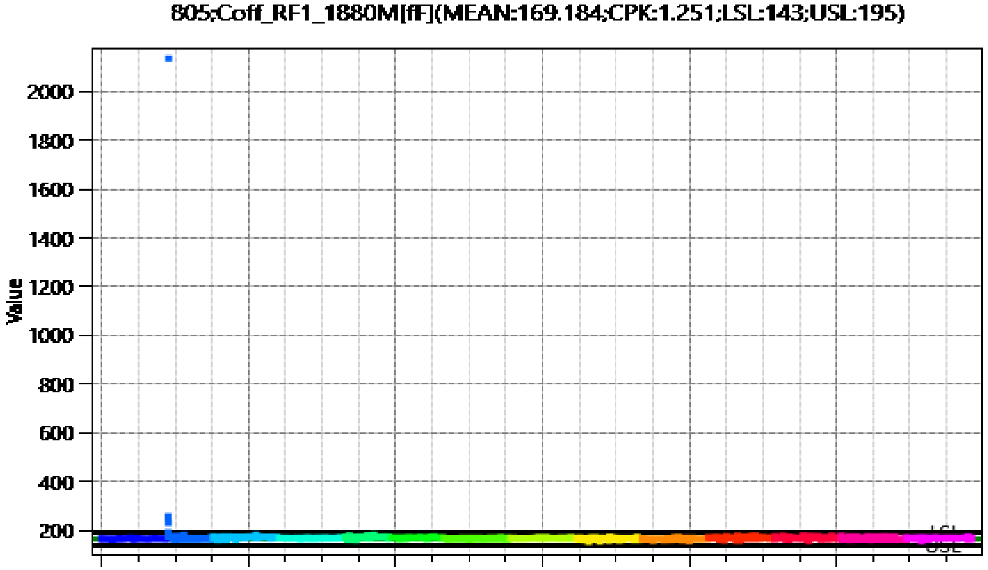


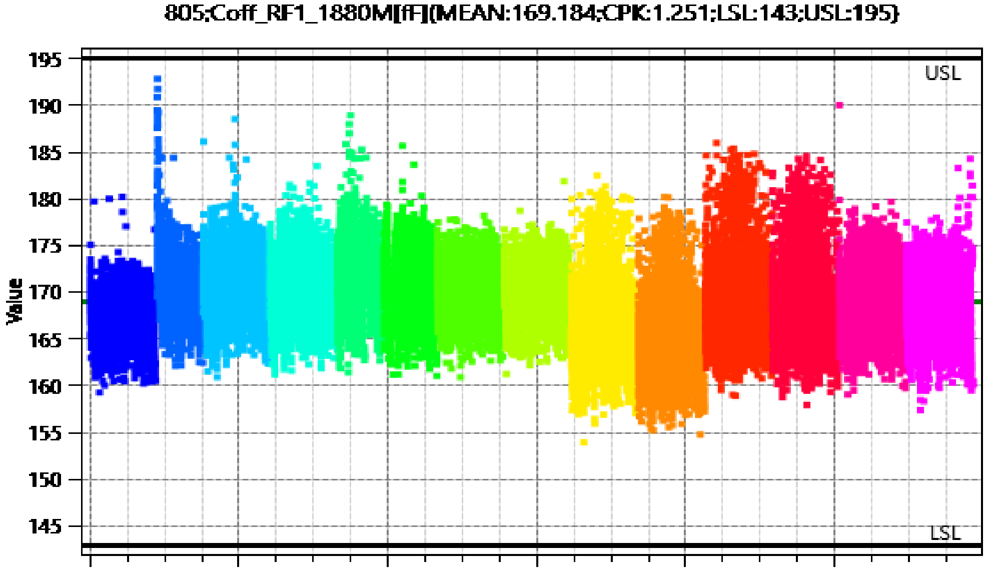


805: Coff_RF1_1880M

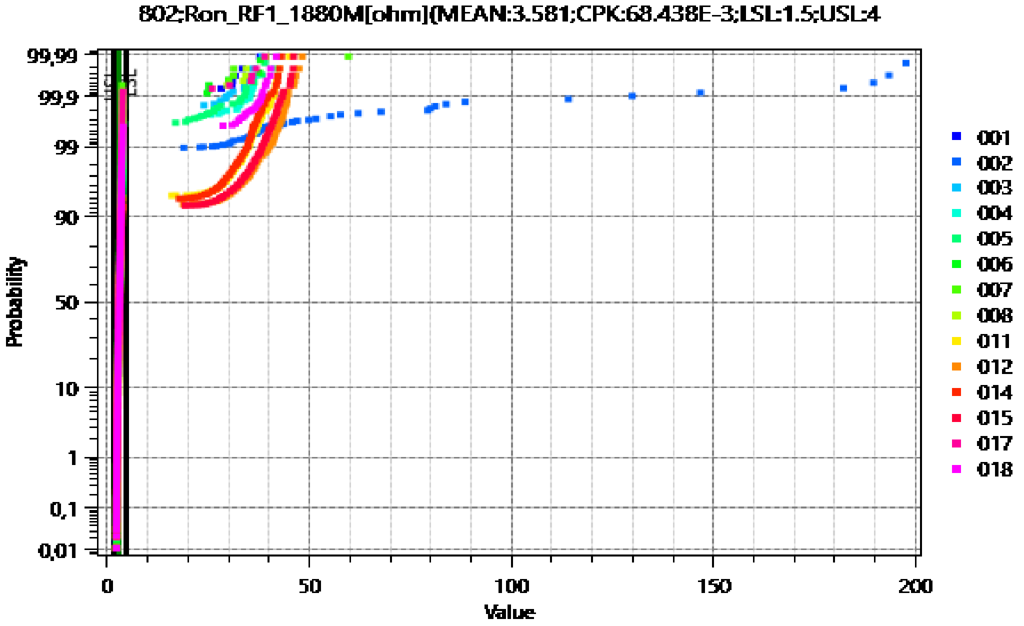


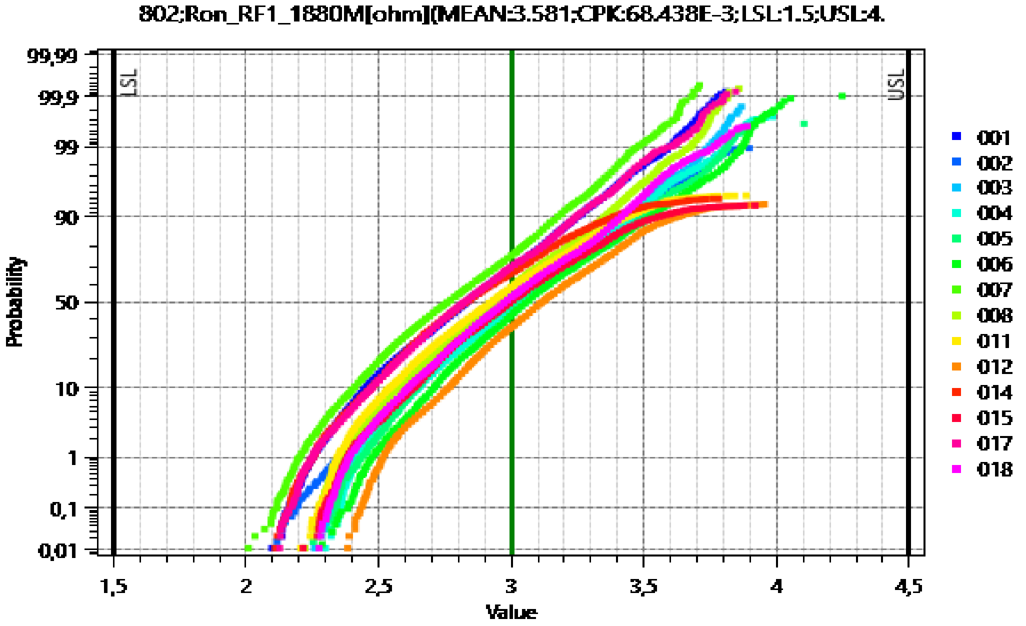


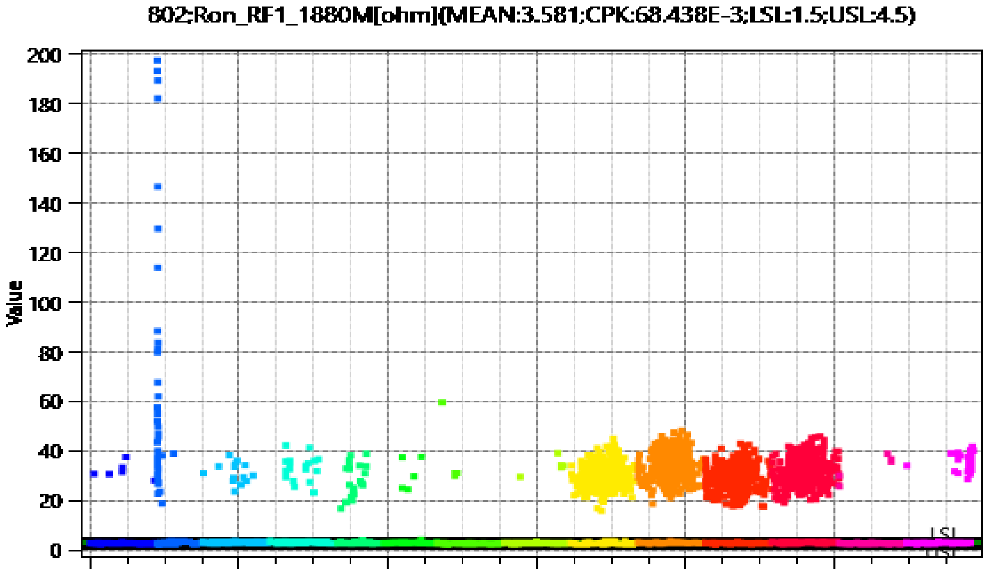


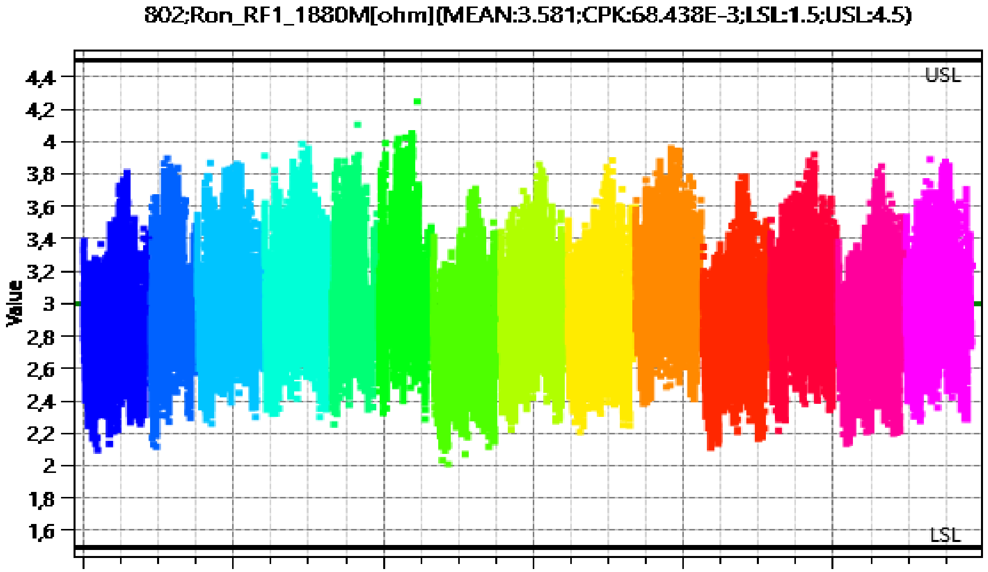


802: Ron_RF1_1880M

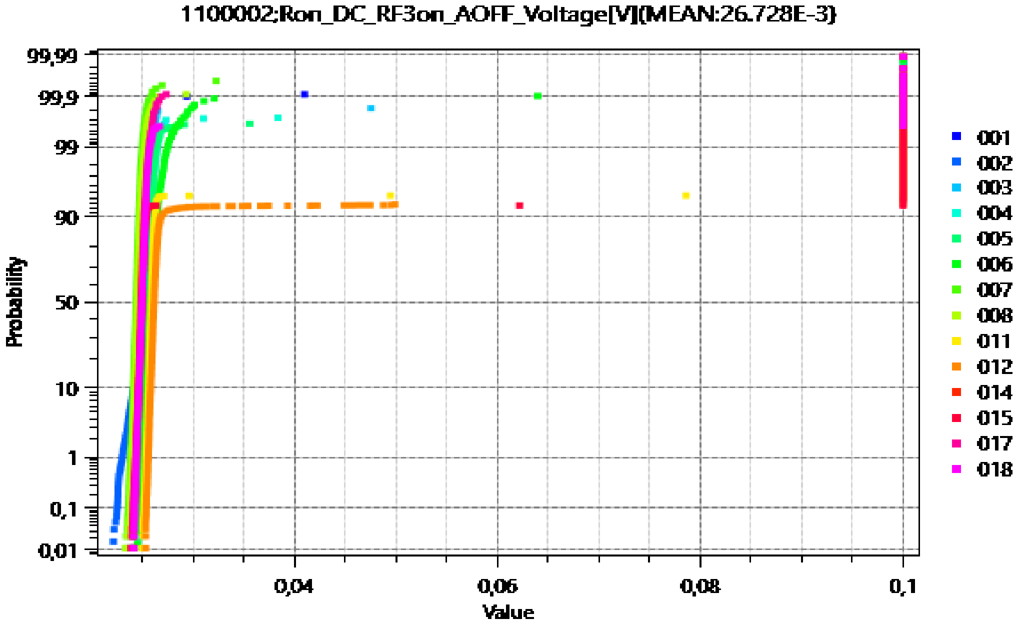


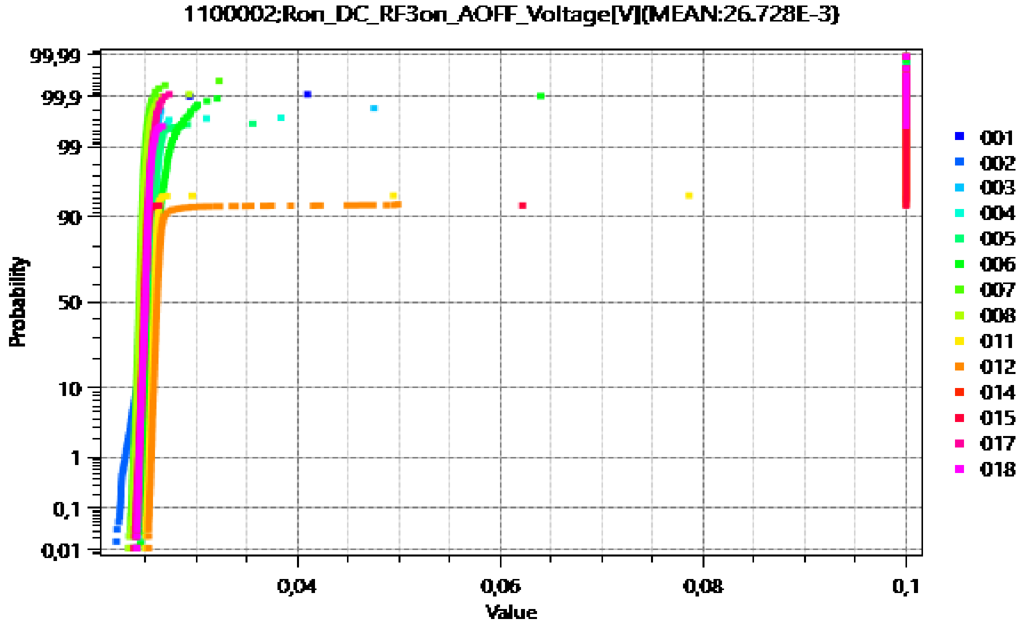


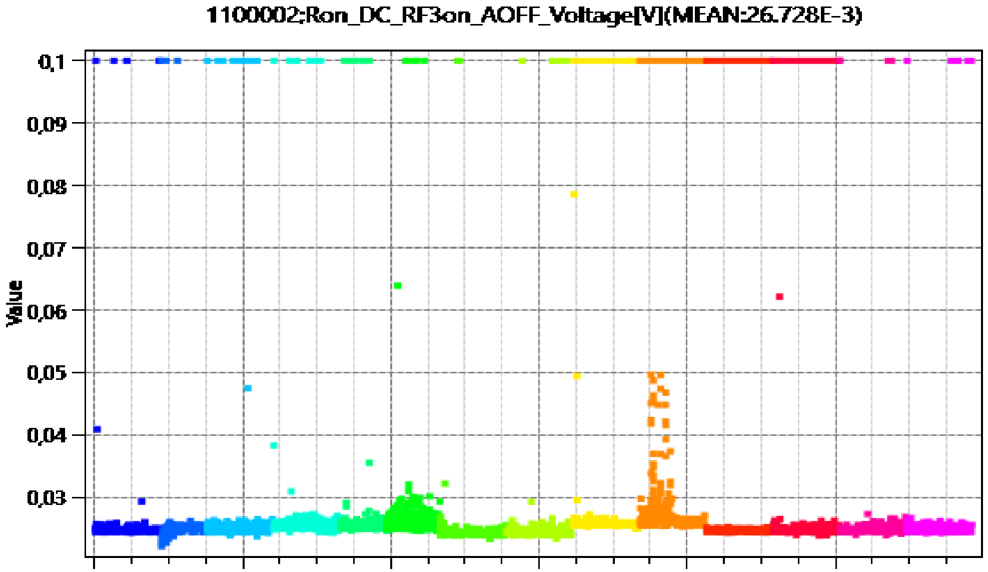


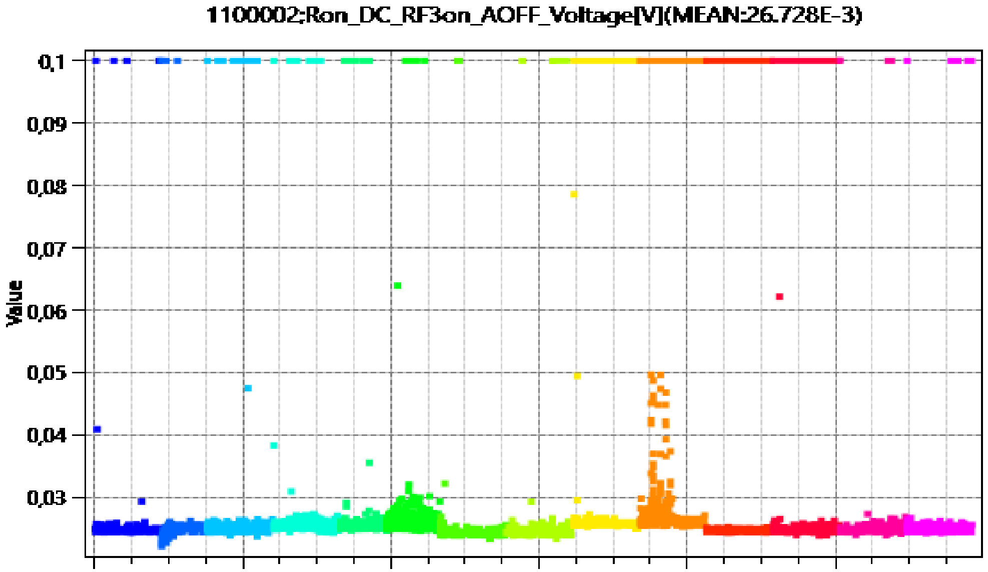


1100002: Ron_DC_RF3on_AOFF_Voltage

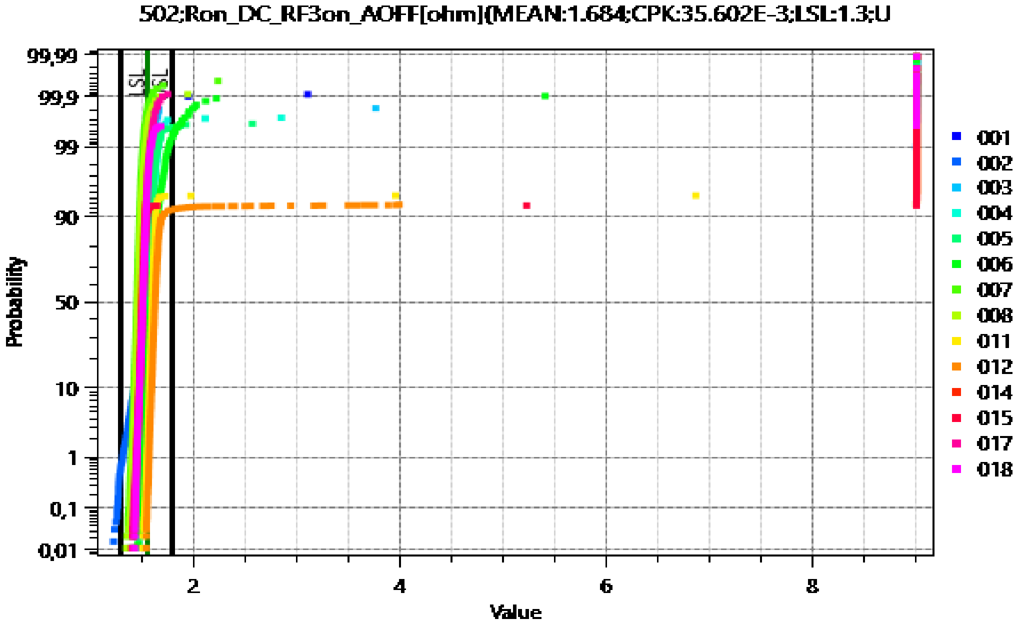


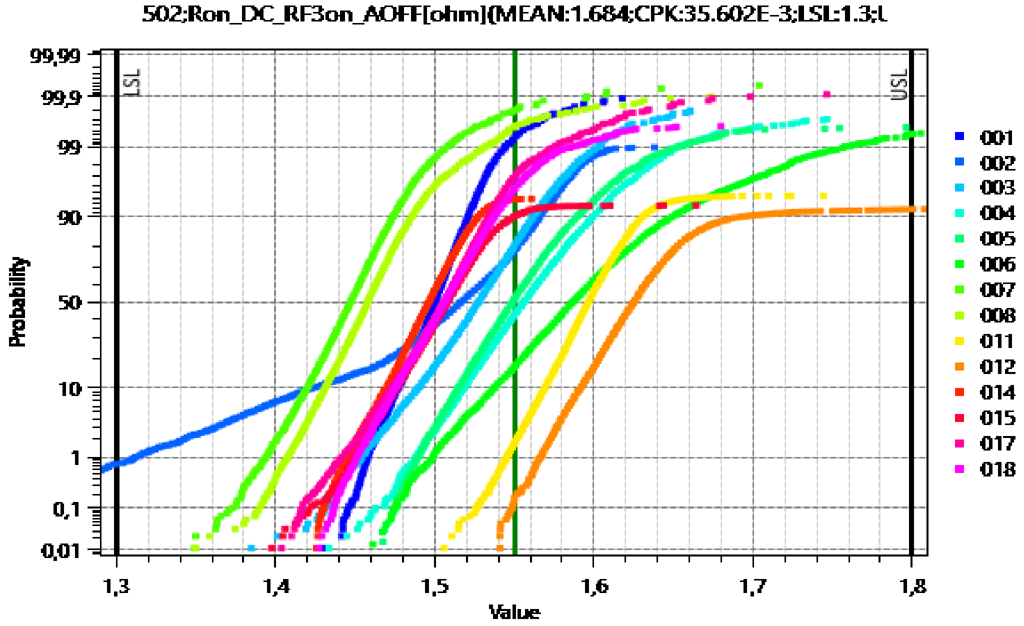


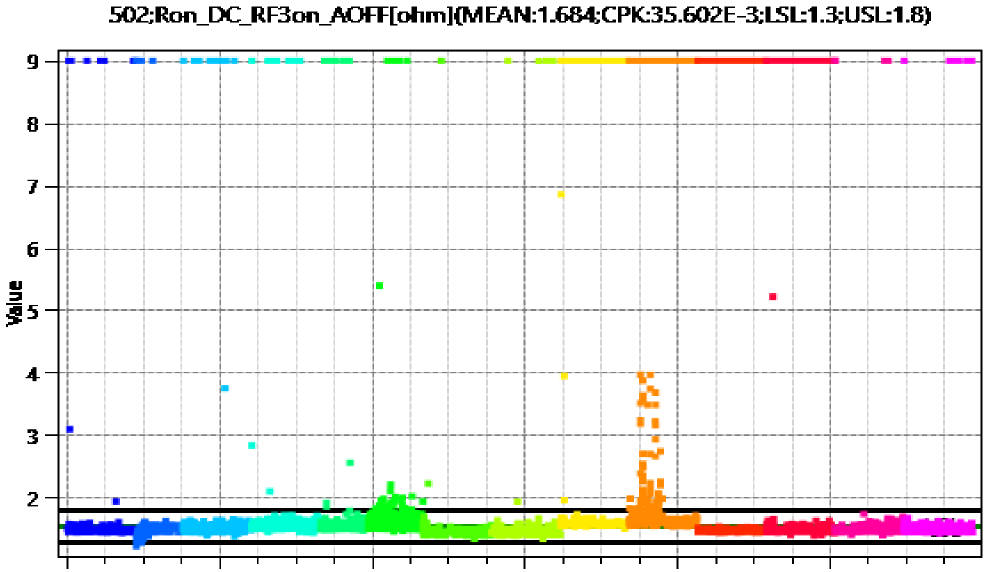


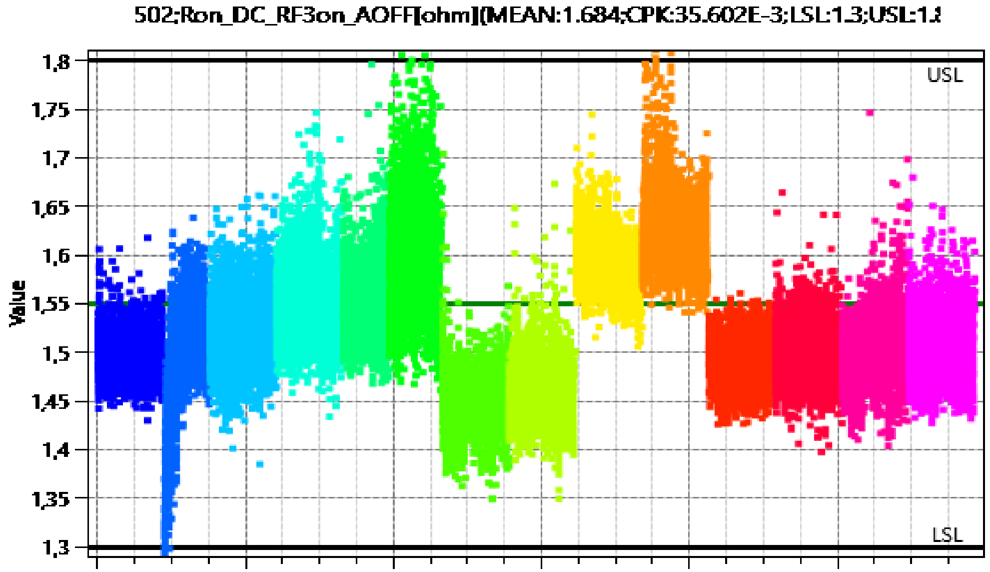


502: Ron_DC_RF3on_AOFF

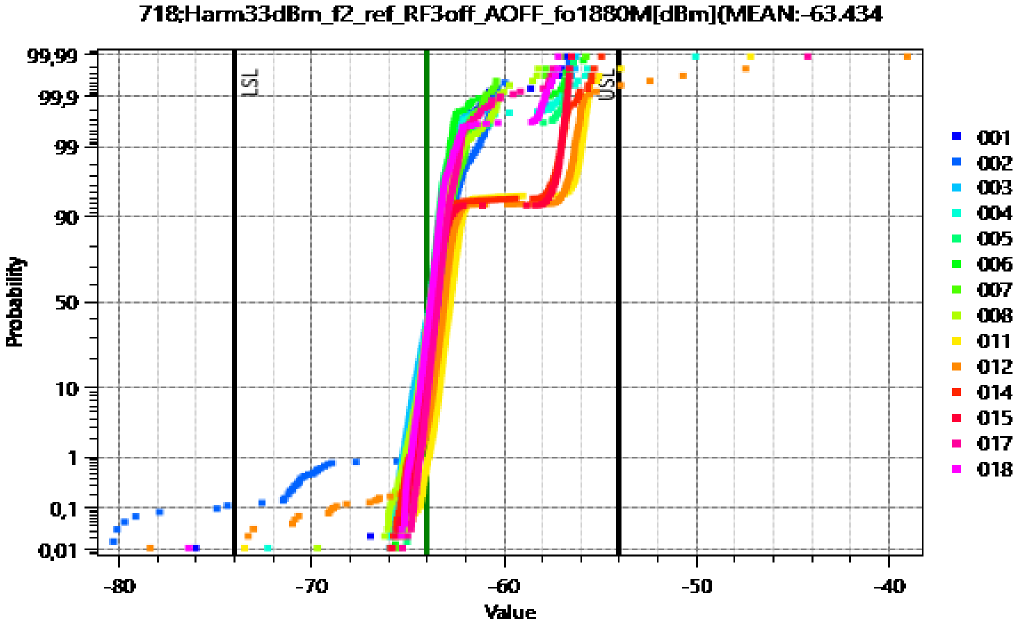


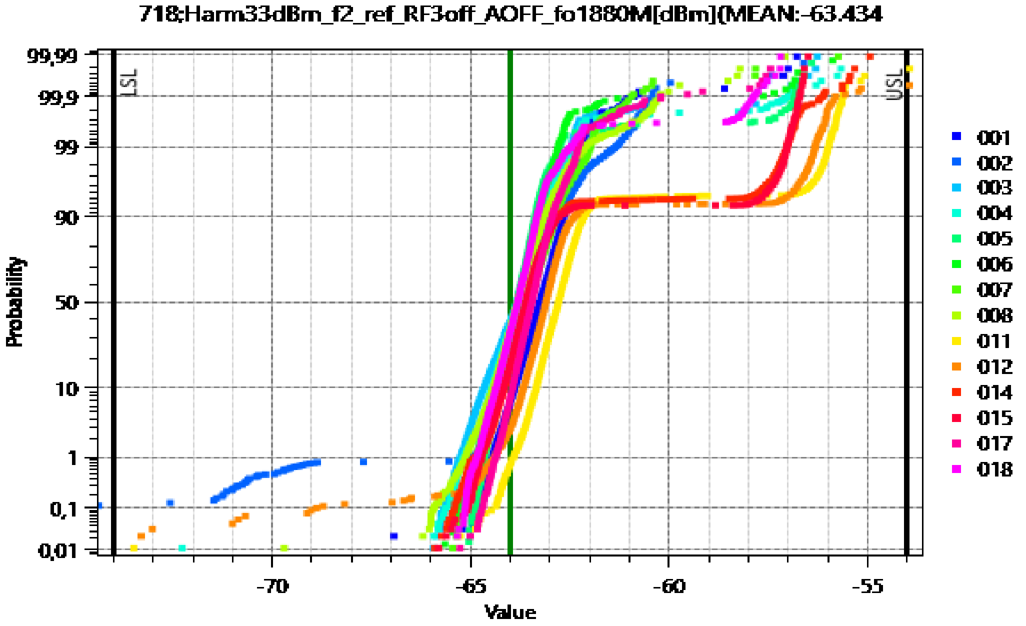


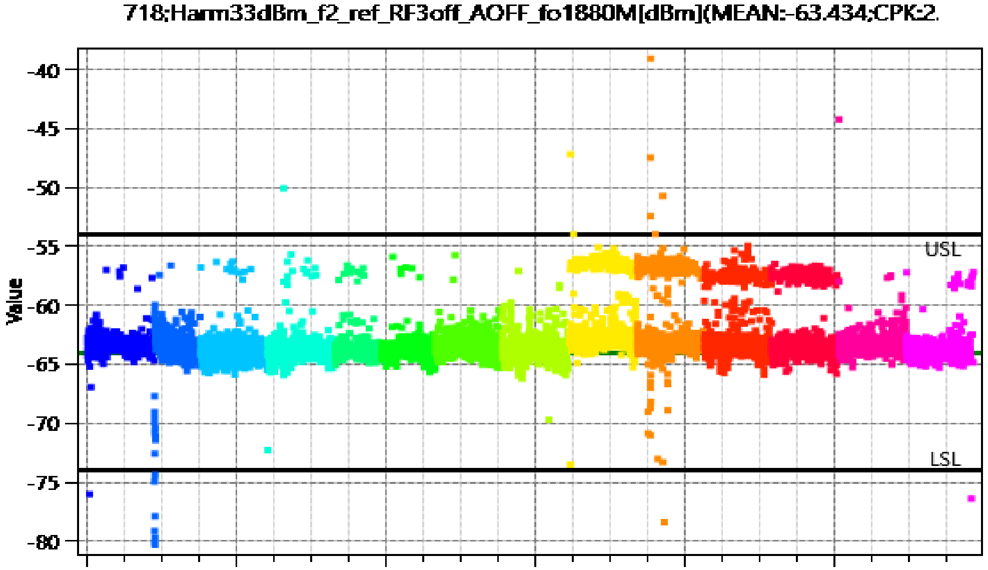


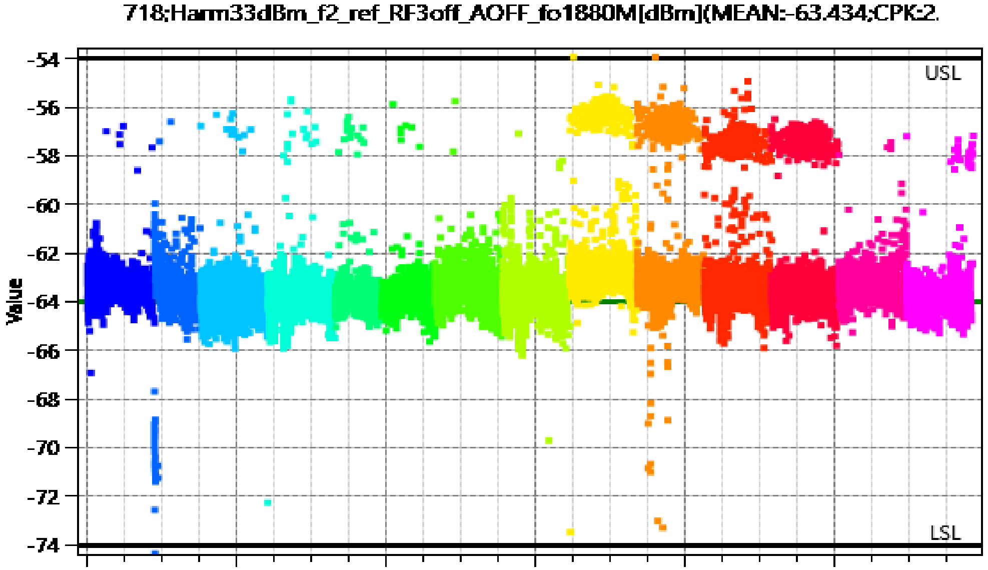


718: Harm33dBm_f2_ref_RF3off_AOFF_fo1880M

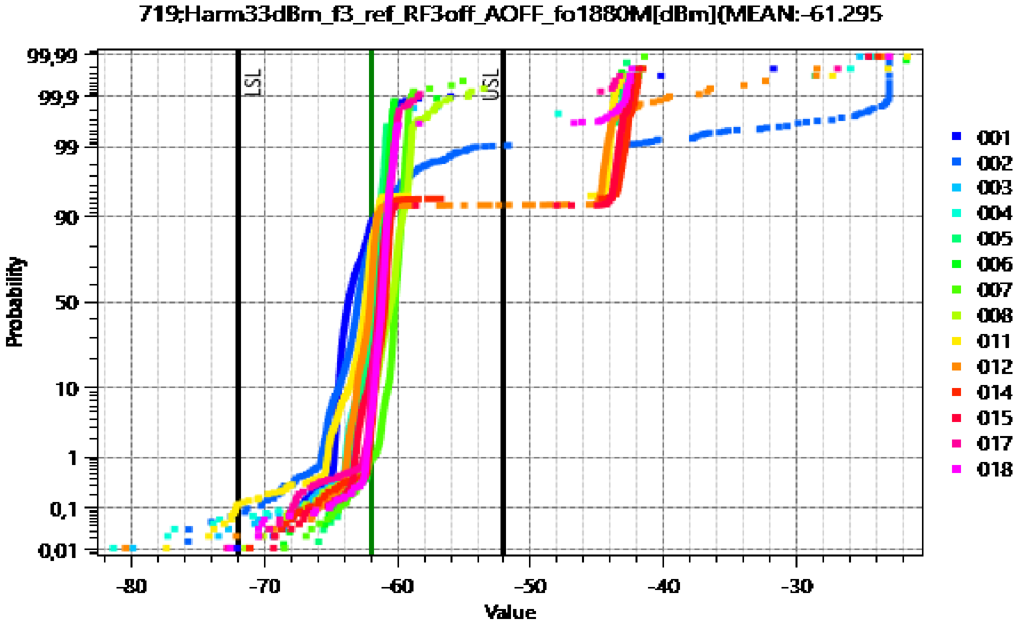


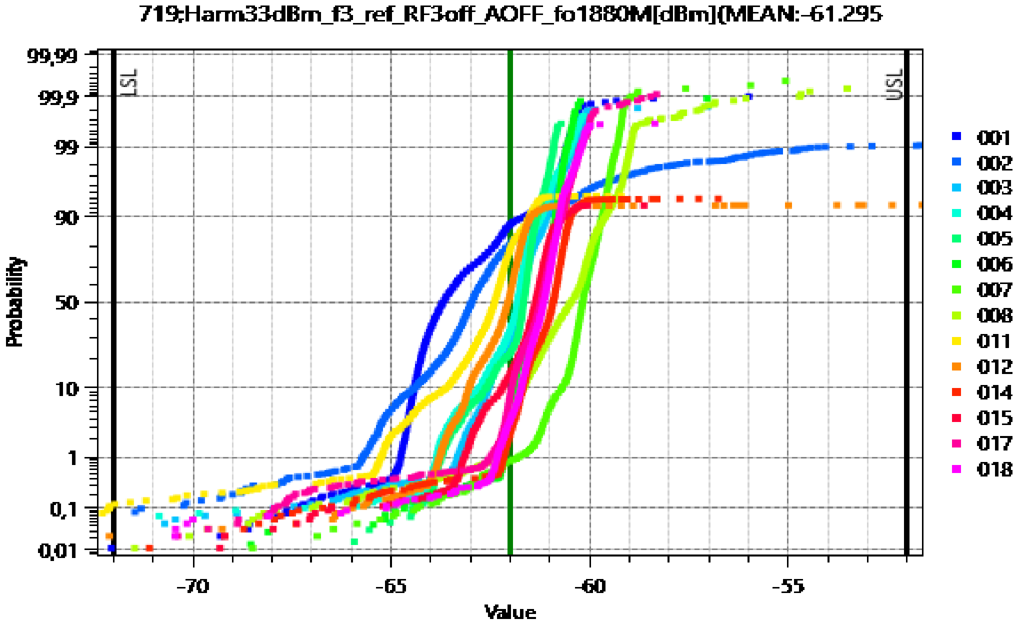


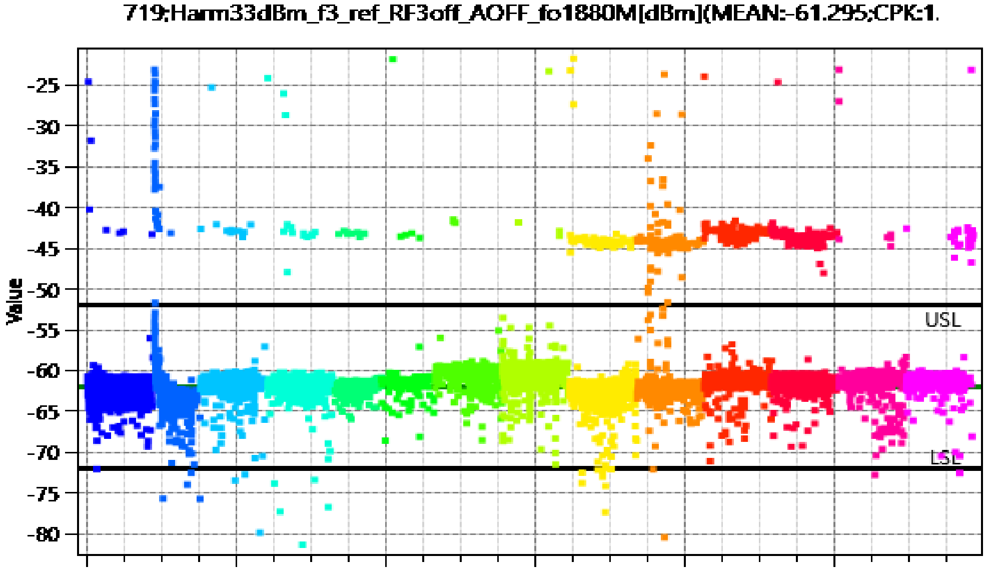


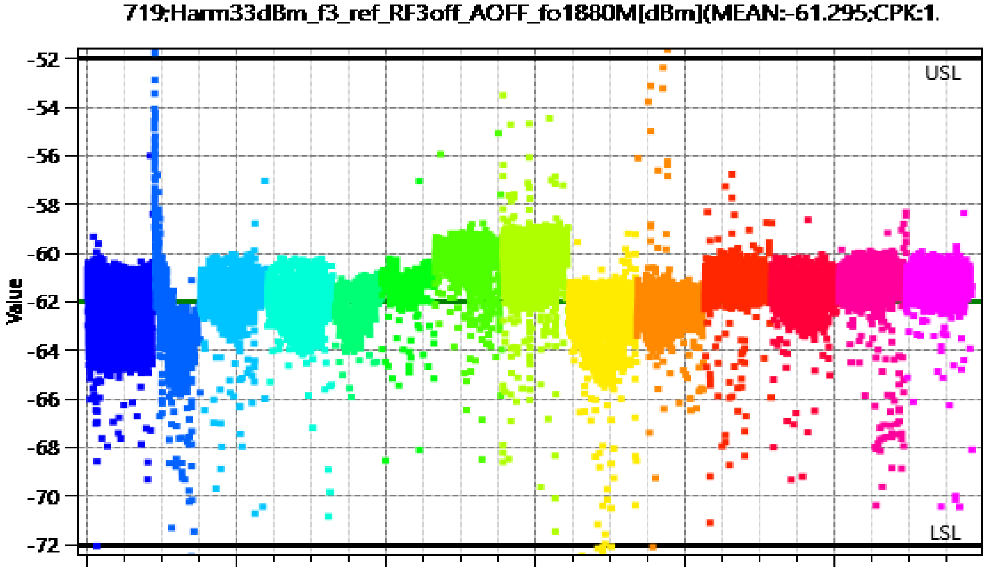


719: Harm33dBm_f3_ref_RF3off_AOFF_fo1880M

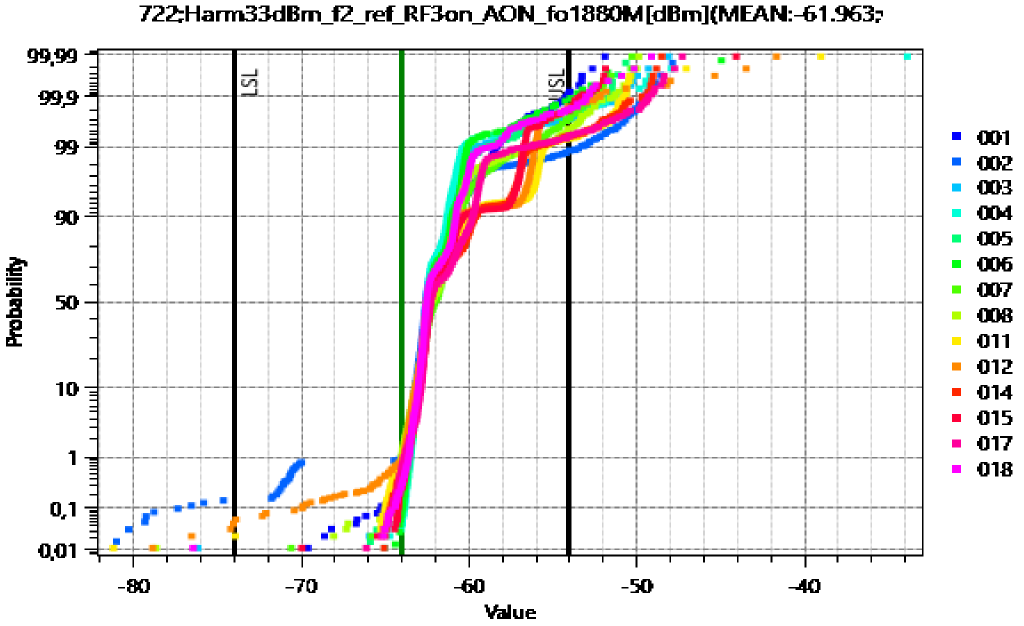


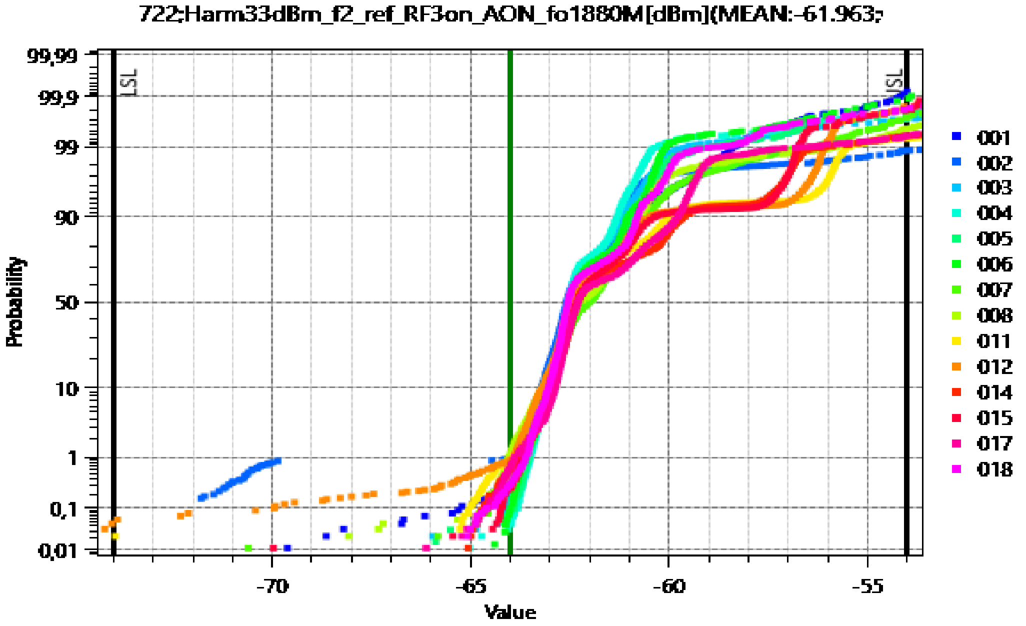


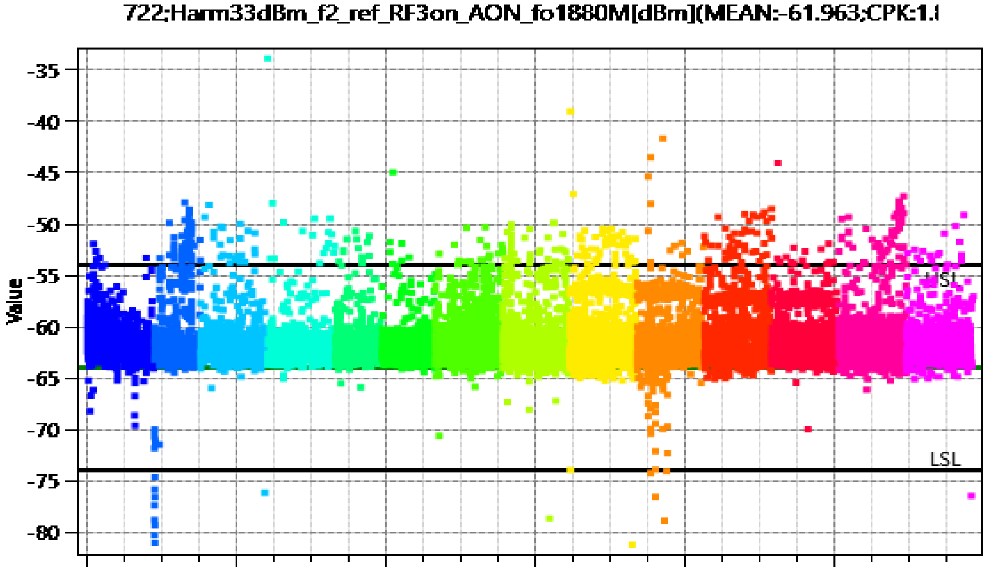


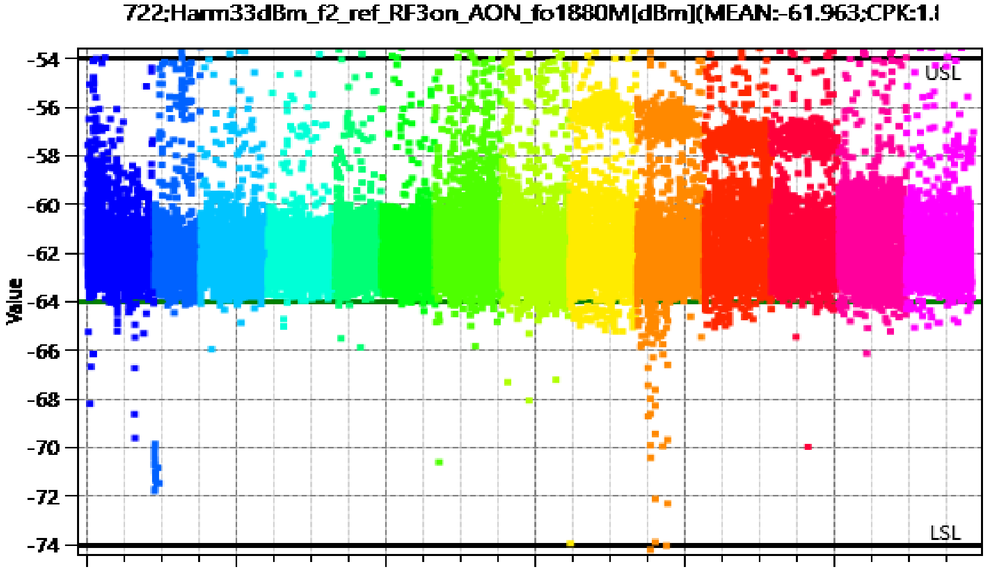


722: Harm33dBm_f2_ref_RF3on_AON_fo1880M

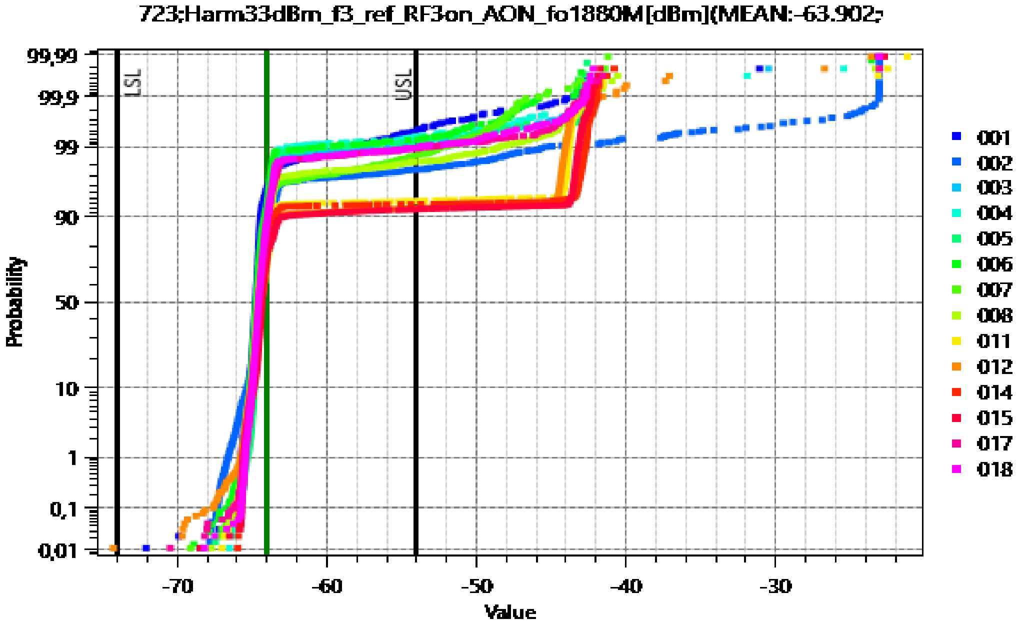


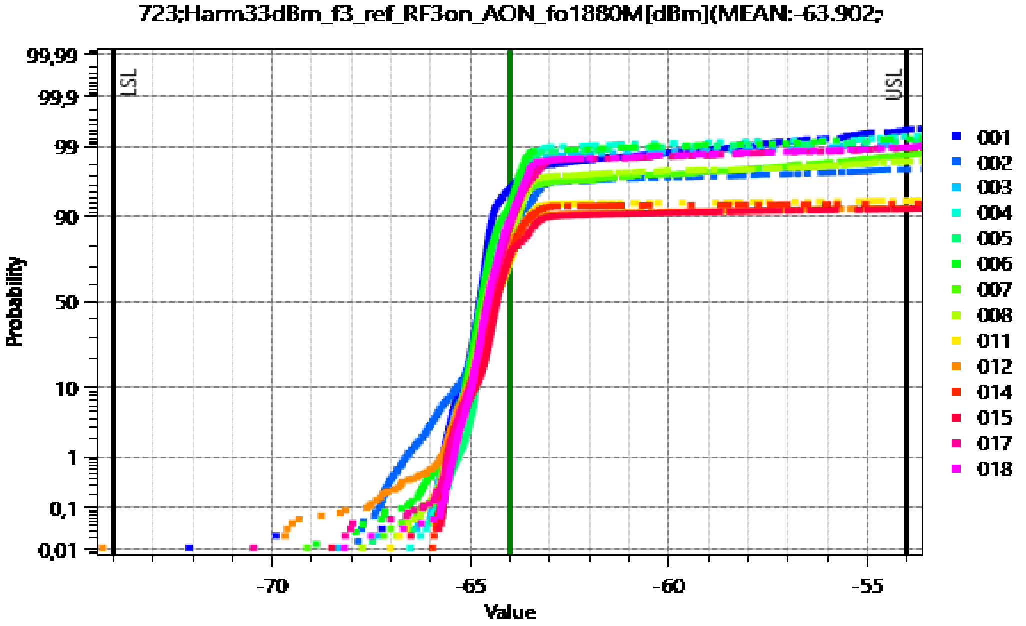


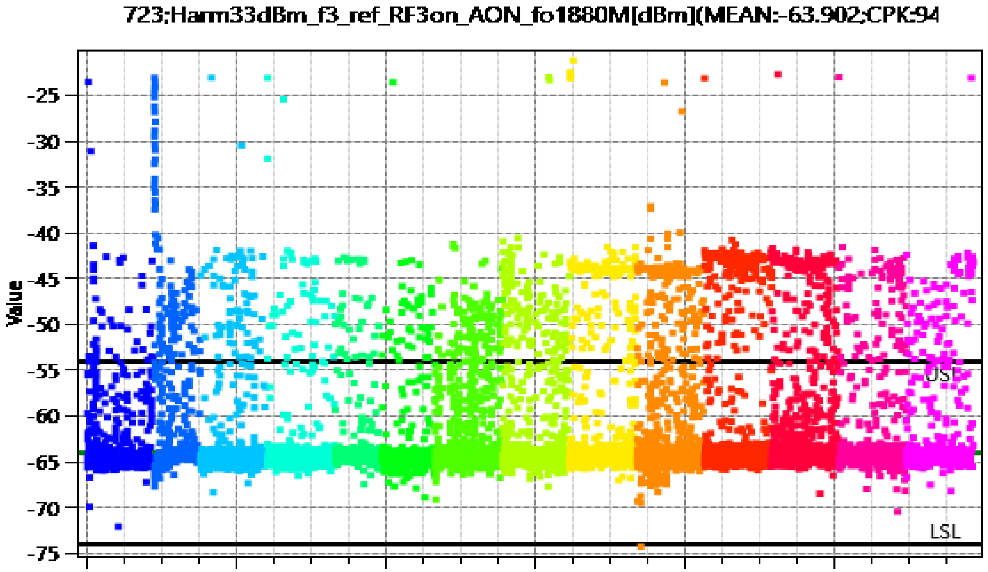


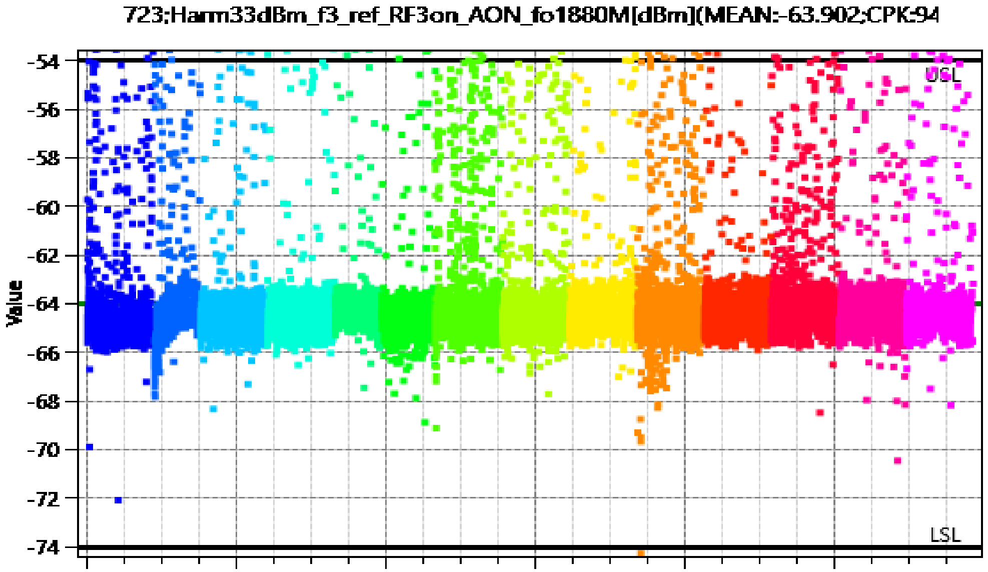


723: Harm33dBm_f3_ref_RF3on_AON_fo1880M

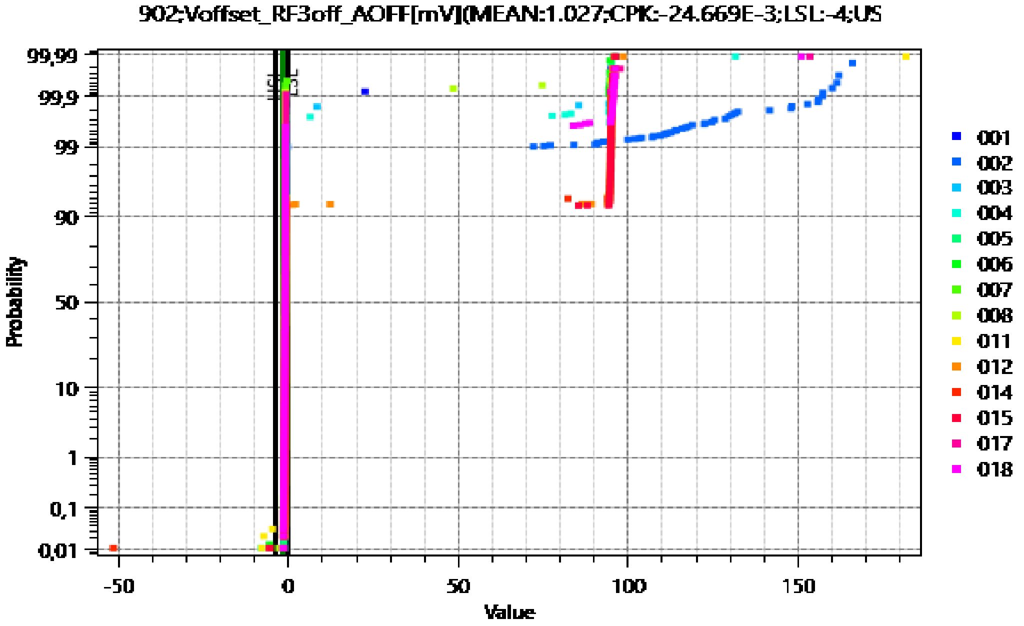


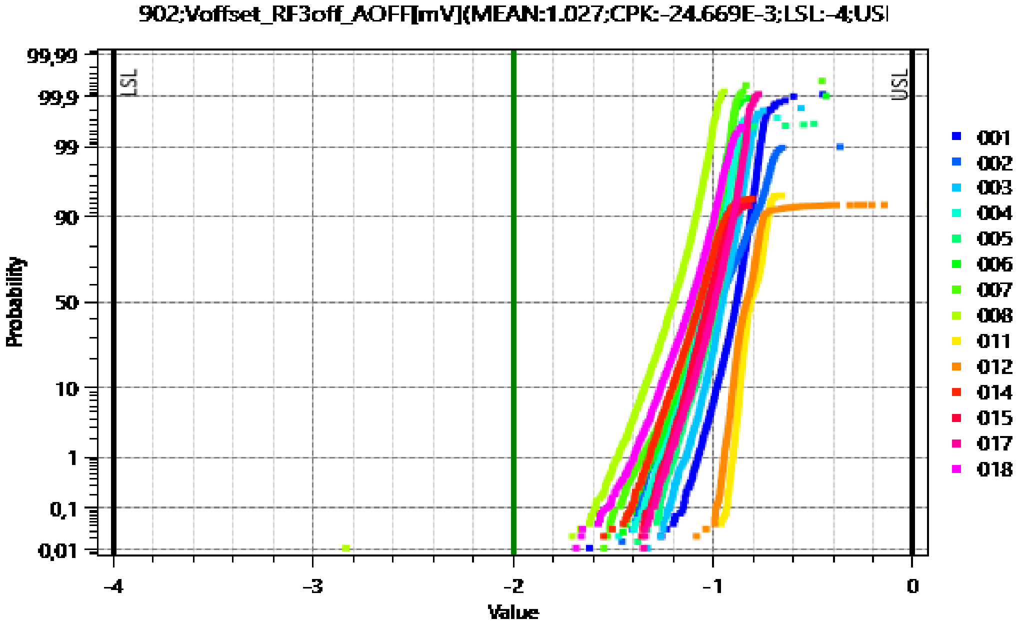


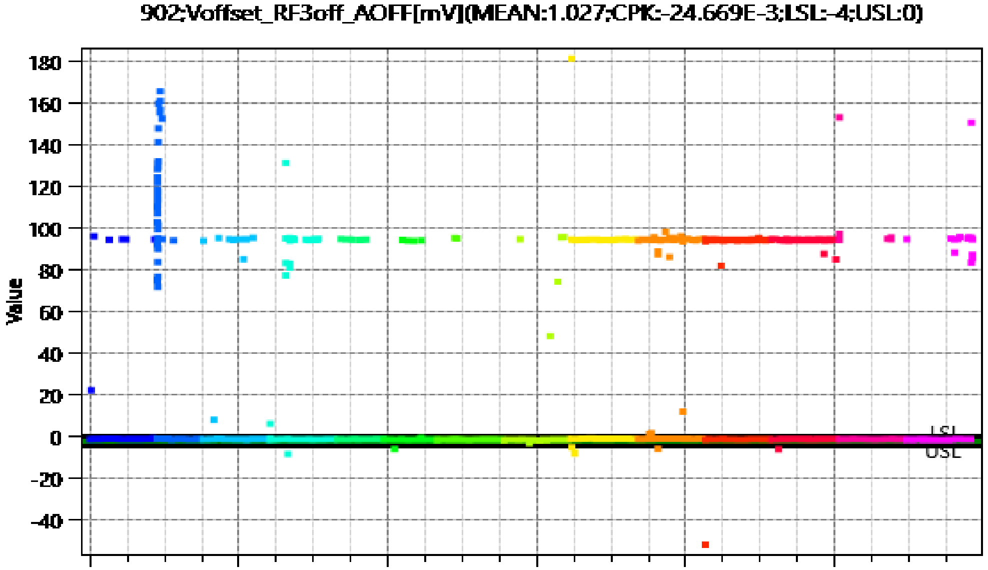


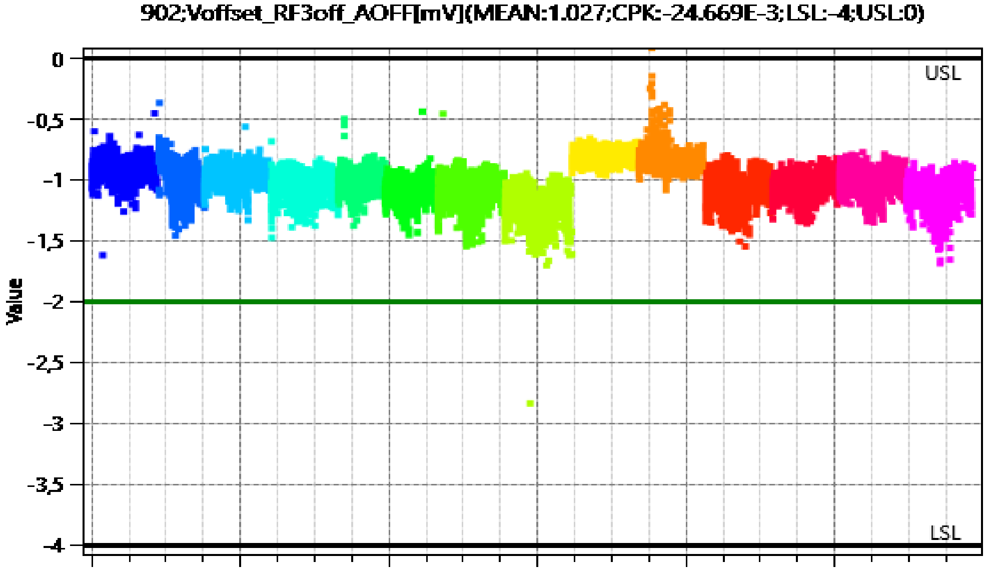


902: Voffset_RF3off_AOFF

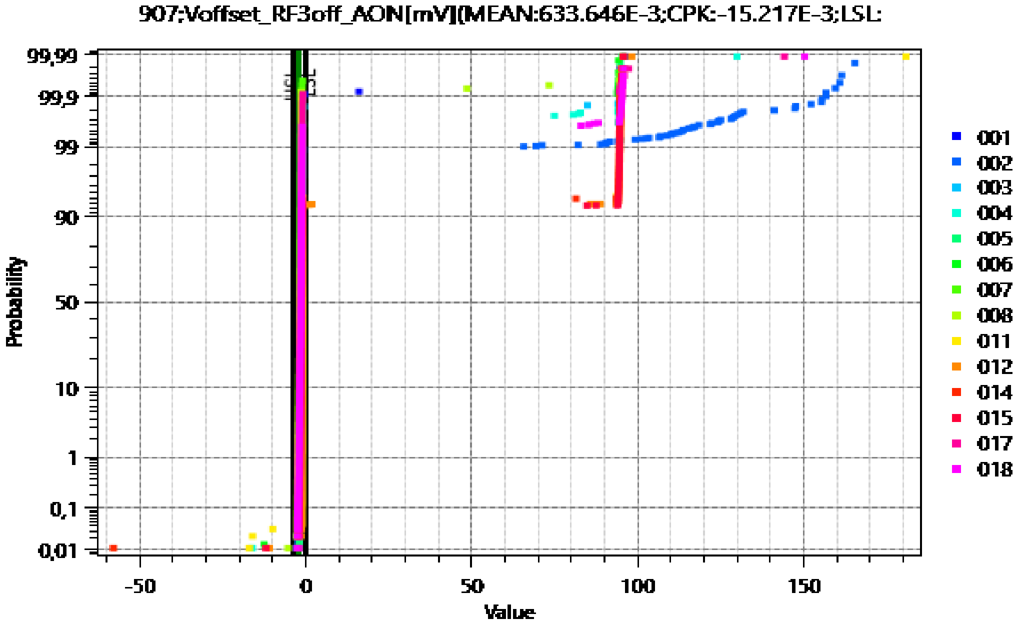


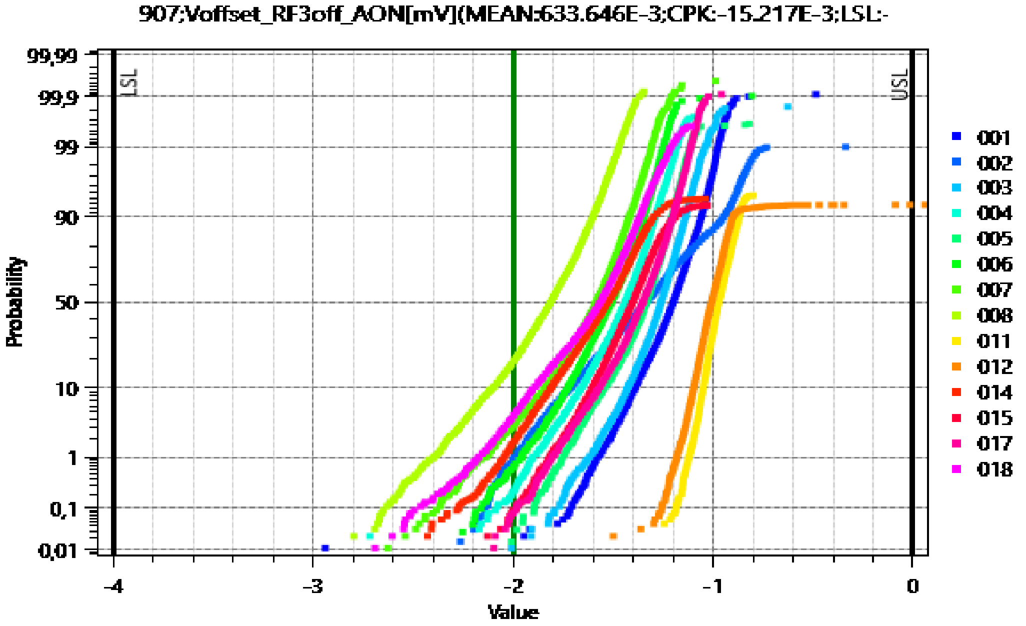


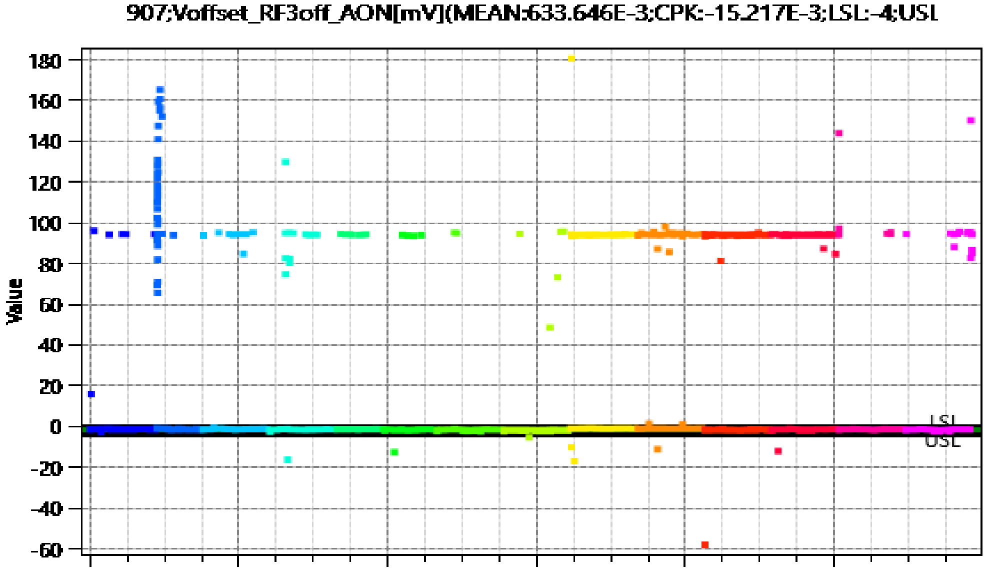


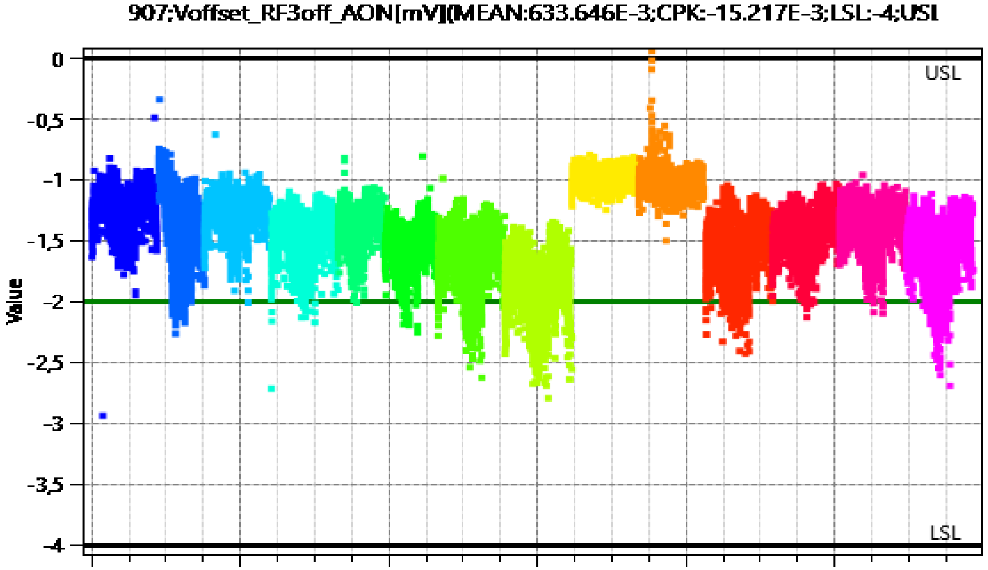


907: Voffset_RF3off_AON

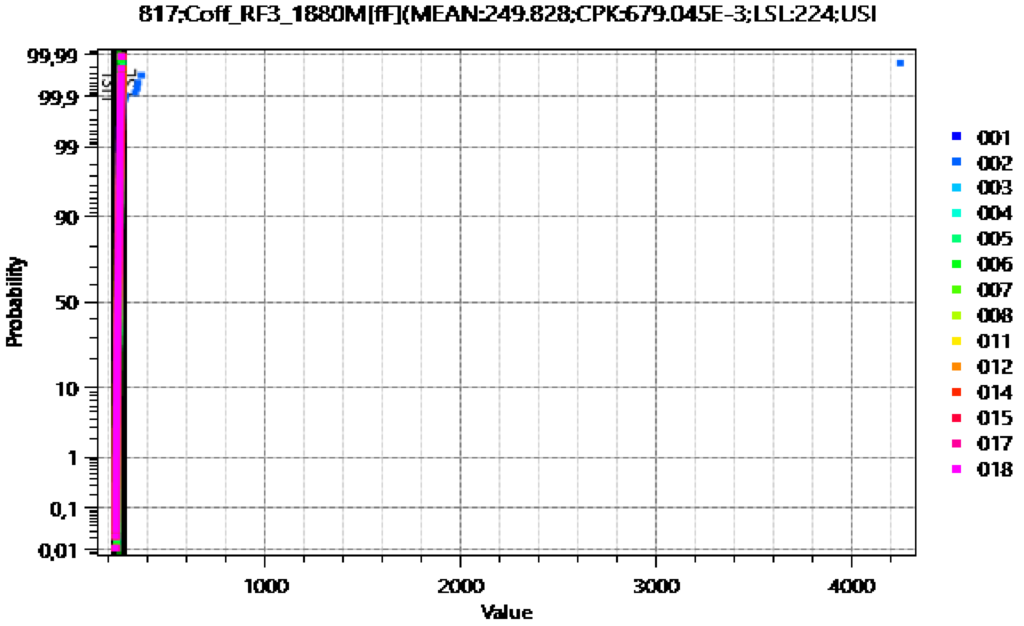


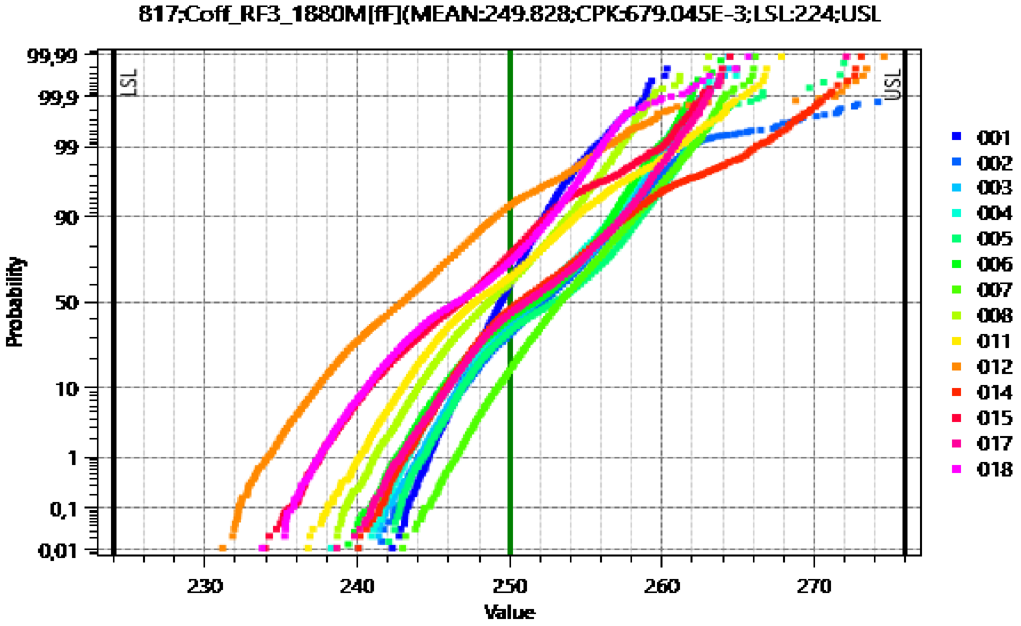


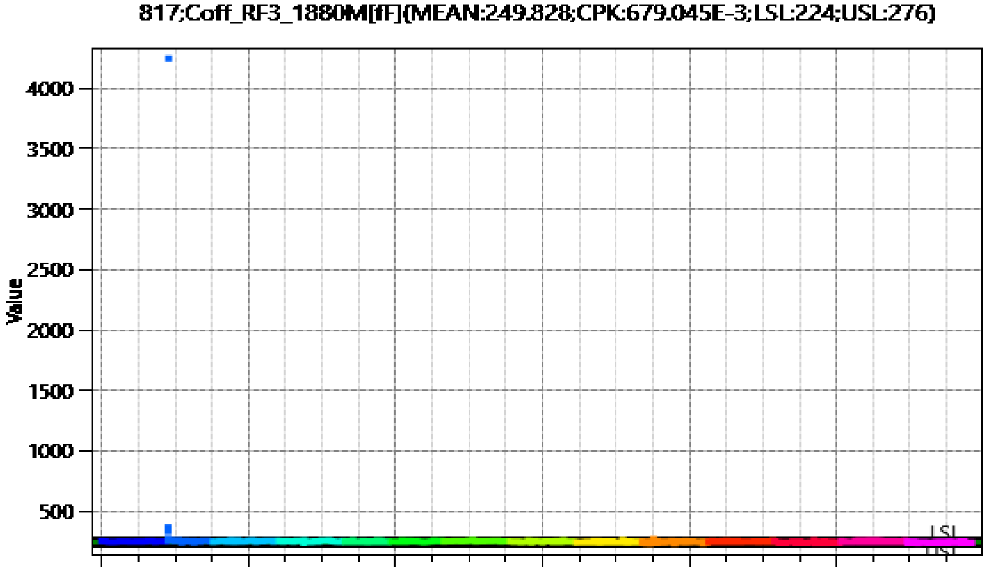


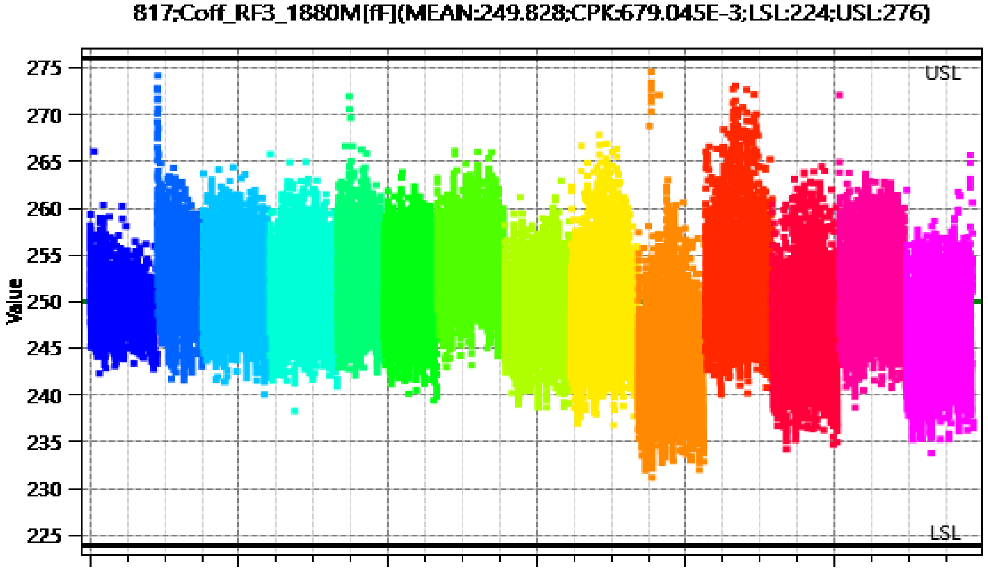


817: Coff_RF3_1880M

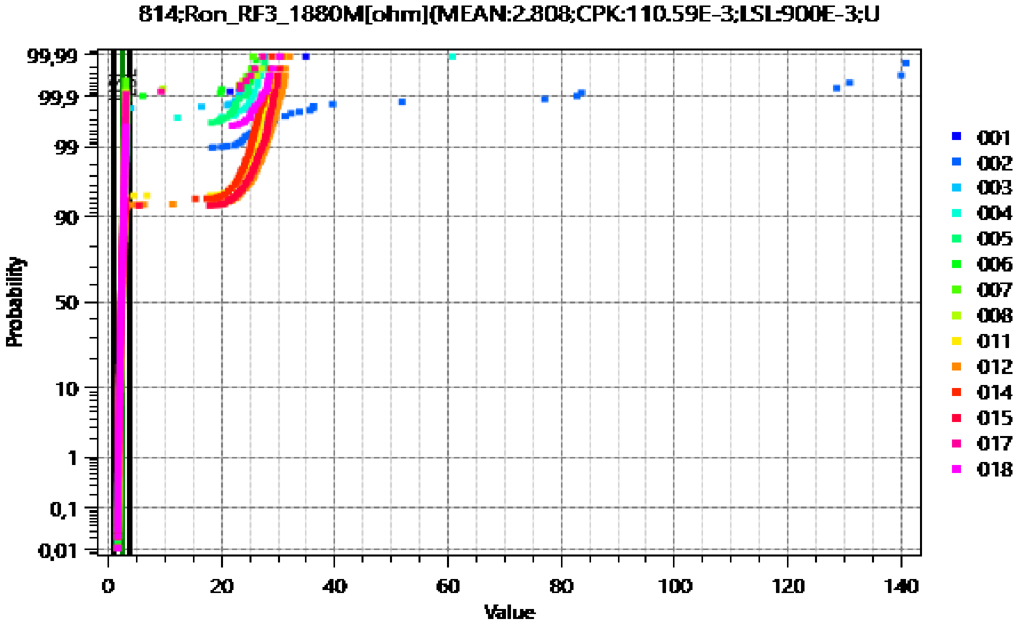


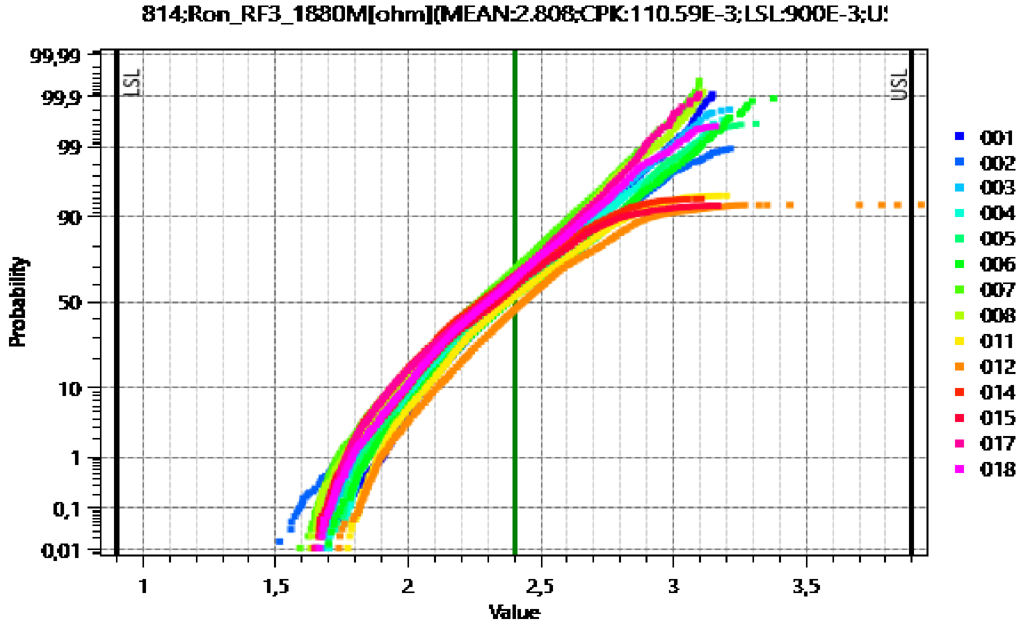


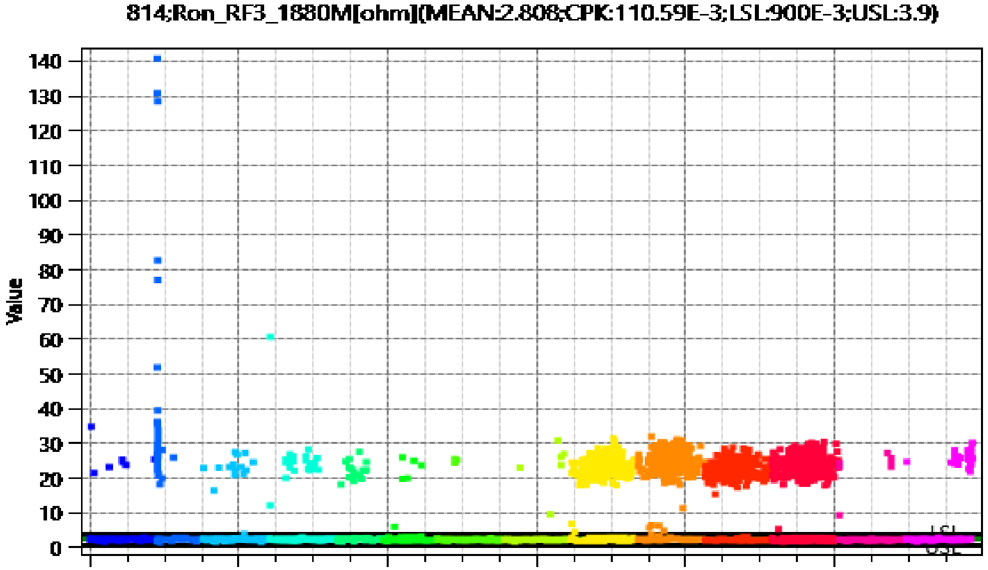


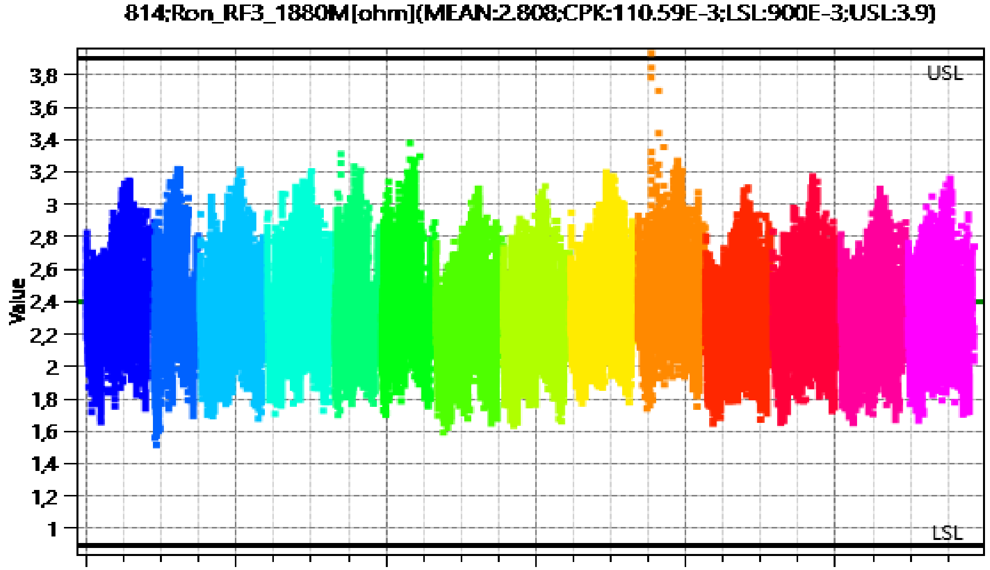


814: Ron_RF3_1880M

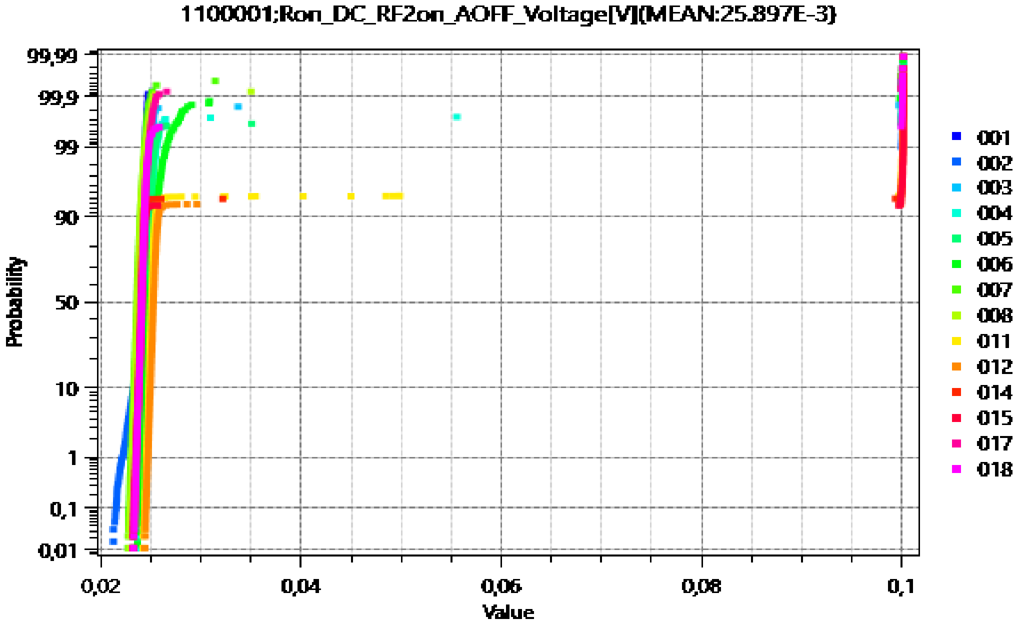


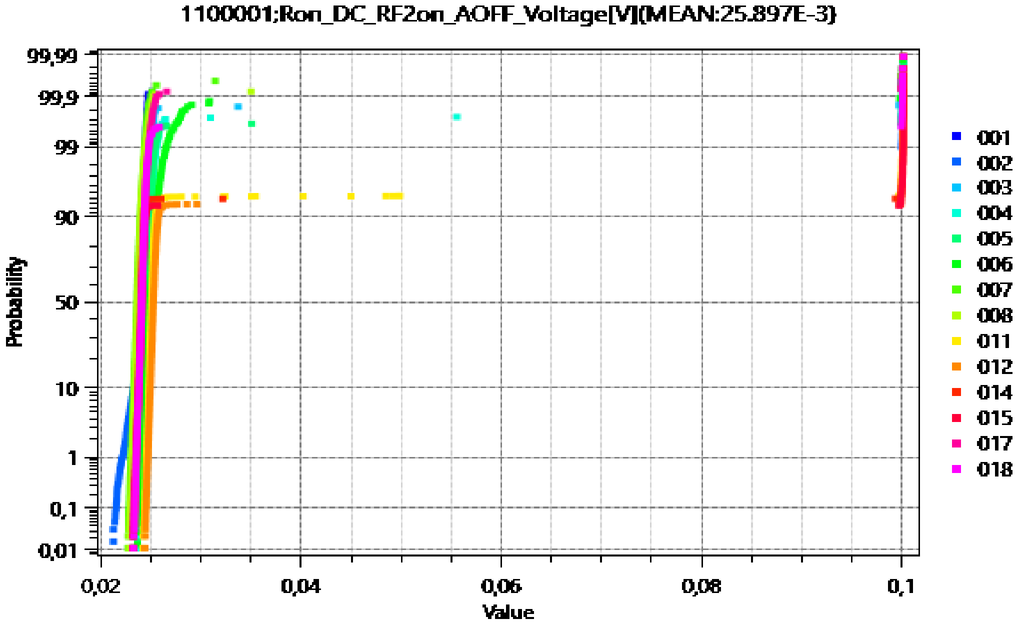


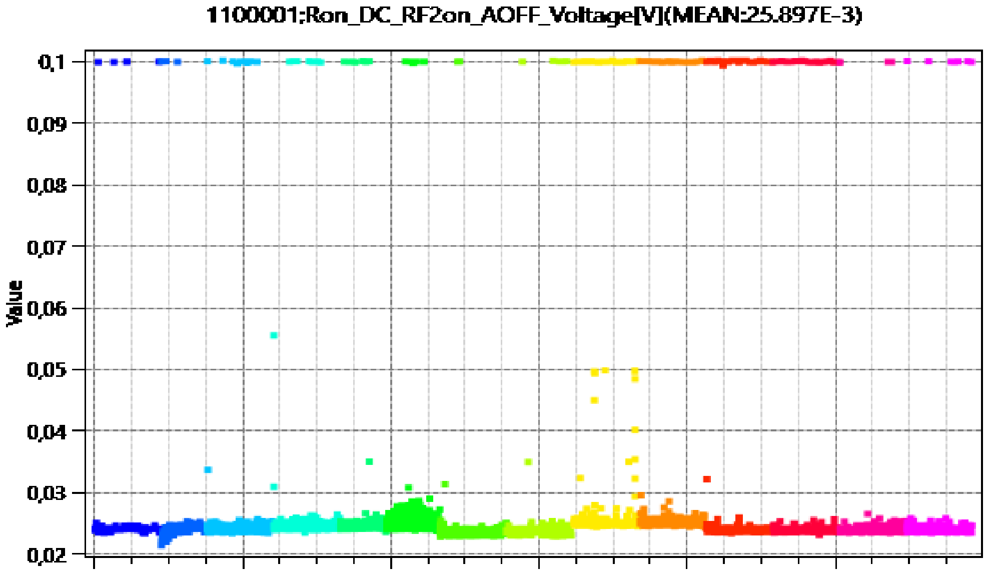


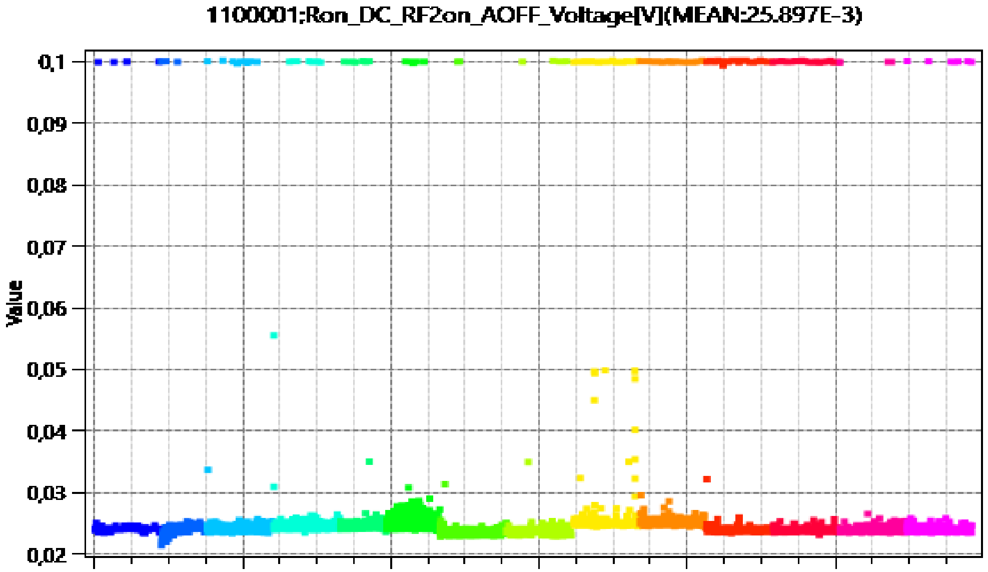


1100001: Ron_DC_RF2on_AOFF_Voltage

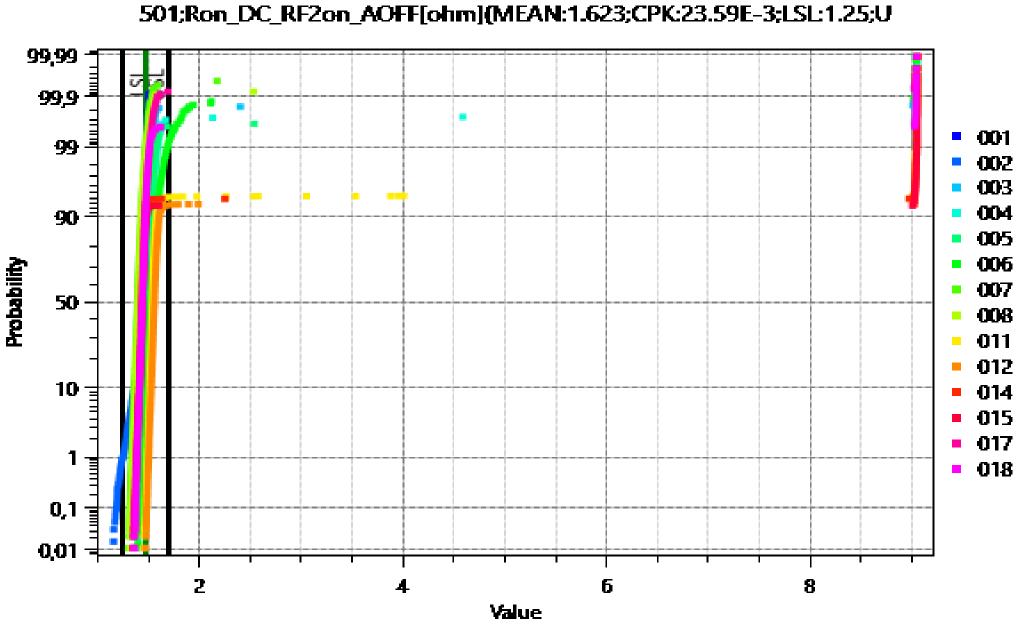


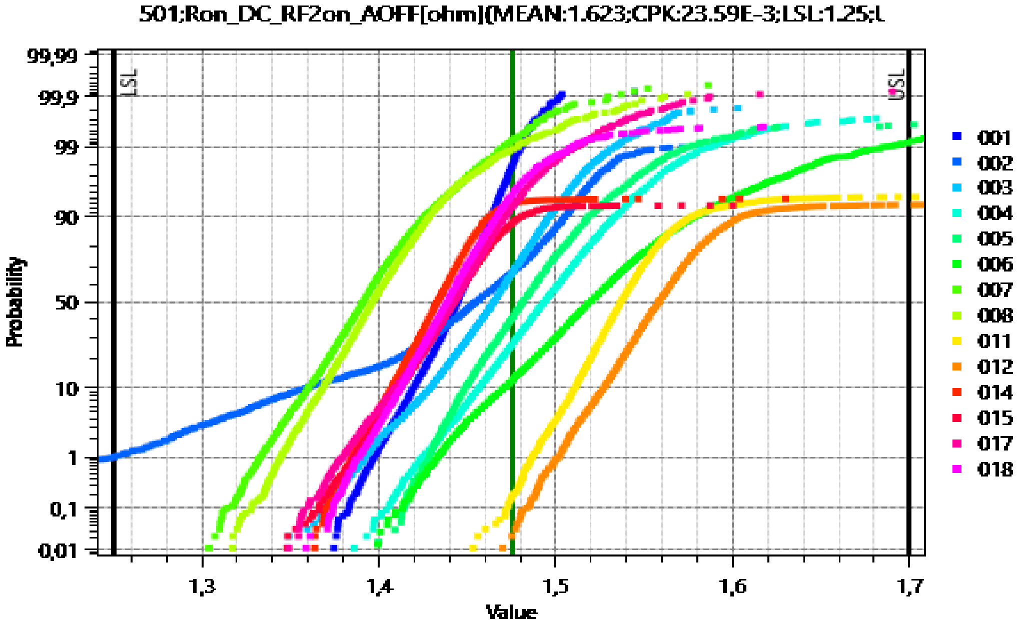


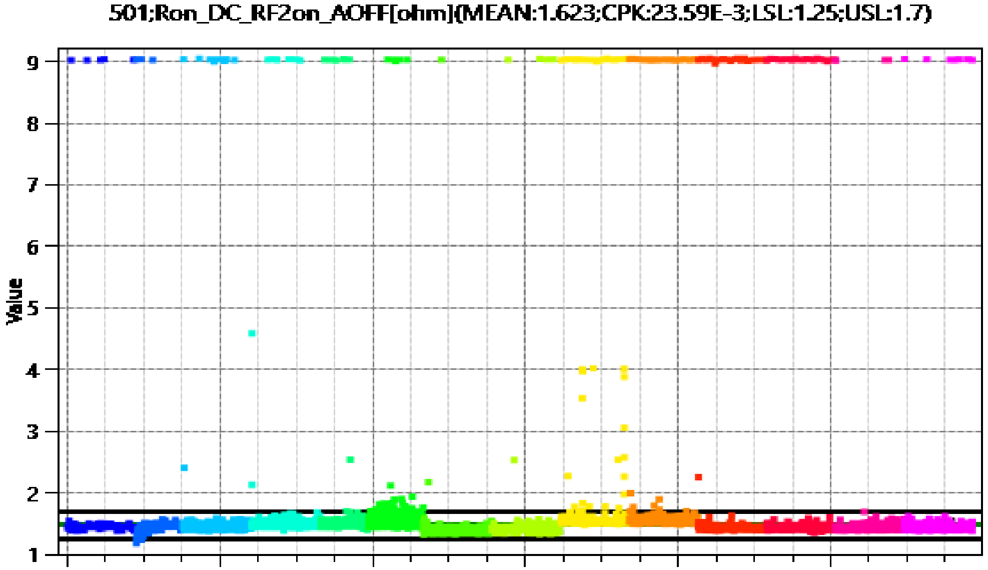


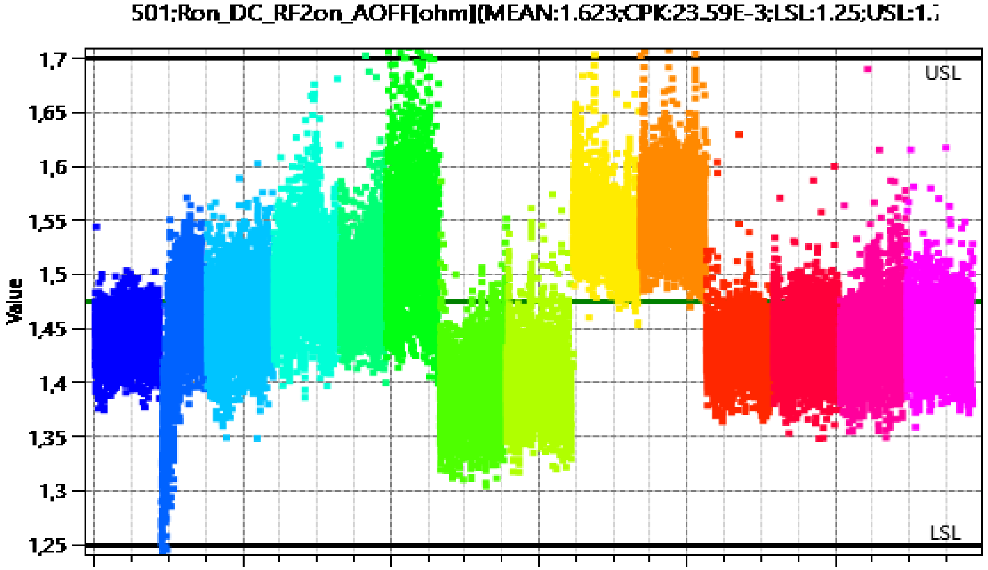


501: Ron_DC_RF2on_AOFF

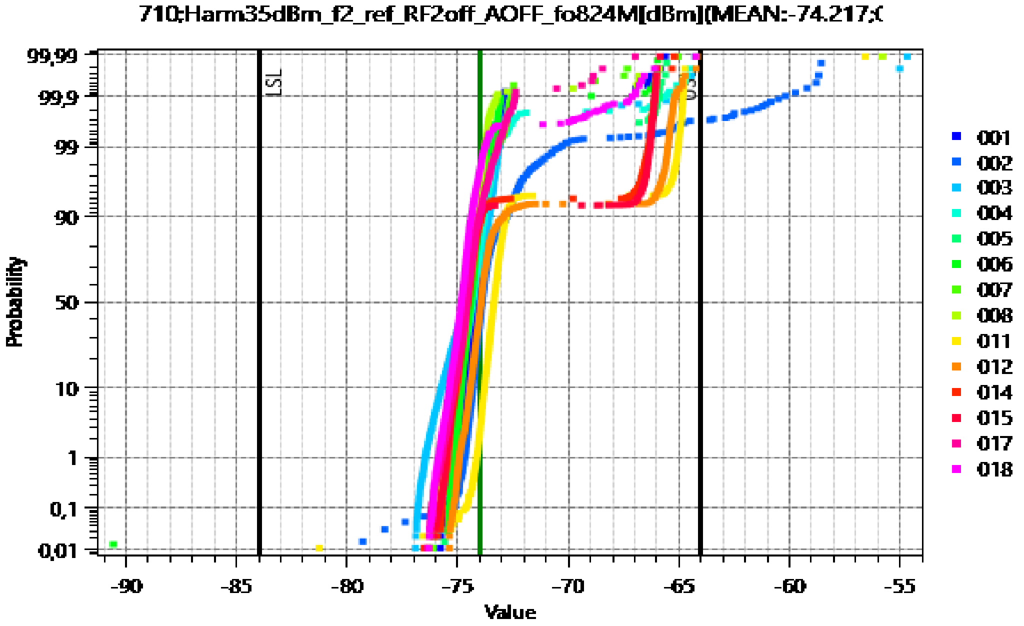


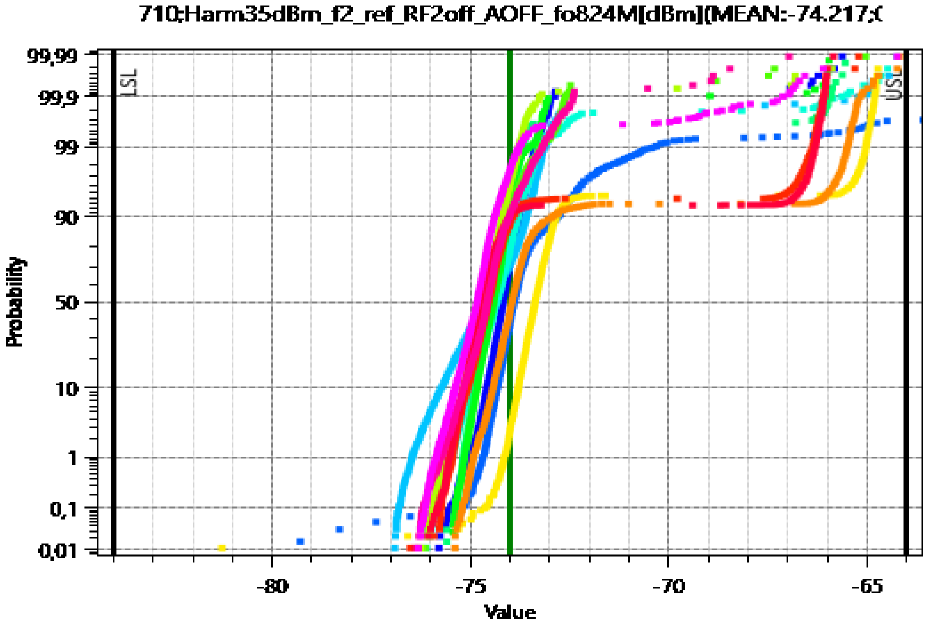


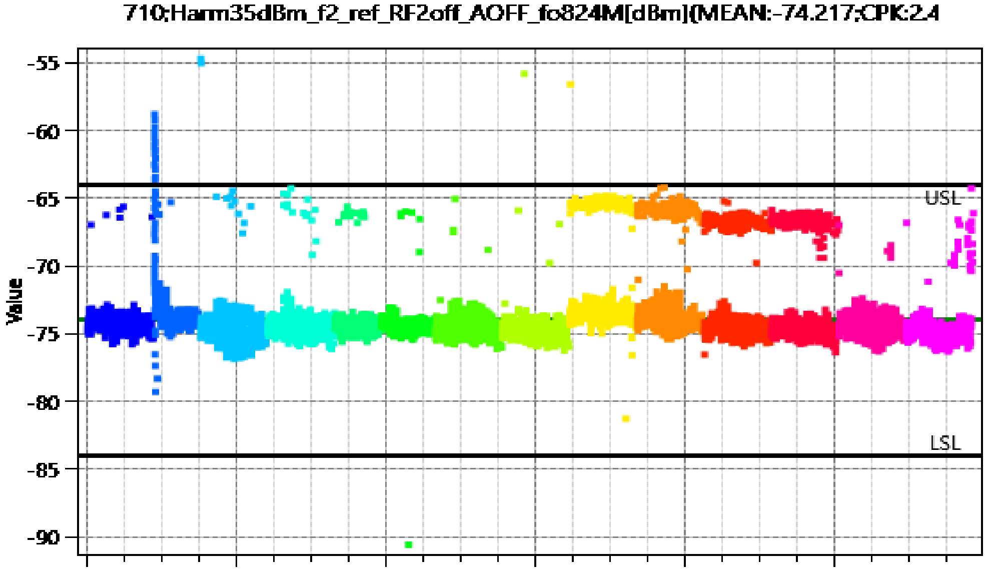


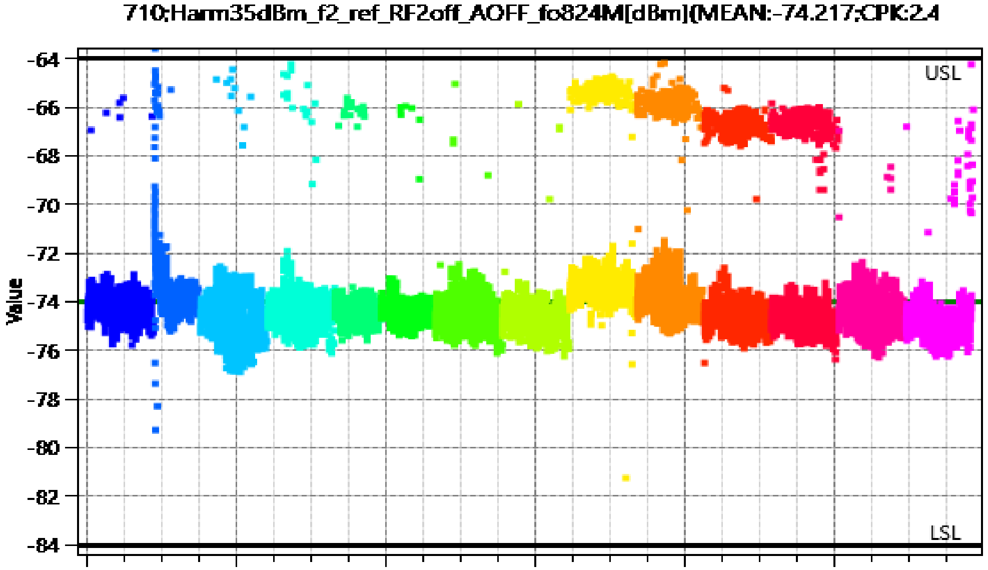


710: Harm35dBm_f2_ref_RF2off_AOFF_fo824M

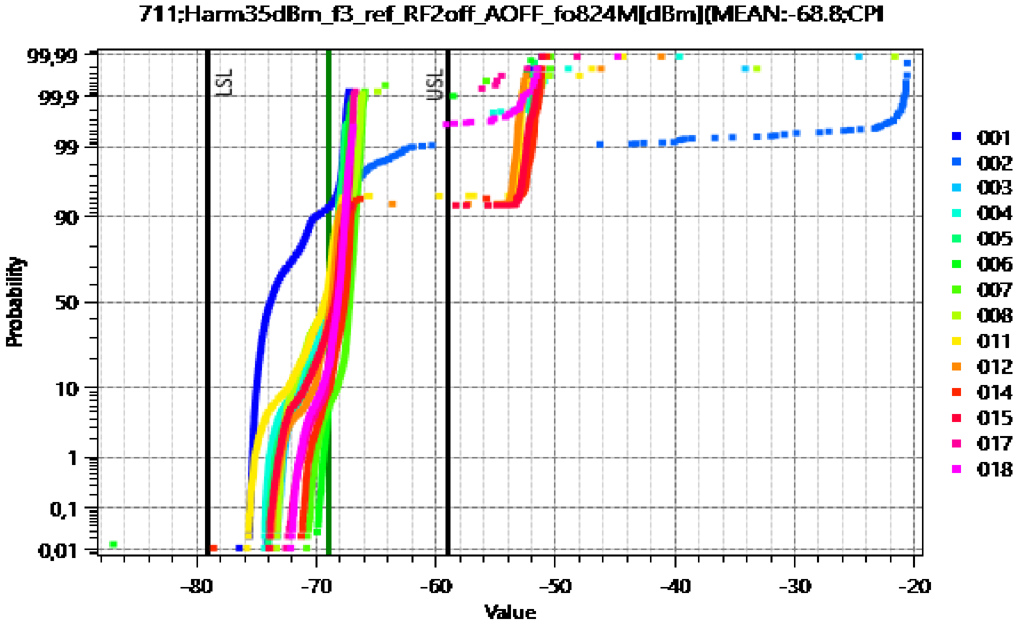


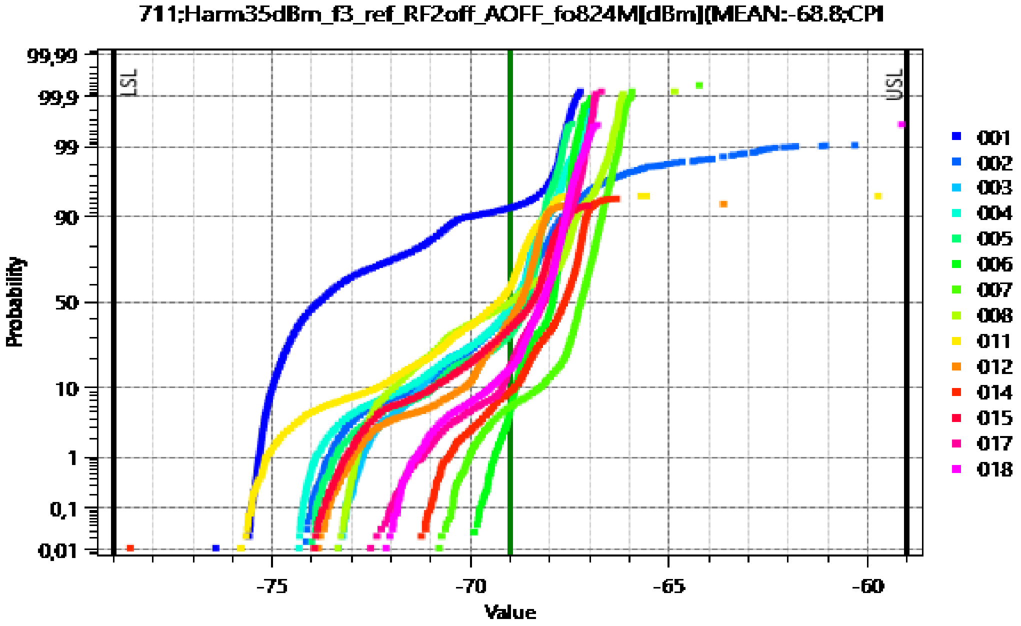


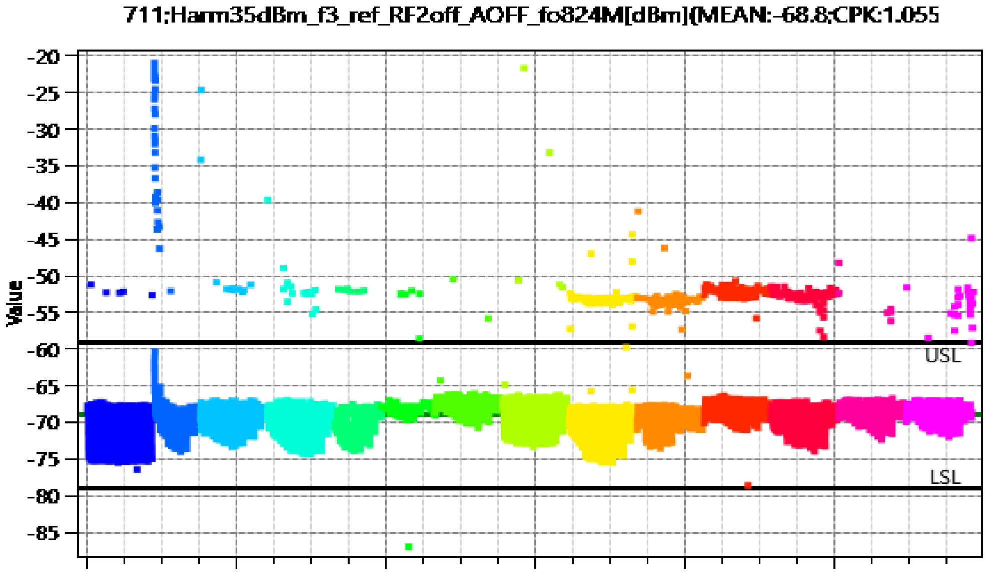


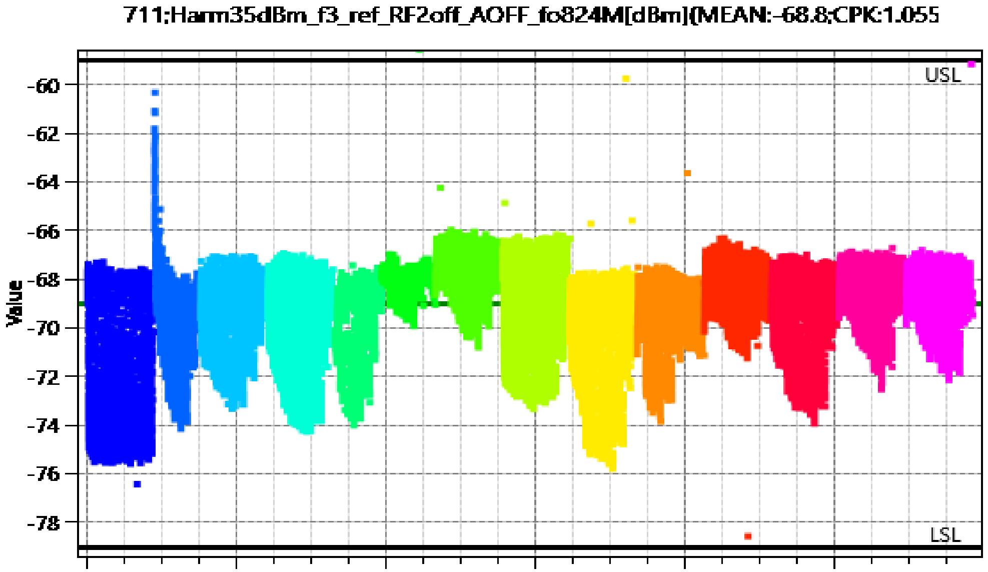


711: Harm35dBm_f3_ref_RF2off_AOFF_fo824M

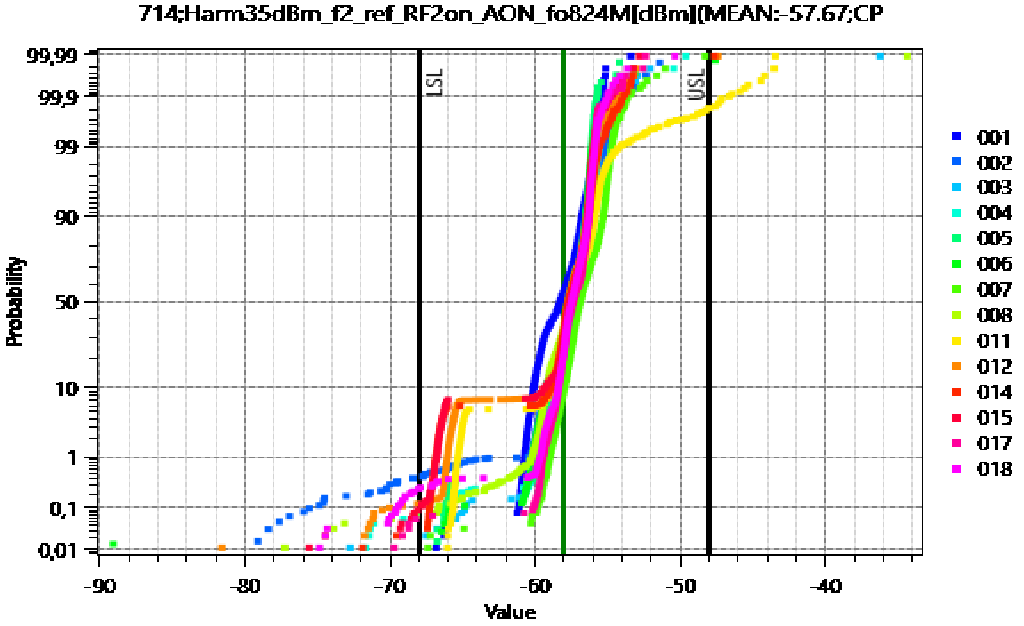


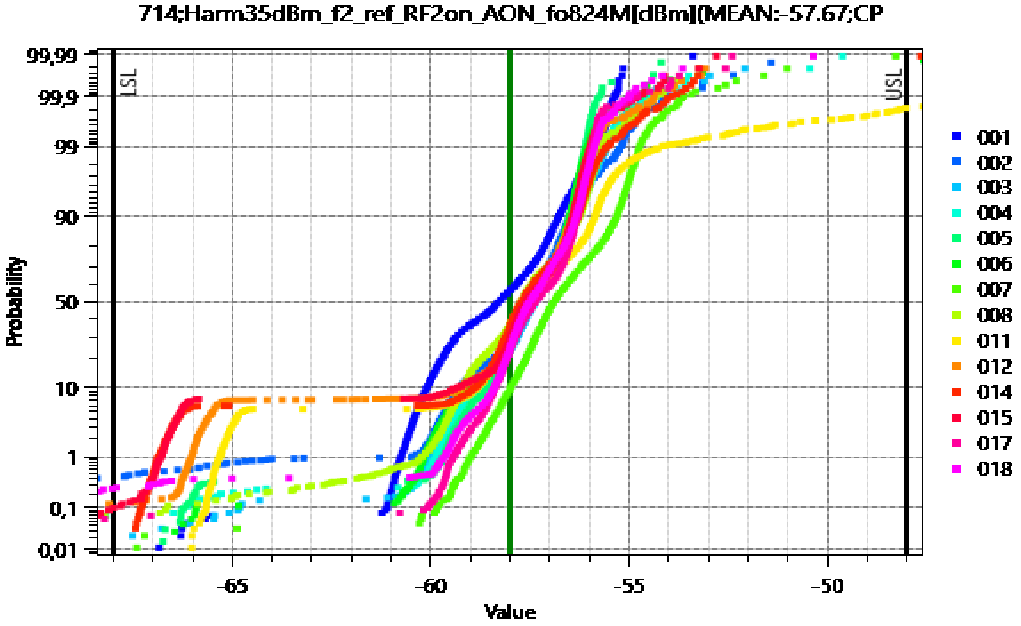


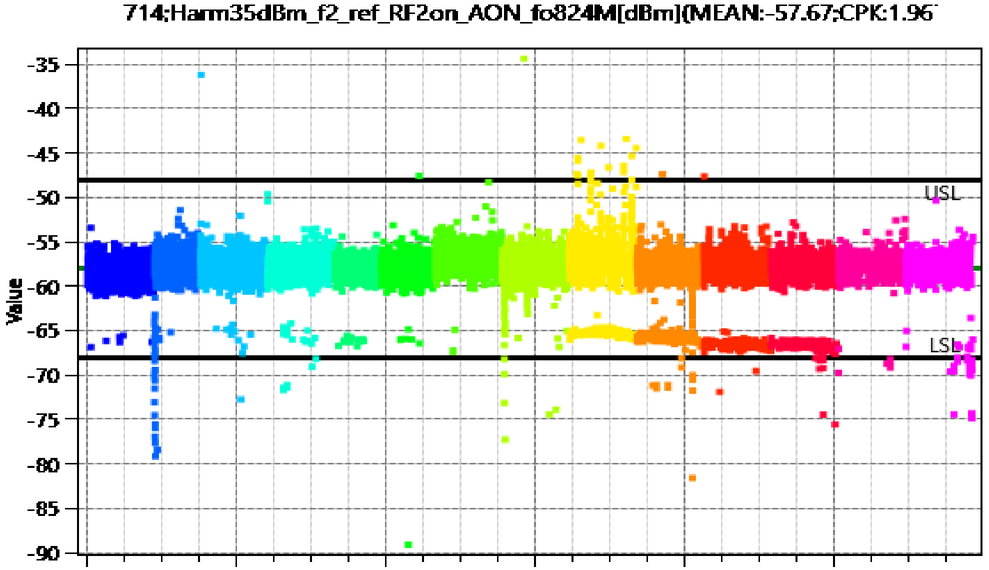


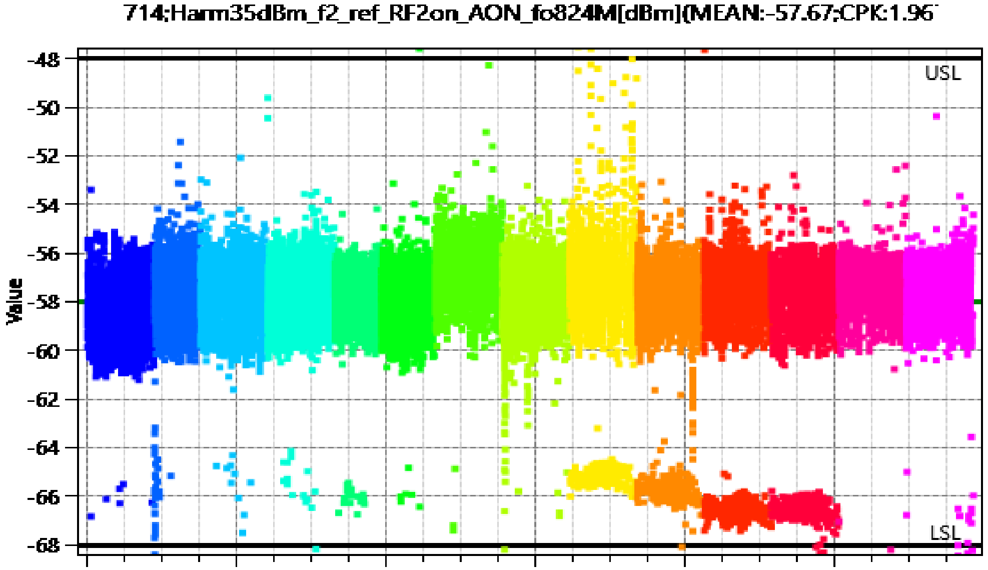


714: Harm35dBm_f2_ref_RF2on_AON_fo824M

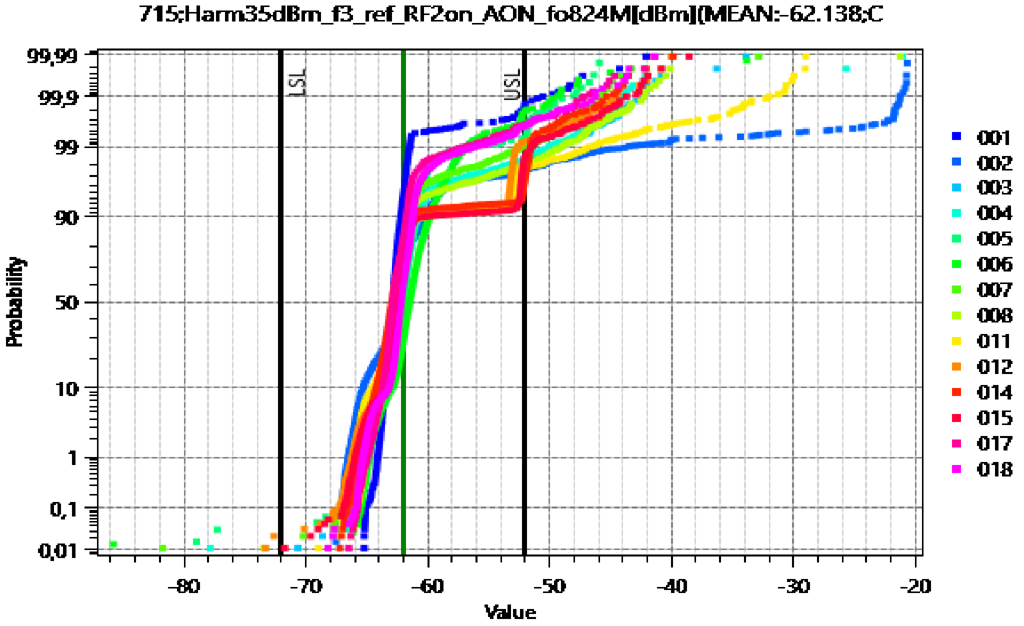


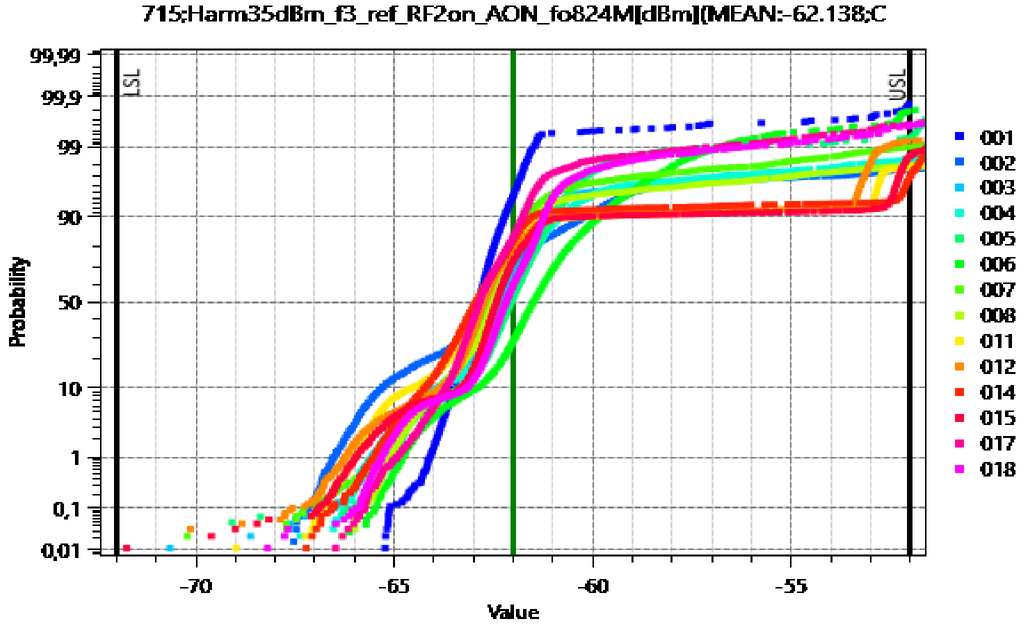


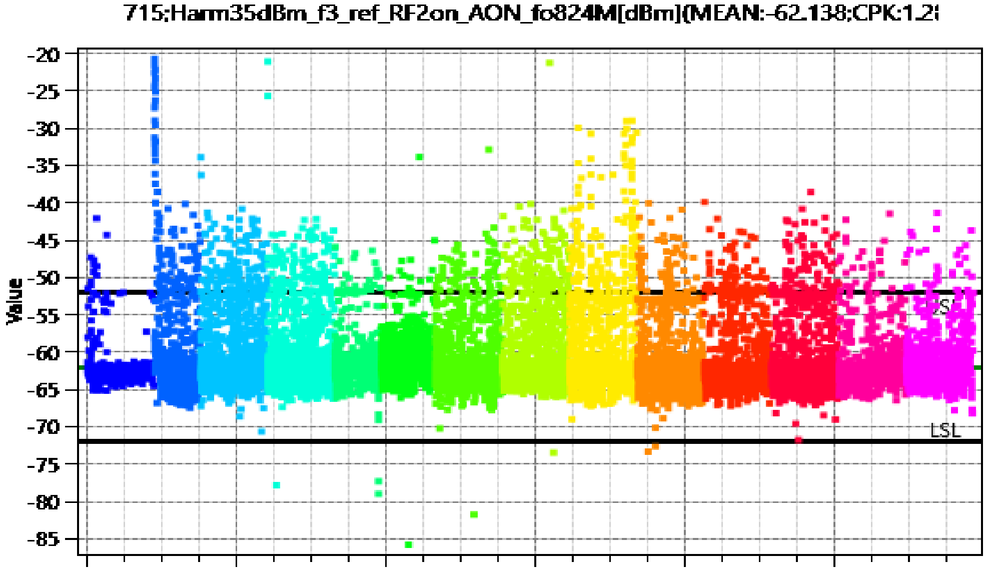


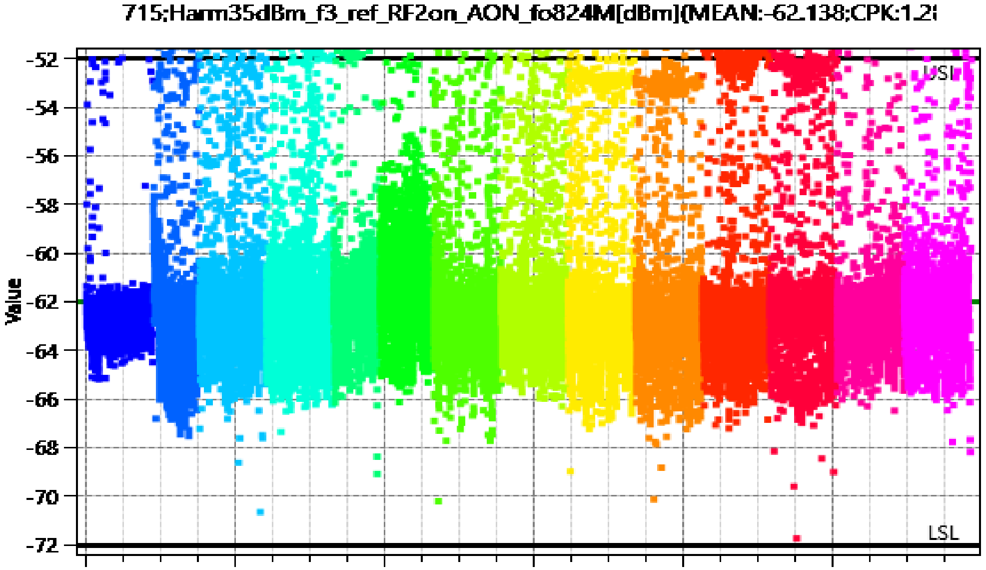


715: Harm35dBm_f3_ref_RF2on_AON_fo824M

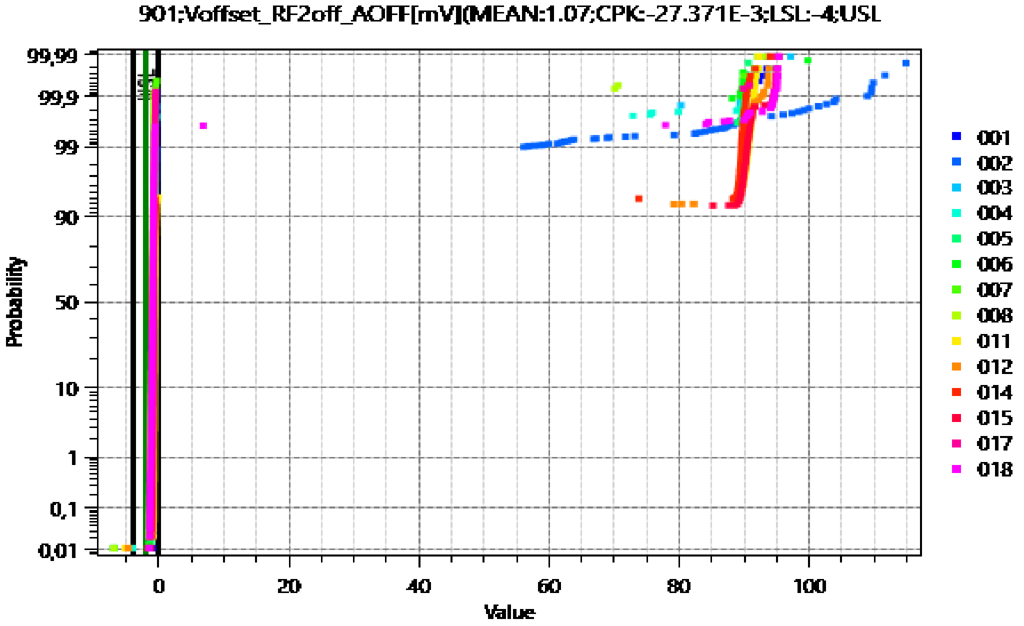


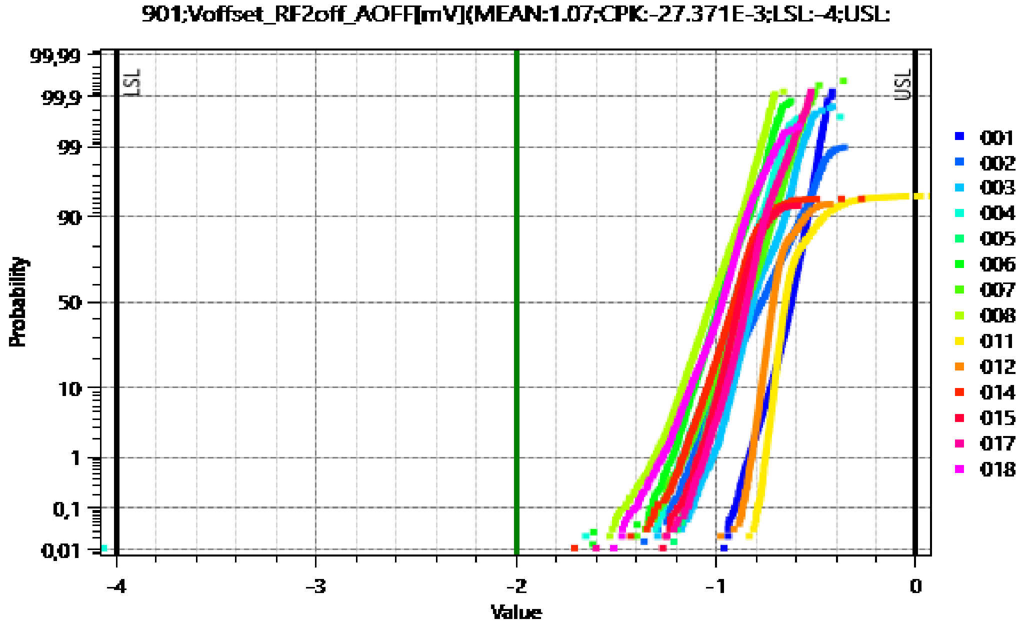


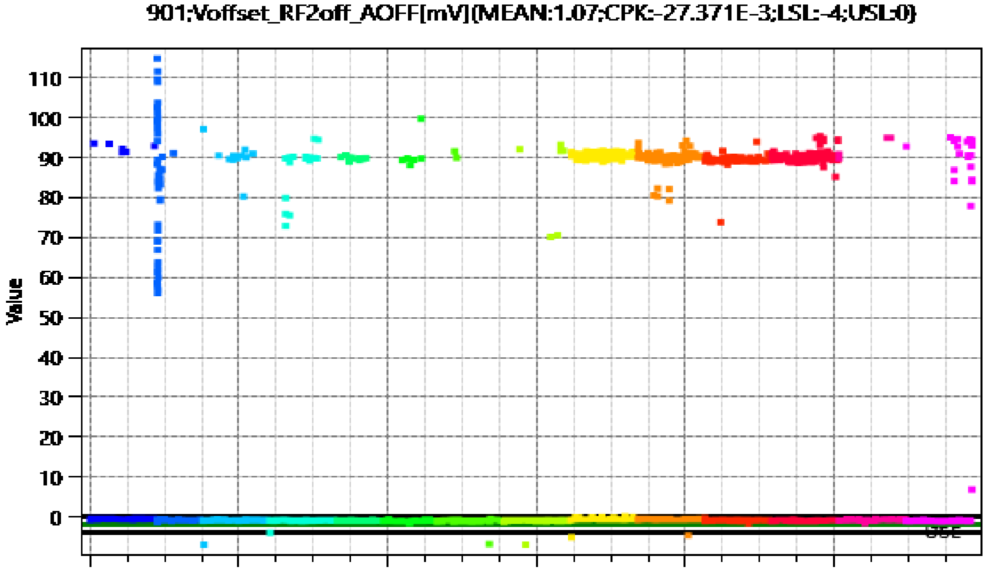


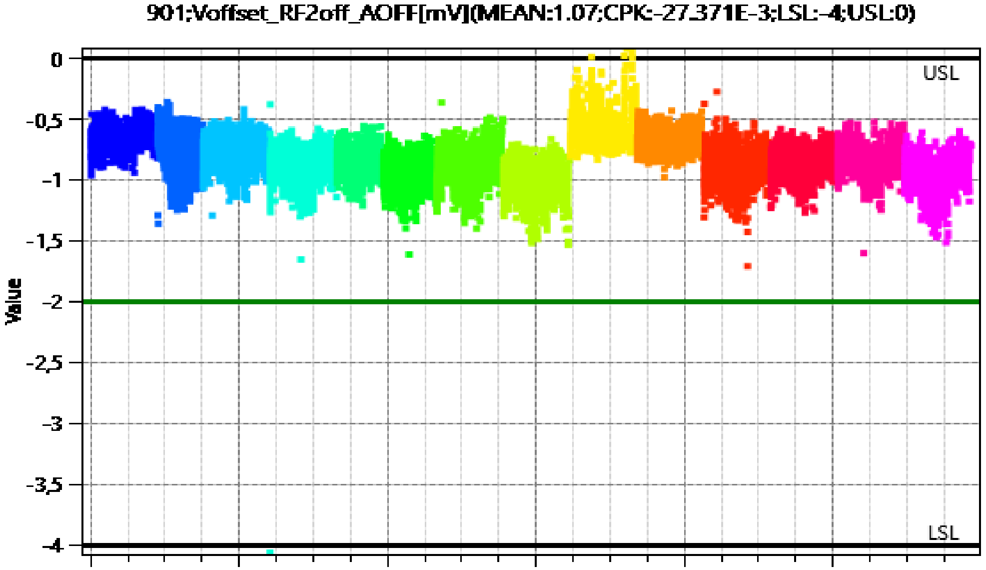


901: Voffset_RF2off_AOFF



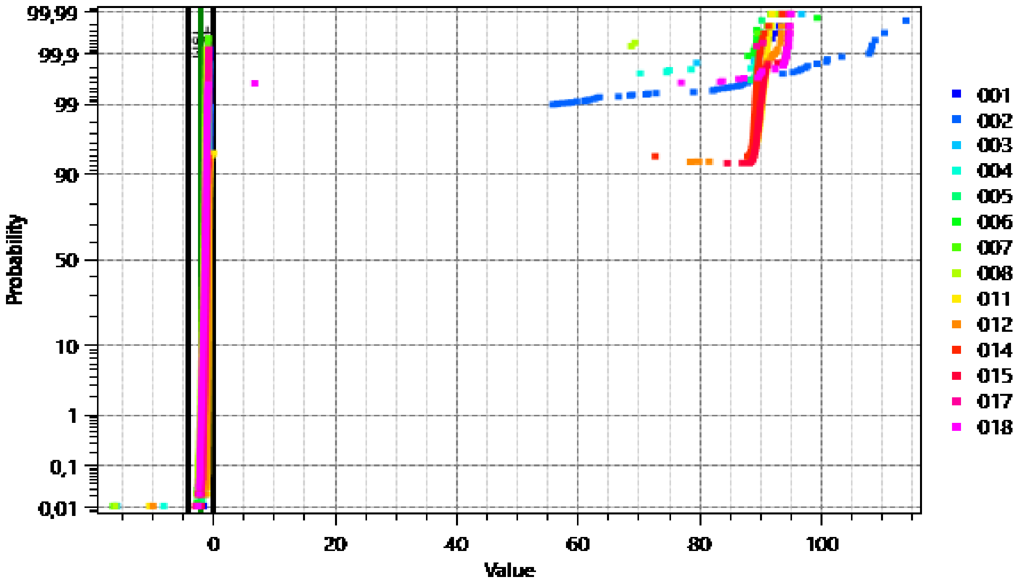




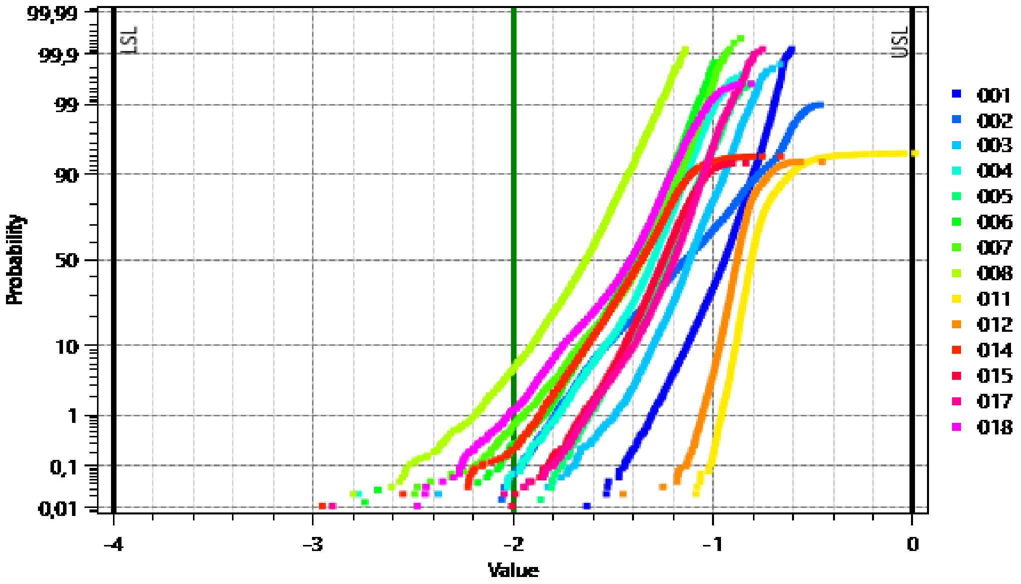


906: Voffset_RF2off_AON

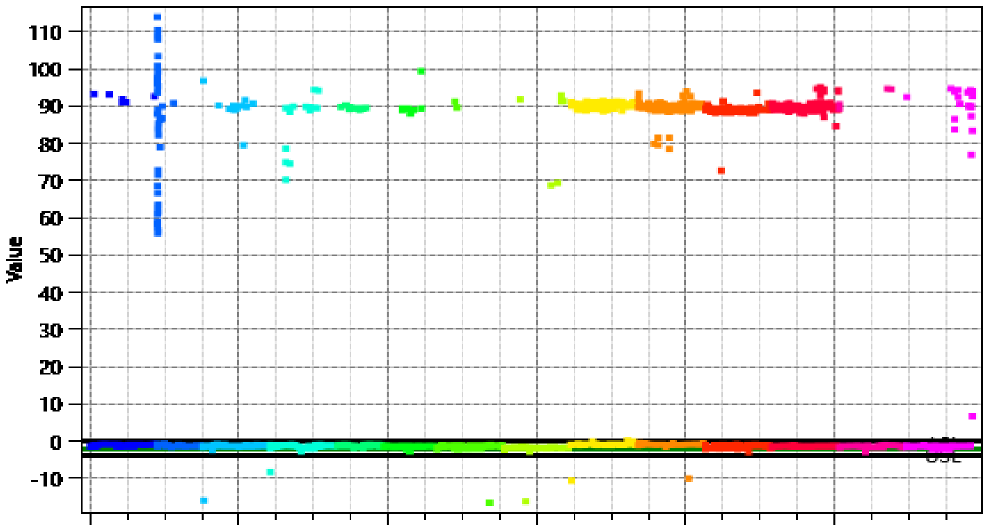
906;Voffset_RF2off_AON[mV](MEAN:679.906E-3;CPK:-17.402E-3;LSL:



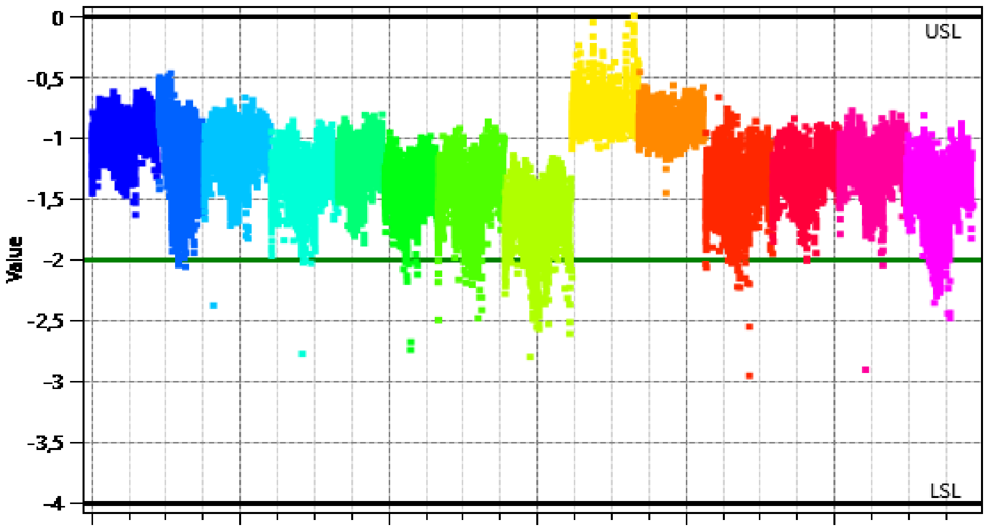
906;Voffset_RF2off_AON[mV](MEAN:679.906E-3;CPK:-17.402E-3;LSL:-



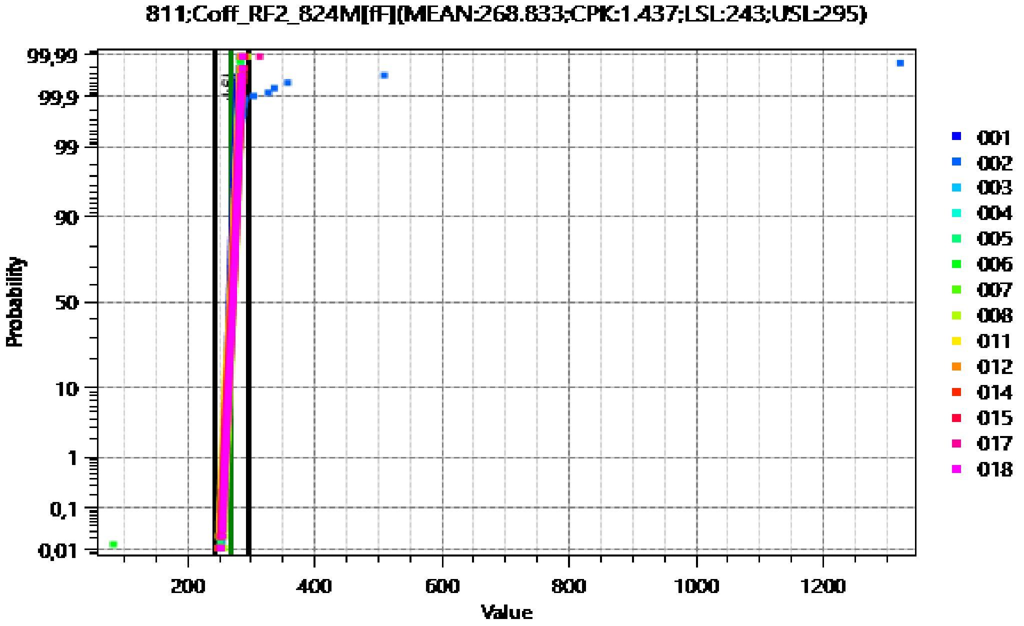
906;Voffset_RF2off_AON[mV](MEAN:679.906E-3;CPK:-17.402E-3;LSL:-4;USL

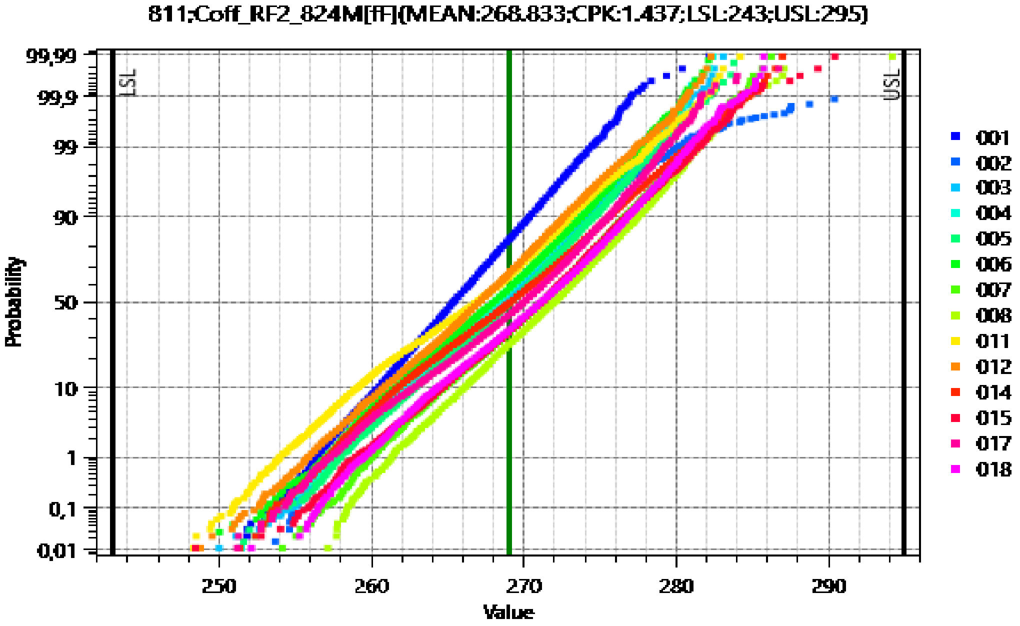


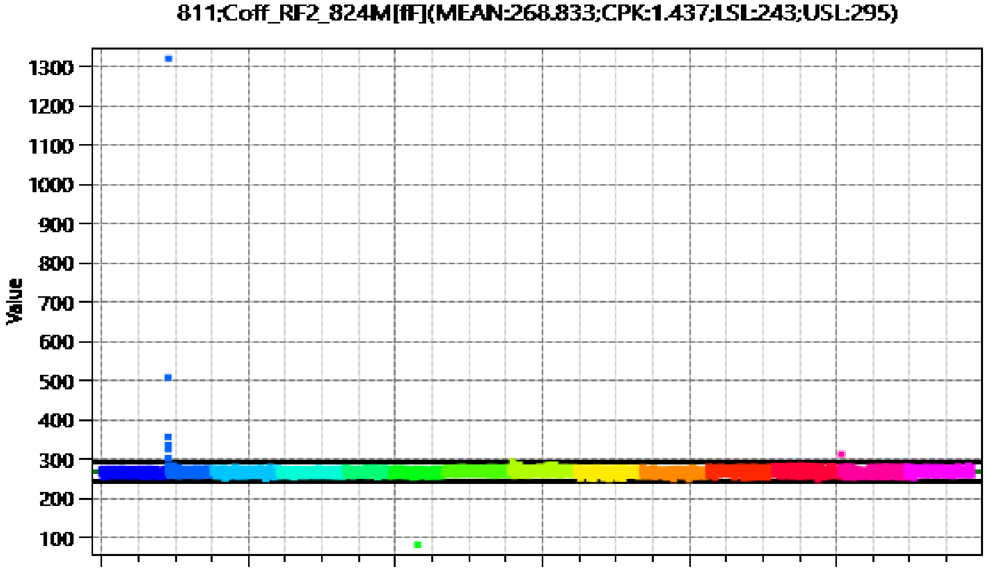
906;Voffset_RF2off_AON[mV](MEAN:679.906E-3;CPK:-17.402E-3;LSL:-4;USL

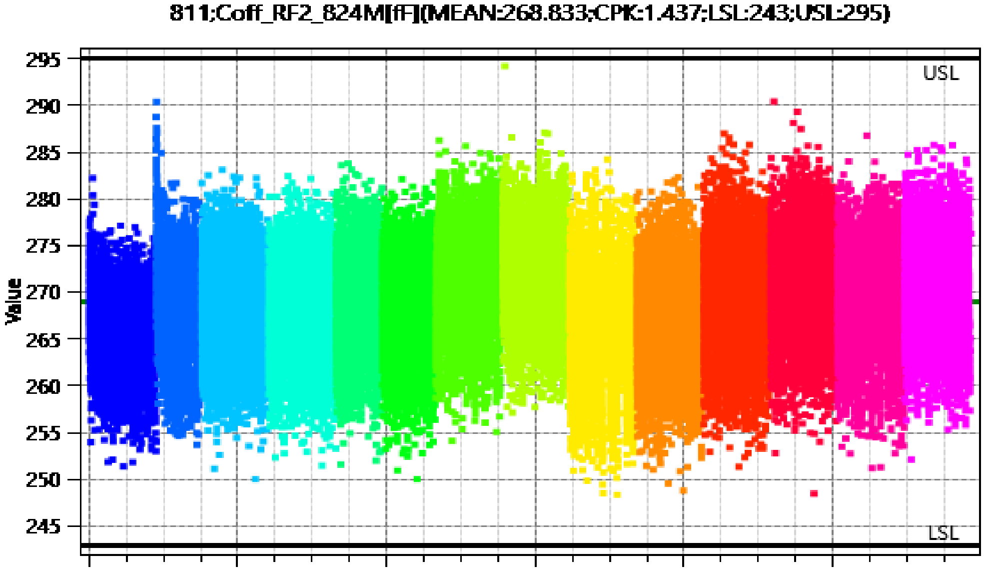


811: Coff_RF2_824M

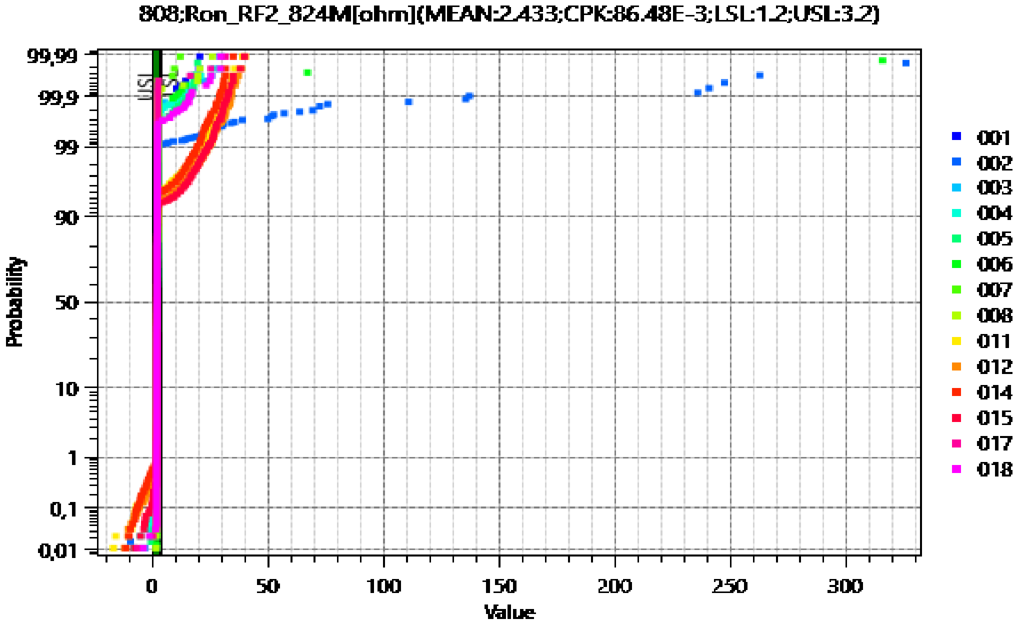


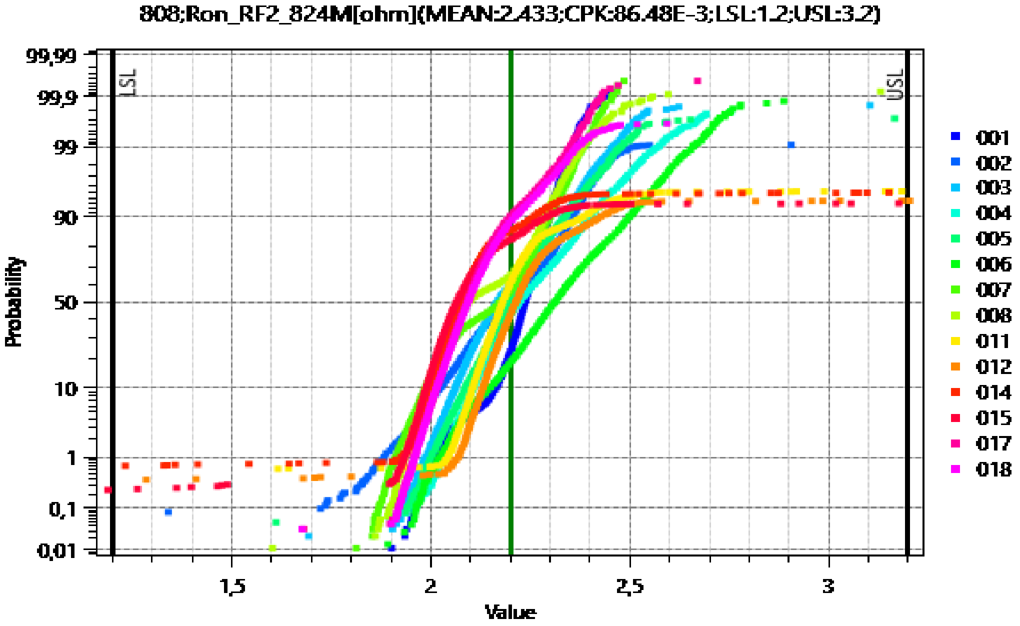


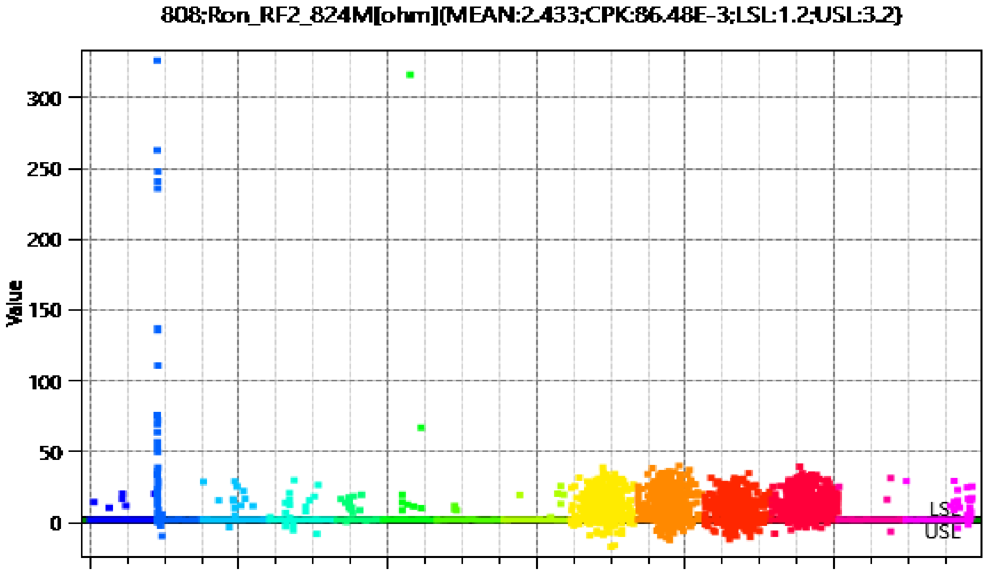


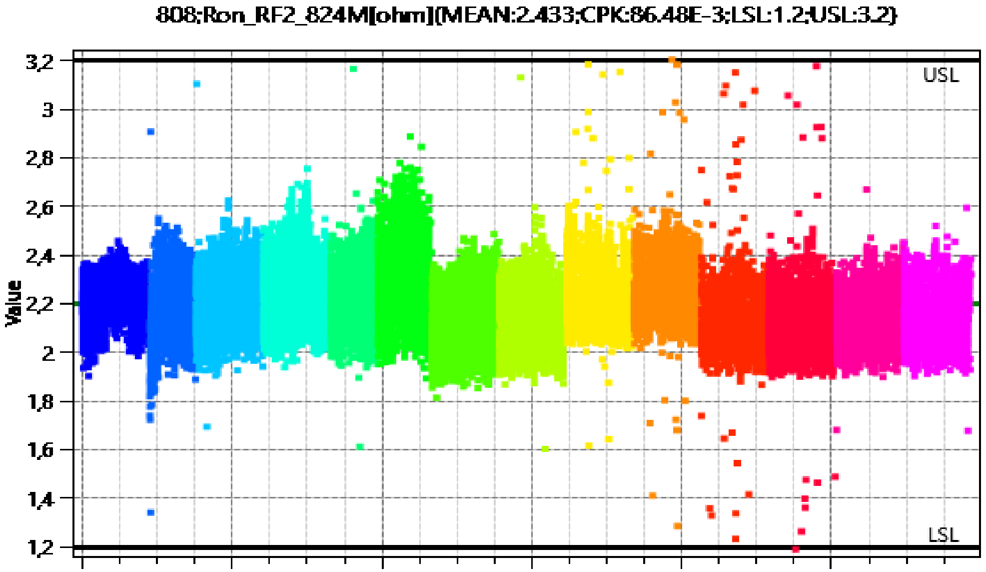


808: Ron_RF2_824M

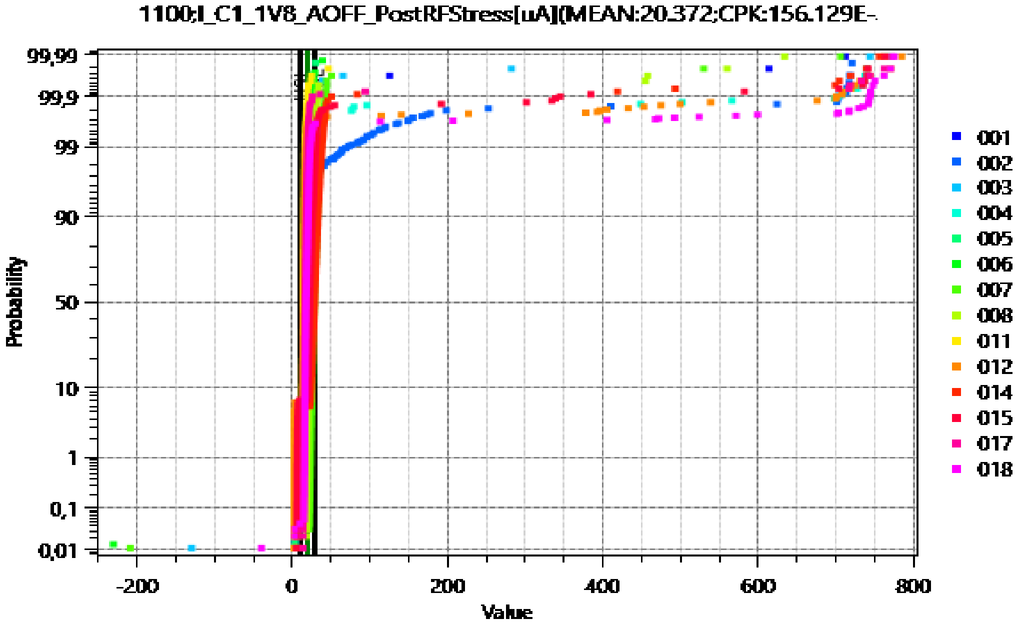


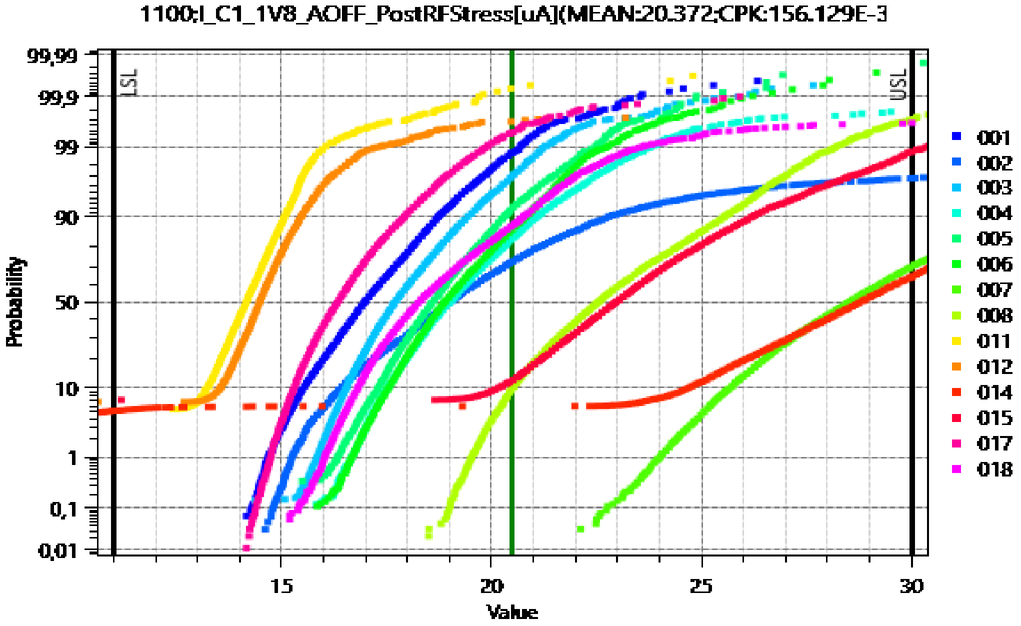


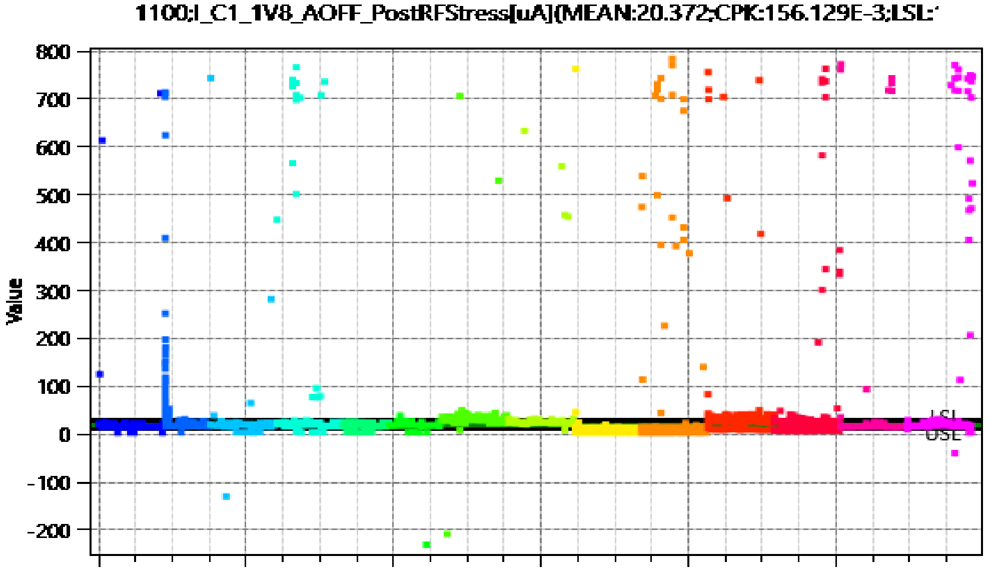


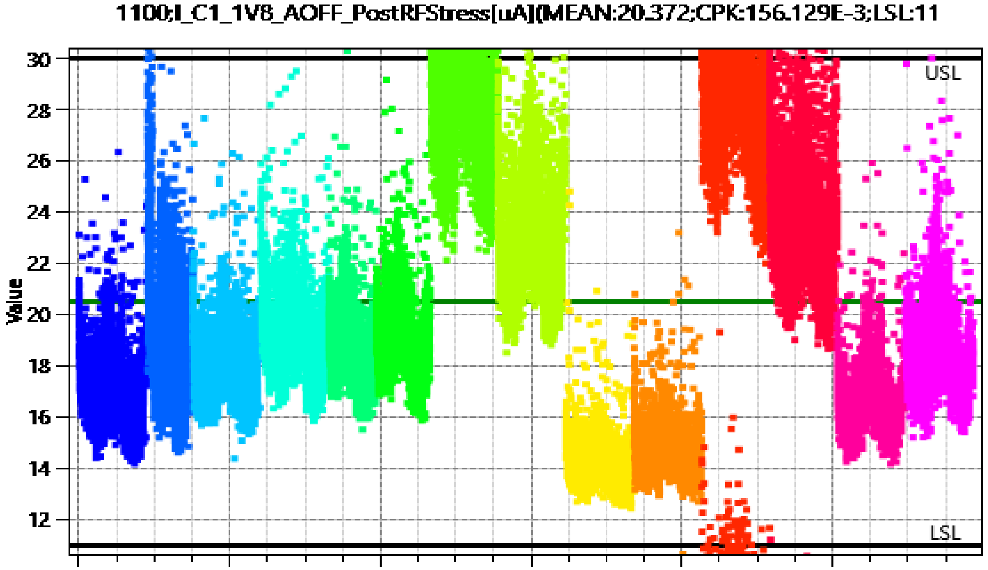


1100: I_C1_1V8_AOFF_PostRFStress

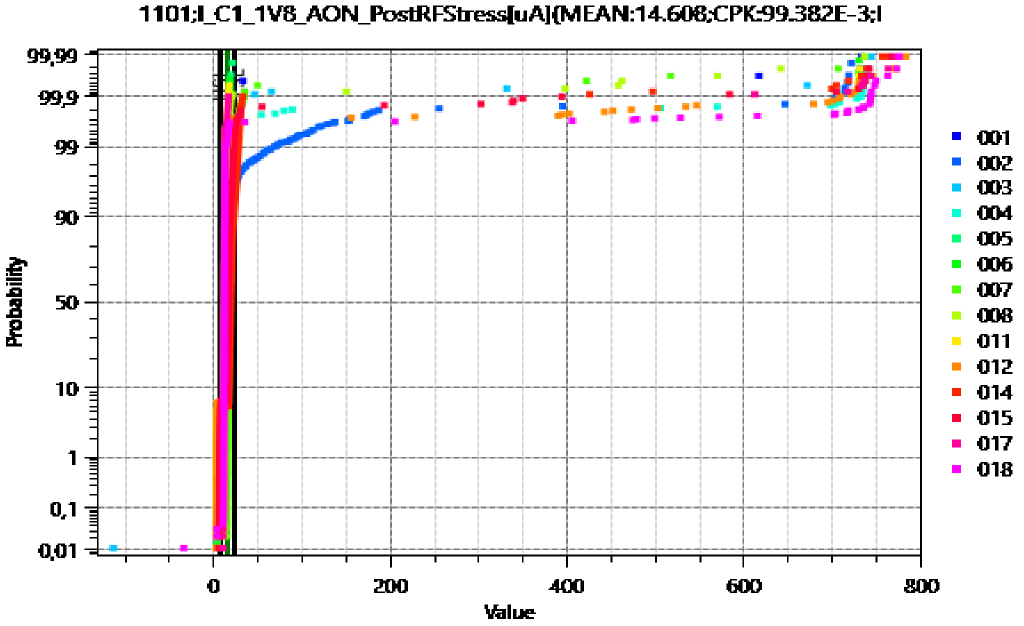


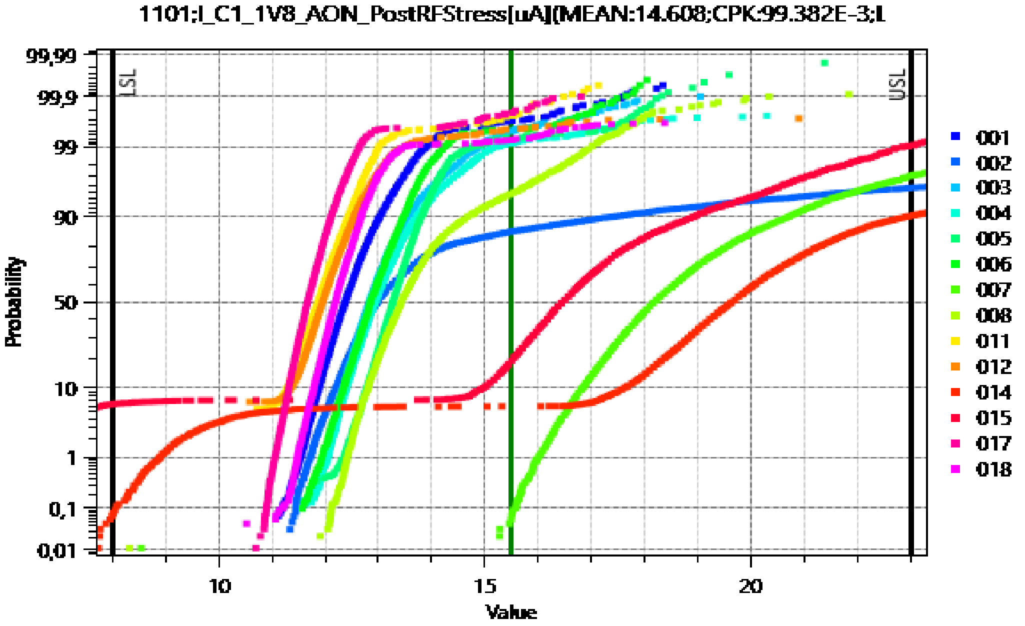


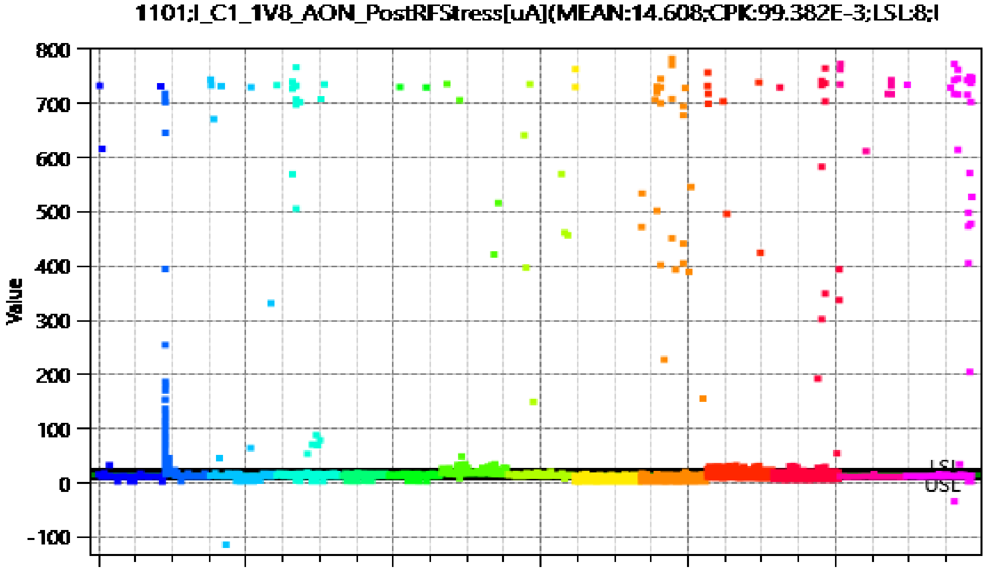


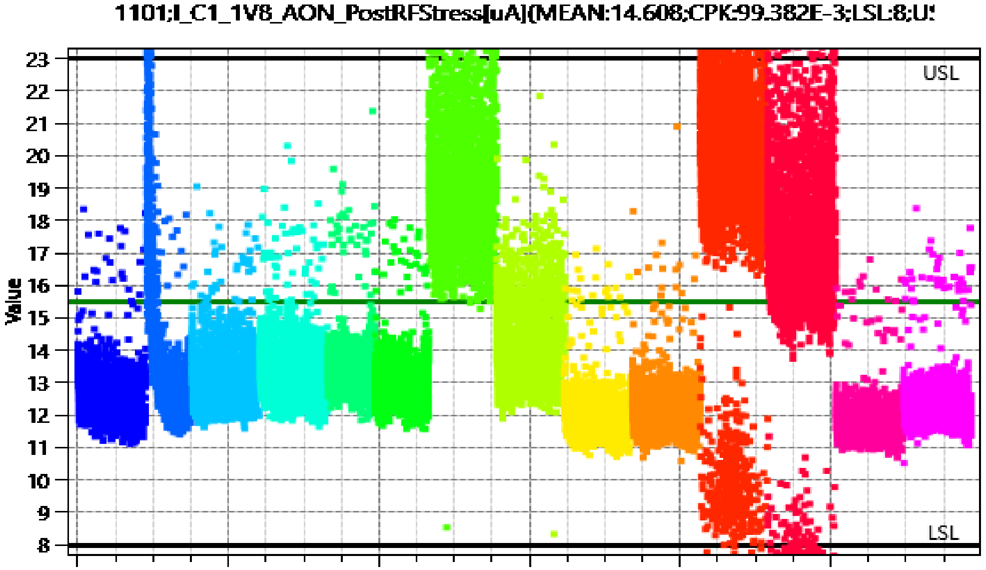


1101: I_C1_1V8_AON_PostRFStress

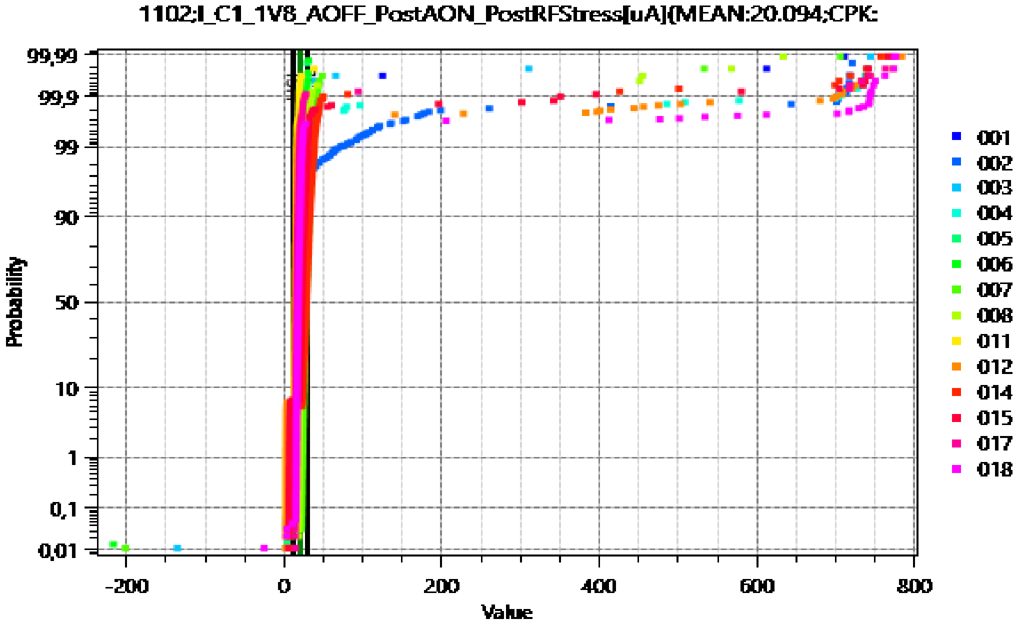


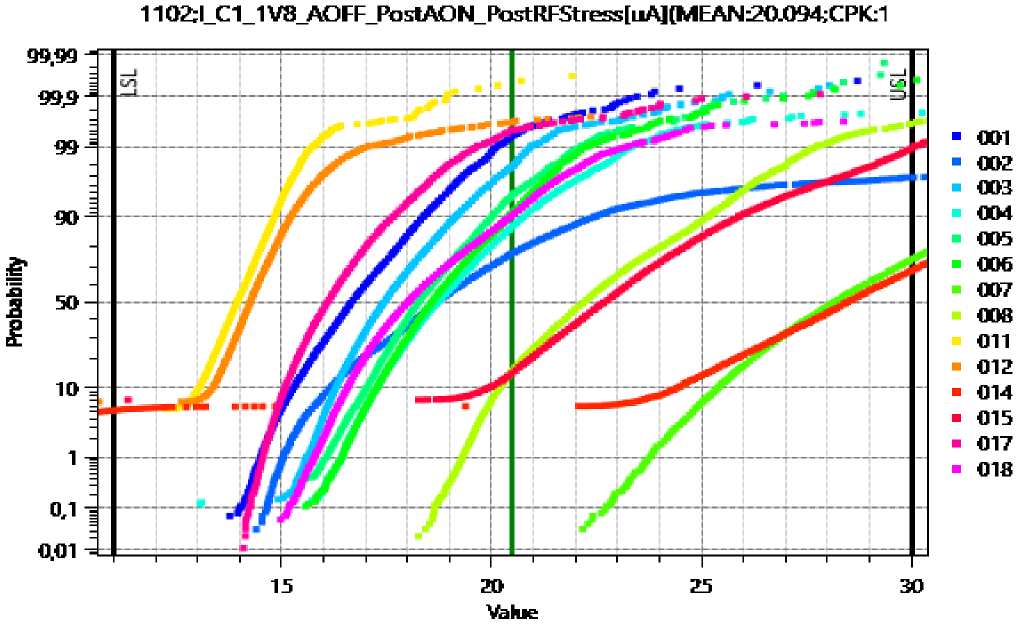


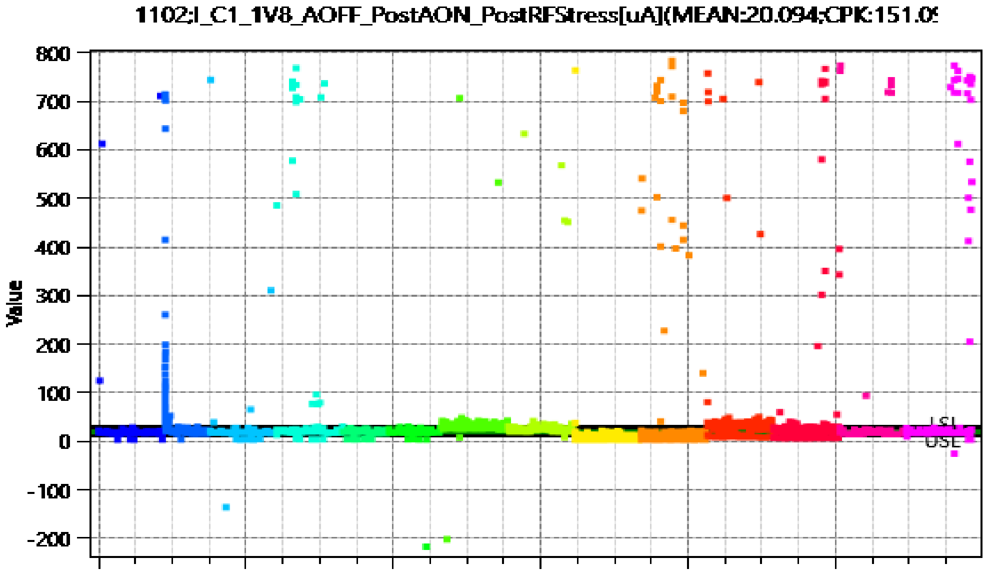


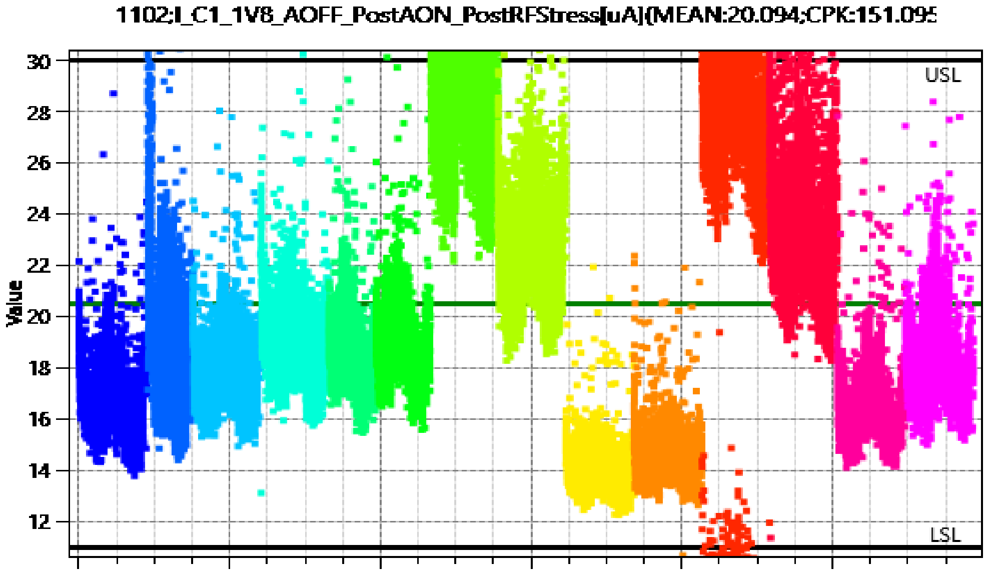


1102: I_C1_1V8_AOFF_PostAON_PostRFStress

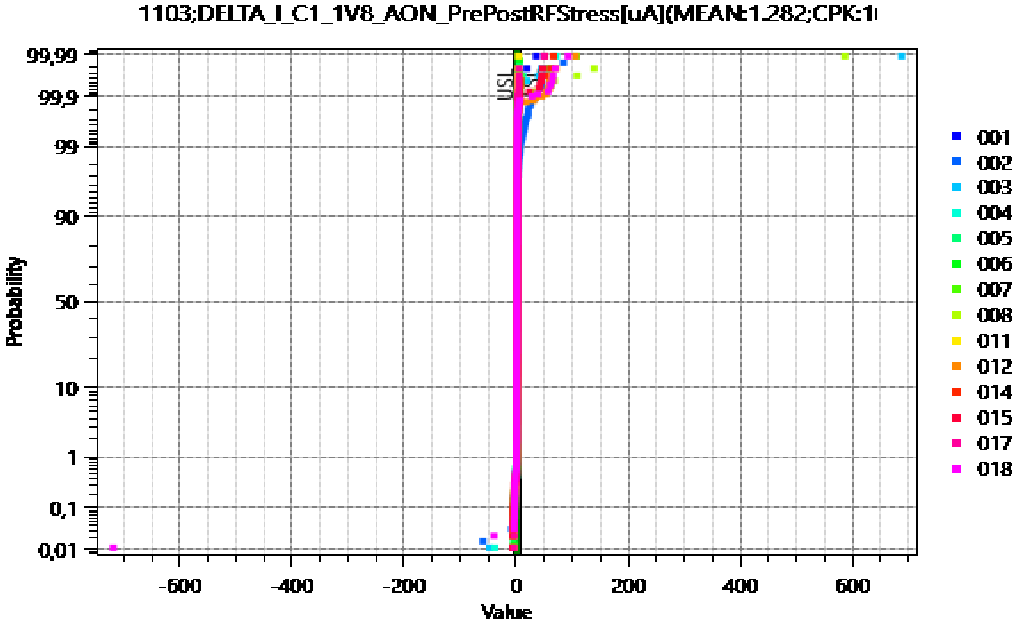


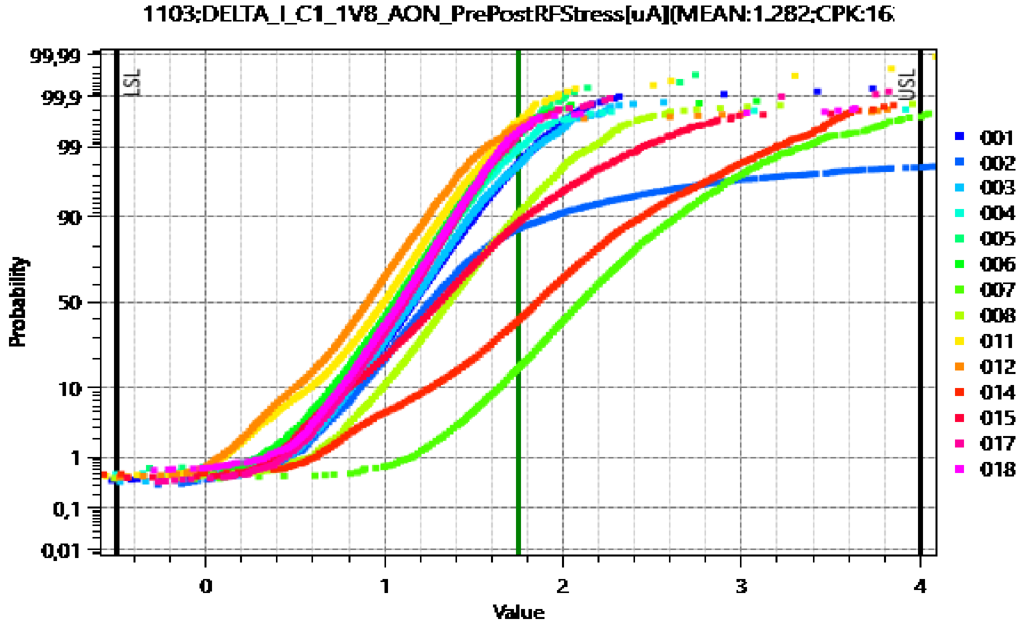


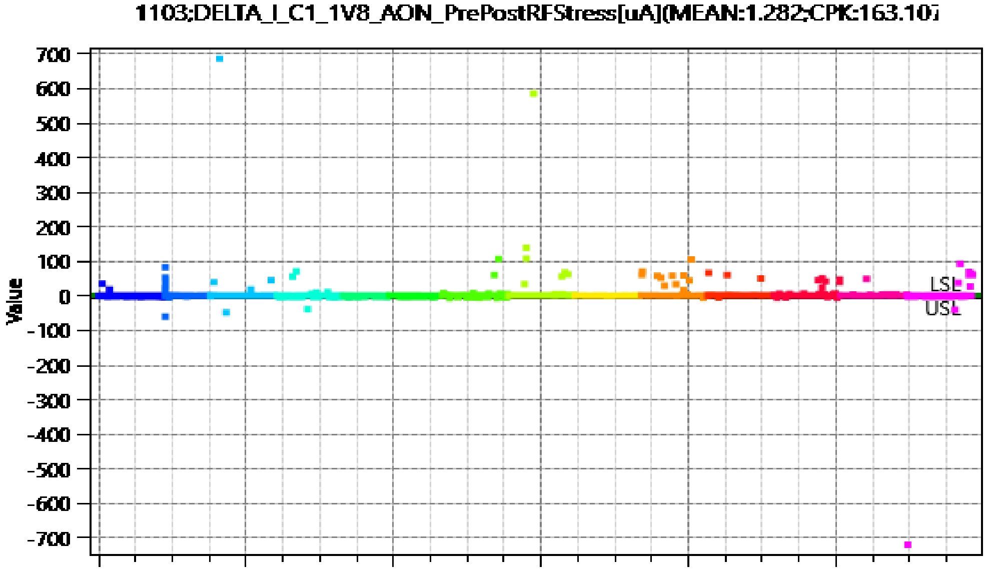


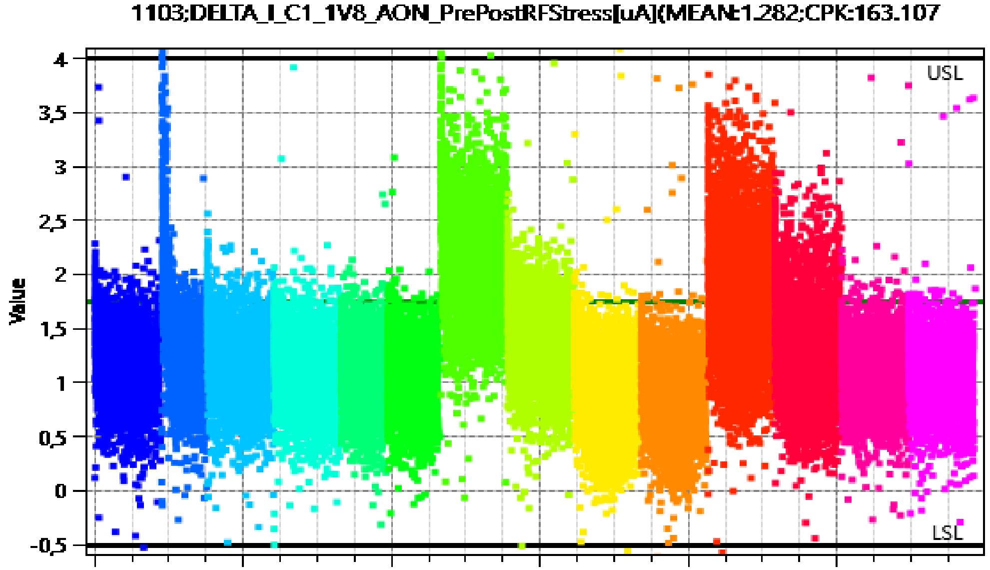


1103: DELTA_I_C1_1V8_AON_PrePostRFStress

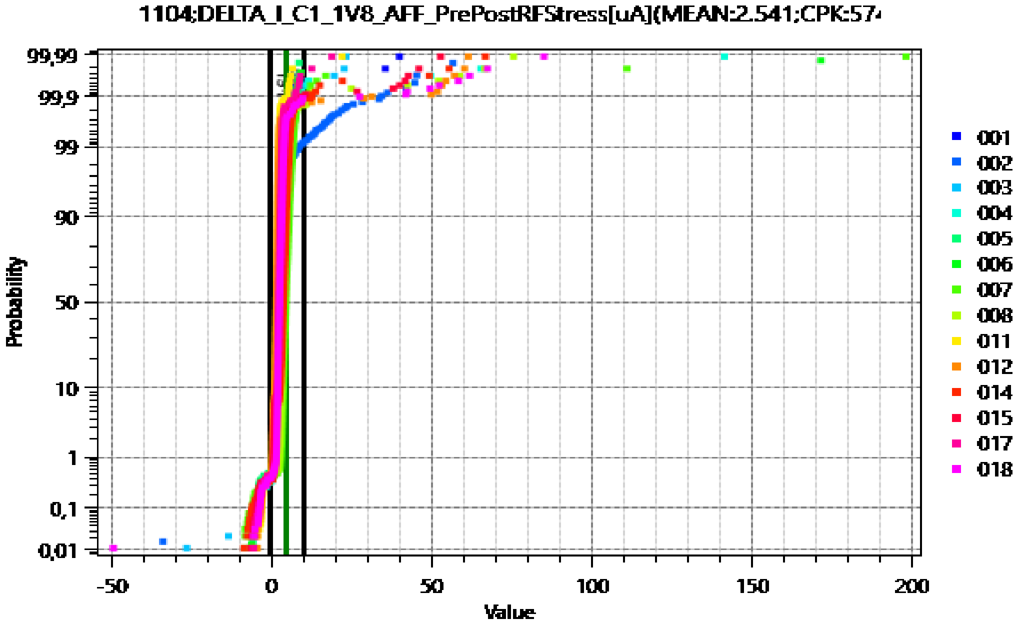


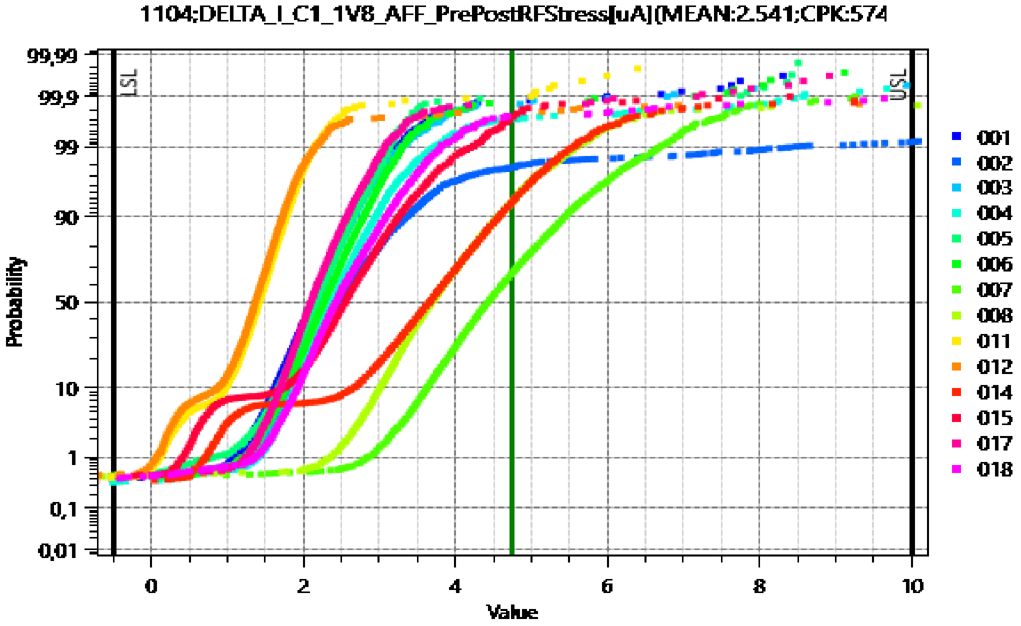


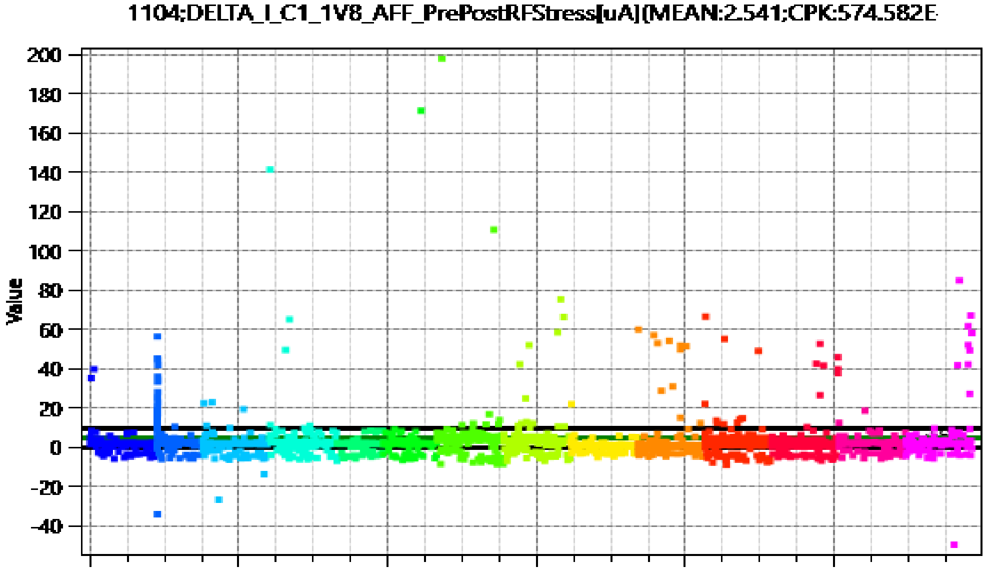


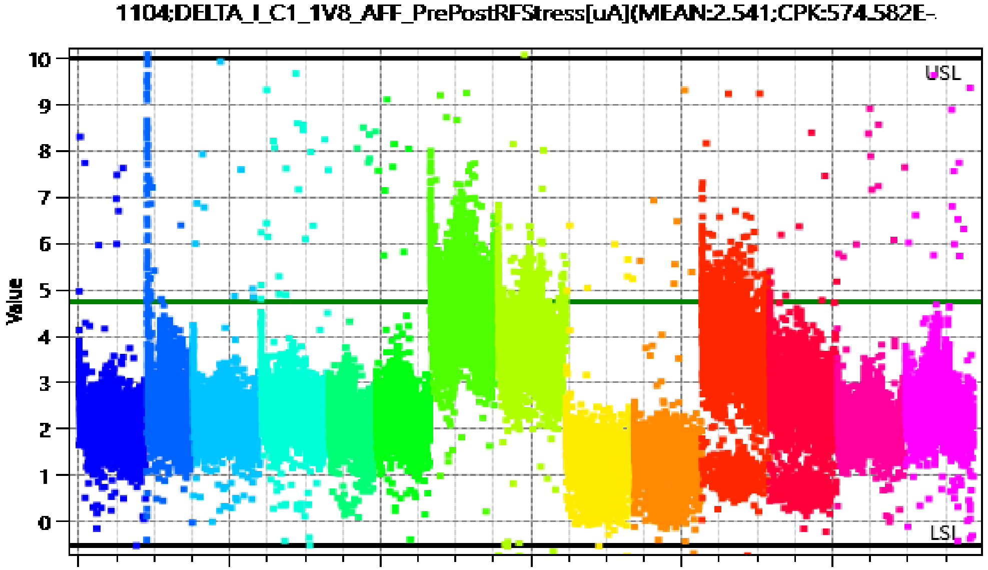


1104: DELTA_I_C1_1V8_AFF_PrePostRFStress









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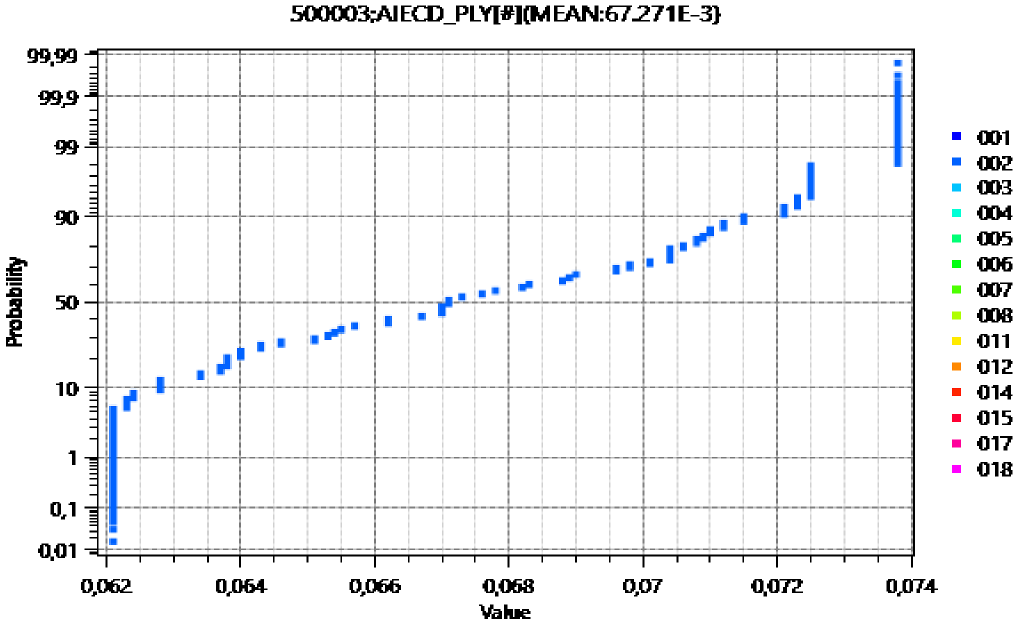
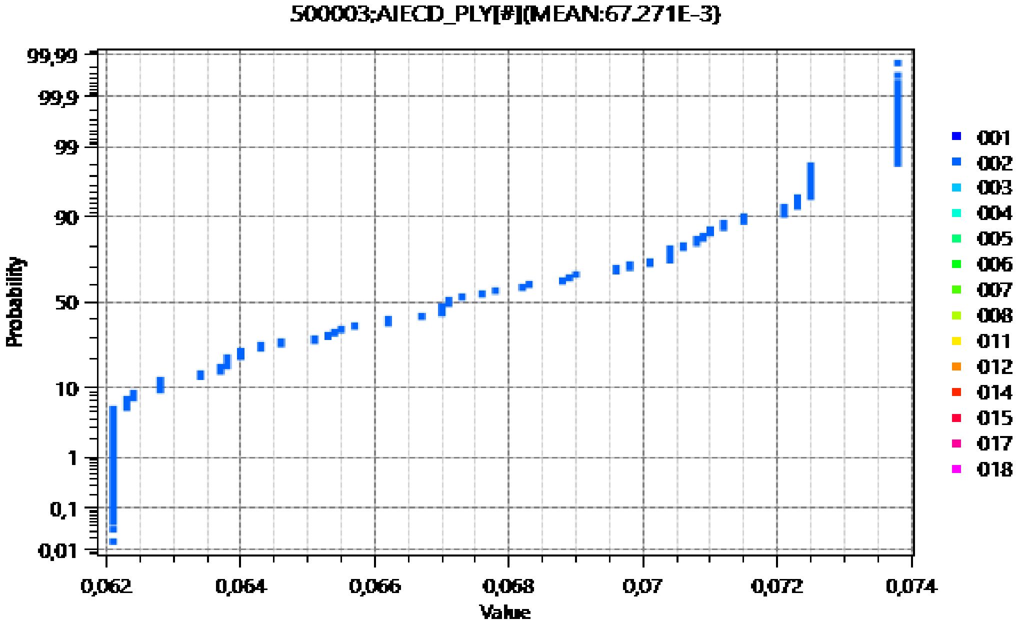
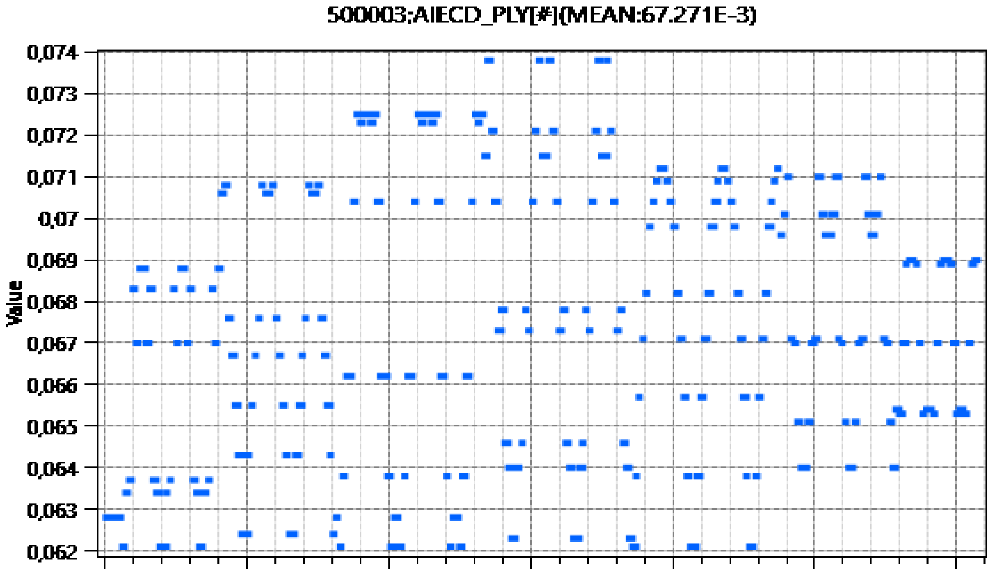
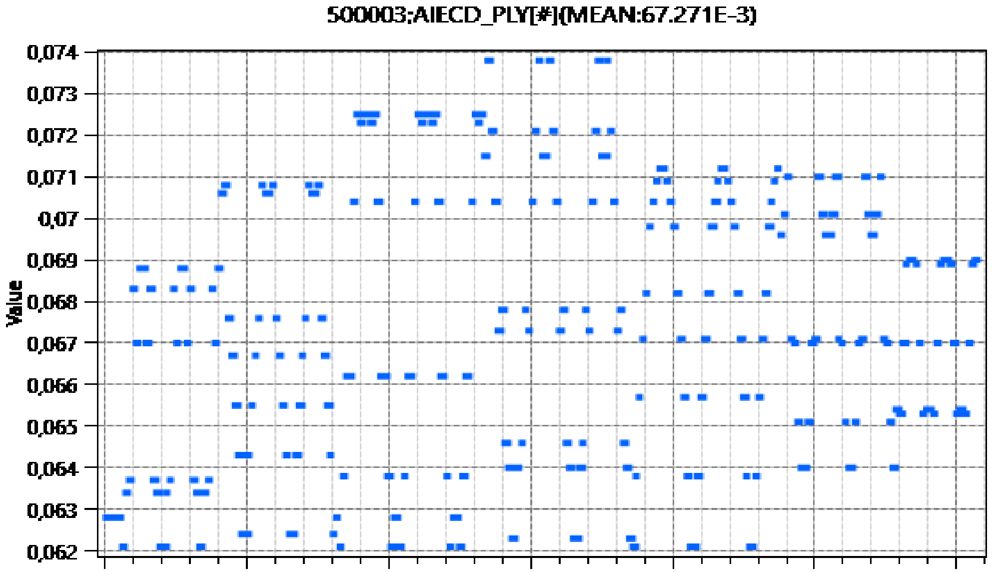
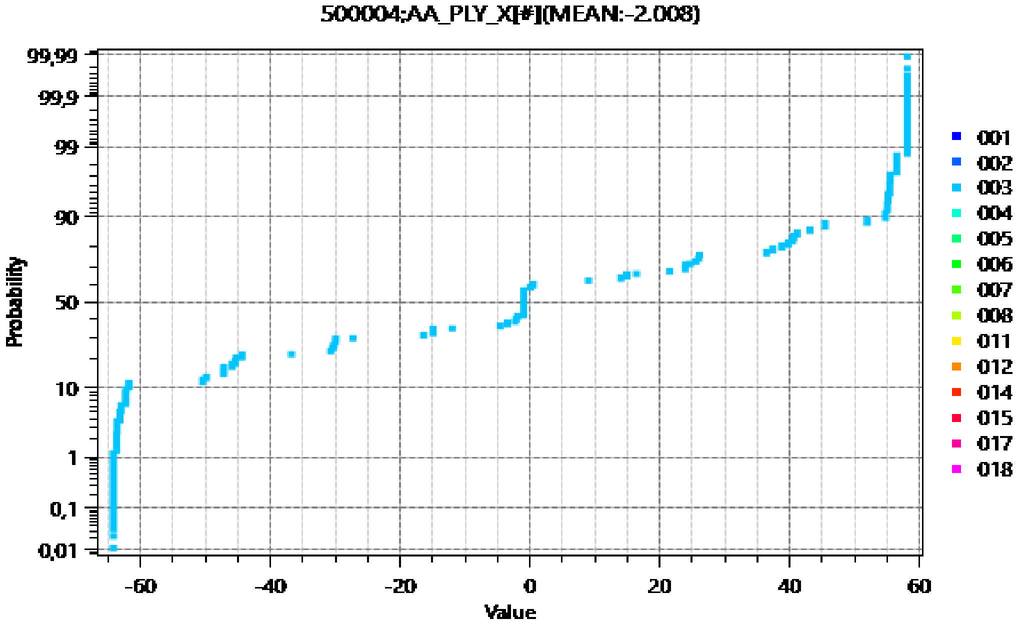


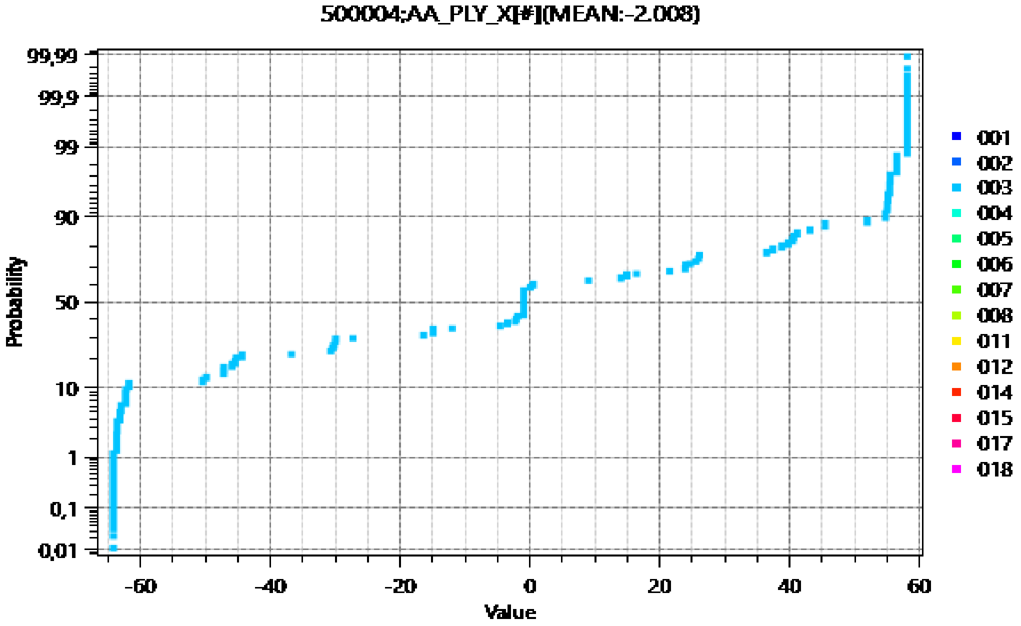


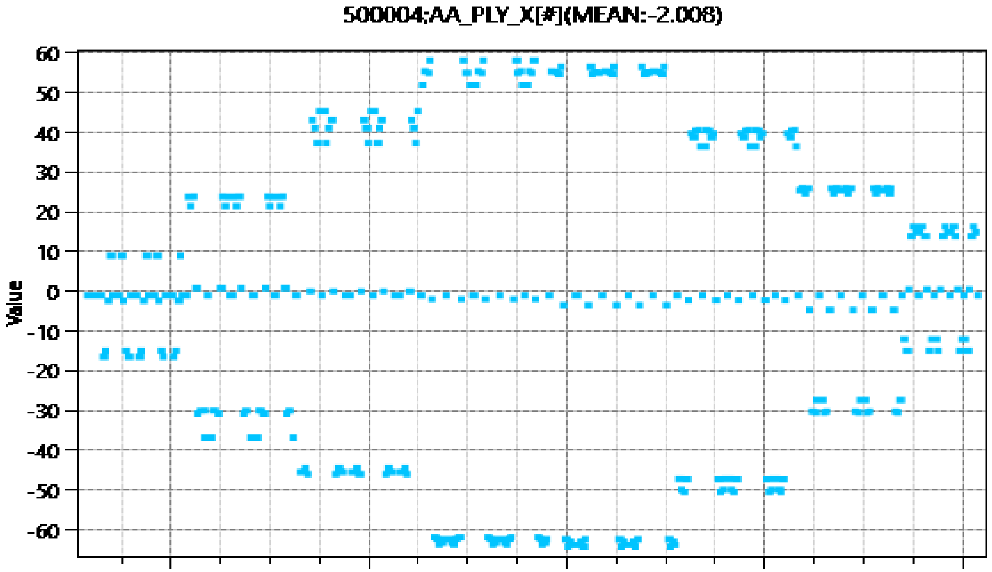


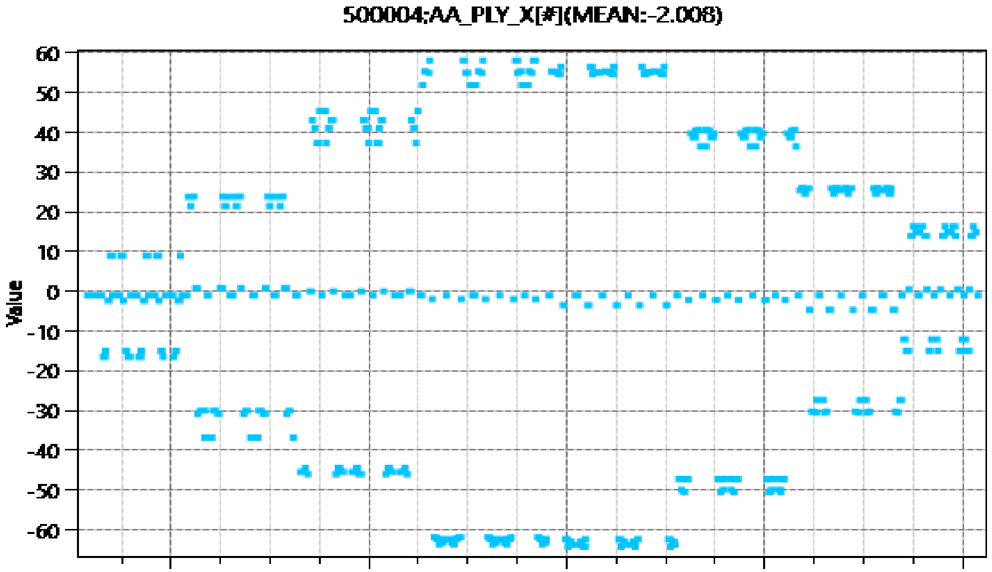


500004: AA_PLY_X

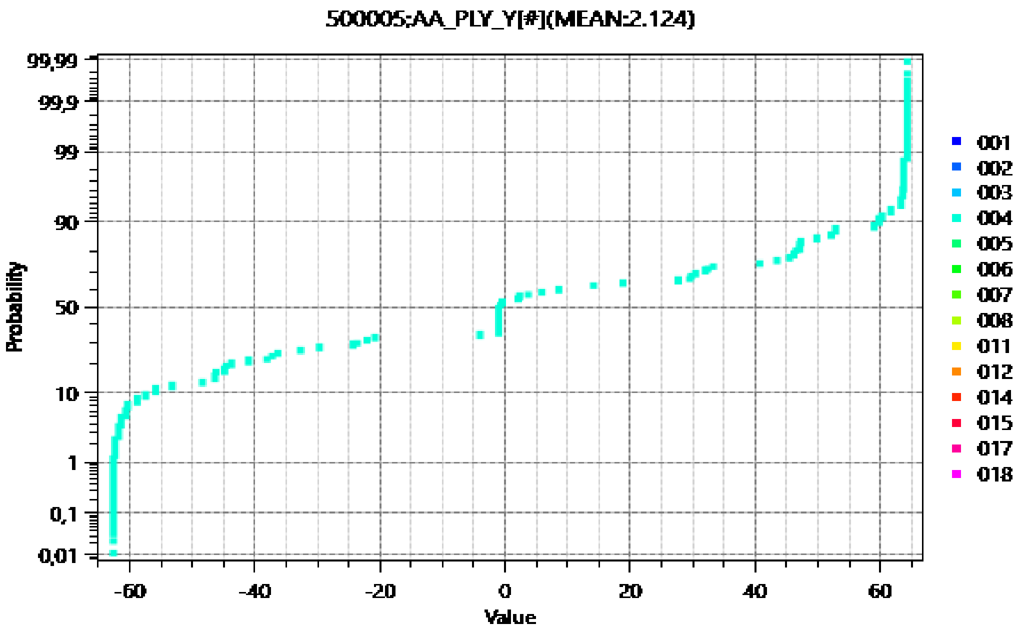


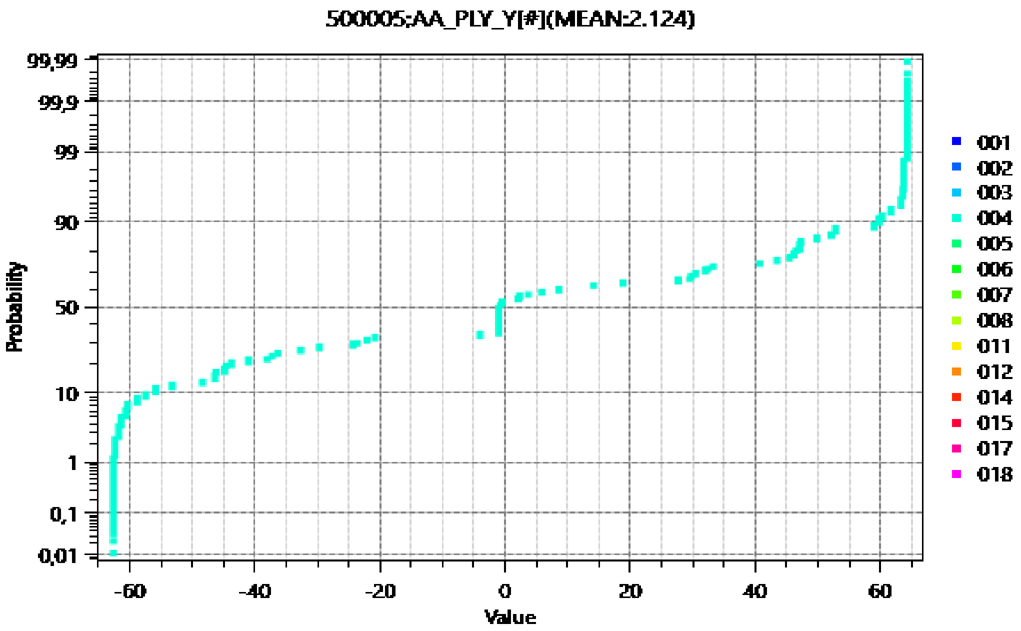


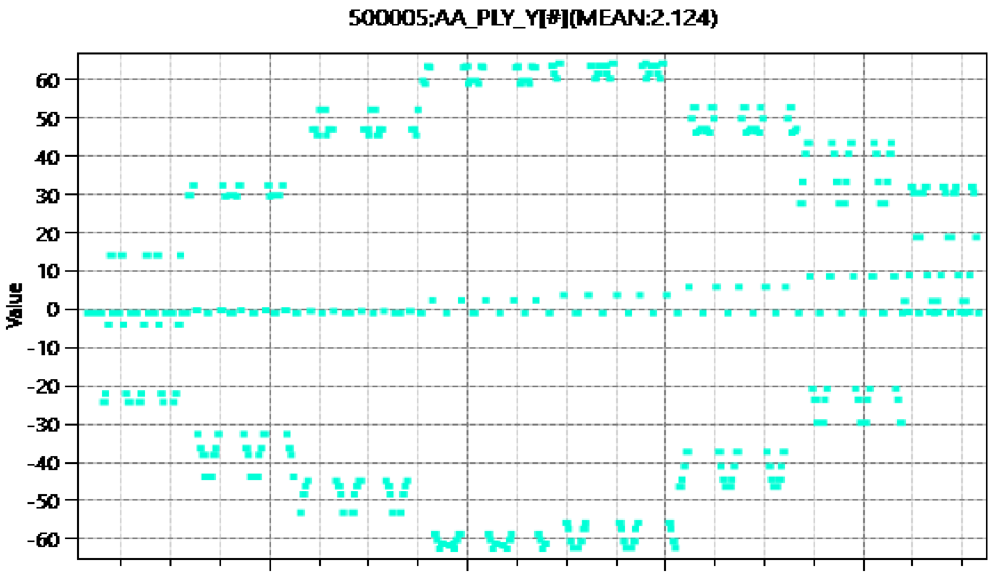


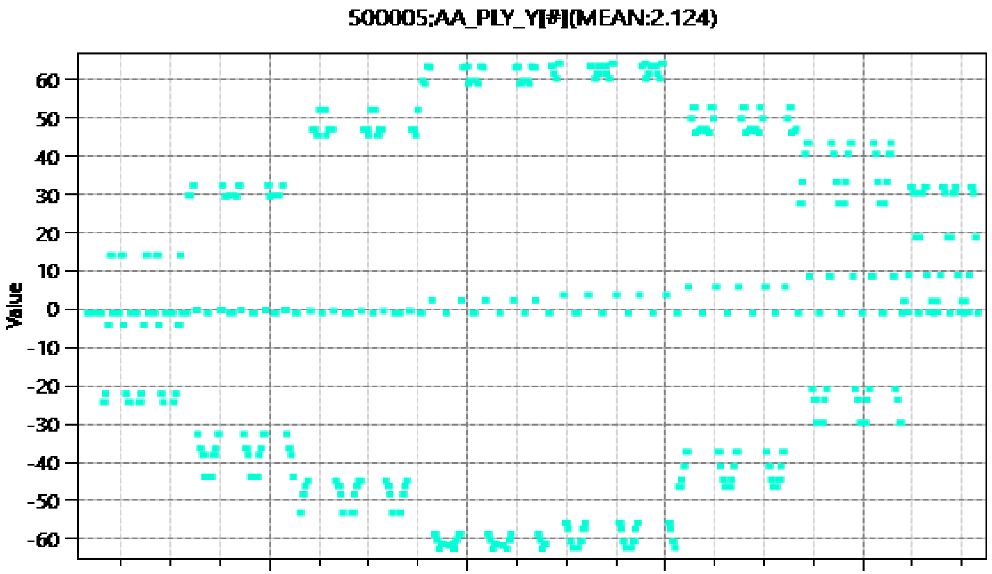


500005: AA_PLY_Y









500006: AEICD_CNT