3. (4 points)

Consider the instructions

```
320 LDUR X7, X3, #0
324 ADDI X5, X3, #8
328 ADD X3, X7, X5
```

Consider the situation when the `320 LDUR` instruction is in the WB stage, the `324 ADDI` instruction is in the MEM stage, and the `328 ADD` instruction is in the EX stage. In the figure below, for the current **two inputs to the ALU**, trace the buses back through the MUXes to the appropriate set of **pipeline registers** (i.e., trace paths from the ALU's input back to the pipeline registers where the appropriate operands are stored). You may use bold dark lines to clearly indicate your work.