5. (5 points) Datapath Timing

Consider the Single-cycle processor shown in the previous question. Suppose the circuit elements take the following times: Instruction memory: 200ps, Register read: 50ps, Register write: 50ps, ALU and all adders: 200ps, Data memory: 200ps, Main Control Unit: 15ps, ALU Ctrl 10ps, Sign Extend & Shift Left Units: 5ps each.
Assume that PC and MUXes do not take any time.

Compute the execution time for each instruction type below:

R-format:	515	ps.	Instruction Fetch + Register Read + Register write + ALU + Main Control + ALU Control
LDUR:	700	ps.	Instruction Fetch + Register Read + Register Write + ALU + Data Access + ?[Main control + ALU Control + Sign Extend]
STUR:	665	ps.	Instruction Fetch + Register Read + ALU + Data Access + Main ?[+ ALU Control + Sign Extend]
CBZ:	465	ps.	Instruction Fetch + Register Read + ALU Main Control + ?[ALU Control + Sign Extend + Shift Left]
B:	425	ps.	Instruction Fetch + Main Control + Alu Control + ALU