4. (8 points) Consider the following ARM code sequence where RAM at address 16 stores the value 2.

```
100     ADDI X1, XZR, #16
104     LDUR X2, [X1, #0]
108     ADDI X3, X1, #8
112     CBNZ X2, #-2
116     SUBI X1, X1, #8
```

Assume this code sequence is run on a datapath with branch in the ID-stage, with **data forwarding** (to both the EX stage and the '=0' unit in the ID stage), **load-use stalling**, and **branch-data stalling**. In the figure below, to the left of each row in the figure below, write the instruction that is executed in that row. If an instruction is stalled, write the instruction that is stalled and then write "STALLED" below that. If an instruction is flushed, write the name of the instruction and then write "FLUSHED" below that.

Also draw where the forwarding occurs (similar to Figure 4.52 of the textbook, on page 119 (6-15) of the course notes, and slide 6-28) in the execution of these instructions. Your arc must clearly go to the ALU input (Rn or Rm) that requires forwarding (Rn is the top input to the ALU; Rm is the bottom input).

The execution of these instructions (including stalls and flushing) may require more rows than provided. If so, just show the first six rows.