2. (10 points)

This question refers to the pipelined datapath without forwarding, shown below.

Consider the instructions

```
100 ADDI X1, X31,#1    ; WB stage
104 CBZ  X2, #20       ; MEM stage
108 LDUR X1,[X4, #20]  ; EX stage
112 AND  X6, X4, X3    ; ID stage
```

The instructions are executing in the stages indicated in the comments and in the figure below.

In the figure below, label all of the *control signals* (including both those coming directly out of the control unit and those coming out of the pipeline registers) with their appropriate values, using don't cares where appropriate.

In this figure, the instructions have been drawn above the appropriate set of pipeline registers. We have also filled in the solution for the WB stage, and given the names of the control signals whose values you need to determine for the other three stages.

MemToReg= 0   RegWrite= 1   MemToReg= 1   RegWrite= 1   MemtoReg= X   RegWrite= 1
Branch= 0   MemRead= 0   Branch= 0   MemRead= 1   RegWrite= 0   MemToReg= 0
MemWrite= 0   MemWrite= 0   Branch= 1
Reg2Loc= 0   ALUOp= 00   MemRead= 0
ALUOp= 10   ALUSrc= 1   MemWrite= 0
ALUSrc= 0

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