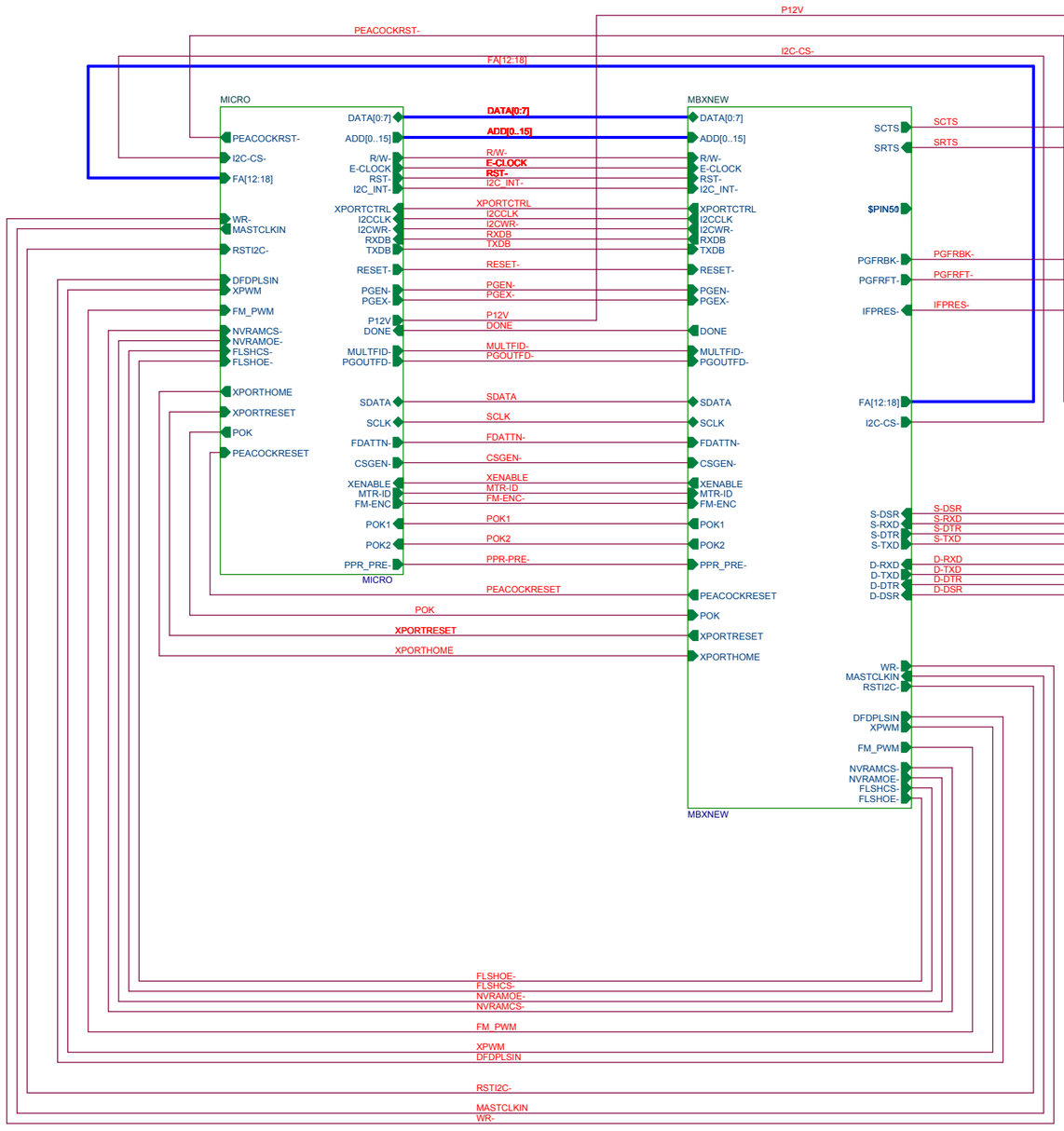
REV	ECN Number	DESCRIPTION	DATE	BY
1		PROTOTYPE VERSION	08/27/03	RBT
A	041680615	Production Release	06/15/04	RBT
C	041680645	Production Release	11/01/04	RBT
D	1022	Modifications for NVRAM Corruptions	05/18/05	RBT



NOTES FOR PCB LAYOUT

1. Place CIN and COUT as close to the MAX1818 as possible.

2. Place all the Decoupling/Bypass capacitors as close to the device VCC pins as possible.

3. Do not place high speed signal traces near the edge of PCB.

4. For Clock Traces: A minimum of 2 equally spaced traces in parallel with clock traces.

5. Avoid 90 deg. corners for trace paths (use 45 deg. stepped corners).

6. Ground trace on the perimeter of the board on both sides of the board grounded together in many places and mounting holes to be plated on the top for chassis grounding.

7. CURRENT TABLE

5V	5A
24V	1A
+12V	3A
-12V	0.5A

8. Place all the Decoupling/Bypass capacitors as close to the FPGA as possible and around the periphery of the FPGA.
(Similar to Previous layout).

9. Follow Spartan II FPGA datasheet for Layout guidlines.

BELL+HOWELL

SCANNER DIVISION

Title: TOP LEVEL HIERARCHY, MOTHERBOARD - SPECTRUM II

Size	Document Number	Rev
C	S005332	D

Date: Thursday, May 26, 2005 Sheet 1 of 5