a simple CMOS beta multiplier 1uA current source

- design review -

Rod Burt, Aug 8, 2024

design goals

- i_out = 1uA
- minimize i_out variations
    - PVT variations
        - Process corners ss, sf, ff, and fs
        - supply Voltage from 1.7V to 1.9V
        - Temperature from -40°C to 125°C
    - device mismatch
- minimize layout area

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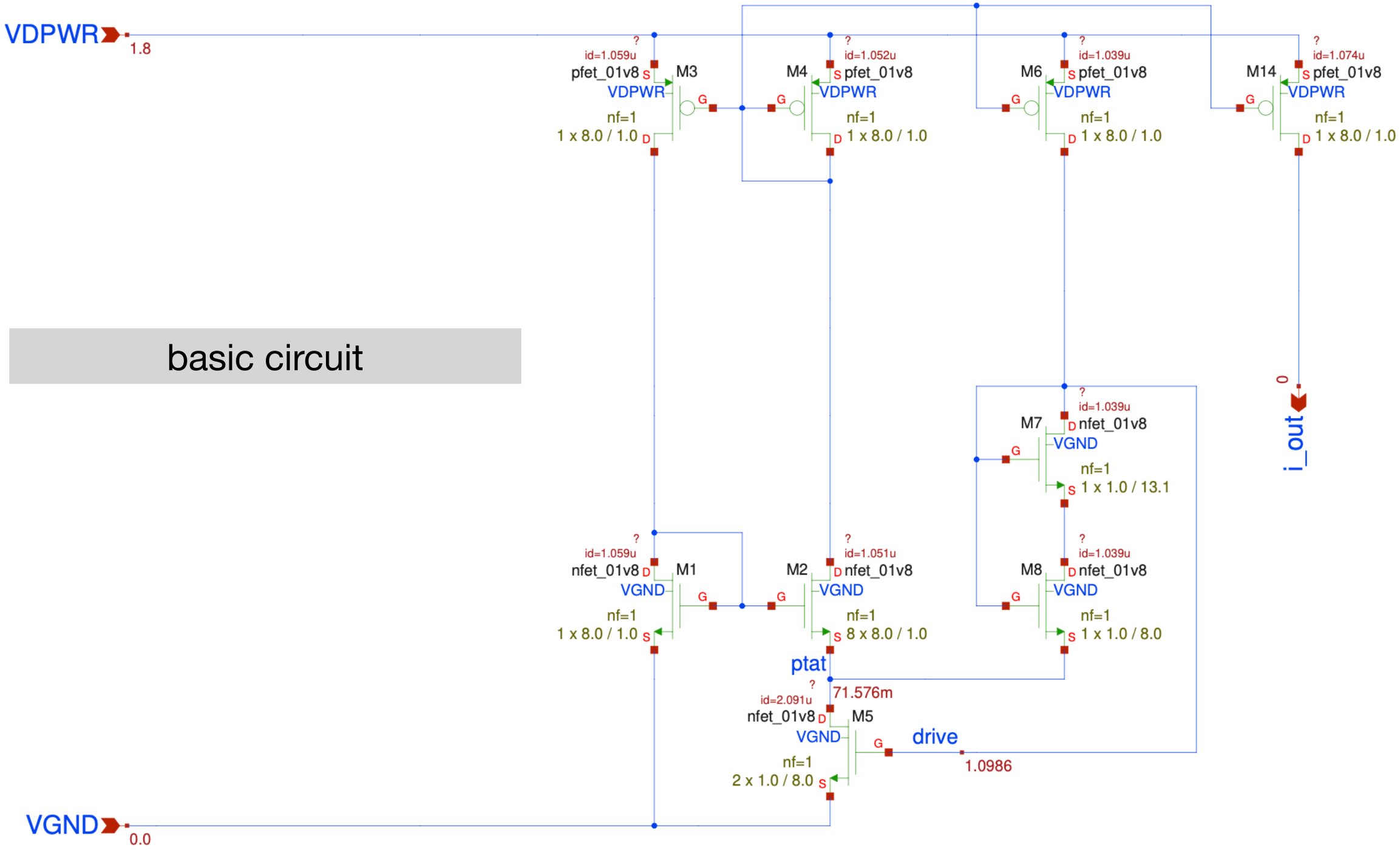
basic circuit



1st order analysis

PMOS devices M3, M4, M6, and M14 form a mirror setting all drain currents to i

NMOS devices M1 and M2 operate in subthreshold and form a beta multiplier setting Vptat = Vgs1 - Vgs2 ≈ nVtln(W/L ratio of M2/M1), for a W/L ratio of M2/M1 = 8

$$Vptat \approx n\frac{kT}{q}ln(8)$$

Vdrive = Vptat + Vgs7,8 (composite device formed by M7 and M8)

$$Vdrive \approx Vptat + Vth + \sqrt{\frac{2i}{uCox\frac{W_{7,8}}{L_{7,8}}}}$$

NMOS device M5 operates in the triode region functioning as a resistor, thus

$$id5 \approx uCox\frac{W_5}{L_5}(Vdrive - Vth - \frac{Vptat}{2})Vptat$$

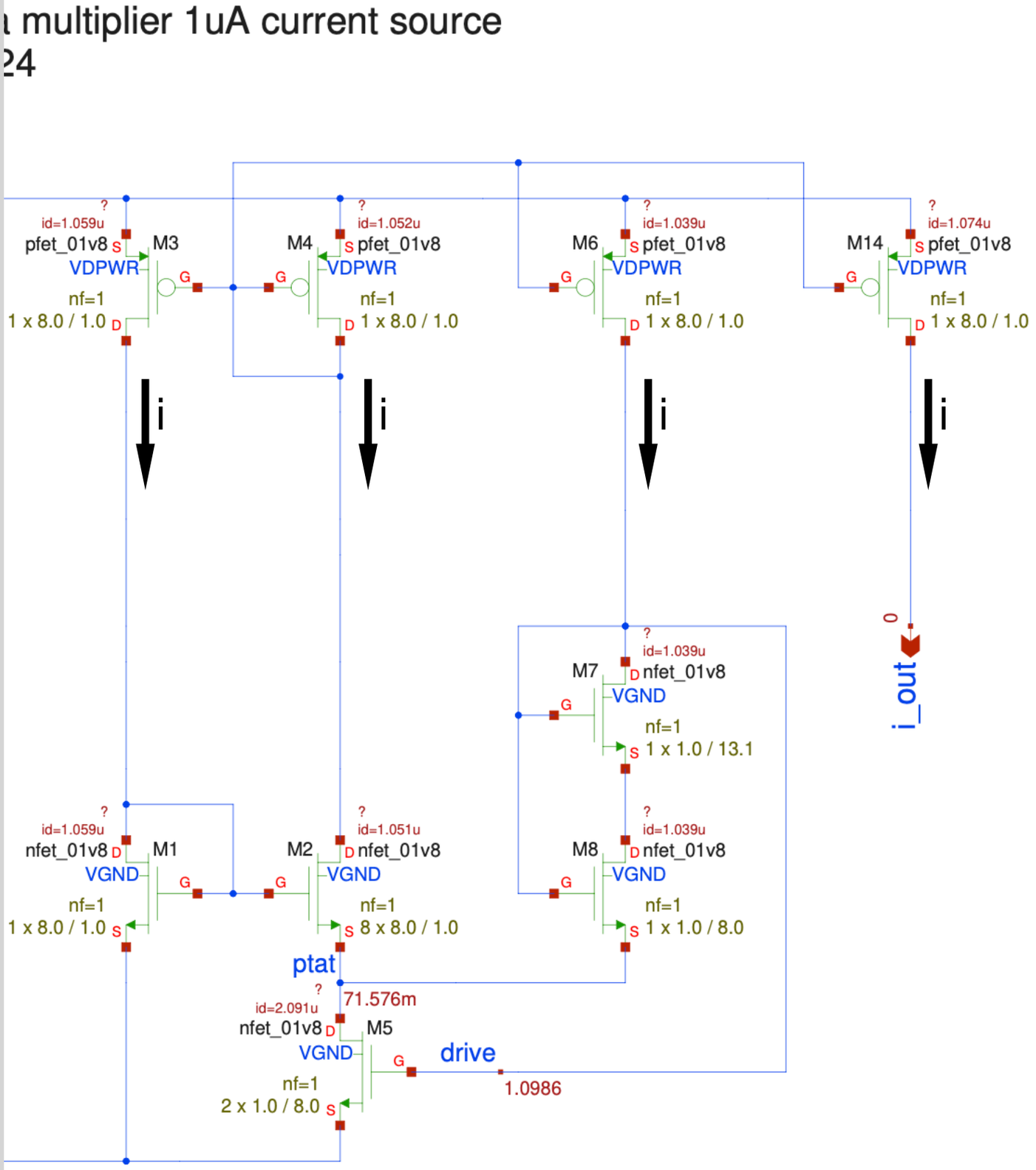
assuming

$$Vgs_{7,8} >> \frac{Vptat}{2}$$

then

$$id5 \approx uCox(\frac{W_5}{L_5})^2(\frac{W_{7,8}}{L_{7,8}})(n\frac{kT}{q}ln(8))^2$$

$$i \approx \frac{id5}{2}$$



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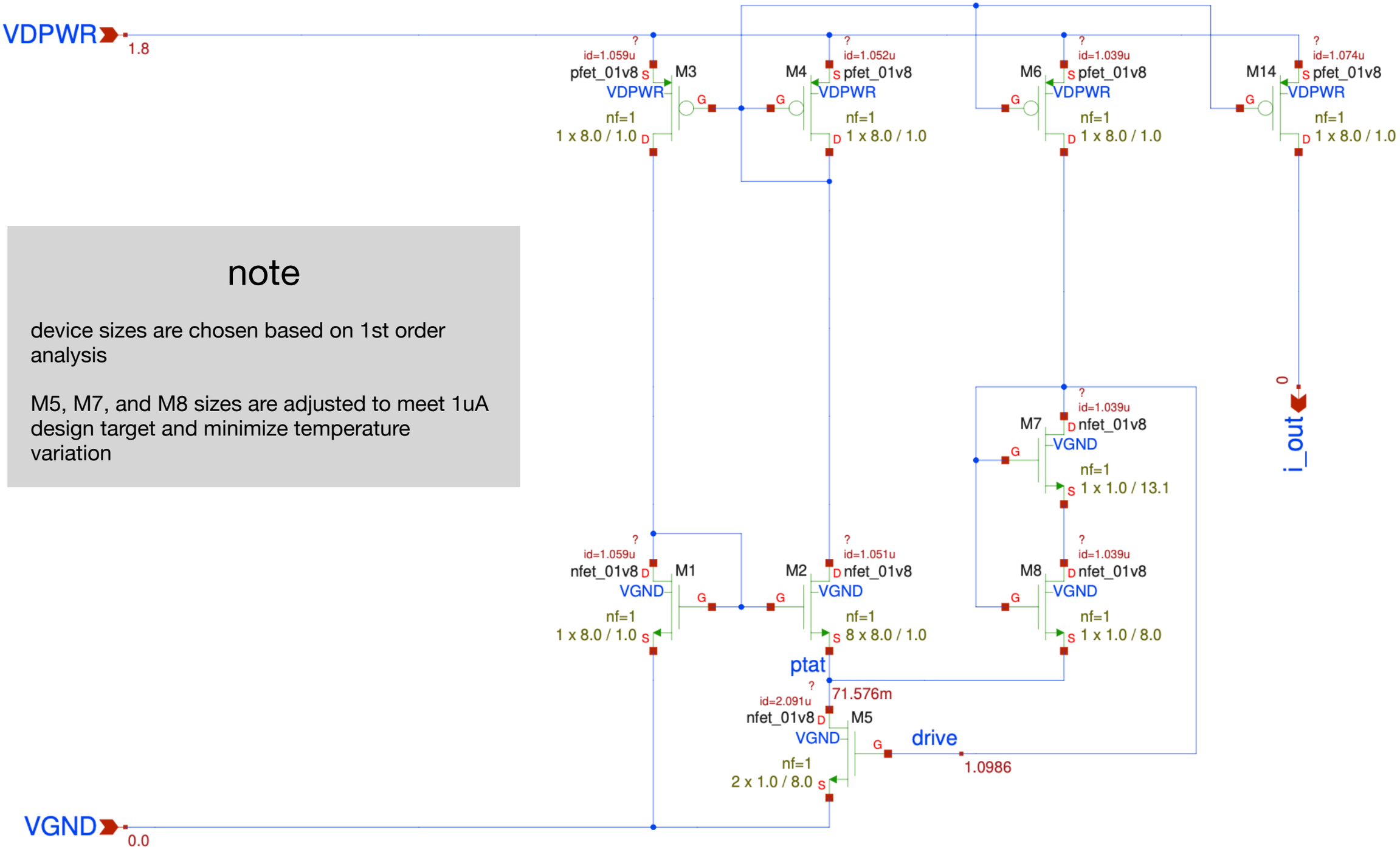
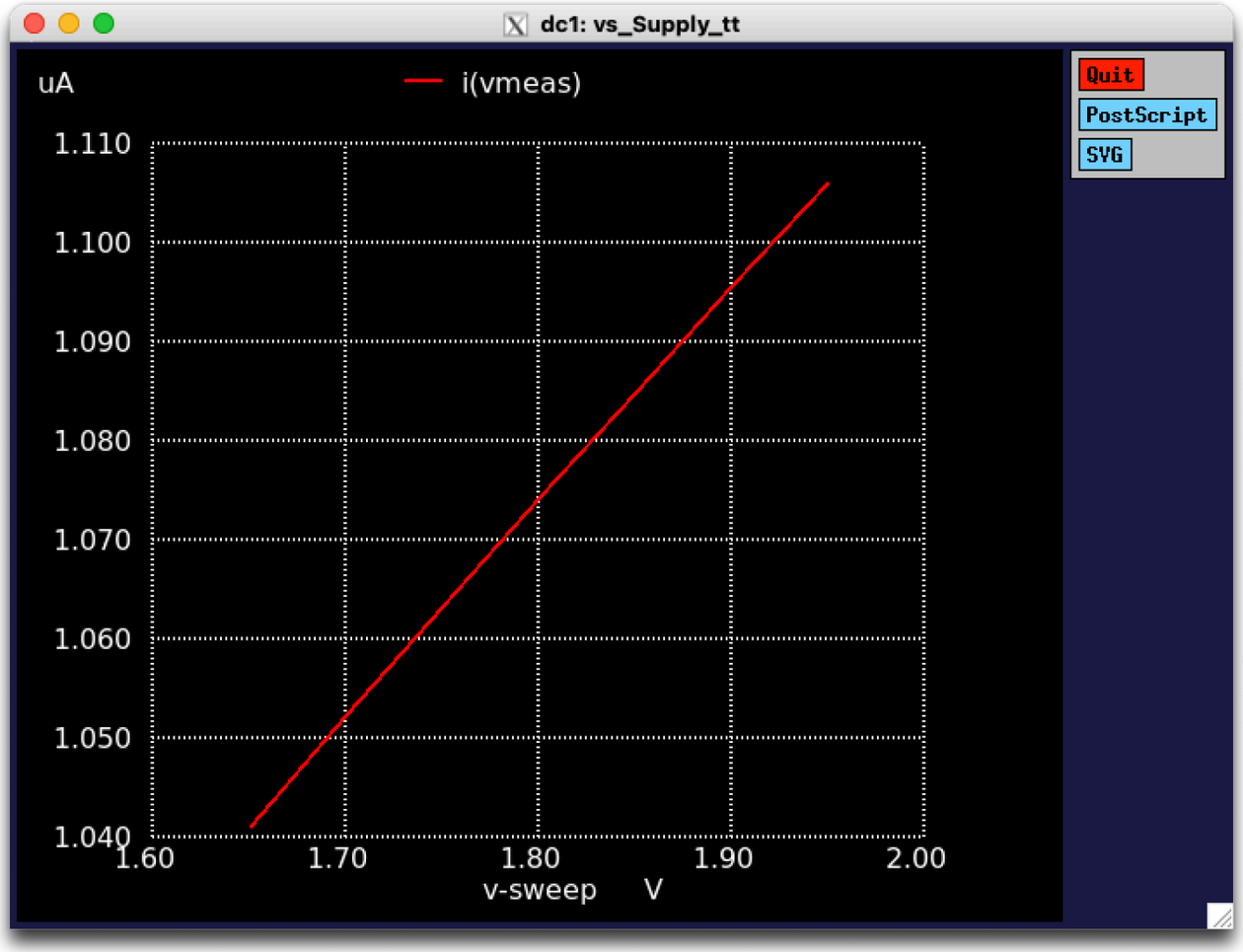


note

device sizes are chosen based on 1st order analysis

M5, M7, and M8 sizes are adjusted to meet 1uA design target and minimize temperature variation

simulation of basic circuit



supply Voltage from 1.7V to 1.9V
i_out variation ≈ +/- 2%

let’s minimize this before we move on to other sims!

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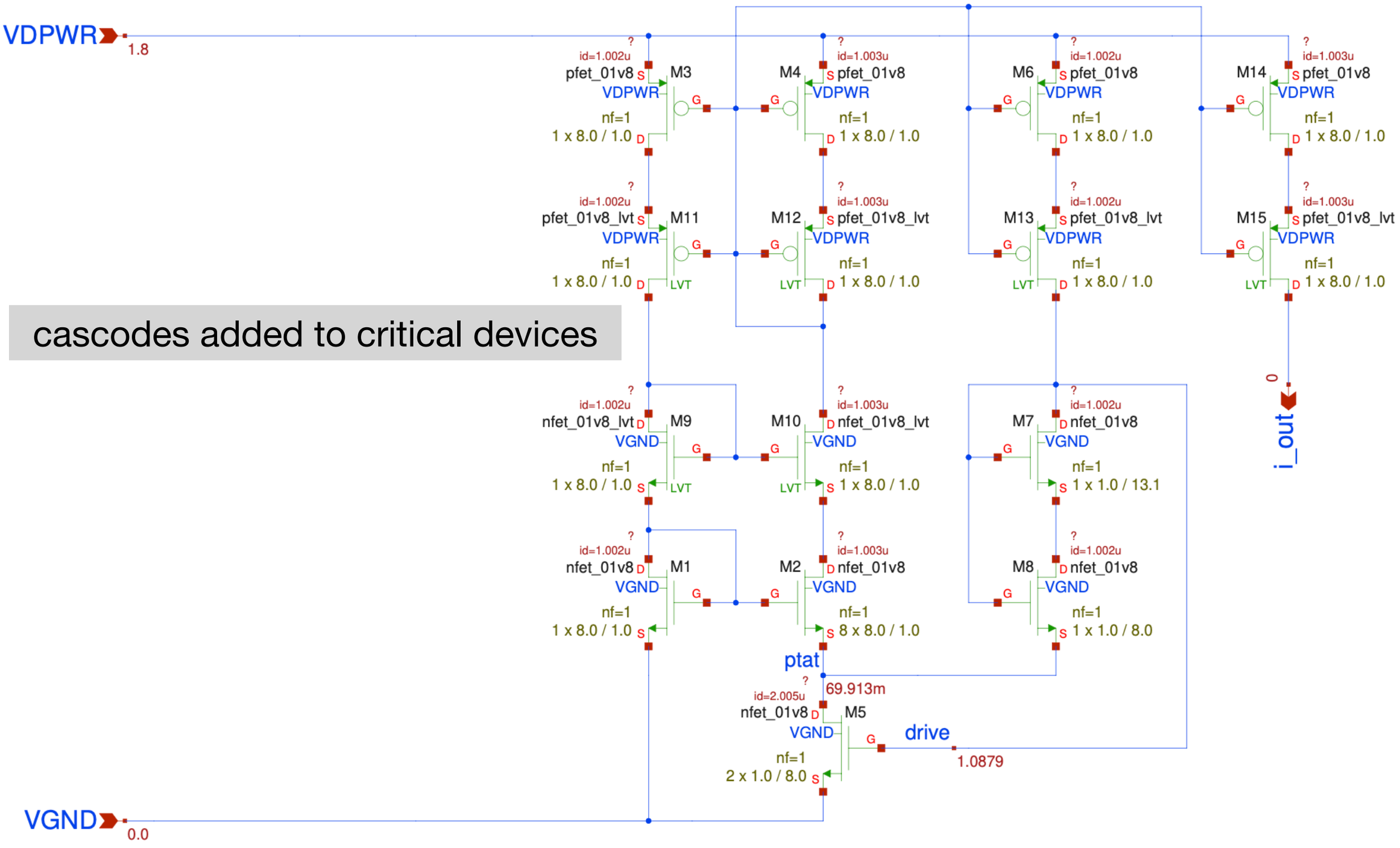
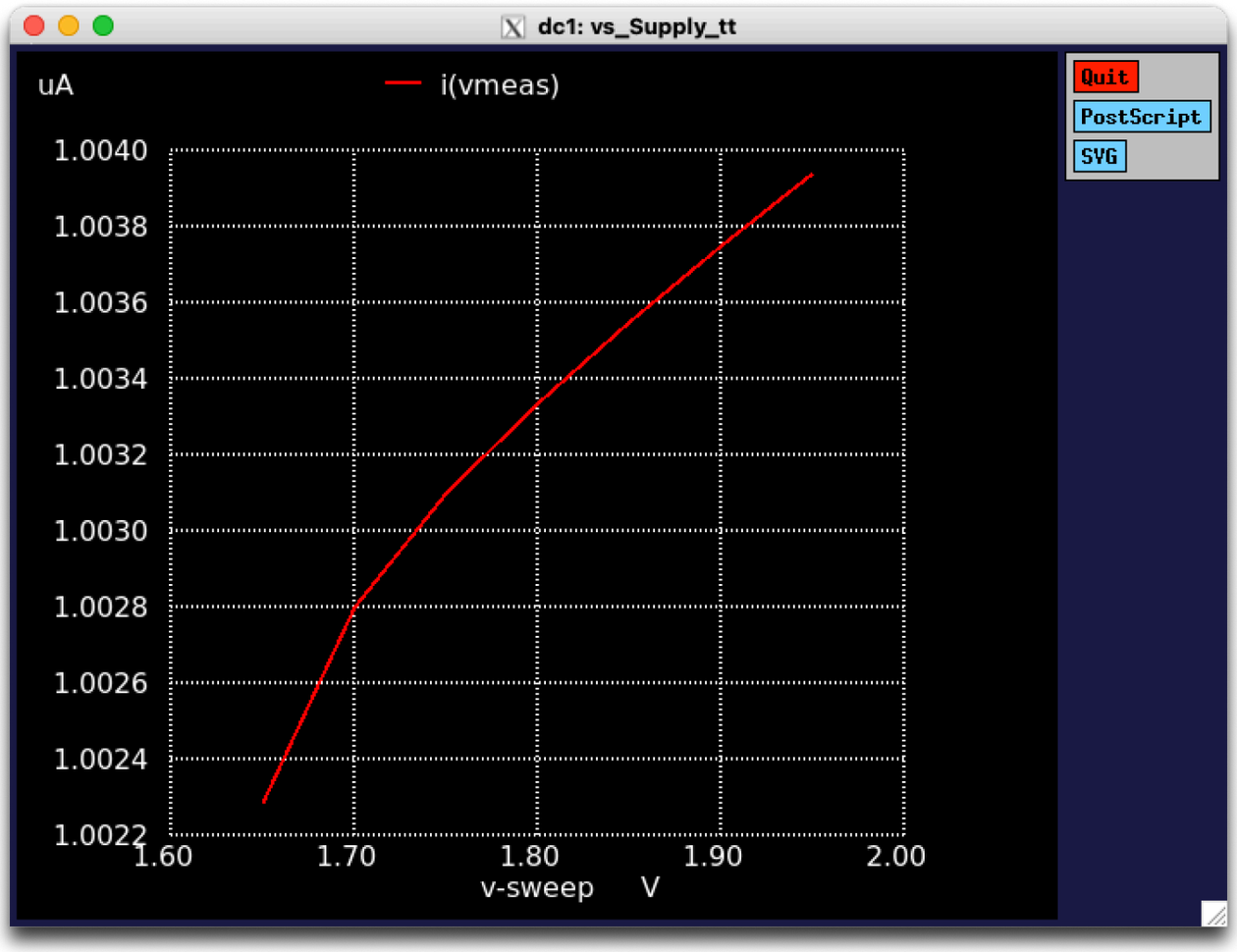


cascodes added to critical devices

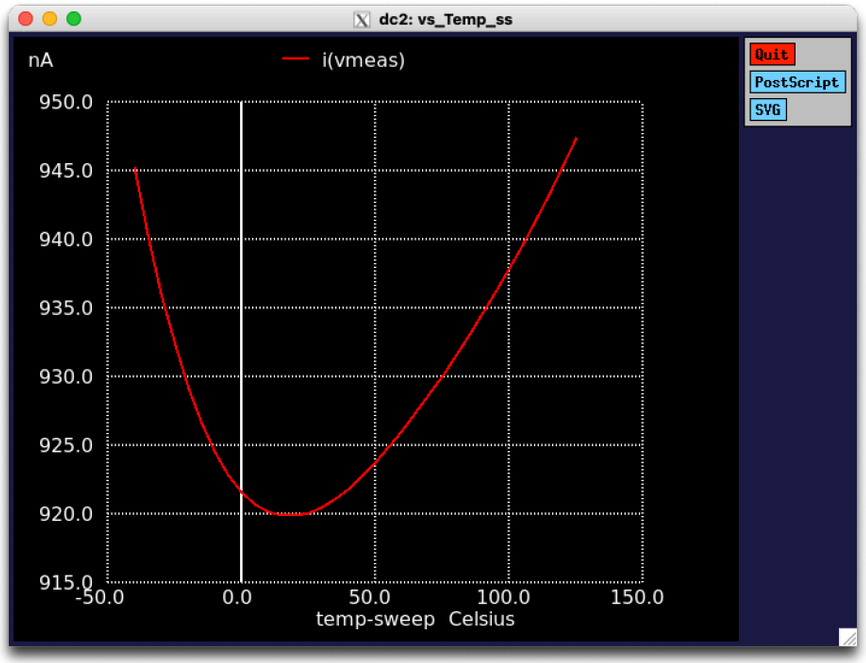
simulation of circuit with cascodes

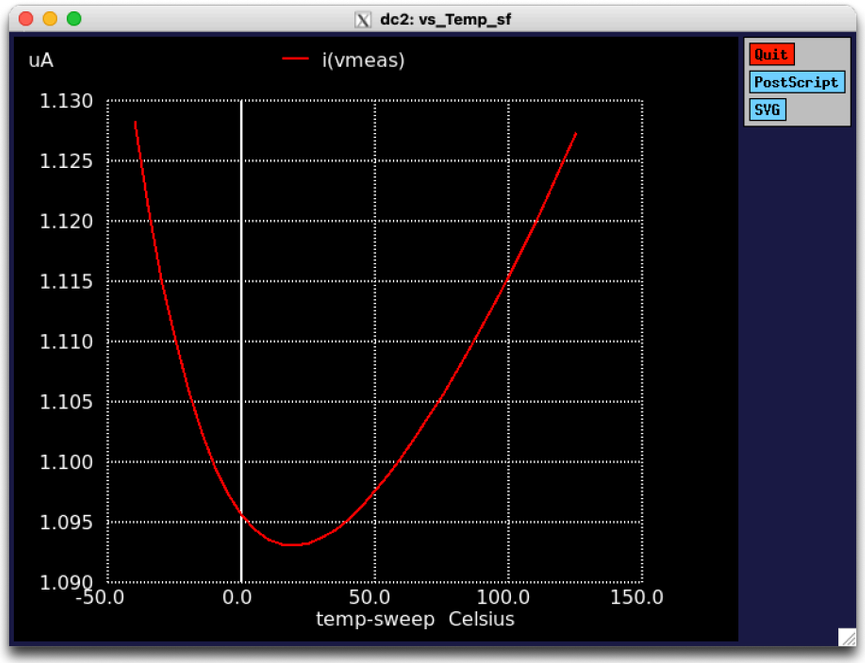


supply Voltage from 1.7V to 1.9V

i_out variation ≈ +/- 0.5%

simulation of circuit with cascodes





Temperature from -40°C to 125°C and Process corners ss, sf, ff, and fs

i_out variation ≈ +/- 10%

final considerations

- Start up

  This circuit may have another valid operating point with all currents = 0. A start up circuit needs to be added to inject a small current to move the circuit into the desired state and then shut off the injected current so as not to add errors in normal operation.

- Stability

  Any feedback loop has the potential to oscillate. This circuit has 2 loops involving the ptat and drive generation. To check for the potential of instability inject a small current pulse into the loops (the ptat node is ideal since it is part of both loops) and look for the level of ringing in the response.

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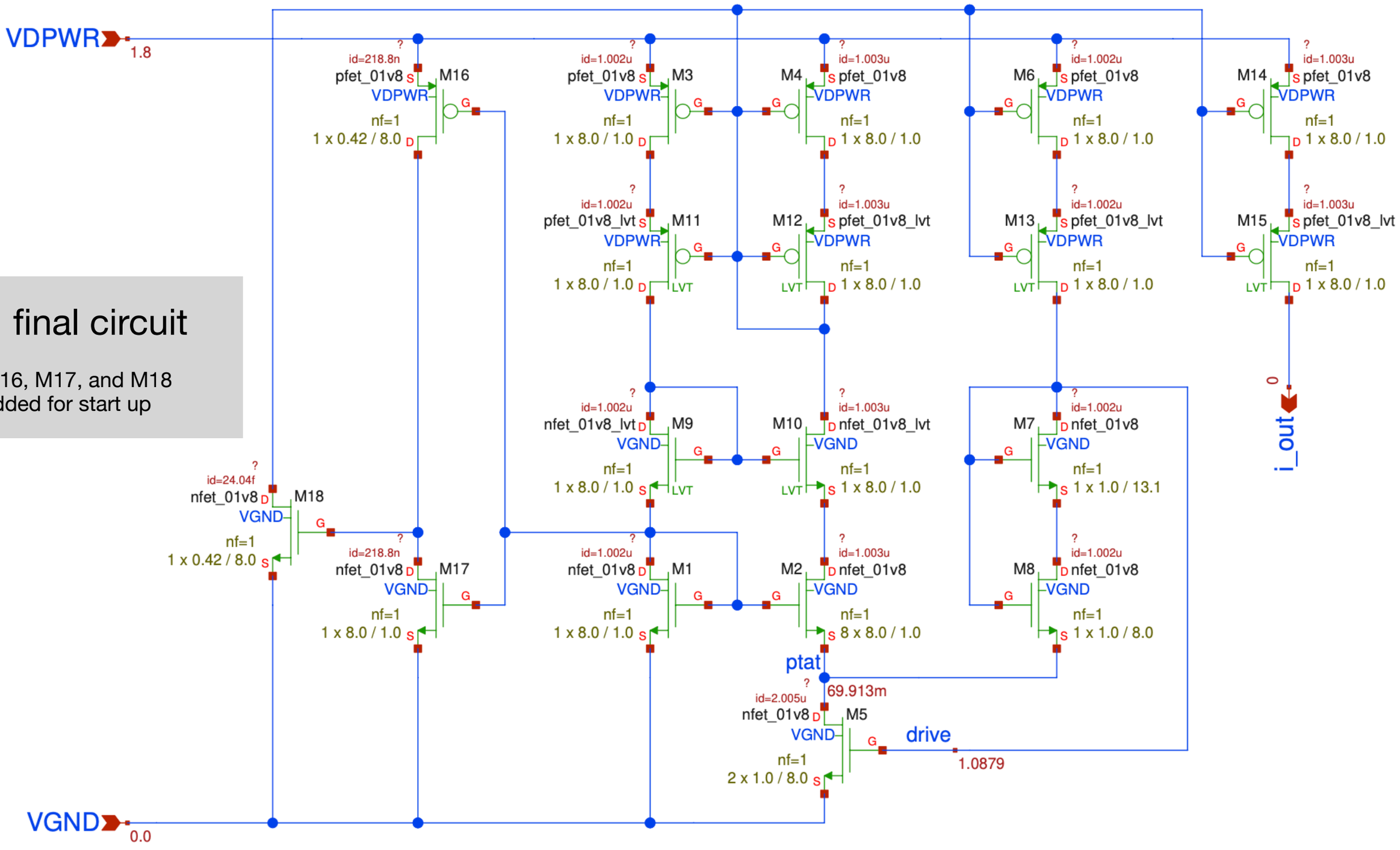
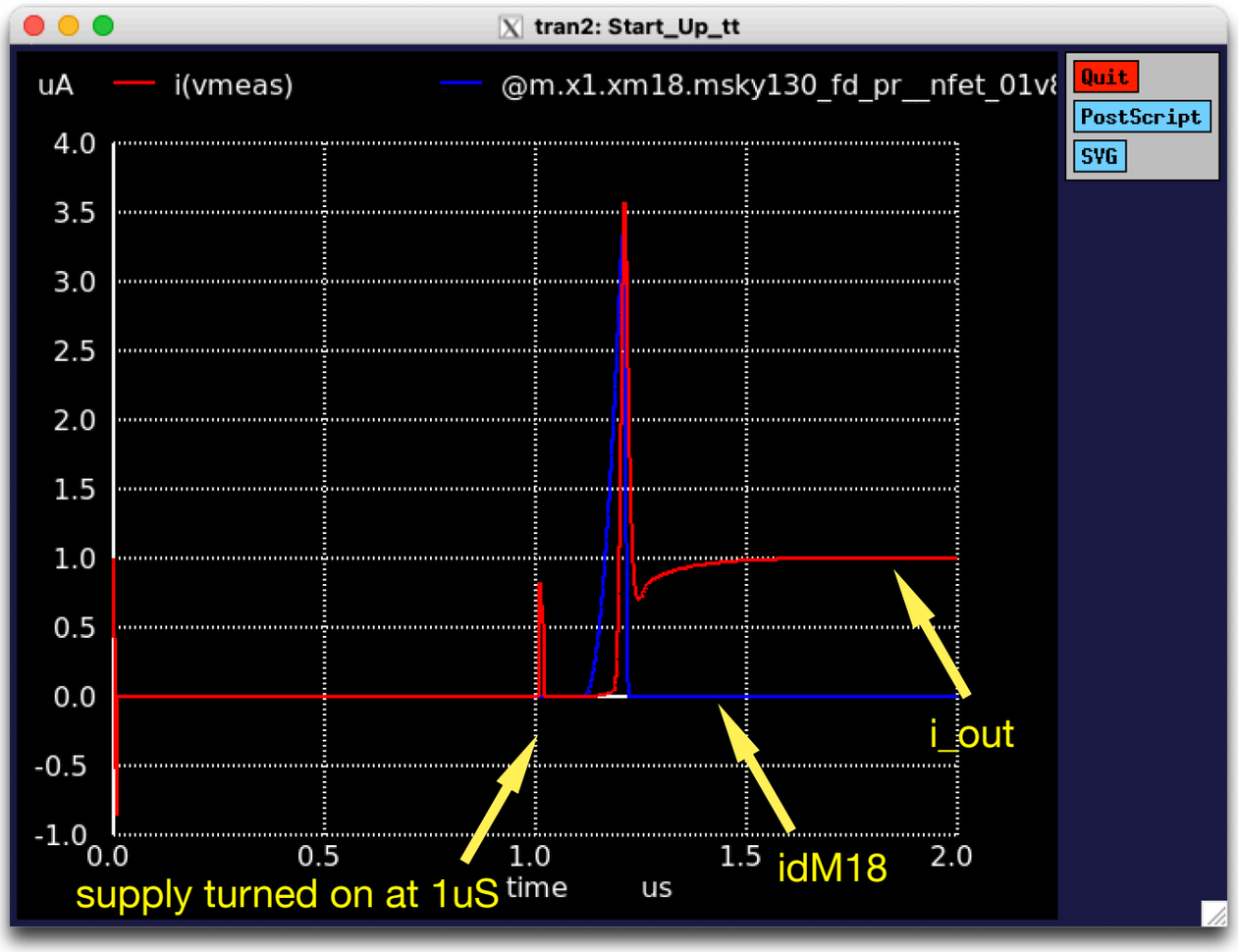
final circuit

M16, M17, and M18 added for start up

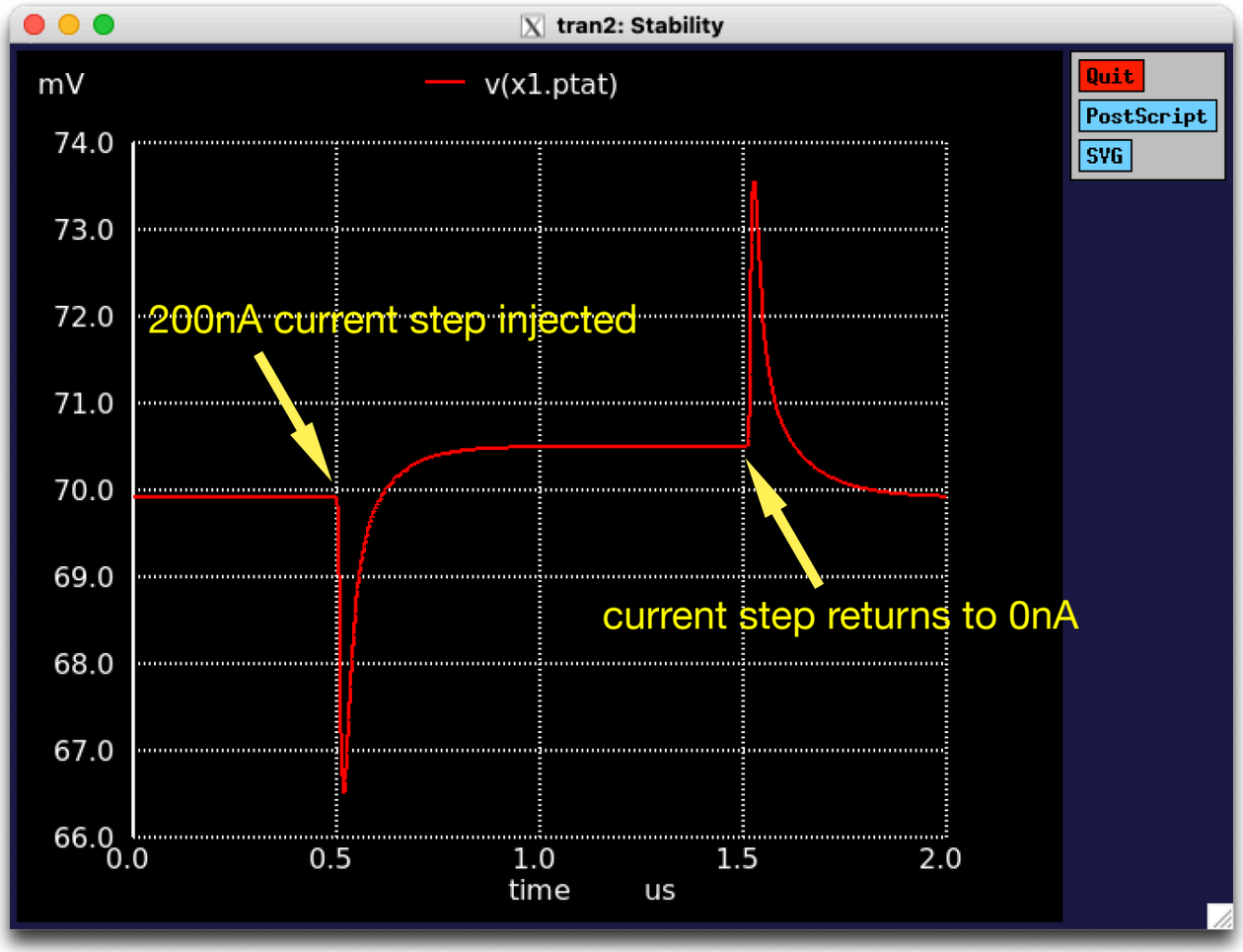


simulation of circuit with start up



circuit starts up and M18 turns off

simulation to check stability



no overshoot in response indicates very good stability

layout considerations

- device matching

  Match both W’s and L’s and create critical ratios with device multipliers.

  Insure that everything the gate sees to the edge of it’s well is the same.

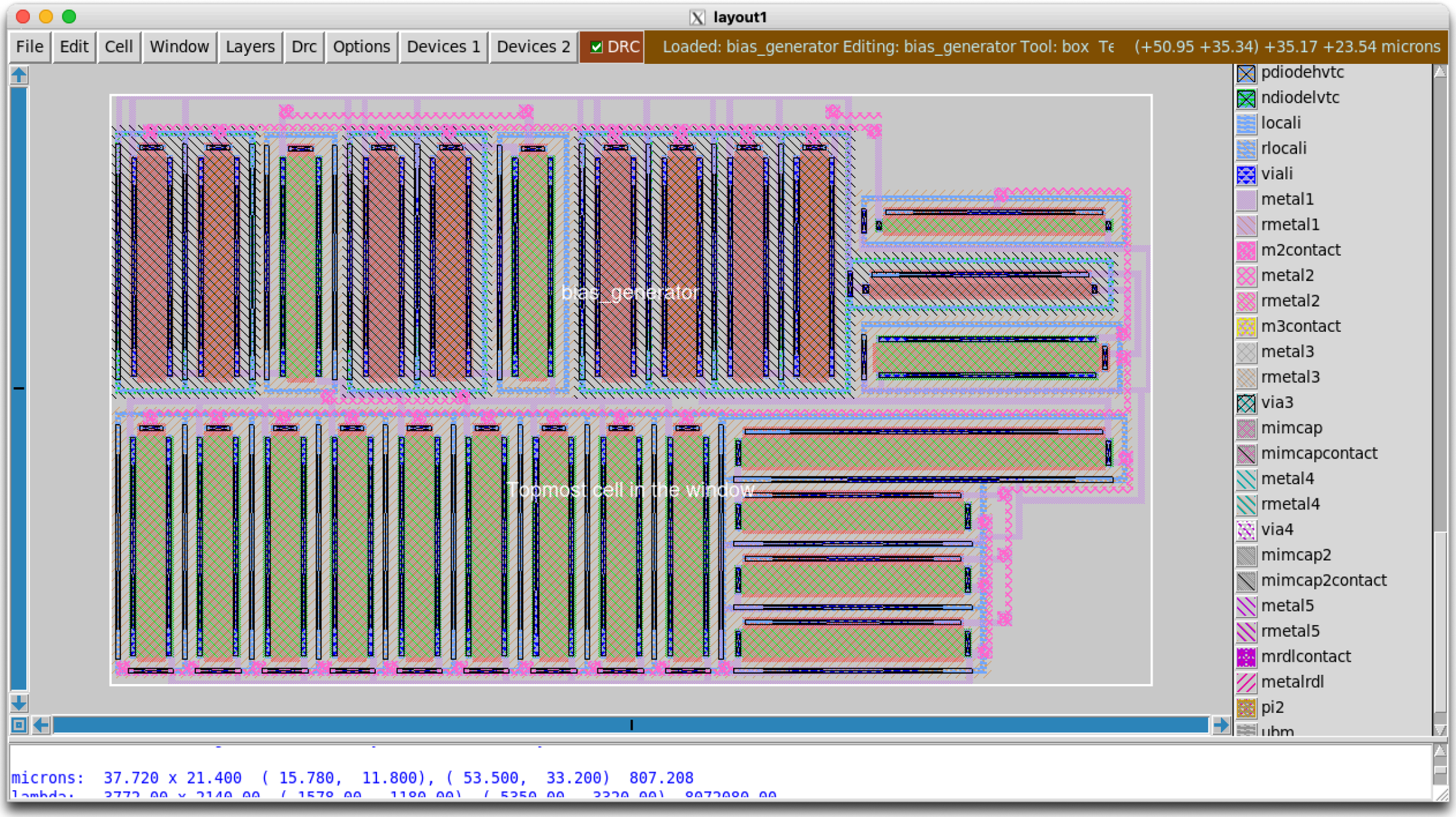
  Current flow from the source to the drain should be in the same direction.

  For large ratios use some form of interdigitation. M1:M2's 1:8 ratio are laid out in a pattern of 4:1:4, 4 cells of M2:1 cell of M1:4 cells of M2.

- merging devices

  Parametrized layout cells on the sky130A PDK allows merging of wells.

layout



layout area ≈ 38um x 22 um

design goal results

- i_out = 1uA ✔
- minimize i_out variations ✔
    - PVT variations ≈ +/- 10%
        - Process corners ss, sf, ff, and fs
        - supply Voltage from 1.7V to 1.9V
        - Temperature from -40°C to 125°C
    - device mismatch still needs to be simulated with monti-carlo
- minimize layout area ✔