EED 401

VLSI Technology and Design

Project Report

SPIKE-FREQUENCY ADAPTATION

Author 1 :
Chaudhary Rishika
R.No. 1710110276

Author 2:
Kakkar Pranika
R.No. 1710110253

Author 3:
Puranik Aditya
R.No. 1710110025

Author 4:
Sachdeva Vaibhav
T.No. 1710110369

Instructor:
Dr.Sonal Singhal
Shaik Jani Babu

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Abstract

Silicon neuron circuits mimic actual neuronal electrophysiological activity. Many circuits can be integrated on a single VLSI (Very Large Scale Integration) unit, and form large spiking neuron networks. Neuronal connectivity can be achieved using time multiplexing and rapid digital asynchronous circuits. Since the basic characteristics of the silicon neurons are decided at the time of design and can not be modified after the chip is manufactured, it is important to implement a circuit that represents an accurate model of real neurons but is at the same time lightweight, low-powered and compatible with asynchronous logic. Here we present a current-mode conductance based neuron circuit, with spike-frequency adaptation, refractory period, and bio-physically realistic dynamics which is compact, low-power and compatible with fast asynchronous digital circuits.

Contents

List of Figures

List of Tables

1 Introduction

When stimulated with a constant stimulus, many neurons initially respond with a high spike frequency that then decays down to a lower steady-state frequency. This dynamics of the spike-frequency response is referred to as "spike-frequency adaptation". Spike-frequency adaptation is a process that is slower than the dynamics of action-potential generation. Spike-frequency adaptation by this definition is an aspect of the neuron's super-threshold firing regime, although the mechanisms causing spike-frequency adaptation could also be at work in the neuron's subthreshold regime.

In the context of spike-frequency adaptation, **spike frequency** is often measured as the instantaneous rate, i.e., the averaged reciprocal interspike intervals at each time. This measures the inverse period of super-threshold firing.

There are many ways to model spike-frequency adaptation. But we can mainly focus on output-driven adaptation (as done in the paper), i.e., adaptation currents that are activated by the neuron's output activity. The two output driven adaptation models are -

1. **Conductance-Based Models**: Conductance-based models are the simplest possible biophysical representation of an excitable cell, such as a neuron, in which its protein molecule ion channels are represented by conductances and its lipid bilayer by a capacitor. In conductance based models any ionic current of a neuron is modeled in detail which requires exact knowledge of the specific type of adaptation currently involved.

2. **Integrate And Fire Model**: I&F neurons integrate pre-synaptic input currents and generate a voltage pulse analogous to an action potential when the integrated voltage reaches a spiking threshold. It describes the membrane potential of a neuron in terms of the synaptic inputs and the injected current that it receives. An action potential (spike) is generated when the membrane potential reaches a threshold, but the actual changes associated with the membrane voltage and conductances driving the action potential do not form part of the model. Spiking neuron models allows us to implement large, massively parallel networks of neurons.

2 Literature Review

Using an integrate-and-fire model is computationally effective, but the model is **unrealistically simple** and **incapable of producing rich spiking and bursting dynamics** exhibited by the neuron. Thus, simple I&F models do not produce a rich enough range of behaviors useful for investigating the computational properties of large neural networks. As suggested in [1], when considering presently available neuron models the Integrate-and-Fire (I&F) neuron model is widely used due to its simplicity—typical I&F neuron cells use approximately 20 transistors to implement low power adaptive neuron circuitry. Therefore,I&F neurons exhibit simple firing behaviour only—this might not be adequate for the development of VLSI circuitry which would be capable of imitating the processing of the

cortex, which is made of a large number of more complex non-linear oscillatory neurons exhibiting a variety of inherent firing patterns.

Wijekoon and Dudek had proposed an alternative phenomenological VLSI model with wide range of spiking patterns, however it was not used to implement systems in real-time as it operated on "**scaled-time**"(i.e. in microsecond rather than millisecond scale).Therefore it cannot be used to implement artificial or hybrid systems that interact with the world in real–time. [1] states that the firing patterns of VLSI neurons are on the microsecond scale rather than the millisecond scale of biological neurons. For comparative purposes, scaled time domain is considered in order to adopt biological classifications methods. In addition both this phenomenological model, and the vast majority of I&F neuron circuits previously proposed do not exhibit conductance-based behavior, which is crucial for implementing bio-physically realistic models of neurons.

There is a class of VLSI conductance-based silicon neurons that has been proposed in the past. These indeed implement faithful models of real neurons, but they use a **considerable amount of silicon real-estate** (i.e. many transistors and large capacitors). To implement Hodgkin–Huxley-type models on analog circuits, specific circuit was designed analog integrated circuits (ASICs) which exploit the intrinsic voltage–current of individual transistors (bipolar and MOSFET) to simulate the membrane equation of neurons including voltage-dependent conductances [2]. Each ionic conductance, source of an associated ionic current, and described by a set of non-linear equations (Hodgkin–Huxley formalism), is computed by a specific circuitry of transistors, resistors, and capacitors , which suggests that a number of components were used.

A new generation of bio-physically realistic circuits has been recently proposed which emulates the dynamics of neuronal proteic channels, reproduces faithful action potential traces, and use a considerable lower number of transistors per neuron model. But these circuits **do not produce fast digital pulses**, and cannot be easily interfaced to asynchronous digital circuits. In [3], showed a new circuit model which accurately models action potentials and channel currents of real neurons. It generates this waveform by taking advantage of the numerous physical similarities between biological channels and silicon channels. As with any circuit, there are some considerations to think about when using this circuit. Since these time constants are slow compared to the normal time constants in silicon technology, there is a trade off between low current levels (in the bias circuitry) and large capacitors.Therefore, we need to optimize for space.

3 Methodology

3.1 Circuit Diagram

The silicon neuron circuit schematic is as shown in figure. The circuit comprises:

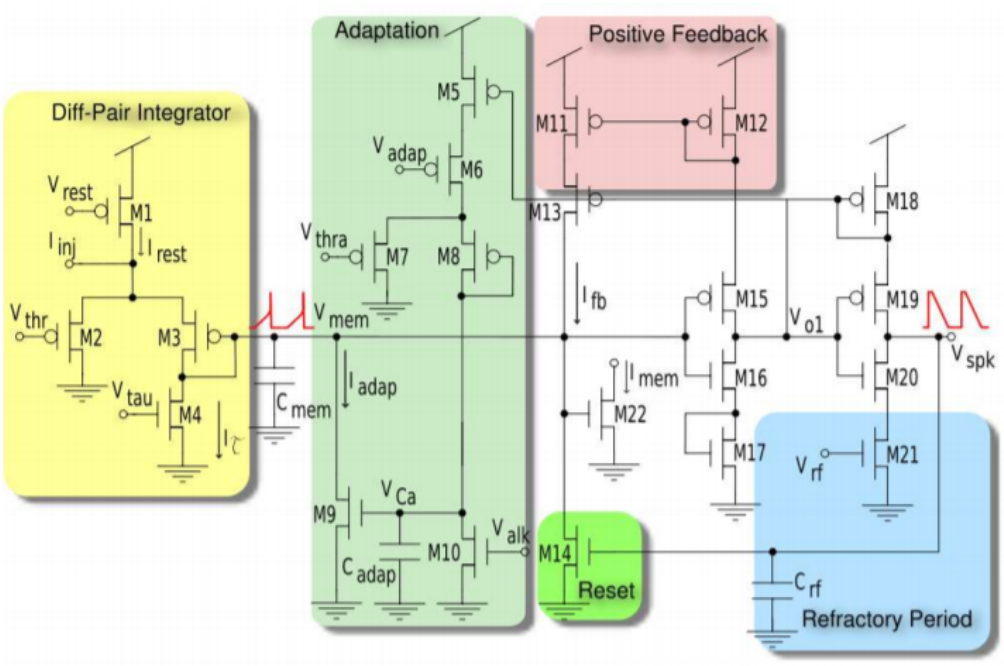


Figure 1: Schematic diagram of Differential-Pair Integrator (DPI) neuron circuit.

1. An input DPI circuit which comprises of transistors M1-M4, M22, models the neuron's leak conductance, and provides exponential sub-threshold dynamics in response to constant input currents.
2. An integrating capacitor Cmem, represents the neuron's membrane capacitance.
3. A second instance of a DPI having transistors M5-M10, models the neuron's Calcium conductance, and implements the spike frequency adaptation mechanism.
4. An inverting amplifier M15-M17 with positive feedback M11-M13.
5. A starved inverter with controllable slew rate M18-M21,which can be used to set arbitrary refractory periods.
6. The neuron's reset transistor is M14.

The read-out transistor M22 is used in simulations and for the analytical derivations, but was actually not included in the final layout of the circuit. We initially set $V_{mem} = \mathbf{0}$.

Note: *Technology used to design the circuit is 45nm.*

C_{mem}	$100\mu m^2$
C_{mem} capacitance(MOSCAP)	0.5 pF
Silicon neuron layout area	913 μm^2
Supply voltage	3.3 V
Power consumption/spike (300ns pulse)	7pJ
Power consumption/spike (100ms, including integration phase)	267pJ

Table 1: Given Silicon Neuron Circuit Specifications

3.2 Working of the Circuit

The circuit operates in the following way:

- The I_{inj} input current is summed up to a constant background current (set by V_{rest}) that can be used for spontaneous activity modeling. The DPI incorporates input currents, thus increasing the V_{mem} membrane voltage. The current input I_{inj} is summed up to a constant background current (set by V_{rest}) that can be used to model spontaneous activity. The DPI incorporates input currents, thus increasing the V_{mem} membrane voltage.

- As V_{mem} reaches the inverting amplifier's switching voltage, feedback current I_{fb} begins to flow through M11-M13, rising V_{mem} sharper. This positive feedback has the effect of making the M15-M16 amplifier switch very rapidly, diminishing its power dissipation dramatically.

- If V_{mem} rises enough to allow the first inverter switch the V_{O1} voltage is taken to ground and V_{spk} is powered to V_{dd}. Then the C_{mem} membrane capacitor is discharged back to ground via the M14 reset transistor, V_{O1} rises sharply back to V_{dd}, and the V_{spk} voltage is gradually reset to zero, at a rate regulated by the V_{rf} bias voltage and the C_{rf}'s size.

- The refractory cycle of the neuron lasts as long as V_{spk} is high enough to hold the reset transistor on. A current with amplitude set by V_{adap} is generated in the adaptation DPI during the spike emission period (when V_{O1} is low), with a gain set by the gate bias voltage V_{thra}, and a time constant set by V_{alk}. The existing I_{adap} adaptation increases with each spike, following I_{mem}'s same dynamics in first order.

- As a result, given I_{adap}'s negative-feedback property, the response of the neuron to a step-input current is characterized by an initial output firing rate proportional to the input current, which gradually decreases until an equilibrium is reached, reproducing the behavior of spike-frequency adaptation observed in real neurons.

- The neuron's subthreshold activity can be analytically interpreted, assuming the relevant transistors are working under the weak-inversion (or subthreshold) regime [4].

We ignore the current I_{adap} adaptation for this study, as this is non-negligible only after the first spike. In weak inversion a saturated n-FET's drain current changes exponentially with its gate voltage [4]. In particular,

$$I_{mem} = I_0 e^{\frac{\kappa V_{mem}}{U_T}} \tag{1}$$

where I_0 is the n-FET's leakage current, *kappa* is the sub-threshold slope factor and UT is the thermal voltage [4]. The sub-threshold branch current I_{M3} of the differential pair is given by:

$$I_{M3} = I_{in} \frac{e^{\frac{\kappa(V_{dd}-V_{mem})}{U_T}}}{e^{\frac{\kappa(V_{dd}-V_{mem})}{U_T}} + e^{\frac{\kappa(V_{dd}-V_{thr})}{U_T}}} \tag{2}$$

where $I_{in} = I_{rest} + I_{inj}$. If we assume that the sub-threshold slope coefficients κ of n and p-FETs are equal, we arbitrarily define $I_g \doteq I_0 e^{\frac{\kappa V_{thr}}{U_T}}$, and take into account eq. 1, we can rewrite I_{M3} as:

$$I_{M3} = I_{in} \frac{1}{1 + \frac{I_{mem}}{I_g}} \tag{3}$$

Kirchhoff's current law on the V_{mem} node yields:

$$C_{mem} \frac{d}{dt} V_{mem} = I_{mem} + I_\tau + I_{fb} \tag{4}$$

where $I_{fb} \approx I_{M16} = I_0 e^{\frac{\kappa^2}{\kappa+1} \frac{V_{mem}}{U_T}}$ and $I_\tau = I_0 e^{\frac{\kappa V_\tau}{U_T}}$. If we differentiate eq. 1 with respect to V_{mem} and combine it with the eq. 4 we obtain:

$$\tau \frac{d}{dt} I_{mem} = -I_{mem}(1 - \frac{I_{M3}}{I_\tau} - \frac{I_{fb}}{I_\tau}) \tag{5}$$

where $\tau \doteq \frac{U_T C_{mem}}{\kappa I_\tau}$. Replacing I_{M3} from eq. 3 into eq. 5 yields:

$$\tau \frac{d}{dt} I_{mem} + I_{mem}(1 - \frac{I_{fb}}{I_\tau}) = I_{in} \frac{\frac{I_{mem}}{I_{tau}}}{1 + \frac{I_{mem}}{I_g}} \tag{6}$$

- This is a first-order non-linear differential equation. However, for small values of V_{mem}(e.g. at the beginning of an action potential) the effect of the DPI dominates on the positive feedback, and we can neglect the current I_{fb}. Moreover, the right-hand term of eq. (6) can be reduced to $I_{in} \frac{I_g}{I_\tau}$, if $I_g \ll I_{mem}$. In these conditions eq. 6 simplifies to:

$$\tau \frac{d}{dt} I_{mem} + I_{mem} = I_{in} \frac{I_g}{I_\tau} \tag{7}$$

- Thus, for small values of V_{mem}, and sufficiently large values I_{mem}, such that $I_{mem} \gg I_g$ the silicon neuron exhibits a classical RC-filter type behavior.

C_{adap}	$1pF$
C_{rf} capacitance(MOSCAP)	$100fF$
C_{mem}	$2\ pF$
V_{dd}	1.3V
I_{inj} (300ns pulse)	$100nA$
V_{thr}	$600mV$
V_{rest}	$1.1V$
V_{adap}	$900mV$
V_{alk}	$190mV$
V_{thra}	$1.1V$

Table 2: Revised Silicon Neuron Circuit Specifications for 45 nm Technology

4 Results

4.1 Expected Results

Mentioned below are the simulation results from our paper which we were trying to achieve:

Fig2 : We plot the effects of the transient simulations, for a step input current and specific V_{thr} bias parameter settings. **The V_{thr} bias voltage effect**: higher values of this bias increase the value of the constant state output of the DPI. The more this bias grows, the more current it injects into the C_{mem} capacitor, resulting in a sharper growth of the membrane current. A sharper increase of this current means that the voltage from V_{mem} exceeds the threshold voltage of the inverting amplifier in a shorter time , resulting in an earlier spike generation.

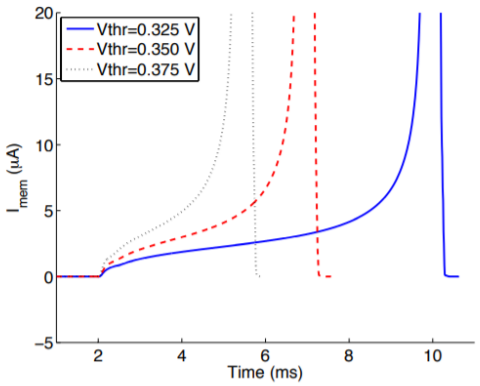
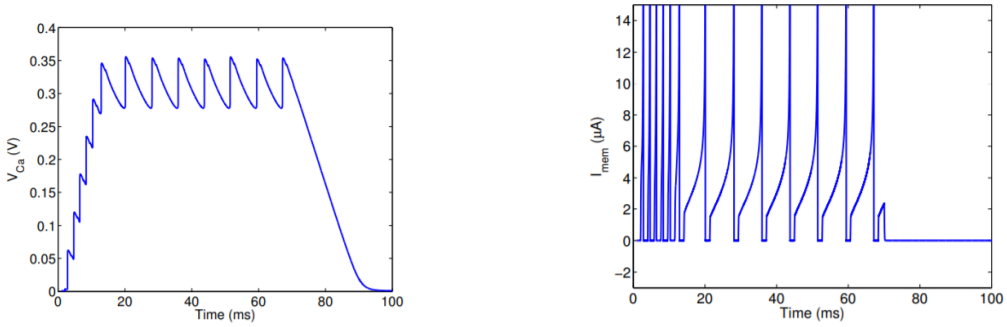


Figure 2: Silicon neuron membrane current I_{mem} in response to a constant step input current, for different values of the V_{thr} bias setting.



(a) (b)

Figure 3: Spike-frequency adaptation: (a) adaptation internal signal related to the Calcium concentration present in real neurons; (b) membrane "potential" signal traces in response to a step input current

Fig3(a & b) : An important feature of this circuit is the inclusion of a second, slower variable (e.g.), allowing the circuit to incorporate a spike frequency adjustment mechanism; We triggered the DPI adaptation (M5- M10) by lowering the value of below and conducting transient simulations, observing the neuron's activity for multiple output spikes.

In Fig. 3(a), we show the voltage measured in these simulations: the voltage steadily increases with every spike, until it reaches an equilibrium, at which the neuron's output spike frequency is maximally reduced.

In Fig. 3(b), we plot the membrane current I_{mem} as a function of time, measured in the same simulation run. As shown, the neuron's spike frequency decreases as V_{ca} increases, until the steady state is reached.

4.2 Simulation Results with 0.45nm Technology

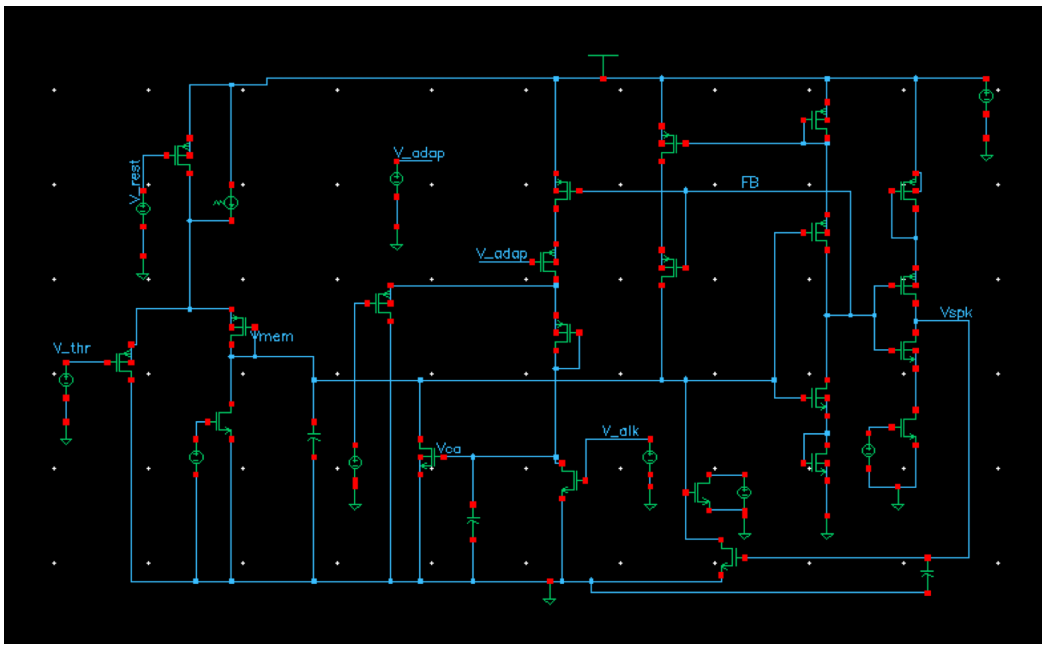


Figure 4: Schematic diagram of Differential-Pair Integrator (DPI) neuron circuit on **45***nm* **technology**.

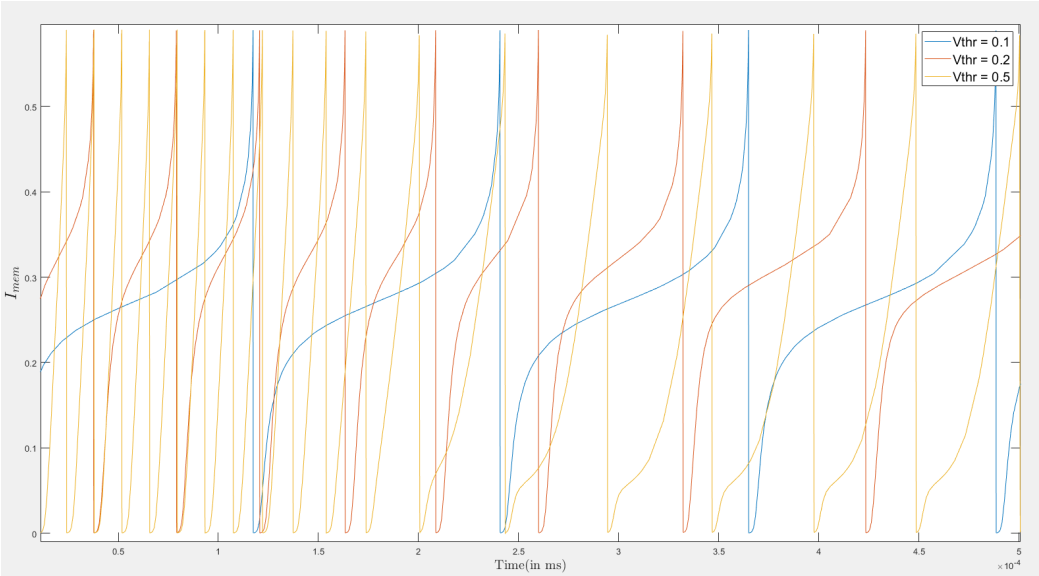
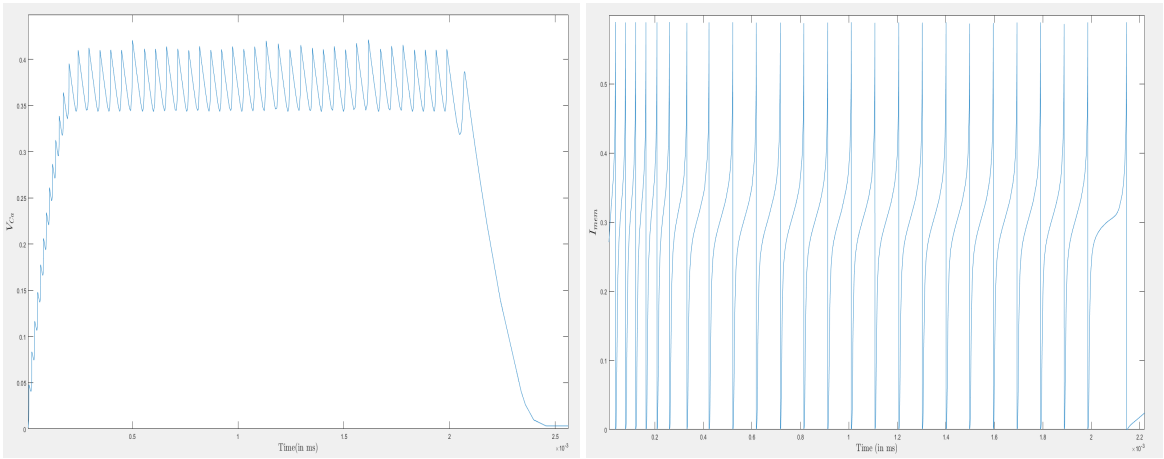


Figure 5: Silicon neuron membrane current I_{mem} in response to a constant step input current, for different values of the V_{thr} bias setting on **45***nm* **technology**.



(a) (b)

Figure 6: Spike-frequency adaptation on **45***nm* **technology**: (a) adaptation internal signal related to the Calcium concentration present in real neurons; (b) membrane "potential" signal traces in response to a step input current

5 Discussion and Conclusion

We have implemented a low-power current-mode conductance-based neuron circuit, with refractory period and spike frequency adaptation mechanisms. The findings shown in each case are consistent and show the expected response of the RC-type to a constant current injection, in the current temporal profile of the membrane. The positive feedback and the spike frequency adaptation mechanisms implemented make this VLSI model equivalent to the "adaptive exponential integrate and [U+FB01]re" (aEIF) model. The V_{ca} voltage increases gradually with each spike, until it reaches an equilibrium at which the spike frequency of the output of the neuron is reduced to a limit. The circuit is compatible with fast asynchronous digital circuits. Earlier it has been demonstrated that aEIF models can reliably predict the spike trains of complex Hodgkin-Huxley type models, powered by specific synaptic inputs based on conductance. Therefore we argue that the circuit mentioned in this work is capable of implementing faithful models of real neurons while satisfying the compactness, low power and consistency with asynchronous logic constraints.

References

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