

# LinnDrum™

## TECHNICAL INFORMATION

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## CPU-COMPUTER SECTION

### I. FUNCTIONS

- A. Generate system clock.
- B. Buffer Z80 data and address lines.
- C. Decode address space.
- D. Control retention of ram data when power is off.

### II. OPERATION

- A. The system clock is a 4MHz crystal controlled digital feedback oscillator. This 4MHz signal is divided down to 2 MHz by one half of U8 (74LS74) to assure 50% duty cycle. This 2MHz signal drives pin 6 of U1 (Z-80).
- B. The Z-80's data lines are each connected to an input and an output of a tri-state buffer (U4 or U5, 74LS244). The buffers are controlled by the RD and WR signals from U1 for bidirectional operation.
  - 1. Address lines A0 through A11 are buffered by U2 and U3 (74LS365).
  - 2. The BUSREQ (pin 25), WAIT (PIN 24), NMI (pin 17), and INT (pin 16) inputs to U1 are pulled up to +5 volts by 2.4 K resistors to disable their function.
- C. 16K of the Z-80's address space is used in the Linndrum. Rom and I/O occupy the bottom 8K of this (A13 low). Ram occupies the upper 8K (A13 high). A13 selects between the two decoders of U7 and is gated by U35 (74LS32) with MREQ. The low numbered decoder of U7 is used to select between Rom, keyboard and I/O. The high numbered decoder selects the 4 ram chips.
  - 1. When A12 through A7 are high, U6 sends a low to U7 to switch from Rom to keyboard and I/O. A6 distinguishes between keyboard and I/O, but is ignored in decoding the Rom.
  - 2. The other half of U7 uses A11 and A12 to select the Ram chips. The select lines to each Ram and the WR signal are gated with the power down signal to prevent memory access when the TTL supply is not at sufficient voltage.
- D. The power down signal is essentially the power stable signal gated by MREQ. This prevents interruption of a memory access in progress when the power goes down.

## CPU-I/O SECTION

### I. FUNCTION

- A. Scan keyboard and debounce.
- B. Decode output devices/Trigger drum voices.
- C. Read trigger inputs.
- D. Read tape inputs.
- E. Drive displays.
- F. Generate tempo clock.

### II. OPERATION

A. To scan the keyboard, the CPU reads the address location of a column of the keyboard matrix.

1. If any keys are depressed in that column, they connect the low on one of the U29 gates (74LS05) to a corresponding input of U28 (74LS244). When U28 is enabled, the computer reads the results of that column scan. The play/stop switch has its own input to U28 which is read with each keyboard read.

B. Output device decoding/Drum voice triggering.

1. U20 and U21 (74LS138) are enabled by the out strobe enable line from U7 & U35. They decode address lines A0 through A2. A3 selects between U20 and U21. It is connected to an active low enable on U20 and an active high enable on U21. These two decoders send strobes to 16 output devices-one for each of 10 drum sounds, 5 output latches (U16, U17, U18, U22, & U23 (74LS374) and the click/beep generator.
2. Data to the drum card is gated by tri-state buffer U19 (74365) to reduce noise on the drum card. When data is to be used, the computer sets the pin 9 output of U16 low to enable D0, D1, D2, and D3 on the drum card
3. Whenever a key closure or opening is detected, the Z-80 sends an IOREQ to trigger one half of U30 (LM556). U30 generates a 3 ms. pulse which the CPU reads through U28. The CPU waits until the high-going pulse returns low, and reads the key again to see if it is still in the same state. Only when it confirms this does it respond to the key command.

This prevents multiple triggering from contact bounce.

C. The READ INPORT signal from U7 and U35 puts data from the trigger, cassette and sync inputs onto the data bus through U15.

1. The trigger input circuits put out a digital pulse in response to rapid changes in the input signal. A trigger will only be generated if the envelope of the signal is increasing. Sharp transients trigger. Sustained tones will only cause a trigger when they begin. The input signal is applied to a trimpot to adjust gain from 1 to 10. The 2 sides of the A1 OPAMP and D12 and D13 act as a full wave rectifier. The next stage filters this rectified signal. The third stage runs open loop and acts as a combination differentiator-comparator. The output resistors make the  $\pm 15$  volt output of the third stage compatible with TTL logic levels.

D. The sync and cassette input circuits are zero crossing detectors. D7, D8, D9 and D10 provide about 1.4 volts of noise immunity. U38 operates as a logarithmic amplifier and controls the output transistors which translate the signal to TTL levels for U15.

E. The displays are driven by decoders U24, U25, U26 and U27 (74LS47) through resistors in resistor packs RP4, RP5, RP6 and RP7 (150Ω). The 2 pairs of decoders are fed data from latches U22 and U23, which are each selected by device decoder U20 (74LS138). Data from the computer is written into the latches as though they were memory locations.

1. The LED indicators are driven directly from latches U17, U18 and part of U16 via resistors in resistor packs RP1, RP2 and RP3 (150Ω). The latches are selected by U20 (74LS138). The output of U16 that drives the "pattern" LED also feeds an inverter which drives the "song" LED whenever the "pattern" LED is off.

2. U16 also drives the cassette output, the trigger output, a line to enable the tape sync output and a line that enables data to the drum card.

F. The tempo clock is generated by an RC controlled oscillator U30 (LM556). The tempo pot on the front panel varies the frequency from about 60 hz to 300 hz. This is divided in half by U8 and is put on the data bus by U15. When playing and recording, the CPU uses this signal to determine the length of a 1/192 note.

G. While the Linndrum is playing or recording, it sets a latch output of U16 high, allowing the inverted tempo signal to go out to the tape sync output transistor Q3.

1. At the same time it sends the trigger signal from another latch output of U16 to the trigger output transistor. When the Linndrum is running on external sync, the trigger output will follow the tempo of the sync input. The sync output will follow the tempo of the internal oscillator.
2. The cassette output is driven by a latch output from U16. Two 220 resistors divide the voltage to approximately 2.5V for cassette recorder line inputs.

#### DRUM SOUND GENERATOR CIRCUIT OVERVIEW

The three drum sound generator circuits (SNR/SSTK, TOM/CGA, MUX DRUMS) share a common method of doing the following:

1. Decoding strobe and data lines from the CPU.
  2. Clocking data out of the proms.
  3. Converting data from the proms to an analog waveform.
- 
1. A drum strobe consists of two low-going pulses on a voice strobe line, each with its four bit data "word". The first pulse clocks a low on DO into the DO latch, resetting the drum circuit. The second pulse clocks a high on DO and data on the other three lines into their latches, to select the appropriate drum sound.
  2. On the second pulse of the drum strobe, the output of the DO latch enables the counters. The outputs of the counters sequentially address all 4,096 words in the prom. For each address output by the counters, the data word at that address is output to the D to A converter. When count is complete it will reset the latches for a one chip sound; otherwise, it will continue the count for each prom in the drum sound.
  3. The prom output is fed to a multiplying digital to analog converter (Am 6070). The 6070 output is the product of the current input (pin 11) and the transfer function of the digital input. The differential current outputs are converted to a voltage by an op amp.

## DRM BOARD-MUX DRUMS

### I FUNCTIONS

- A. Decode strobe & data lines
  - 1. Bass, Tamb, Cbsa
  - 2. HiHat
  - 3. Ride & Crash
  - 4. Claps & Cowbell
- B. Provide sequential addressing of proms
  - 1. Bass, Tamb, Cbsa
  - 2. HiHat
  - 3. Ride & Crash
  - 4. Claps & Cowbell
- C. Provide multiplex timing circuitry
- D. Convert prom data to an analog signal
- E. Select correct output channel for drum played
- F. Filter bass output
- G. Control hihat decay

### II OPERATING DESCRIPTION

- A. Decodes strobe & data lines
  - 1. Bass, Tambourine, and Cabasa: Use drum strobes and D0 & D1 data decoded by a latch (U57, U56, U59 respectively) to select drum and volume level to play.
  - 2. HiHat: Uses two latches (U60 & U39) to decode the drum strobe and D0, D1, D2. D0 enables or disables the drum circuit. D1 selects volume level to play, and D2 selects between open & closed HiHat.
  - 3. Ride and Crash: Each uses a latch (U21 and U40 respectively) to decode drum strobes.
  - 4. Claps and Cowbell: Share a latch (U58) to decode the drum strobe and D0.
- B. Provides sequential addressing of proms
  - 1. Bass, Tambourine and Cabasa: Use a 13 bit ripple counter to address the proms. On the second pulse of the drum strobe the counters are enabled and begin sequentially counting through the prom's

addresses. When the count reaches 4096 the 13th bit goes high, clearing the latches and disabling the counters.

2. HiHat: Uses a 15 bit ripple counter to address its proms. On the second pulse of the drum strobe the counters are enabled and begin sequentially counting through the proms' addresses. The 13th and 14th bits are used to enable the four hihat proms in order. This is done with U34 (74 LS 139) which decodes these two inputs and outputs a low to the correct prom select. When the count reaches 16384, the 15th bit goes high, clearing the latches and disabling the counters.
3. Ride and Crash: Each use a 16 bit ripple counter to address the proms. On the second pulse of the drum strobe the counters are enabled and begin sequentially counting through the proms' addresses. The 13th, 14th and 15th bits are decoded by U1 and U20 respectively (74 LS 138's) to provide a low to the correct prom select. When the count reaches 32768 the 16th bit goes high, clearing the latches and disabling the counters.
4. Claps and Cowbell: Each uses a 13 bit ripple counter to address its prom. On the second pulse of the drum strobe the counters are enabled and begin sequentially counting through the prom's addresses. When the count reaches 4096 the 13th bit goes high, clearing the latches and disabling the counters.

#### C. Provide Multiplex timing circuitry

1. U77 (74LS627) is a voltage controlled oscillator used to generate a clock for the MUX drum circuit. TP1 varies a voltage input on U77 pin 2. This voltage determines the frequency of the square wave output on pin 6.
2. This output is applied to the clock 2 input of the counter U75 (74LS393). Outputs A2 (LSB) & B2 are decoded by U34 (74LS139) and U36 (74LS74) to provide timed enables for the 6070, 74LS138 and 4051 every time a drum circuit is enabled.
3. B2 is used as the clock 1 input. Outputs A1, B1 and C1 (MSB) are decoded by U74 (74LS138) to enable each drum circuit one at a time.
4. When U74 enables a drum circuit, it outputs a low pulse that enables that voice's prom. If the voice's counter is enabled it increments the counters. The prom outputs the data stored at that

address onto the data bus. If the counters are not enabled the prom outputs the data stored at address 000H, which is 00H.

D. Convert prom data to an analog signal

1. The output of the proms is fed to a multiplying DAC. The DAC output is the product of the current input (pin 11) and the transfer function of the data input. The differential current outputs are converted to a voltage by U89 (TL082).

E. Select correct output channel for drum played

1. The multiplexed analog signal is fed to pin 3, U83 (CD4051). After the signal for each voice has settled, U83 is enabled to connect the signal to one of the sample and hold capacitors and op-amps. The digital inputs on pins 9, 10, and 11 select which output channel.

F. Filter bass output

1. The bass signal is run through a voltage controlled filter. This circuit is the same as the TOM/CGA filter.

G. The Hat signal is run through a voltage controlled amplifier U91 (CEM3360).

1. When a HAT strobe occurs, U37 (LM556) outputs a 5 ms high going pulse. This charges the 1 $\mu$ f capacitor, which discharges through two paths. If the HAT is open (pin 5, U39 high), it discharges only through the 1Meg resistor. If the HAT is closed (pin 5, U39 low), it also discharges through the HiHat decay control on the front panel.
2. The VCA makes the shaped pulse the amplitude envelope for the Hat output.

## DRM BOARD-SNR/SSTK,CLICK,BEEP

- A. Decode strobe and data lines.
- B. Generate clock of proper frequency based on tuning pot setting on the mixer and the CV input.
- C. Provide sequential addressing for proms.
- D. Convert prom data to an analog signal.
- E. Select correct output for drum played.
- F. Provide click output
- G. Provide beep output.

- A) On the first pulse, D0 is low; which will clear the counters and reset the circuit in case it had been playing a drum. The rest of the data bits are not used.  
On the second pulse, all four data bits are used to select which drum and what volume to play at.

	D0 U41,Q1	D1 U41,Q2;Q2	D2 U42,Q1	D3 U42,Q2	
NODRUMS	H	X X	X	X	
SSTK	L	H L	H	H	
SNAR1	L	L H	L	L	
SNAR2	L	L H	H	L	
SNAR3	L	L H	L	H	

D0 - Used to turn drum circuit on and off.

D1 - Selects between SNR prom and SSTK prom and correct output channel.

D2&D3 - Selects volume for drum played.

- B) The snare tuning pot on the MXR board supplies a voltage level to U95 which sums it with the control voltage input, if any. This is passed on to the diode protected CV input of U80, a voltage controlled oscillator. U80 outputs a square

wave signal whose frequency is determined by the voltage on the CV input. This output provides clock pulses to the counters.

- C) The counters U61 & U62 (74 LS 393's) are set up as a 13 bit ripple counter. The first 12 bits count through the addresses of the prom selected. When the count reaches 4096 the 13th bit goes high, is inverted by U76 (74LS00) and clears the latches.
- D) The output of the proms is fed to a multiplying digital to analog converter (DAC). The DAC output is a product of the current input (pin 11) and the transfer function of the data input. The volume level selected by D2 & D3 determines the current input on pin 11. The differential current outputs are converted to a voltage by U103 (4558).
- E) U90 (CD4053) selects the correct output for the drum played based on the signal at pin 11. A low from Q2 of U42 selects pin 13 as the output and a high on Q2 selects pin 12.
- F) When a click strobe is received from the CPU the falling edge of the pulse triggers U65 (LM556). This output is a high going 1 ms. pulse. It is routed through a blocking cap to the click direct output jack and to the MXR board via the 40 pin dip connector.
- G) When a beep signal is received from the CPU, U76 buffers it and routes it thru a  $.01\mu f$  blocking cap to the 40 pin dip connector.

## DRM BOARD-TOM/CGA

### I. FUNCTIONS

- A. Decode strobe and data lines.
- B. Generate clock of proper frequency based on tuning pot settings on the mixer and the CV input.
- C. Provide sequential addressing for proms.
- D. Provide prom select signals.
- E. Convert prom data to an analog signal.
- F. Filter analog signals.
- G. Select correct output for drum played.

### II. OPERATING DESCRIPTION

- A. On the first pulse, D0 is low; which will clear the counters, and reset the circuit in case it had been playing a drum. The rest of the data bits are not used.  
On the second pulse, all four data bits are used to select which drum is to play.

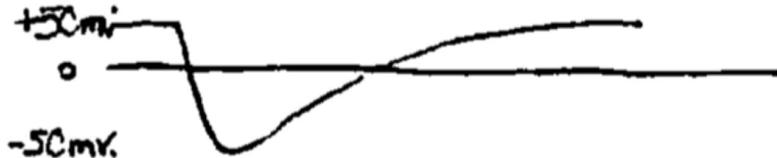
	DO U73,Q1	D1 U73,Q2	D3 U72,Q2	D2 U72,Q1
NO DRUMS	"C"	"B"	"A"	
NO DRUMS	L	X	X	X
LO CGA	H	L	L	L
HI CGA	H	L	L	H
LO TOM	H	H	L	L
MID TOM	H	H	L	H
HI TOM	H	H	H	L

- B. The five tuning pots on the MXR board supply voltage levels to U81 (4051). One of these levels is selected by the data on A, B, and C inputs and passed on to the output (pin 3). U80 (74 LS 627) is a voltage

controlled oscillator used to generate the clock signal, based on the voltage level applied to its control voltage input. The output of U80 provides the clock for the counters.

- C. The counters U70 & U71 (74 LS 393's) are set up as 14 bit ripple counter. The first 12 bits count through the addresses of the "A" prom. When the count reaches 4096 the 13th bit goes high disabling the "A" prom, and enabling the "B" prom. When the count reaches 8192 the 14th bit goes high to clear the latches and disable the counters.
- D. The Q2 output of U73 enables the TOM or CGA proms. The CGA enable is gated so that neither pair of proms is enabled when no TOMs or CGAs are playing.
- E. The output of the proms is fed to a multiplying DAC. The DAC output is the product of the current input (pin 11) and the transfer function of the data input. The differential current outputs are converted to a voltage by U85 (4558).
- F. The TOM/CGA circuit uses a CEM 3320 voltage controlled filter to reduce noise at low signal levels.

- 1. When a TOM/CGA strobe occurs, U22 (LM556) outputs a 5 ms pulse. U84 (TL082) and related circuitry shapes the pulse as shown in figure 1.



- 2. This shaped pulse is applied to U86 pin 12, the control voltage input of the voltage controlled filter. The CV input controls the frequency of the four poles. It allows the attack transients through with little filtering. As the drum sound decays U86 filters the digitizing noise.

- G. The analog output is fed to U87 (CD4051). U87 connects that signal to one of the output op-amps "U". The digital inputs, pins 9, 10 and 11 select which op-amp. Pin 6 is used to reduce output noise when no TOMs or CGAs are playing.

## DRM BOARD/5VSR BOARD-POWER SUPPLY

### I. FUNCTIONS

- A. Supply TTL voltage to all devices except CMOS and OP AMPS.
- B. Supply CMOS voltage to CMOS rams (U9, U10, U11, U12,) and three CMOS I.C.'s (U33, U36, U37) on CPU board and U63 on the DRM board.
- C. Supply battery voltage to the CMOS devices for memory retention when AC power is interrupted.
- D. Supply analog voltage to all OP Amps on DRM & CPU boards.
- E. Generate power stable line for CPU.

### II. OPERATING DESCRIPTION

#### A. TTL VOLTAGE

1. Voltage from the transformer is rectified by diodes D10, D11, D12, D13 and filtered by C36 (27,000 $\mu$ F). All these components are located on the drum board.
2. This front end voltage approximately 12V is fed through pin 2 of the 7 pin molex. This is filtered further on the 5VSR board by C3.
3. The switching regulator UR2 alternately connects and disconnects the front end to the inductor L1. VR2 varies the duty cycle of alternation to control the voltage after the LC choke. Ground is supplied on pins 3 and 5 of the 7 pin molex.
4. C2 is the timing cap for the switching frequency. C1 is a filter cap for the current limit circuit. L1 is an RF choke to smooth the output of VR2.
5. The current limit circuit is used with National regulators only. When the current through R5 is too high, its voltage drop causes transistor Q1 and Q2 to pull down the voltage on the voltage reference line of VR2.
6. The output of the regulator VR2 is seen at pin 7 of the 7-pin molex. This output may be varied by adjusting the value of the trimpot on the 5VSR board which in conjunction with R3 & R4 sets a voltage for the Error Amplifier Input of VR2.

## B. CMOS VOLTAGE

1. Front end is applied on pin 1 of VR1. R2 sets a ground reference above ground causing an output of approximately 5.9V. This is dropped through D1 to approximately 5.3V. This output can be seen on pin 1 of the 7 pin molex. The diode keeps the batteries from draining through VR1 in power down mode. R1 is for trickle charging the batteries.

## C. BATTERIES

1. BATT 1, BATT 2, BATT 3 are in series to provide approximately 4.0 volts when completely charged. They should never be below 3.2 volts.

## D. ANALOG VOLTAGE (DRM BOARD)

1. D14, D15, D16, D17, form a bridge providing front ends for +15 and -15 volts; around a center tapped ground on the transformer.

### 2. -15 VOLTS

- a. The -15v front end is filtered by C17 and fed to pin 2 of VR 4.
- b. Pin 1 of VR4 is ground.
- c. VR4 regulates this front end to approximately -15v. C19 filters the output voltage on pin 3 of VR4.

### 3. +15 VOLTS

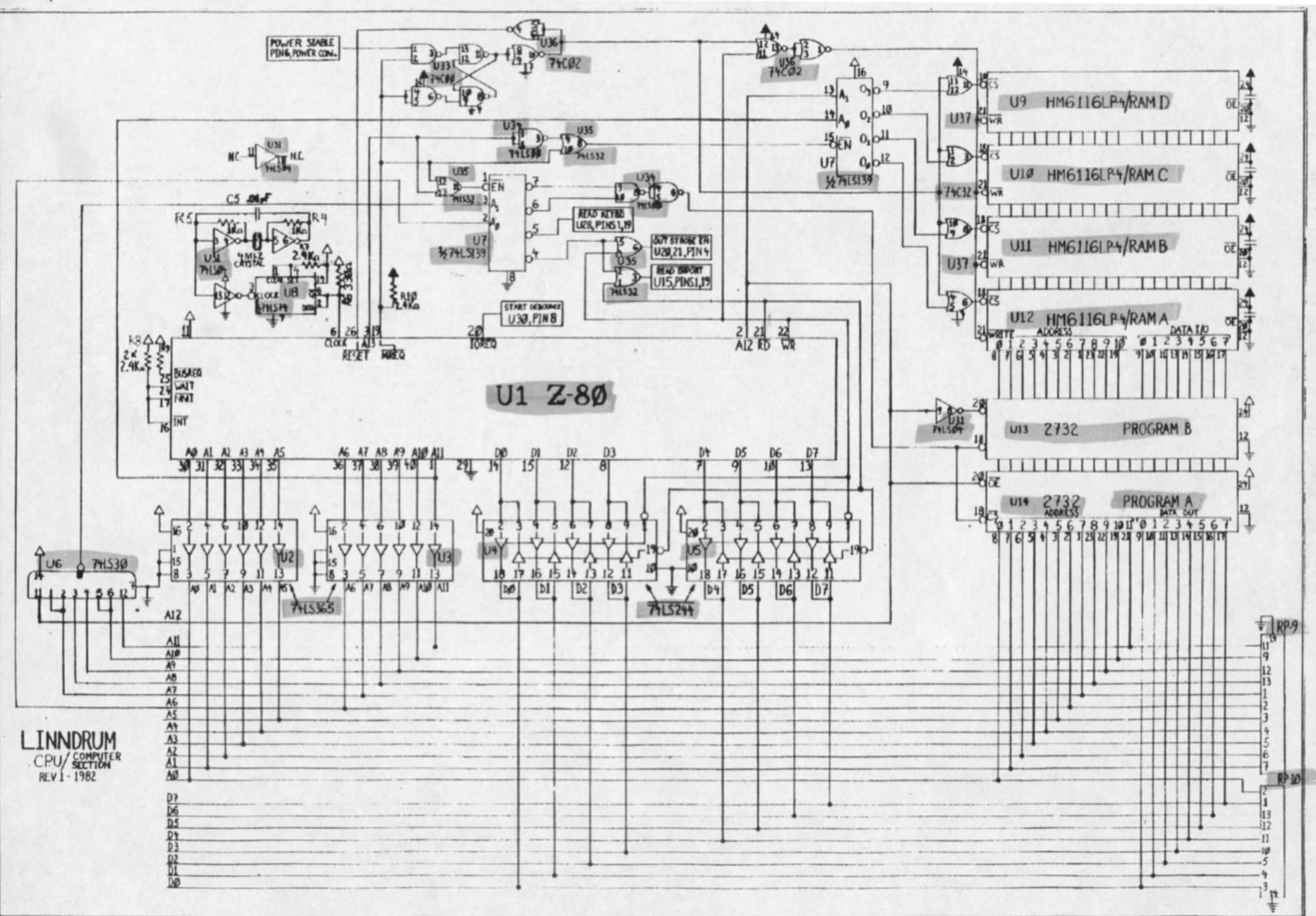
- a. The +15v front end is filtered by C16 and fed to pin 1 of VR3.
- b. Pin 2 of VR3 is ground.
- c. VR3 regulates this front end to approximately +15v. C18 filters the output voltage on pin 3 of VR3.

## E. POWER STABLE

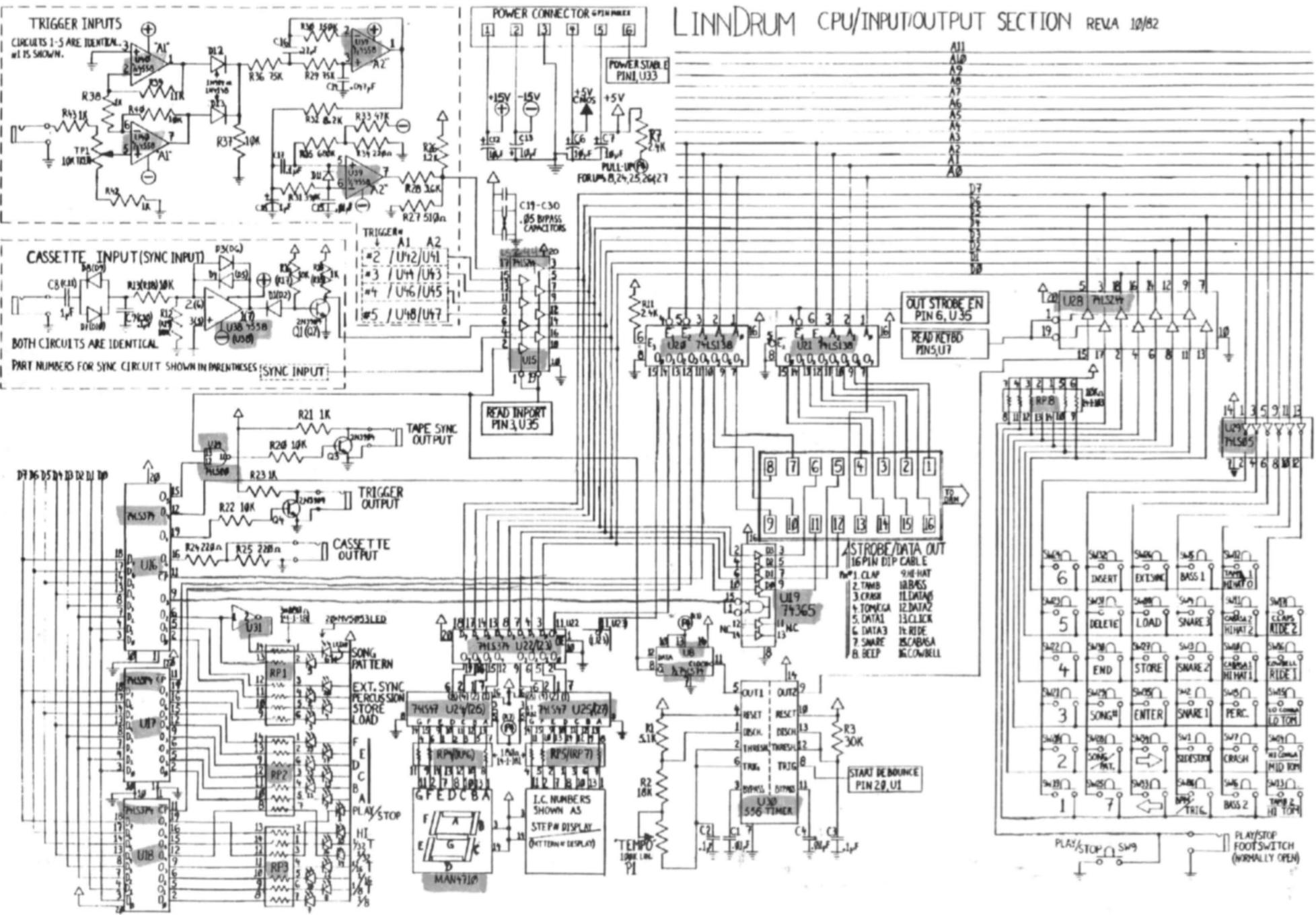
1. The circuit consisting of R20, C11 and VR2 on DRM board sets up a stable voltage reference of 1.23 volts, for pin 15 of U63.
2. +15 volt front end is fed thru a voltage divider consisting of R25 and R26.
3. The divided front end is fed to the circuit consisting of R24, D18, and C15. This circuit delays the signal, fed to pin 14 of U63, by the

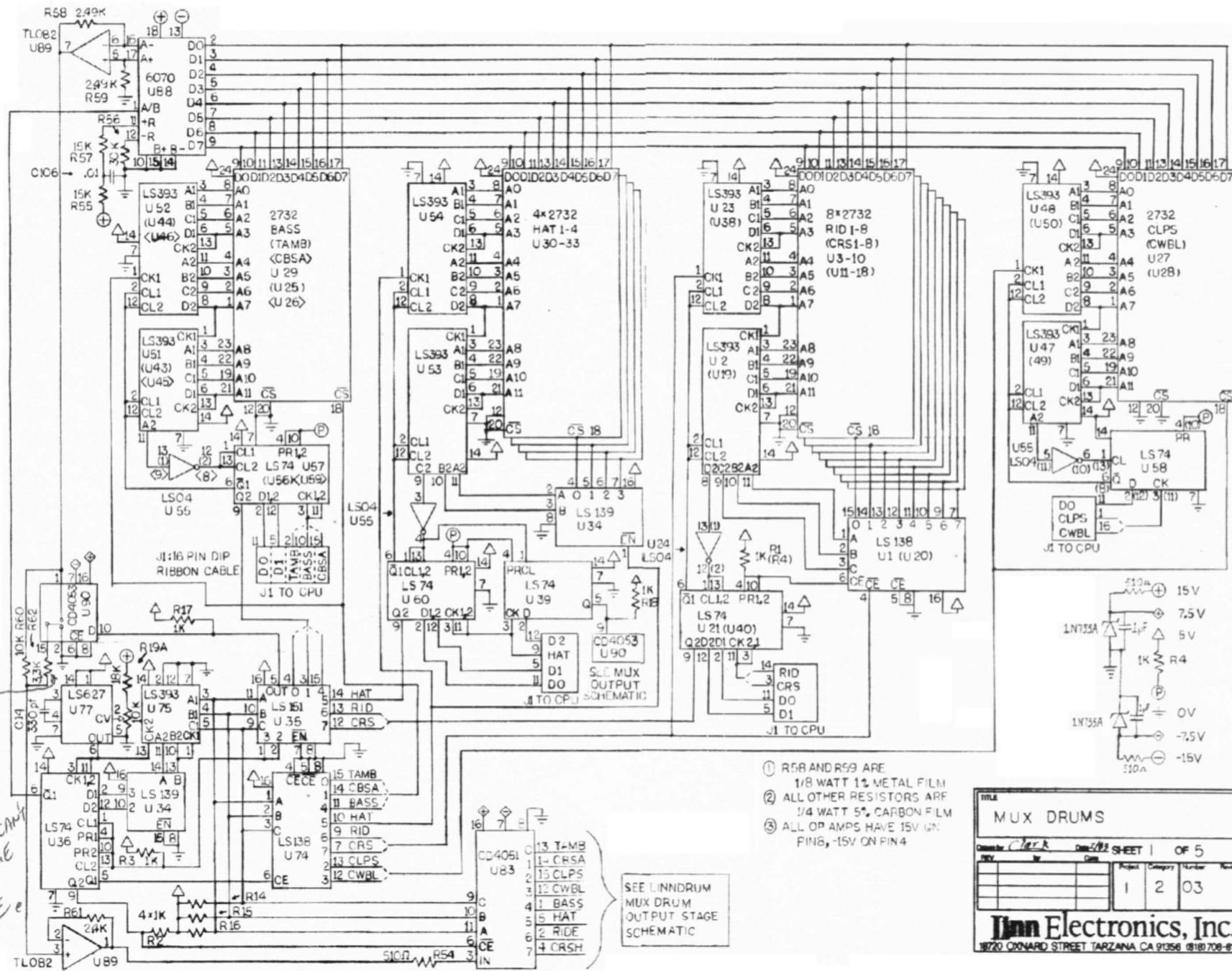
amount of time it takes to charge C15 (approx. .5 sec).

4. U63 compares that with the reference voltage on pin 15, if it exceeds that voltage, it will cause the output on pin 16 to go high, indicating stable AC power to the CPU board.
5. R23 sets the amount of hysteresis.



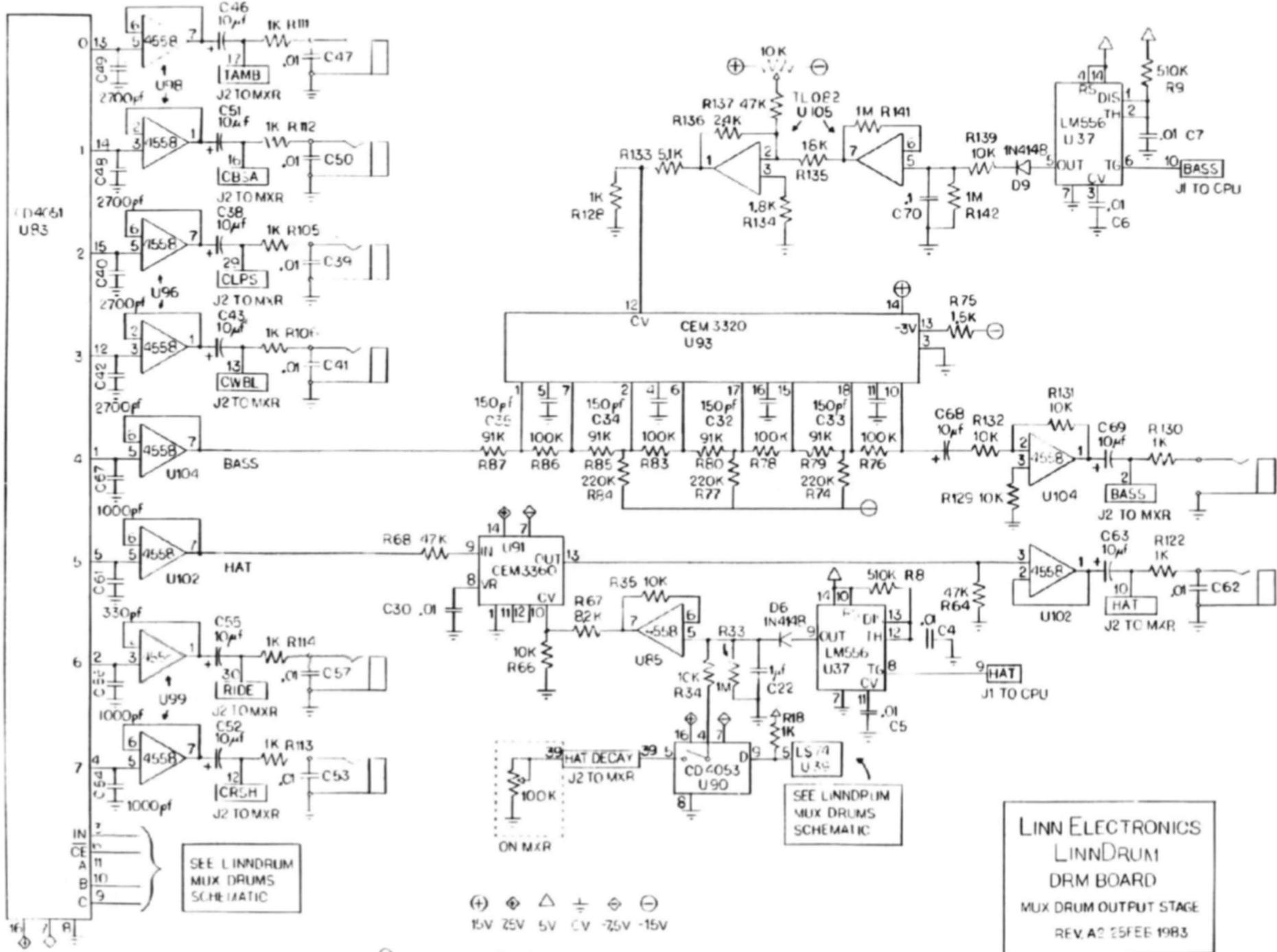
# LINNDRUM CPU/INPUT/OUTPUT SECTION REVA 10/82





Title		MUX DRUMS			
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Project	1	2	3	4	5
Category	1	2	3	4	5
Number	03				

**JLinn Electronics, Inc.**  
18720 OXNARD STREET TARZANA CA 91356 (818) 708-8131



- (1) ALL RESISTORS ARE 1/4 WATT, 5%, CARBON FILM  
 (2) ALL OP AMPS HAVE +15V ON PIN 9, -15V ON PIN 4

**LINN ELECTRONICS**  
**LINNDRUM**  
**DRM BOARD**  
**MUX DRUM OUTPUT STAGE**  
 REV A2 25FEB 1983

LINN ELECTRONICS

LINN DRUM

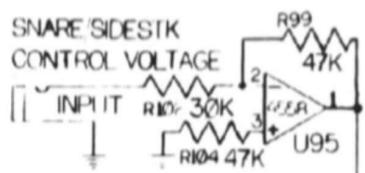
DRM BOARD

SNARE/SIDESTICK

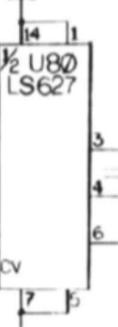
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SNARE/SIDESTICK

CONTROL VOLTAGE



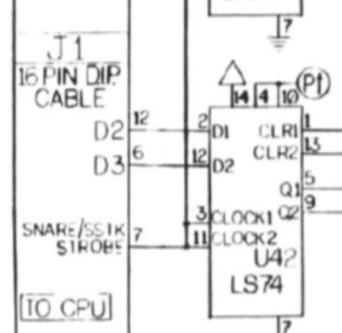
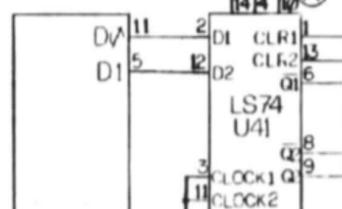
$\frac{1}{2}$  U80  
LS627



ON MIXER  
BOARD

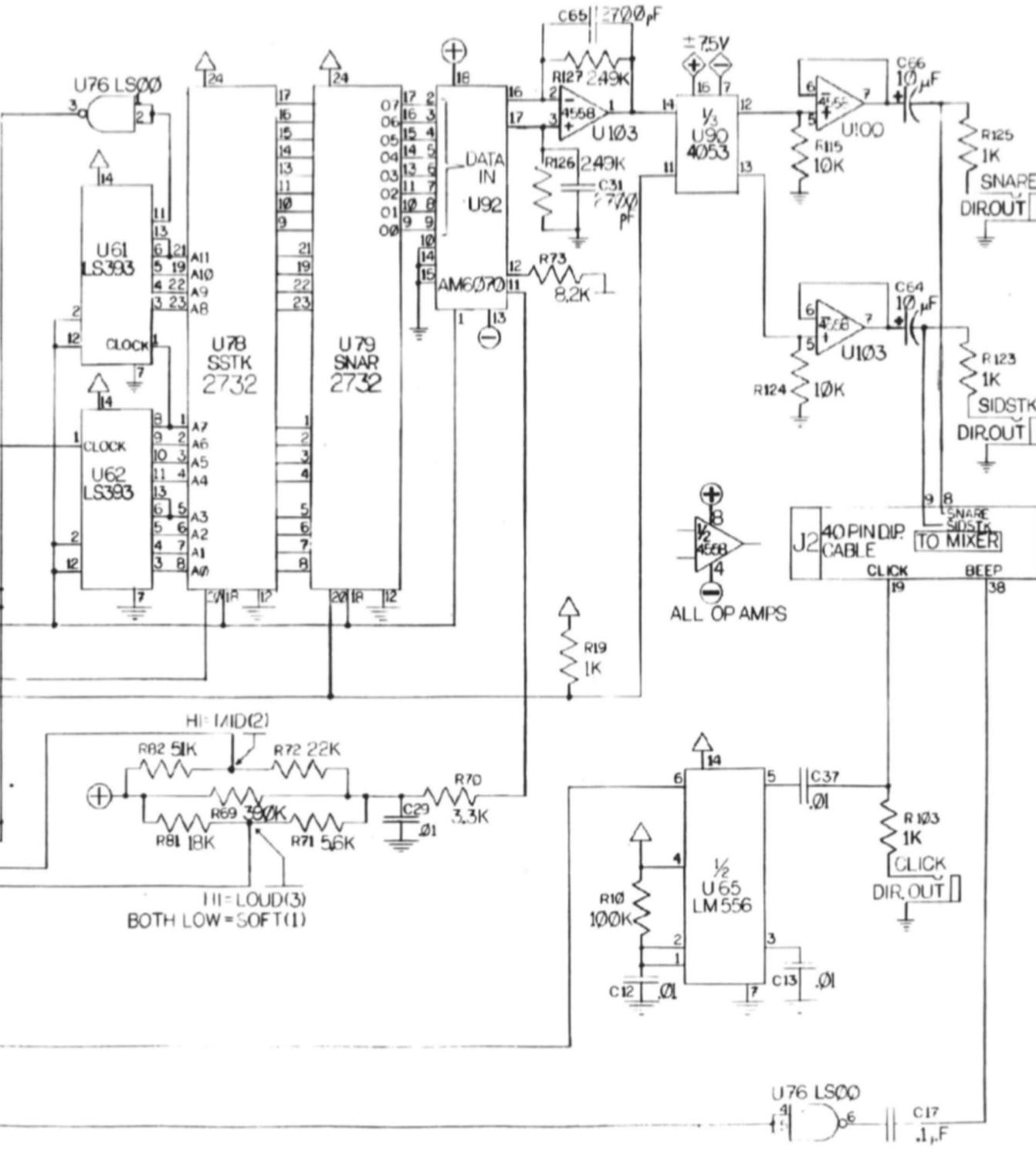
SNARE  
TUNING  
100K

ON MIXER  
BOARD

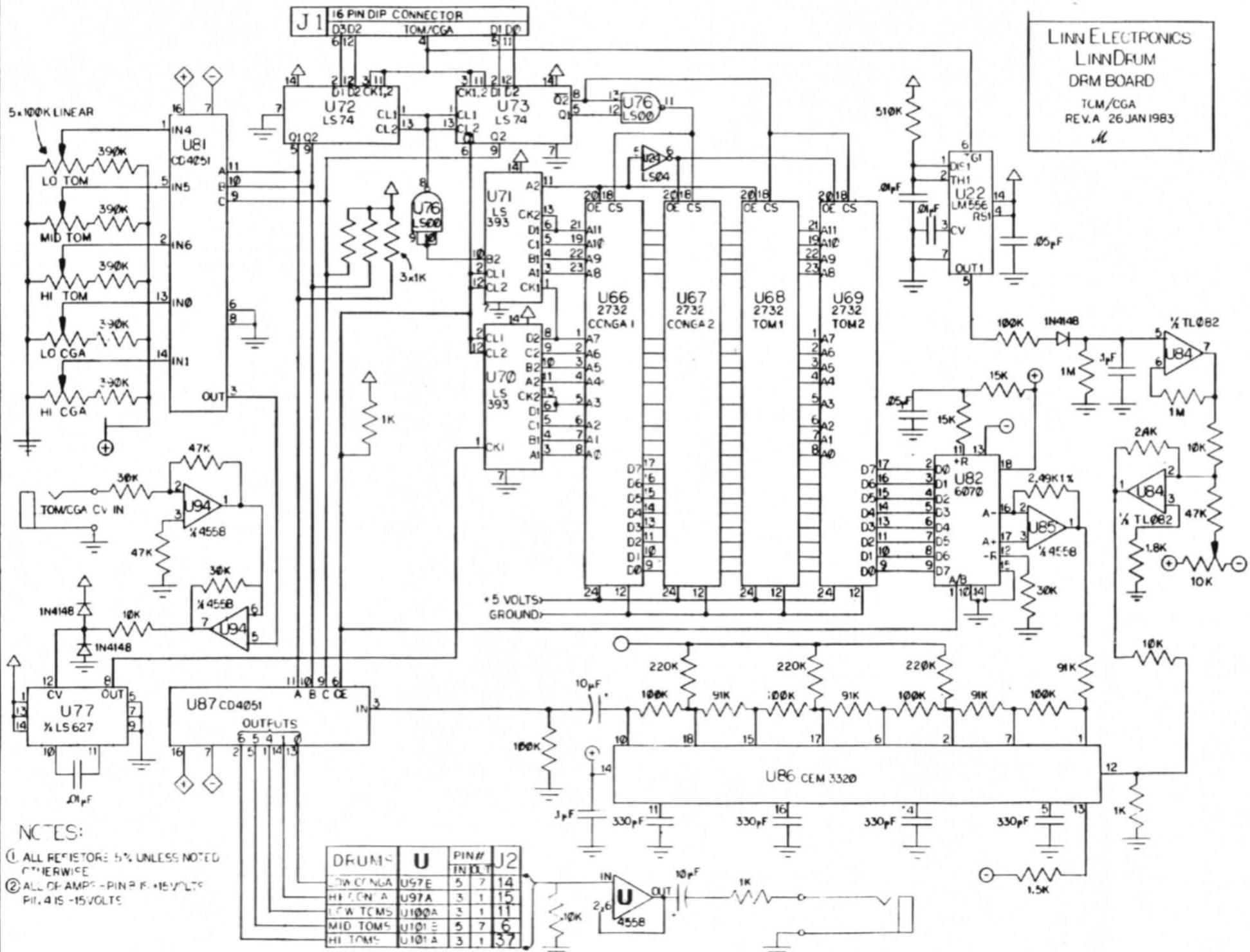


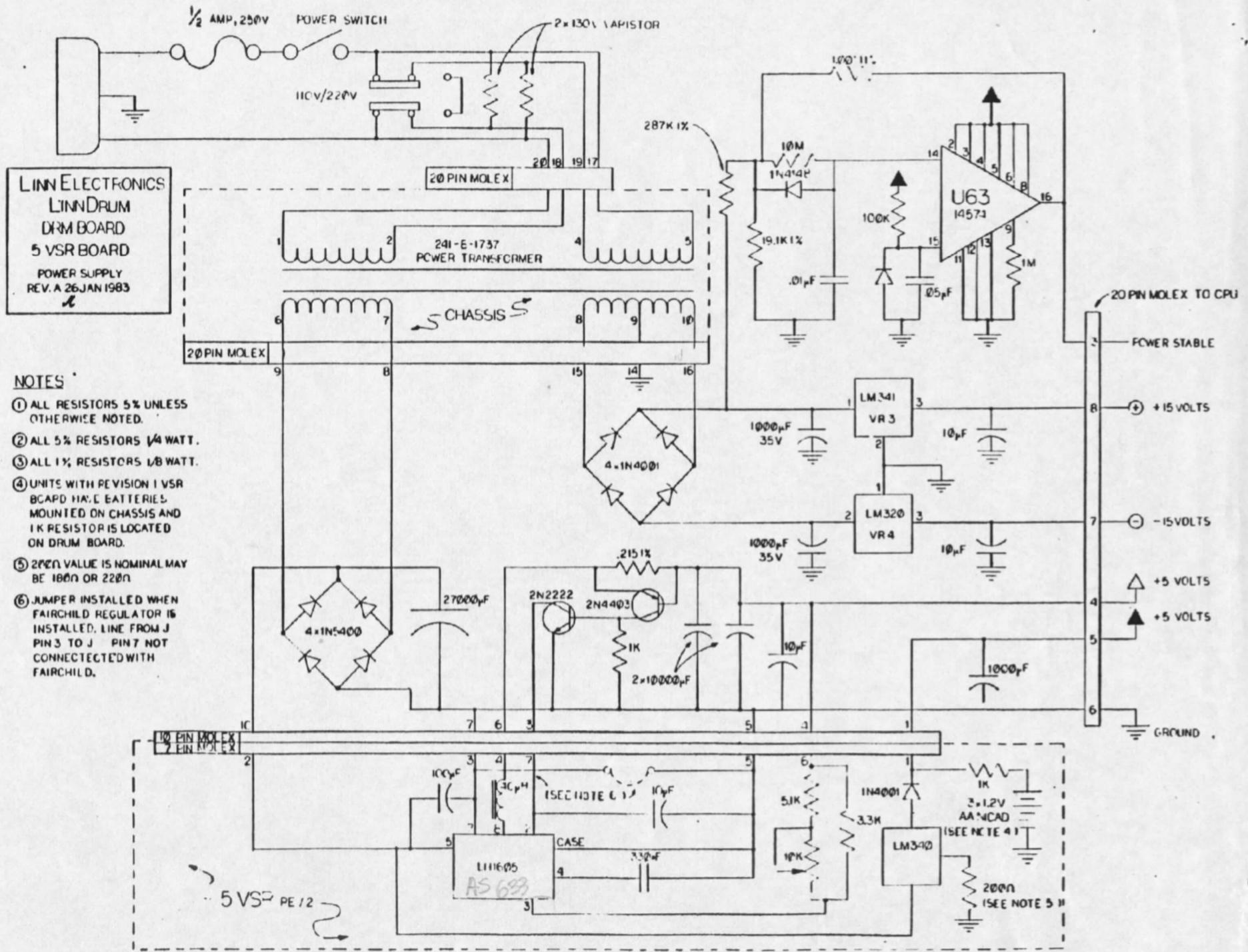
CLOCK  
STROBE

BEEP

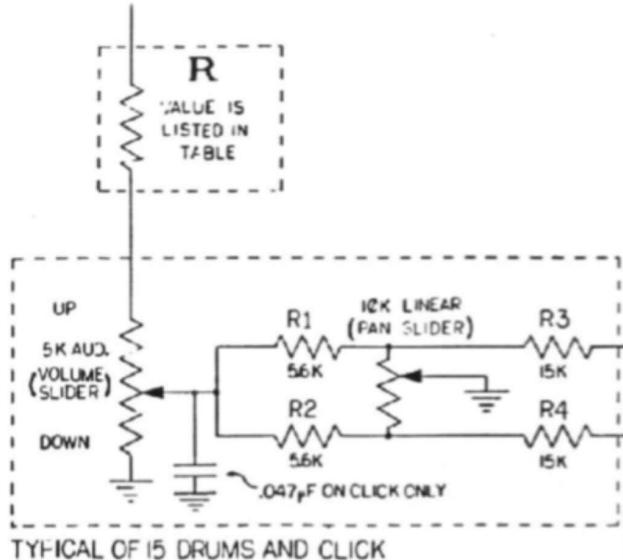


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LINNDRUM  
DRM BOARD  
TCM/CGA  
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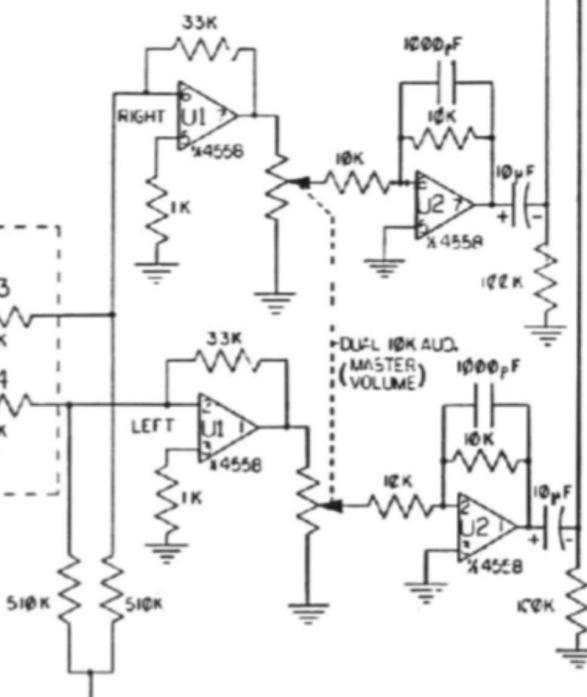
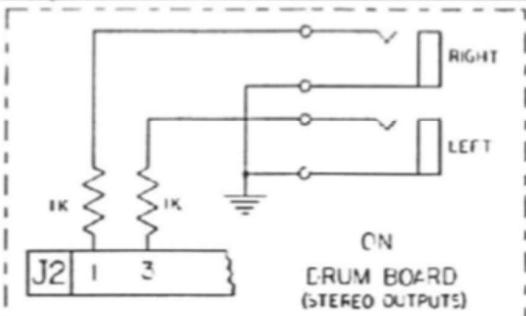




DPM SIGNAL  
INPUT  
FROM J2  
(SEE TABLE)



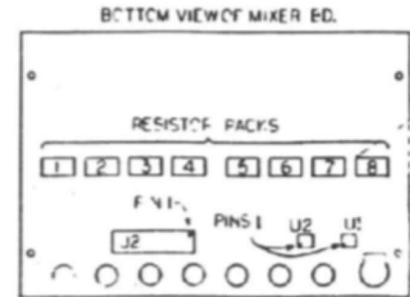
TYICAL OF 15 DRUMS AND CLICK



J2 40 PIN DIP CONNECTOR		PAD	RESISTOR PACK PIN-CUTS			
PIN NO.	FUNCTION	R VALUE	R1	R2	R3	R4
1	RIGHT CHANNEL OUT	RP#1	RP#2	RP#3	RP#4	RP#5
2	BASS	10Ω	RP2 3,14	RP2 4,13	RP1 1,2,3	RP1 1,2,4
3	LEFT CHANNEL OUT					
4	GND					
5	-15 VOLTS					
6	MID T.C.3	0Ω	RP4 2,15	RP4 1,16	RP3 7,7	RP3 9,8
7	+15 VOLTS					
8	SNARE	0Ω	RP2 2,15	RP2 1,16	RP1 10,7	RP1 9,8
9	S. STICK	0Ω	RP2 5,12	RP2 6,11	RP1 15,2	RP1 16,1
10	HAT	510Ω	RP2 7,10	RP2 5,9	RP1 11,6	RP1 12,5
11	LOW TOM	0Ω	RP4 5,12	RP4 4,11	RP3 13,4	RP3 14,3
12	CRASH	510Ω	RP6 5,11	RP6 5,12	RP5 14,3	RP5 13,4
13	COWBELL	510Ω	RP6 2,15	RP6 1,16	RP7 10,7	RP7 9,8
14	C CONGA	0Ω	RP8 6,11	RP8 5,12	RP7 14,3	RP7 13,4
15	H CONGA	0Ω	RP6 7,10	RP6 6,9	RP5 15,2	RP5 16,1
16	CAJASA	10KΩ	RP6 2,15	RP6 1,16	RP5 10,7	RP5 9,8
17	TAM5	10KΩ	RP6 5,14	RP6 4,13	RP5 11,6	RP5 12,5
18	NO CONNECTION					
19	CLK	0Ω	RP8 7	RP8 8,9	RP7 5,2	RP7 16,1
20	SWA= TUNING VOLTAGE	-				
21	NC CONNECTION					
22	NO CONNECTION					
23	NO CONNECTION					
24	H HIGH TUNING VOLTAGE	-				
25	MID TUNING VOLTAGE	-				
26	L LOW TUNING VOLTAGE	-				
27	L CONGA TUNING VOLTAGE	-				
28	H CONGA TUNING VOLTAGE	-				
29	CAPS	24KΩ	RP6 2,14	RP8 4,13	RP7 11,6	RP7 12,5
30	RIDE	10KΩ	RP4 7,10	RP4 8,9	RP3 15,2	RP3 16,1
31	NO CONNECTION					
32	NO CONNECTION					
33	NO CONNECTION					
34	-15 VOLTS					
35	NO CONNECTION					
36	NO CONNECTION					
37	HIT TOM	0Ω	RP4 4,13	RP4 3,14	RP3 12,5	RP3 11,6
38	BEEEP					
39	H HAT DECAY CONTROL OUTP. IT					
40	NO CONNECTION					

### NOTES:

- ① U1/U2 PIN 8 IS +15 VOLTS/PIN 4 IS -15 VOLTS.
- ② R1/R2 ARE IN THE SAME RESISTOR PACK.
- ③ R3/R4 ARE IN THE SAME RESISTOR PACK.
- ④ RP1, RP3, RP5, RP7 ARE ALL 4116R-R01-153.
- ⑤ RP2, RP4, RP6, RP8 ARE ALL 4116R-R01-1A2
- ⑥ ALL RESISTORS ARE ±% UNLESS OTHERWISE NOTED.



0	0	0	0	0	0	0	0
16	15	14	13	12	11	10	9
1	2	3	4	5	6	7	8
c	c	c	c	c	c	c	c

LINN ELECTRONICS  
LINN DRUM  
MXR BOARD  
REV. E 27 JAN 82  
*ml*

SQUARE  
TUNING

HITOM  
TUNING

MID  
TUNING

LOW TUNING  
TUNING

HI CGA  
TUNING

LOW CGA  
TUNING

Hihat  
DECAY

MASTER  
VOLUME

[R1]

[R2]

[R3]

[R4]

[R7]

[R2]

[R3]

[R4]

[R5]

BASS PAN

SNAR PAN

SSTK PAN

H HAT PAN

HI TOM PAN

MID TOM PAN

LOW TOM PAN

RIDE PAN

CRASH PAN

CBSA PAN

TAMB PAN

HI CGA PAN

LOW CGA PAN

COW PAN

CLAP PAN

CLICK PAN

RPI

RP2

RP3

RP4

RP5

RP6

RP7

RP8

[R16]

[R17]

BASS VOL

SNAR VOL

SSTK VOL

Hihat VOL

HI TOM VOL

MID TOM VOL

LOW TOM VOL

RIDE VOL

CRASH VOL

CBSA VOL

TAMB VOL

HI CGA VOL

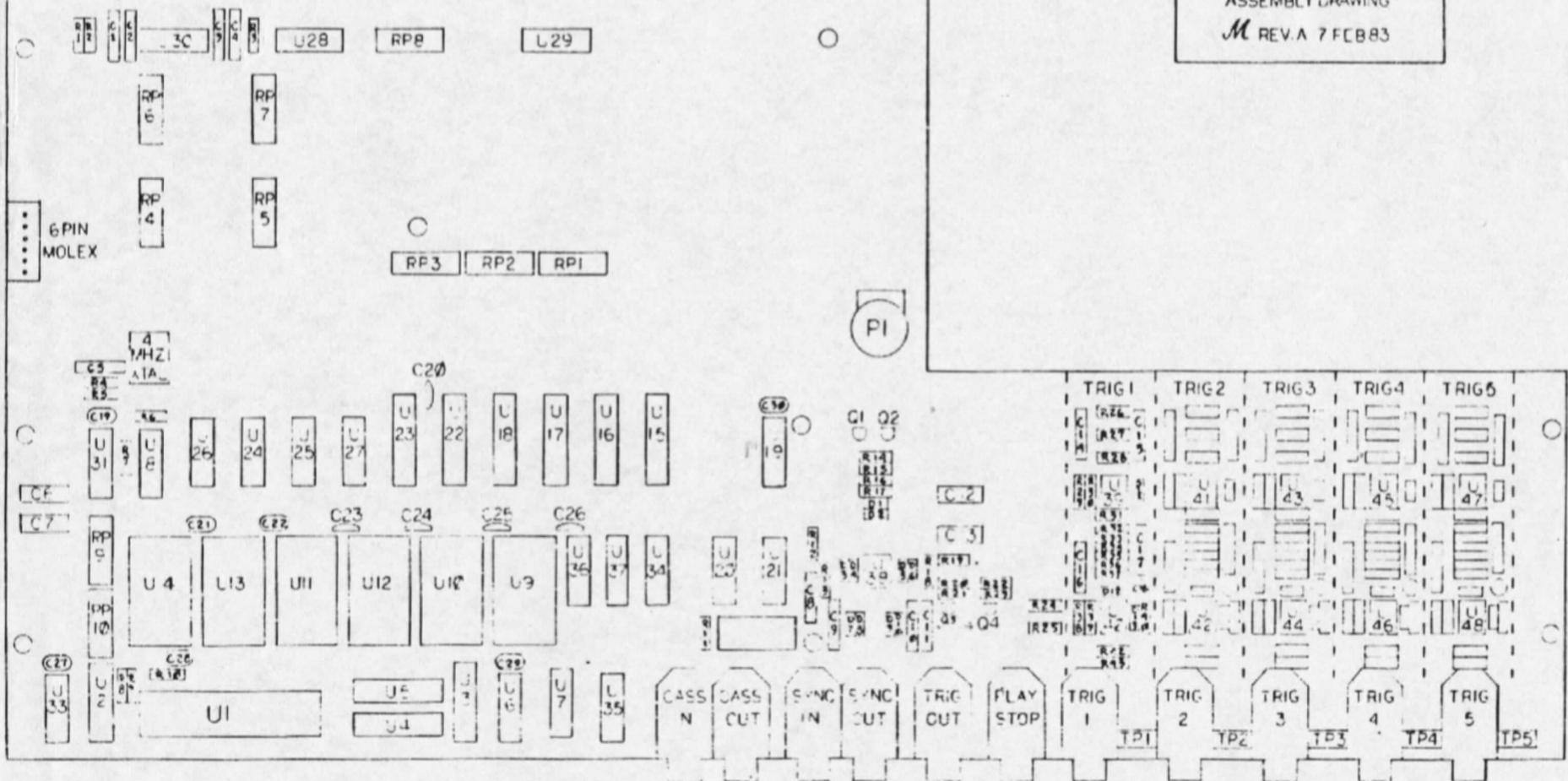
LOW CGA VOL

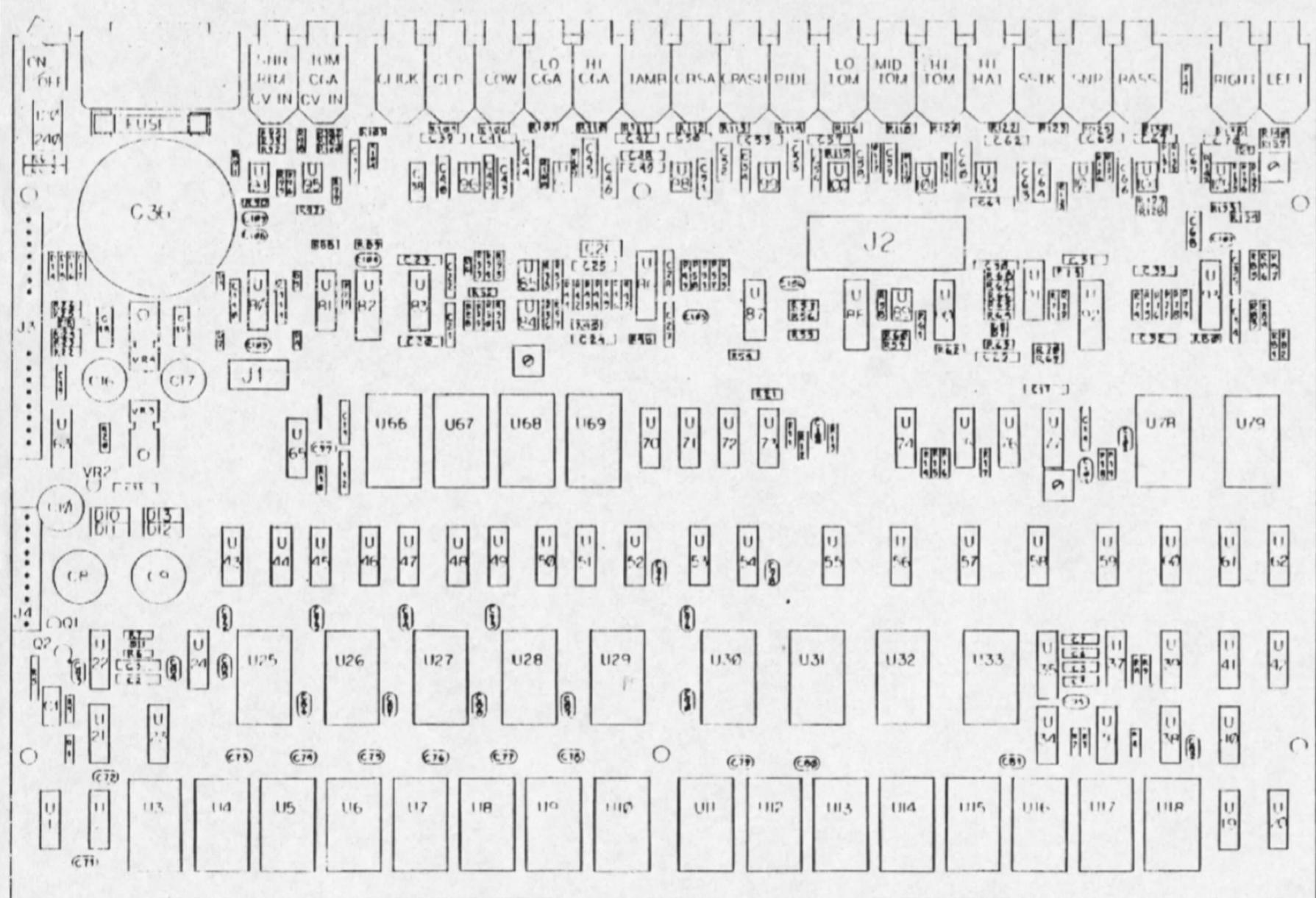
COW VOL

CLAP VOL

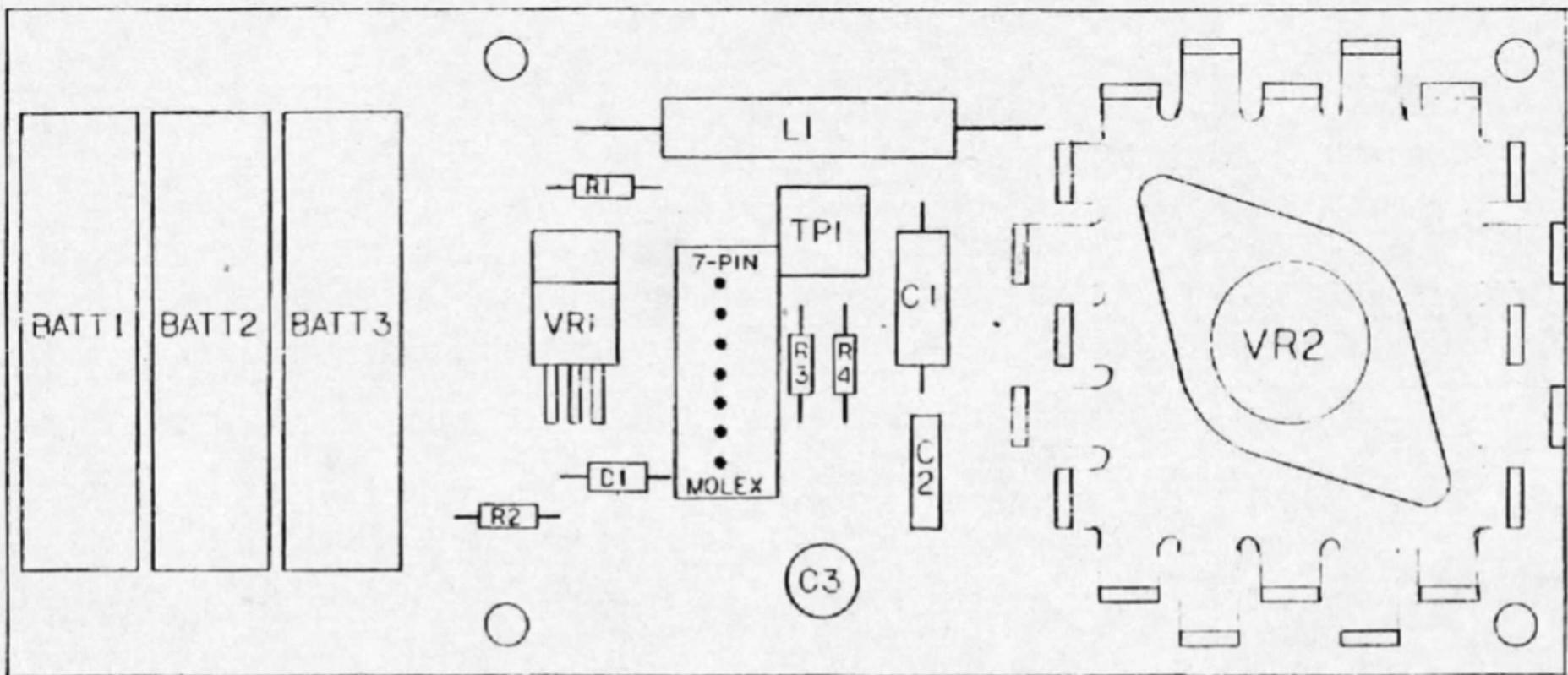
CLICK VOL

LINN ELECTRONICS  
 LINNDRUM  
 CPU BOARD  
 ASSEMBLY DRAWING  
*M* REV.A 7 FEB 83





LINN ELECTRONICS  
LinnDrum  
DEM BOARD  
ASSEMBLY DRAWING  
REV A ZEFERRA



LINN ELECTRONICS  
 LINN DRUM  
 5 VSR BOARD  
 ASSEMBLY DRAWING  
*M* REV A 8 FEB 83