ABSTRACT

A BJT Common-Emitter Circuit was built such that its' voltage gain was -10 for a 4.7kΩ load (which happened to match the value of the collector resistor in the circuit). The circuit was designed for an input voltage of 0.02 volts, which was fabricated with the output of a simple voltage divider to a 10 volt source. During the design procedure, the values of R_1, R_2, R_C, R_E, V_{CEQ}, I_{CQ}, h_{ie}, and h_{ib} were calculated and used in the circuit to the closest standard component value. The design will assumed an emitter capacitor is not used. The circuit was simulated with B2 SPICE to verify proper operation, and then built in lab. In the real DC portion of the circuit, the values of V_{CEQ} and I_{CQ} (the q-point of the circuit) and R_2 was adjusted until each was within 5% of the calculated value in the design. The AC portion was added and the voltage gain was calculated for the circuit. The load resistance was then varied proportionally to the collector resistor and the gain for each case was computed. Input and output voltage waveforms were sketched for each case, and then an emitter capacitor was added to the circuit and the whole process was repeated. It was concluded that the voltage gain of the circuit approached infinity as the load resistance did, and that adding an emitter capacitor to the circuit substantially increased the voltage gain (By about a factor of 10).

INTRODUCTION

A small signal AC, BJT Common-Emitter Amplifier is composed of AC input and output ports, coupling capacitors, and a simple DC Common-Emitter Transistor Circuit. The DC portion is usually built with a voltage divider biasing network for the transistor, a collector resistor to limit the current through the transistor, and an emitter resistor. The idea is to bias the transistor into the forward-active mode, so it may amplify voltage or current. The emitter resistor is included to allow for much lower and more practical resistance values in the divider network. The AC portion includes an AC source (In our case, the source was the FGEN of the board divided by a factor of 100), a load, and an output jack. The AC portions of the circuit are coupled off of the DC circuit with capacitors (our design used capacitances of 22 µF). This is done so the AC parts of the circuit do not affect the bias of the transistor. Figure 8.1 shows a circuit diagram of the design used.

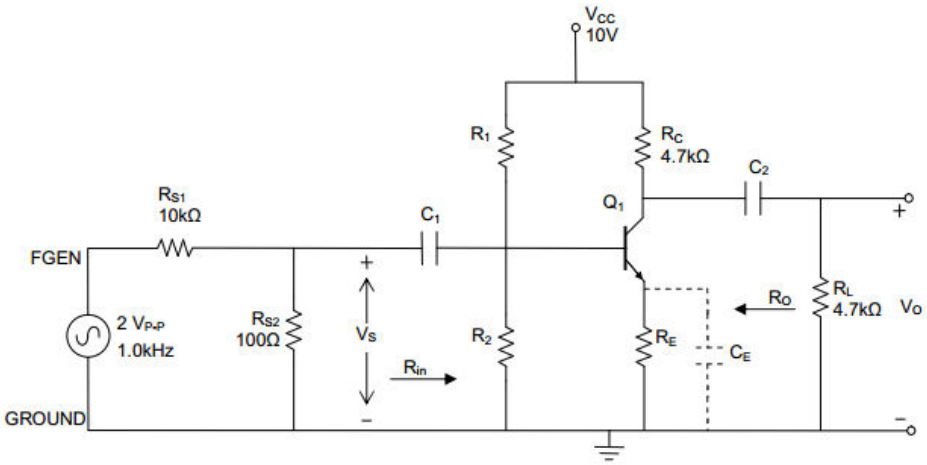

Figure 8.1: Circuit Design Diagram [1]

Once a common-emitter amplifier is operational, it inverts the input signal and multiplies it by factors dependent on the component values and design of the circuit. These factors are

called voltage and current gain, and can be determined as noted below (They are negative since a CE amplifier is an inverting amplifier and shifts the output 180 degrees out of phase from the input). Note when the load resistance of the circuit is infinite (or an open circuit), there is no current or voltage dropped at the load, so both the current and voltage gains of the amplifier will be maximized. Changing R_L will change the voltage and current gains, which is an idea that will be explored later in this report. Amplifiers also have input and output resistances, which are the Thevenin equivalent resistances seen at their input and output jacks, respectively. However, the scope of this lab only briefly explores this concept, so it will be ignored at large by this report.

$$A_v = -\frac{V_o}{V_i} \quad A_i = -\frac{I_O}{I_i}$$

BACKGROUND

Several pieces of information from the design procedure section of lab 8 in the manual [1] were referenced when writing this section.

All that is left in designing the amplifier is filling in the component values in Figure 8.1. However, the circuit at large is very complex and difficult to analyze in its current state. Right now, the diagram shows both AC and DC portions. However, if the circuit is simplified by drawing only the components operating at AC and their respective values, it takes a much simpler state that is much easier to analyze. The new circuit is called the small signal AC equivalent circuit, and it makes use of the hybrid π-model, which shows that at small signal AC, a transistor functions like a resistor (called a diffusion resistor (noted by r_π or h_{ib})) in parallel with a dependent current source. Also note that capacitors function as shorts at AC, and the design has chosen not to use an emitter capacitor. The small signal AC equivalent circuit for Figure 8.1 is shown in Figure 8.2.

Figures 8.2: Small Signal AC Equivalent Circuit

This new diagram reveals something interesting when the voltage gain formula is applied to it. The input voltage, or the denominator of the formula, while known to be 0.02 volts AC, can be more generally expressed as the emitter resistor in series with the input resistance (noted by the parameter h_{ie}) of the transistor. Likewise, the output can be shown to be the collector and load resistors in parallel. h_{ib} is still unknown, because it tends to be much less than R_E, it can be set to zero to obtain an approximation for R_E that will be correctly when h_{ib} is known.

$$A_V = -\frac{R_L||R_C}{R_{E,approx}}$$

$$R_{E,approx} = \frac{-(R_L||\,R_C)}{A_v}$$

$$R_{E,approx} = \frac{-(4.7\ k\Omega\ ||\ 4.7\ k\Omega)}{-10} \approx 235\ \Omega$$

Finding the quiescent point of the circuit at DC requires knowledge of the BJT used and its properties. Thankfully, the 2N3904 transistor implemented used in the design is the same transistor used in the previous transistor labs, so beta and V_{BE} (on) are known to be 220 and 0.67 volts from those labs. We also need to know the resistances of the transistor at AC (R_{ac}) and at DC (R_{dc}), which are both easily found as:

$$R_{ac} = (R_C \,||\, R_L) + R_E = 2.35\ k\Omega + 235\ \Omega \approx 2.585\ k\Omega$$
$$R_{dc} = R_C + R_E = 4.7\ k\Omega + 235\ \Omega \approx 4.935\ k\Omega$$

This makes finding V_{CEQ} and I_{CQ} a matter of plugging in numbers:

$$I_{CQ} = \frac{V_{CC}}{R_{ac} + R_{dc}} = \frac{(10\ V)}{(2.585\ k\Omega + 4.935\ k\Omega)} = 1.32979\ mA$$
$$V_{CEQ} = I_{CQ} R_{ac} = (1.33\ mA)(2.585\ k\Omega) = 3.4375\ V$$

Now, the values of r_π and h_{ib} are given as:

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{(220)(0.026\ V)}{1.33\ mA} \approx 4.301\ k\Omega$$
$$h_{ib} = \frac{r_\pi}{\beta} = \frac{4.3\ k\Omega}{220} \approx 19.552\ \Omega$$

Since h_{ib} is now known, correcting $R_{E,approx.}$ is very simple:

$$R_E = R_{E,approx} - h_{ib} = 235\ \Omega - 19.552\ \Omega \approx 215\ \Omega$$

The only values left to find are the resistances of the resistors in the bias network, R_1 and R_2. Starting from the basics, since the circuit must be bias stable, the following is known about their Thevenin equivalent resistance:

$$R_{TH} = 0.1\beta R_E = 0.1(220)(215\ \Omega) = 4.73986\ k\Omega$$

By association, the Thevenin equivalent voltage of the bias network is:

$$V_{TH} = V_{BB} = V_{BE}(on) + I_{BQ} R_B + I_{CQ} R_E = 0.9851\ V$$

Finally, R_1 and R_2 can be given by:

$$R_2 = \frac{R_B}{\left(1 - \frac{V_{BB}}{V_{CC}}\right)} = \frac{R_{TH}}{\left(1 - \frac{V_{TH}}{V_{CC}}\right)} = \frac{(4.74\ k\Omega)}{\left(1 - \frac{0.985\ V}{10\ V}\right)} \approx 5\ k\Omega$$
$$R_1 = R_{TH} \cdot \frac{V_{CC}}{V_{TH}} = (4.74\ k\Omega) \cdot \frac{10\ V}{0.9851\ V} = 48\ k\Omega$$

For convenience, this report lists all of the calculated design parameters in Figure 8.3.

Parameter	Value
B	220
R_E	215 Ω
R_1	48 kΩ
R_2	5 kΩ
R_C	4.7 kΩ
h_{ie}	19.552 Ω
h_{ib}	215 Ω
I_{CQ}	1.33 mA
V_{CEQ}	3.44 V

Figure 8.3: Design Parameters

EXPERIMENTAL PROCEDURE

The DC portion of the circuit in Figure 8.1 was constructed with the values specified in Figure 8.3. The voltage from the transistor's collector to ground and the voltage from the transistor's emitter to ground were measured and used to find V_{CEQ}. The current coming from the collector was measured as well, and both values were compared to the values from design in figure 8.3. Because the actual values varied from the design values by more than five percent, R_2 was replaced with a resistor decade box and varied until the values were within. The measurements for the initial value of R_2 and the used value of R_2 are shown in Figure 8.4.

Resistance	V_{C0}	V_{E0}	V_{CEQ}	I_{CQ}	V_{CEQ} % Accuracy	I_{CQ} % Accuracy
R_2 = 5 kΩ (Fixed)	4.62 V	0.256 V	4.37 V	1.14 mA	65.6	85.71
R_2 = 5.4 kΩ (Decade Box)	3.74 V	0.297 V	3.45 V	1.39 mA	91.2	95.49

Figure 8.4: Bias Modifications

Afterwards, the AC portion of the circuit was added, making the complete circuit in Figure 8.1. R_L was initially set to the value of R_C and then varied to be a tenth of R_C and ten times R_C. For each case, the gain at the load was measured, sketched, and compared to the simulated values. Then, a filter capacitor was added to the circuit and the process was repeated. Figure 8.5 shows the data measured in lab, Figure 8.6 shows the corresponding simulated data, and Figure 8.7 shows graphs of each waveform. In Figure 8.7, the two graphs marked "Scaled" had to be put on a different on their own separate scales, because their amplitudes were initially way higher than the oscilloscope's screen could display. All other graphs are on an identical scale.

R_L	$V_{O\text{-}PP}$		A_V	
	With C_E	Without C_E	With C_E	Without C_E
$0.1R_C$	351.26 mV	34.13 mV	-17.56	-1.75
R_C	1.90 V	187.14 mV	-95.15	-9.58
$10R_C$	3.41 V	388.71 mV	-170.55	-17.31

Figure 8.5: AC Gain Measurements

R_L	$V_{O\text{-}PP}$		A_V	
	With C_E	Without C_E	With C_E	Without C_E
$0.1R_C$	324.85 mV	35.06 mV	-16.24	-1.75
R_C	1.77 V	192.07 mV	-88.5	-9.6
$10R_C$	3.41 V	350 mV	-170.5	-17.5

Figure 8.6: Simulated AC Gain Measurements

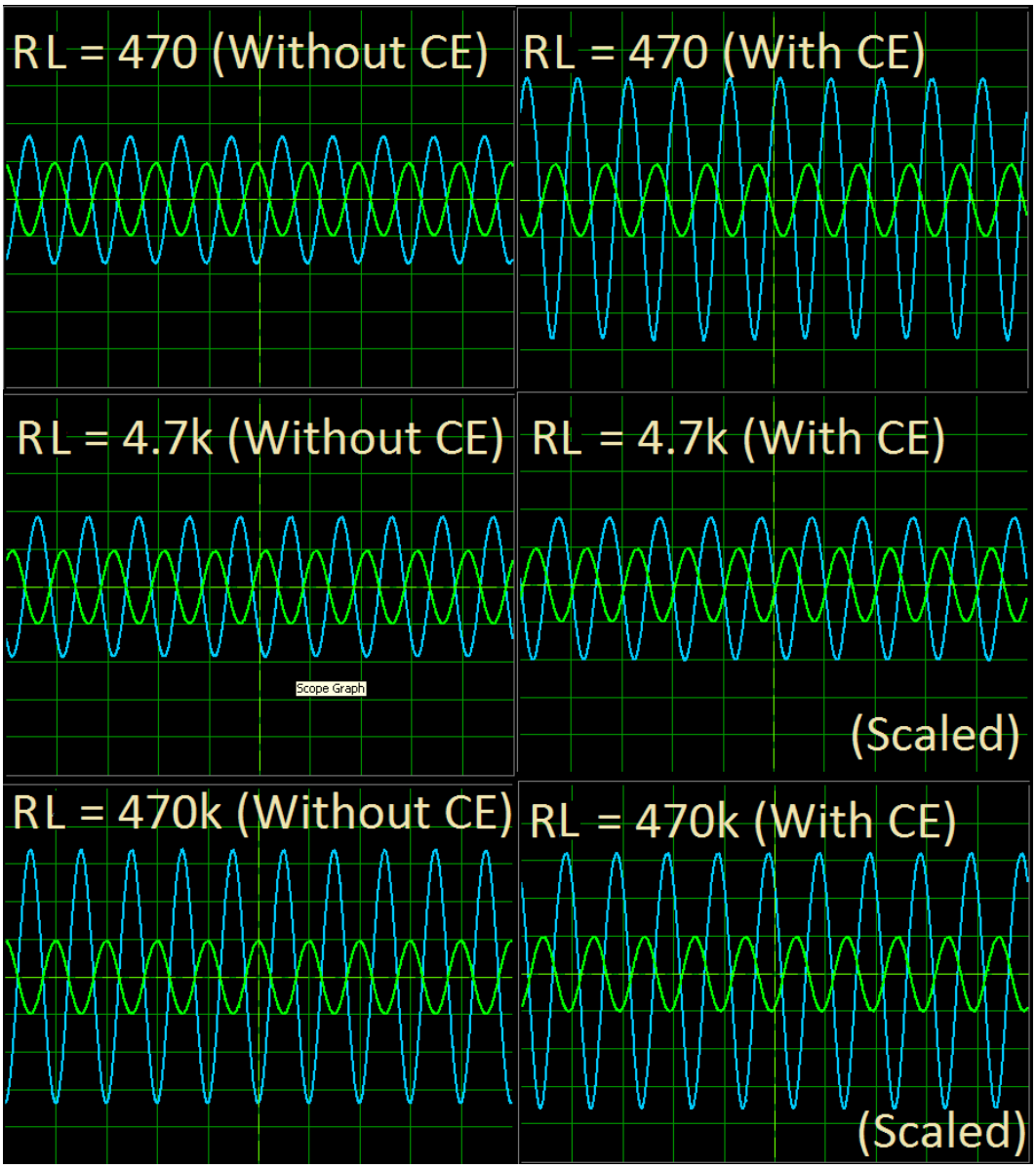

Figure 8.7: Graphs of Input Voltage versus Output Voltage for Gain Measurements

Because time in the lab allotted, the output resistance of the circuit quickly measured. This was done by removing R_L and C_E, and then measuring the open circuit gain. A resistor decade box was then added and adjusted until the gain was exactly half of the open circuit gain. At this point, the voltage on the load was equal to the voltage on the output. The output and load create what is essentially an imaginary voltage divider, so for both voltages to be equal, the resistances of the load and output must be equal. Therefore, the load resistance at this point is equal to the output resistance (which is the Thevenin resistance a load sees when connected to the amplifier). Figure 8.8 shows the steps in this process.

$V_{O\text{-}PP}$ (Open Circuit)	Target $V_{O\text{-}PP}$	Target A_V	Output Resistance (R_O)
371.65 mV	185.825 mV	-9.29	4.56 kΩ

Figure 8.8: Key Values for Calculating Output Resistance

DISCUSSION OF EXPERIMENTAL RESULTS

The design process determined that the component values in Figure 8.3 should be used with a 4.7 kΩ load resistor to hit a target voltage gain of A_v equal to -10 without an emitter capacitor. Figure 8.5 clearly shows that the actual voltage gain in this case was A_v = -9.58, which is reasonably close to -10, especially when factoring in tolerance values for each component. This validates that the logic used in the design process, and that the circuit has effectively reached its goal in design.

Additionally, as discussed several times above in DC analysis, including an emitter resistor in an amplifier is beneficial because it allows for R_1 and R_2 to be much smaller values while still biasing the transistor in the same manner. However, there is a trade-off: At AC, the emitter resister causes the gain of the circuit to become significantly less than it would be with the same component values everywhere else in the circuit. Because the capacitors used act as open circuits at DC and short circuits at AC, this is seen very easily in Figures 8.5 through 8.7. When C_E is removed, R_E becomes included in the AC equivalent circuit, and the gains of the amplifier at different values of R_L is dwindled by almost a factor of ten. Keep in mind that the C_E graphs for R_L = 4.7 kΩ and R_L = 47 kΩ had to be scaled separately from all of the other graphs, and that the amplitudes for those graphs were much larger than the others.

The data trends are due to a property called the Resistance reflection rule, which is useful in the AC small signal analysis of BJT amplifiers. The rule provides a way to calculate the exact resistance from the input of the amplifier to the base (R_{ib}), but also states that the voltage across the emitter resistor at AC, V_{re}, must be:

$$V_{re} = (1 + \beta) I_b R_E$$

This portion of the rule comes from the facts that $I_c = \beta I_b$ and $I_e = I_c + I_b$ for an NPN transistor in forward active mode. If R_E is zero at AC (or the emitter is connected directly to ground), V_{re} is zero and no voltage is dropped from the output, so $V_o = V_{RC}$ and the gain of the amplifier is maximized for its component values. However, when R_E is non-zero at AC, because typical values of β range from about 100 to 250, 1 + β is a very large number that magnifies V_{re} to a very considerable amount of voltage. This means that V_o must now be $V_{RC} - V_{RE}$, which is considerably less than V_{RC} in parallel V_{RL}. Therefore, the data follows the expected mathematical trends.

Figure 8.7 also shows that as the load resistance of the circuit increases, the amplitude of the output voltage increase and, by association, the voltage gain of the circuit increases. This also makes sense, since $V_{RC} = V_{RL} = \beta I_b (R_C \parallel R_L)$ from simple circuit analysis of Figure 8.2. The larger the collector resistor in parallel with the load resistor, the larger V_o and the larger the voltage gain of the circuit.

Figure 8.6 shows the simulated data is almost exactly on par with the actual data, and the simulated data shows the same mathematical trends as discussed above. Therefore, the simulated data checks with the real values.

While it was not the primary focus of this lab, the numbers shown for the output resistance of the amplifier in Figure 8.8 make sense, as a typical BJT common-emitter amplifier is expected to have moderate to high output resistance, and 4.5 kΩ falls directly in this range.

CONCLUSIONS

Since a resistor decade box was allowed to be used to correct R_2 to stabilize the circuit's Q-point to the Q-point used in design (shown in Figure 8.4), the values of A_v in the simulated and real circuits do not differ by very much (shown in Figures 8.5 and 8.6). The slight differences are due to tolerance values of the real components, as previously discussed. Once the Q-point was stabilized, all measured gains agreed with the expected values from design, shown in the simulated data.

The voltage gain of the circuit will vary greatly with its' DC operating point at the same component values, so the choice of Q-point was very important to the circuit, and correcting the actual Q-point to match the Q-point specified in design was very important to getting the expected voltage gains shown by the simulations to match the actual voltage gains in the real circuit. While V_{BE} is supposed to always be 0.67 volts, it does vary slightly at small signal AC. This is why the hybrid-π model for a transistor includes r_π in between the base and emitter of the transistor in the first place, as V_π exists to model these variations. V_π does not move the Q-point of the circuit, but it does affect the bias stability of the circuit around the Q-point if V_π is large, as discussed in the design process.

The data trends have shown that increasing R_L increases A_v, which follows the mathematical trends because the voltage gain of the amplifier is maximized when the resistance at the load is infinite, or an open circuit. They have also shown that including C_E, which shorts R_E at AC, dramatically improves the voltage gain of the circuit for the same component values. This matches the simulated and expected data, since R_E helps simplify the bias network at DC, but drops a considerable amount of voltage from the output if it is included at AC.

Acknowledgements: My lab partners were David Saxton and Joshua Blake.

References:

1. D J Dumin (Edited by J E Harriss), ECE 311 LABORATORY MANUAL VER 1.5, pg. 68 to 73, Clemson University, Clemson, SC, July 2011.