PSoC® Creator™
Project Datasheet for Number2

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1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through JTAG, serial wire debug (SWD), and single wire viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C58LP series member PSoC 5LP device. For details on all the systems listed above, please refer to the PSoC 5LP Technical Reference Manual.

Figure 1. CY8C58LP Device Series Block Diagram

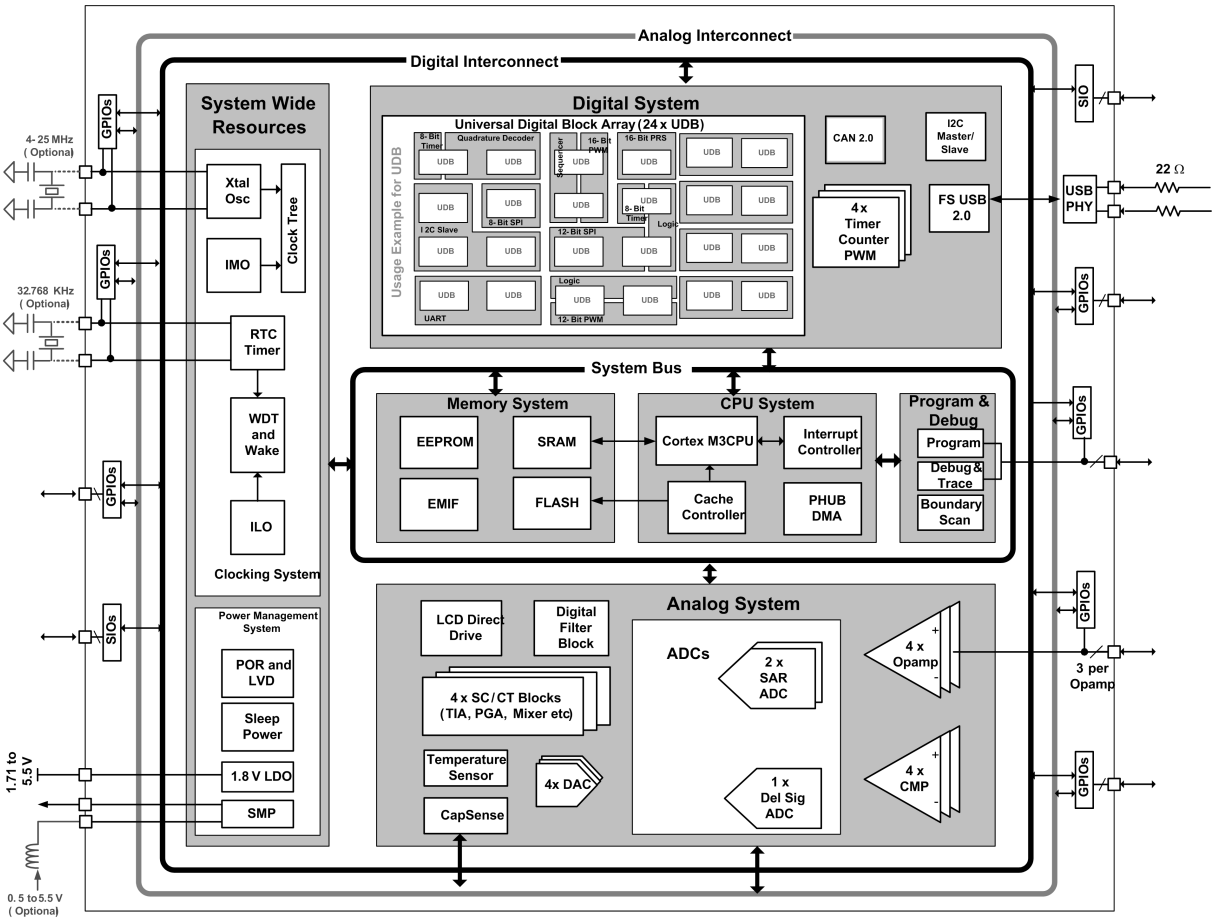


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CY8C5888LTI-LP097
Package Name	68-QFN
Family	PSoC 5LP
Series	CY8C58LP
Max CPU speed (MHz)	80
Flash size (kB)	256
SRAM size (kB)	64
EEPROM size (bytes)	2048
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85
JTAG ID	0x2E161069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by Bus Clock, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

Table 2. Device Resources

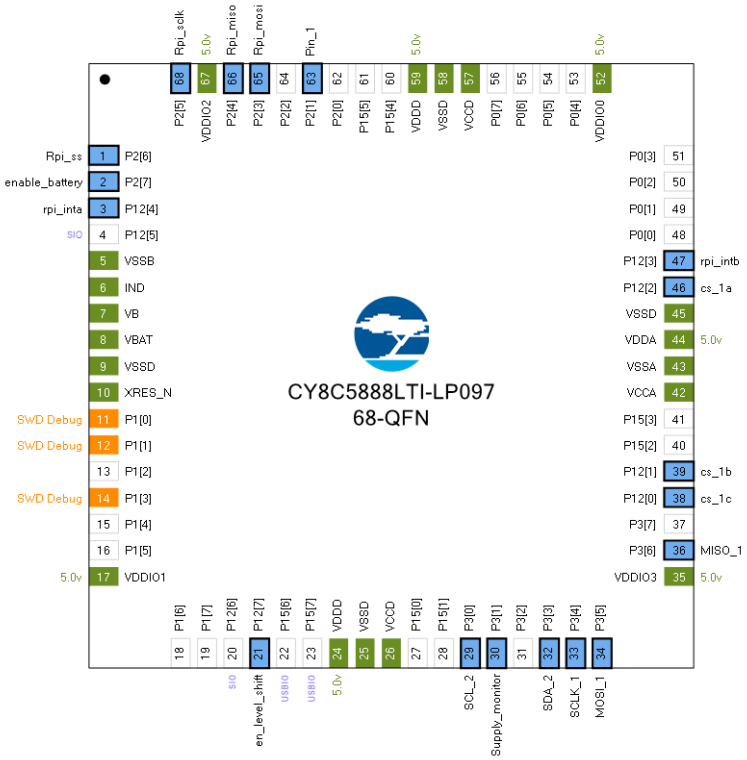
Resource Type	Used	Free	Max	% Used
Digital Clocks	4	4	8	50.00 %
Analog Clocks	0	4	4	0.00 %
CapSense Buffers	0	2	2	0.00 %
Digital Filter Block	0	1	1	0.00 %
Interrupts	1	31	32	3.13 %
IO	21	27	48	43.75 %
Segment LCD	0	1	1	0.00 %
CAN 2.0b	0	1	1	0.00 %
I2C	0	1	1	0.00 %
USB	0	1	1	0.00 %
DMA Channels	2	22	24	8.33 %
Timer	0	4	4	0.00 %
UDB				
Macrocells	63	129	192	32.81 %
Unique P-terms	153	231	384	39.84 %
Total P-terms	160			
Datapath Cells	6	18	24	25.00 %
Status Cells	10	14	24	41.67 %
Status Registers	1			
StatusI Registers	5			
Sync Cells (x5)	2			
Routed Count7 Load/Enable	2			
Control Cells	7	17	24	29.17 %
Control Registers	5			
Count7 Cells	2			
Opamp	0	4	4	0.00 %
Comparator	1	3	4	25.00 %
Delta-Sigma ADC	0	1	1	0.00 %
LPF	0	2	2	0.00 %
SAR ADC	0	2	2	0.00 %

Resource Type	Used	Free	Max	% Used
Analog (SC/CT) Blocks	0	4	4	0.00 %
DAC				
VIDAC	0	4	4	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[6]	Rpi_ss	Dgtl In	HiZ digital	HiZ Analog Unb
2	P2[7]	enable_battery	Dgtl Out	Strong drive	HiZ Analog Unb
3	P12[4]	rpi_inta	Dgtl Out	Strong drive	HiZ Analog Unb
4	P12[5]	SIO [unused]			HiZ Analog Unb
5	VSSB	VSSB	Dedicated		
6	IND	IND	Dedicated		
7	VB	VB	Dedicated		
8	VBAT	VBAT	Dedicated		
9	VSSD	VSSD	Power		
10	XRES_N	XRES_N	Dedicated		
11	P1[0]	Debug:SWD_IO	Reserved		
12	P1[1]	Debug:SWD_CK	Reserved		
13	P1[2]	GPIO [unused]			HiZ Analog Unb
14	P1[3]	Debug:SWV	Reserved		
15	P1[4]	GPIO [unused]			HiZ Analog Unb
16	P1[5]	GPIO [unused]			HiZ Analog Unb
17	VDDIO1	VDDIO1	Power		
18	P1[6]	GPIO [unused]			HiZ Analog Unb
19	P1[7]	GPIO [unused]			HiZ Analog Unb
20	P12[6]	SIO [unused]			HiZ Analog Unb
21	P12[7]	en_level_shift	Dgtl Out	Strong drive	HiZ Analog Unb
22	P15[6]	USB IO [unused]			HiZ Analog Unb
23	P15[7]	USB IO [unused]			HiZ Analog Unb
24	VDDD	VDDD	Power		
25	VSSD	VSSD	Power		
26	VCCD	VCCD	Power		
27	P15[0]	GPIO [unused]			HiZ Analog Unb
28	P15[1]	GPIO [unused]			HiZ Analog Unb
29	P3[0]	SCL_2	Dgtl I/O	Res pull up	HiZ Analog Unb
30	P3[1]	Supply_monitor	Analog	HiZ analog	HiZ Analog Unb
31	P3[2]	GPIO [unused]			HiZ Analog Unb
32	P3[3]	SDA_2	Dgtl I/O	Res pull up	HiZ Analog Unb
33	P3[4]	SCLK_1	Dgtl Out	Strong drive	HiZ Analog Unb
34	P3[5]	MOSI_1	Dgtl Out	Strong drive	HiZ Analog Unb
35	VDDIO3	VDDIO3	Power		
36	P3[6]	MISO_1	Dgtl In	Res pull up	HiZ Analog Unb
37	P3[7]	GPIO [unused]			HiZ Analog Unb
38	P12[0]	cs_1c	Dgtl Out	Strong drive	HiZ Analog Unb
39	P12[1]	cs_1b	Dgtl Out	Strong drive	HiZ Analog Unb
40	P15[2]	GPIO [unused]			HiZ Analog Unb
41	P15[3]	GPIO [unused]			HiZ Analog Unb
42	VCCA	VCCA	Power		
43	VSSA	VSSA	Power		
44	VDDA	VDDA	Power		
45	VSSD	VSSD	Power		

Pin	Port	Name	Type	Drive Mode	Reset State
46	P12[2]	cs_1a	Dgtl Out	Strong drive	HiZ Analog Unb
47	P12[3]	rpi_intb	Dgtl Out	Strong drive	HiZ Analog Unb
48	P0[0]	GPIO [unused]			HiZ Analog Unb
49	P0[1]	GPIO [unused]			HiZ Analog Unb
50	P0[2]	GPIO [unused]			HiZ Analog Unb
51	P0[3]	GPIO [unused]			HiZ Analog Unb
52	VDDIO0	VDDIO0	Power		
53	P0[4]	GPIO [unused]			HiZ Analog Unb
54	P0[5]	GPIO [unused]			HiZ Analog Unb
55	P0[6]	GPIO [unused]			HiZ Analog Unb
56	P0[7]	GPIO [unused]			HiZ Analog Unb
57	VCCD	VCCD	Power		
58	VSSD	VSSD	Power		
59	VDDD	VDDD	Power		
60	P15[4]	GPIO [unused]			HiZ Analog Unb
61	P15[5]	GPIO [unused]			HiZ Analog Unb
62	P2[0]	GPIO [unused]			HiZ Analog Unb
63	P2[1]	Pin_1	Dgtl Out	Strong drive	HiZ Analog Unb
64	P2[2]	GPIO [unused]			HiZ Analog Unb
65	P2[3]	Rpi_mosi	Dgtl In	HiZ digital	HiZ Analog Unb
66	P2[4]	Rpi_miso	Dgtl Out	Strong drive	HiZ Analog Unb
67	VDDIO2	VDDIO2	Power		
68	P2[5]	Rpi_sclk	Dgtl In	HiZ digital	HiZ Analog Unb

Abbreviations used in Table 3 have the following meanings:

- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl I/O = Digital In/Out
- Res pull up = Resistive pull up
- HiZ analog = High impedance analog

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode	Reset State
P0[0]	48	GPIO [unused]			HiZ Analog Unb
P0[1]	49	GPIO [unused]			HiZ Analog Unb
P0[2]	50	GPIO [unused]			HiZ Analog Unb
P0[3]	51	GPIO [unused]			HiZ Analog Unb
P0[4]	53	GPIO [unused]			HiZ Analog Unb
P0[5]	54	GPIO [unused]			HiZ Analog Unb
P0[6]	55	GPIO [unused]			HiZ Analog Unb
P0[7]	56	GPIO [unused]			HiZ Analog Unb
P1[0]	11	Debug:SWD_IO	Reserved		
P1[1]	12	Debug:SWD_CK	Reserved		
P1[2]	13	GPIO [unused]			HiZ Analog Unb
P1[3]	14	Debug:SWV	Reserved		
P1[4]	15	GPIO [unused]			HiZ Analog Unb
P1[5]	16	GPIO [unused]			HiZ Analog Unb
P1[6]	18	GPIO [unused]			HiZ Analog Unb
P1[7]	19	GPIO [unused]			HiZ Analog Unb
P12[0]	38	cs_1c	Dgtl Out	Strong drive	HiZ Analog Unb
P12[1]	39	cs_1b	Dgtl Out	Strong drive	HiZ Analog Unb
P12[2]	46	cs_1a	Dgtl Out	Strong drive	HiZ Analog Unb
P12[3]	47	rpi_intb	Dgtl Out	Strong drive	HiZ Analog Unb
P12[4]	3	rpi_inta	Dgtl Out	Strong drive	HiZ Analog Unb
P12[5]	4	SIO [unused]			HiZ Analog Unb
P12[6]	20	SIO [unused]			HiZ Analog Unb
P12[7]	21	en_level_shift	Dgtl Out	Strong drive	HiZ Analog Unb
P15[0]	27	GPIO [unused]			HiZ Analog Unb
P15[1]	28	GPIO [unused]			HiZ Analog Unb
P15[2]	40	GPIO [unused]			HiZ Analog Unb
P15[3]	41	GPIO [unused]			HiZ Analog Unb
P15[4]	60	GPIO [unused]			HiZ Analog Unb
P15[5]	61	GPIO [unused]			HiZ Analog Unb
P15[6]	22	USB IO [unused]			HiZ Analog Unb
P15[7]	23	USB IO [unused]			HiZ Analog Unb
P2[0]	62	GPIO [unused]			HiZ Analog Unb
P2[1]	63	Pin_1	Dgtl Out	Strong drive	HiZ Analog Unb
P2[2]	64	GPIO [unused]			HiZ Analog Unb
P2[3]	65	Rpi_mosi	Dgtl In	HiZ digital	HiZ Analog Unb
P2[4]	66	Rpi_miso	Dgtl Out	Strong drive	HiZ Analog Unb
P2[5]	68	Rpi_sclk	Dgtl In	HiZ digital	HiZ Analog Unb
P2[6]	1	Rpi_ss	Dgtl In	HiZ digital	HiZ Analog Unb
P2[7]	2	enable_battery	Dgtl Out	Strong drive	HiZ Analog Unb
P3[0]	29	SCL_2	Dgtl I/O	Res pull up	HiZ Analog Unb
P3[1]	30	Supply_monitor	Analog	HiZ analog	HiZ Analog Unb
P3[2]	31	GPIO [unused]			HiZ Analog Unb
P3[3]	32	SDA_2	Dgtl I/O	Res pull up	HiZ Analog Unb
P3[4]	33	SCLK_1	Dgtl Out	Strong drive	HiZ Analog Unb

Port	Pin	Name	Type	Drive Mode	Reset State
P3[5]	34	MOSI_1	Dgtl Out	Strong drive	HiZ Analog Unb
P3[6]	36	MISO_1	Dgtl In	Res pull up	HiZ Analog Unb
P3[7]	37	GPIO [unused]			HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl Out = Digital Output
- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- Dgtl I/O = Digital In/Out
- Res pull up = Resistive pull up
- HiZ analog = High impedance analog

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type	Reset State
cs_1a	P12[2]	Dgtl Out	HiZ Analog Unb
cs_1b	P12[1]	Dgtl Out	HiZ Analog Unb
cs_1c	P12[0]	Dgtl Out	HiZ Analog Unb
Debug:SWD_CK	P1[1]	Reserved	
Debug:SWD_IO	P1[0]	Reserved	
Debug:SWV	P1[3]	Reserved	
en_level_shift	P12[7]	Dgtl Out	HiZ Analog Unb
enable_battery	P2[7]	Dgtl Out	HiZ Analog Unb
GPIO [unused]	P15[1]		HiZ Analog Unb
GPIO [unused]	P15[3]		HiZ Analog Unb
GPIO [unused]	P0[0]		HiZ Analog Unb
GPIO [unused]	P15[0]		HiZ Analog Unb
GPIO [unused]	P15[4]		HiZ Analog Unb
GPIO [unused]	P3[7]		HiZ Analog Unb
GPIO [unused]	P15[2]		HiZ Analog Unb
GPIO [unused]	P2[0]		HiZ Analog Unb
GPIO [unused]	P3[2]		HiZ Analog Unb
GPIO [unused]	P15[5]		HiZ Analog Unb
GPIO [unused]	P0[1]		HiZ Analog Unb
GPIO [unused]	P1[2]		HiZ Analog Unb
GPIO [unused]	P1[4]		HiZ Analog Unb
GPIO [unused]	P1[5]		HiZ Analog Unb
GPIO [unused]	P0[7]		HiZ Analog Unb
GPIO [unused]	P0[6]		HiZ Analog Unb
GPIO [unused]	P0[5]		HiZ Analog Unb
GPIO [unused]	P0[3]		HiZ Analog Unb
GPIO [unused]	P0[2]		HiZ Analog Unb
GPIO [unused]	P2[2]		HiZ Analog Unb
GPIO [unused]	P0[4]		HiZ Analog Unb
GPIO [unused]	P1[6]		HiZ Analog Unb
GPIO [unused]	P1[7]		HiZ Analog Unb
MISO_1	P3[6]	Dgtl In	HiZ Analog Unb
MOSI_1	P3[5]	Dgtl Out	HiZ Analog Unb
Pin_1	P2[1]	Dgtl Out	HiZ Analog Unb
rpi_inta	P12[4]	Dgtl Out	HiZ Analog Unb
rpi_intb	P12[3]	Dgtl Out	HiZ Analog Unb
Rpi_miso	P2[4]	Dgtl Out	HiZ Analog Unb
Rpi_mosi	P2[3]	Dgtl In	HiZ Analog Unb
Rpi_sclk	P2[5]	Dgtl In	HiZ Analog Unb
Rpi_ss	P2[6]	Dgtl In	HiZ Analog Unb
SCL_2	P3[0]	Dgtl I/O	HiZ Analog Unb
SCLK_1	P3[4]	Dgtl Out	HiZ Analog Unb
SDA_2	P3[3]	Dgtl I/O	HiZ Analog Unb
SIO [unused]	P12[5]		HiZ Analog Unb
SIO [unused]	P12[6]		HiZ Analog Unb

Name	Port	Type	Reset State
Supply_monitor	P3[1]	Analog	HiZ Analog Unb
USB IO [unused]	P15[7]		HiZ Analog Unb
USB IO [unused]	P15[6]		HiZ Analog Unb

Abbreviations used in Table 5 have the following meanings:

- Dgtl Out = Digital Output
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- Dgtl I/O = Digital In/Out

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	DMA
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	False
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x80
Stack Size (bytes)	0x0800
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	SWD+SWV (serial wire debug and viewer)
Enable Device Protection	False
Embedded Trace (ETM)	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 8. System Operating Conditions

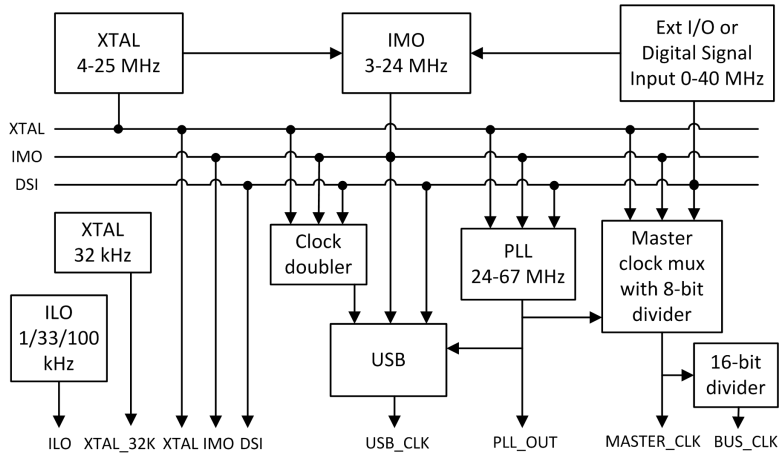
Name	Value
VDDA (V)	5.0
VDDD (V)	5.0
VDDIO0 (V)	5.0
VDDIO1 (V)	5.0
VDDIO2 (V)	5.0
VDDIO3 (V)	5.0
Variable VDDA	False
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 74.7 MHz Internal Main Oscillator (IMO) ±1% at 3 MHz
  - 1 kHz, 33 kHz, and 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - 12 to 80 MHz clock doubler output, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 80 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
BUS_CLK	DIGITAL	MASTER_CLK	? MHz	24 MHz	±1	True	True
PLL_OUT	DIGITAL	IMO	24 MHz	24 MHz	±1	True	True
MASTER_CLK	DIGITAL	PLL_OUT	? MHz	24 MHz	±1	True	True
IMO	DIGITAL		3 MHz	3 MHz	±1	True	True
ILO	DIGITAL		? MHz	1 kHz	-50,+100	True	True
USB_CLK	DIGITAL	IMO	48 MHz	? MHz	±0	False	False
XTAL	DIGITAL		25 MHz	? MHz	±0	False	False
XTAL_32KHZ	DIGITAL		32.768 kHz	? MHz	±0	False	False
Digital_Signal	DIGITAL		? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

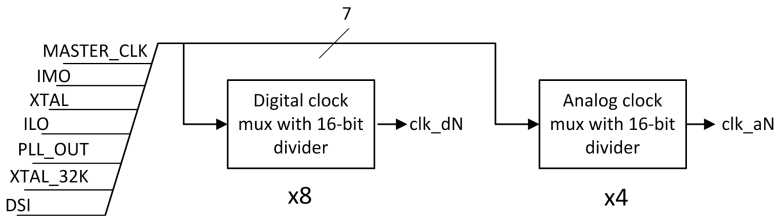


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
Clock_2	DIGITAL	MASTER_CLK	12 MHz	12 MHz	±1	True	True
I2C_1_IntClock	DIGITAL	MASTER_CLK	6.4 MHz	6 MHz	±1	True	True
SPIM_1_-IntClock	DIGITAL	MASTER_CLK	2 MHz	2 MHz	±1	True	True
Clock_1	DIGITAL	MASTER_CLK	10 kHz	10 kHz	±1	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 5LP Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CyPLL API routines
  - CyIMO API routines
  - CyILO API routines
  - CyMaster API routines
  - CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	Vector	Priority
I2C_1_I2C_IRQ	0	0	7

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 5LP Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains the following DMA components: (0 is the highest priority)

Table 12. DMAs

Name	Priority	Channel Number
DMA_RX	2	0
DMA_TX	2	1

For more information on DMAs, please refer to:

- PHUB and DMAC chapter in the PSoC 5LP Technical Reference Manual
- DMA chapter in the System Reference Guide
  - DMA API routines and related registers
- Datasheet for cy_dma component

6 Flash Memory

PSoC 5LP devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 13 lists the Flash protection settings for your design.

Table 13. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x3FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - Factory Upgrade
- R - Field Upgrade
- W - Full Protection

For more information on Flash memory and protection, please refer to:

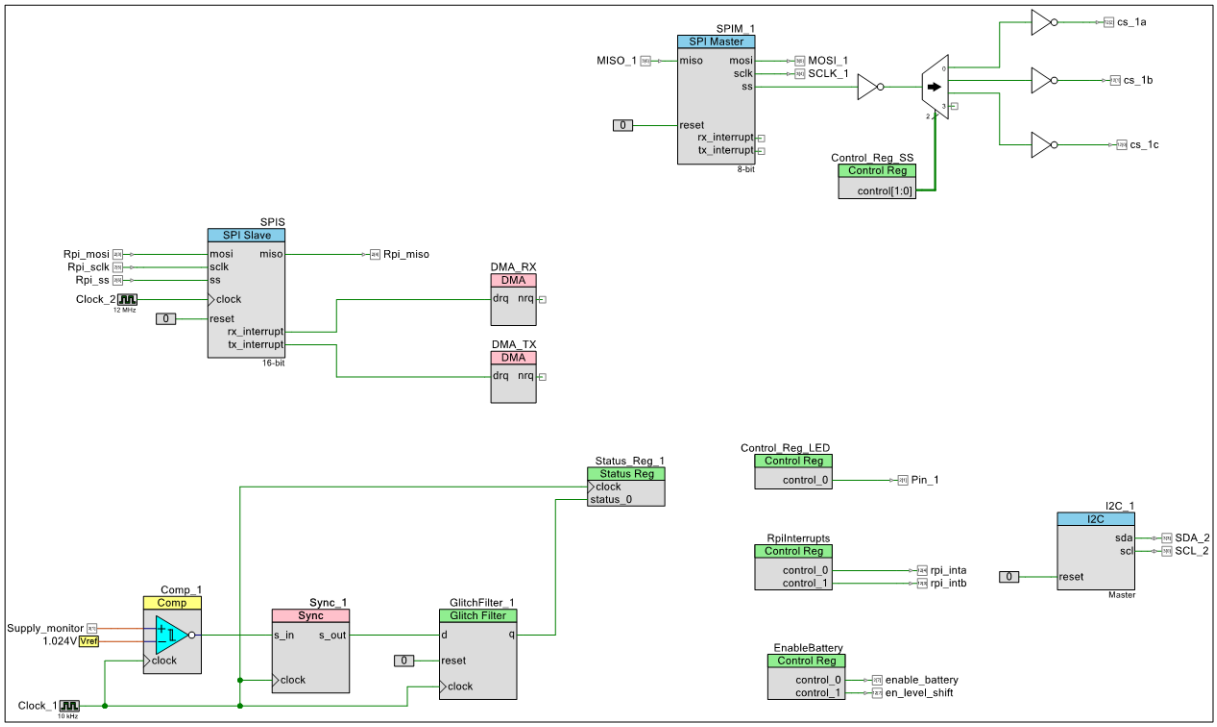
- Flash Protection chapter in the PSoC 5LP Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyWrite API routines
  - CyFlash API routines

7 Design Contents

This design's schematic content consists of the following schematic sheet:

7.1 Schematic Sheet: Page 1

Figure 5. Schematic Sheet: Page 1



This schematic sheet contains the following component instances:

- Instance Comp_1 (type: Comp_v2_0)
- Instance Control_Reg_LED (type: CyControlReg_v1_80)
- Instance Control_Reg_SS (type: CyControlReg_v1_80)
- Instance demux_1 (type: demux_v1_10)
- Instance EnableBattery (type: CyControlReg_v1_80)
- Instance GlitchFilter_1 (type: GlitchFilter_v2_0)
- Instance I2C_1 (type: I2C_v3_50)
- Instance RpiInterrupts (type: CyControlReg_v1_80)
- Instance SPIM_1 (type: SPI_Master_v2_50)
- Instance SPIS (type: SPI_Slave_v2_70)
- Instance Status_Reg_1 (type: CyStatusReg_v1_90)
- Instance Sync_1 (type: cy_sync_v1_0)

8 Components

8.1 Component type: Comp [v2.0]

8.1.1 Instance Comp_1

Description: Analog voltage comparator.
Instance type: Comp [v2.0]
Datasheet: online component datasheet for Comp

Table 14. Component Parameters for Comp_1

Parameter Name	Value	Description
Hysteresis	Enable	Enable to add output hysteresis.
Pd_Override	Disable	Power down override to allow comparator to continue operating during sleep.
Polarity	Inverting	Allows output to be inverted.
Speed	Slow	Set comparator response speed.
Sync	Normal	Allows synchronization with clock.
User Comments		Instance-specific comments.

8.2 Component type: cy_sync [v1.0]

8.2.1 Instance Sync_1

Description: Synchronizes the input signal(s) to its input clock
Instance type: cy_sync [v1.0]
Datasheet: online component datasheet for cy_sync

Table 15. Component Parameters for Sync_1

Parameter Name	Value	Description
SignalWidth	1	This parameter configures the number of signals that will be synchronized to the associated clock.
User Comments		Instance-specific comments.

8.3 Component type: CyControlReg [v1.80]

8.3.1 Instance Control_Reg_LED

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 16. Component Parameters for Control_Reg_LED

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode

Parameter Name	Value	Description
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)
User Comments		Instance-specific comments.

8.3.2 Instance Control_Reg_SS

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 17. Component Parameters for Control_Reg_SS

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	true	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	2	Defines the number of outputs needed (1-8)
User Comments		Instance-specific comments.

8.3.3 Instance EnableBattery

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 18. Component Parameters for EnableBattery

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode

Parameter Name	Value	Description
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	1	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	2	Defines the number of outputs needed (1-8)
User Comments		Instance-specific comments.

8.3.4 Instance RpiInterrupts

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.80]
Datasheet: online component datasheet for CyControlReg

Table 19. Component Parameters for RpiInterrupts

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	1	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	2	Defines the number of outputs needed (1-8)
User Comments		Instance-specific comments.

8.4 Component type: CyStatusReg [v1.90]

8.4.1 Instance Status_Reg_1

Description: The Status Register allows the firmware to read values from digital signals.
Instance type: CyStatusReg [v1.90]
Datasheet: online component datasheet for CyStatusReg

Table 20. Component Parameters for Status_Reg_1

Parameter Name	Value	Description
Bit0Mode	Transparent	Bit Mode for Bit 0 of the Status Register
Bit1Mode	Transparent	Bit Mode for Bit 1 of the Status Register
Bit2Mode	Transparent	Bit Mode for Bit 2 of the Status Register
Bit3Mode	Transparent	Bit Mode for Bit 3 of the Status Register
Bit4Mode	Transparent	Bit Mode for Bit 4 of the Status Register

Parameter Name	Value	Description
Bit5Mode	Transparent	Bit Mode for Bit 5 of the Status Register
Bit6Mode	Transparent	Bit Mode for Bit 6 of the Status Register
Bit7Mode	Transparent	Bit Mode for Bit 7 of the Status Register
BusDisplay	false	Displays the input terminals as bus
Interrupt	false	Shows the interrupt terminal
MaskValue	0	Defines the value of the interrupt mask
NumInputs	1	Defines the number of status inputs (1-8)
User Comments		Instance-specific comments.

8.5 Component type: demux [v1.10]

8.5.1 Instance demux_1

Description: De-Multiplexer with configurable number of output terminals and terminal width.
Instance type: demux [v1.10]
Datasheet: online component datasheet for demux

Table 21. Component Parameters for demux_1

Parameter Name	Value	Description
NumOutputTerminals	4	Number of output terminals of the De-Multiplexer. Acceptable values are 2, 4, 8 and 16.
TerminalWidth	1	Width of each terminal
User Comments		Instance-specific comments.

8.6 Component type: GlitchFilter [v2.0]

8.6.1 Instance GlitchFilter_1

Description: Removes unwanted pulses from a digital signal
Instance type: GlitchFilter [v2.0]
Datasheet: online component datasheet for GlitchFilter

Table 22. Component Parameters for GlitchFilter_1

Parameter Name	Value	Description
BypassFilter	None	Specifies the logic level to be directly propagated to the output.
GlitchLength	26	Defines the number of samples for which input has to be stable before being propagated to the output.
SignalWidth	1	Determines the bus width of d and q terminals.
User Comments		Instance-specific comments.

8.7 Component type: I2C [v3.50]

8.7.1 Instance I2C_1

Description: Standard I2C communication interface
Instance type: I2C [v3.50]
Datasheet: online component datasheet for I2C

Table 23. Component Parameters for I2C_1

Parameter Name	Value	Description
Address_Decode	Hardware	Determines either hardware or software address match logic.
BusSpeed_kHz	400	I2C Data Rate in kbps. Standard settings are 50, 100, 400 or 1000. The value must be between 1 and 1000.
EnableWakeup	false	Determines if I2C is selected as wakeup source.
ExternalBuffer	false	Exposes scl and sda in and out terminals outside the component.
Externi2cIntrHandler	false	Allows I2C interrupt handler to be set outside the I2C component. This feature intended only for PM/SM bus usage.
ExternTmoutIntrHandler	false	Allows I2C timeout interrupt handler to be set outside the I2C component. This feature intended only for PM/SM bus usage.
Hex	false	Indicates that address has been input in hexadecimal format.
I2C_Mode	Master	Determines I2C mode (Slave/Master/Multi-Master/Multi-Master-Slave).
I2cBusPort	Any	Determines which I2C pins have been selected. Select I2C0/I2C1 and connect to corresponding pins to be able use I2C as wakeup source.
Implementation	UDB	Determines either I2C implementation Fixed Function or UDB.
NotSlaveClockMinusTolerance	25	Internal component clock negative tolerance value in Master, Multi-Master or Multi-Master-Slave mode.
NotSlaveClockPlusTolerance	5	Internal component clock positive tolerance value in Master, Multi-Master or Multi-Master-Slave mode.
PrescalerEnabled	false	Enables prescaler (7-bit counter) to expand timeout timer range.
PrescalerPeriod	3	Prescaler period of timeout timer.
SclTimeoutEnabled	false	Enables low time monitoring of scl line.
SdaTimeoutEnabled	false	Enables low time monitoring of sda line.
Slave_Address	8	7-bits I2C slave address.

Parameter Name	Value	Description
SlaveClockMinusTolerance	5	Internal component clock negative tolerance value in Slave mode.
SlaveClockPlusTolerance	50	Internal component clock positive tolerance value in Slave mode.
TimeoutImplementation	UDB	Determines either timeout timer feature implementation as UDB or Fixed Function. The Fixed Function implementation only available for PSoC5LP.
TimeOutms	25	Determines maximum time allowed for scl or sda to be low state (in mS). The timeout timer generates interrupt after timeout expires.
TimeoutPeriodff	39999	Period of timeout timer (Fixed Function).
TimeoutPeriodUdb	39999	Period of timeout timer (UDB).
UdbInternalClock	true	Determines either internal or external clock source for I2C UDB.
UdbSlaveFixedPlacementEnable	false	Enables fixed placement for I2C UDB. Only available in slave mode.
User Comments		Instance-specific comments.

8.8 Component type: SPI_Master [v2.50]

8.8.1 Instance SPIM_1

Description: Serial Peripheral Interface Master
Instance type: SPI_Master [v2.50]
Datasheet: online component datasheet for SPI_Master

Table 24. Component Parameters for SPIM_1

Parameter Name	Value	Description
BidirectMode	false	Bidirectional mode setting
ClockInternal	true	Allow use of the internal clock and desired bit rate or an external clock source
DesiredBitRate	1000000	Desired Bit Rate in bps
HighSpeedMode	false	Enables using of the High Speed Mode
InterruptOnByteComplete	false	Set Initial Interrupt Source to Enable Interrupt on Byte Transfer Complete
InterruptOnRXFull	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Full
InterruptOnRXNotEmpty	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Not Empty
InterruptOnRXOverrun	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Overrun

Parameter Name	Value	Description
InterruptOnSPIDone	false	Set Initial Interrupt Source to Enable Interrupt on SPI Done
InterruptOnSPIIdle	false	Set Initial Interrupt Source to Enable Interrupt on SPI Idle
InterruptOnTXEmpty	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO Empty
InterruptOnTXNotFull	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO Not Full
Mode	CPHA = 0, CPOL = 0	SPI mode defines the Clock Phase and Clock Polarity desired
NumberOfDataBits	8	Set the Number of Data bits 3-16
RxBufferSize	4	Defines the amount of RAM Set asside for the RX Buffer
ShiftDir	MSB First	Set the Shift Out Direction
TxBufferSize	4	Defines the amount of RAM Set asside for the TX Buffer
User Comments		Instance-specific comments.
UseRxInternalInterrupt	false	Defines whether Rx internal interrupt is used or not
UseTxInternalInterrupt	false	Defines whether Tx internal interrupt is used or not

8.9 Component type: SPI_Slave [v2.70]

8.9.1 Instance SPIS

Description: Serial Peripheral Interface Slave
Instance type: SPI_Slave [v2.70]
Datasheet: online component datasheet for SPI_Slave

Table 25. Component Parameters for SPIS

Parameter Name	Value	Description
BidirectMode	false	Bidirectional mode setting
ClockInternal	false	Defines whether internal clock is used or not
DesiredBitRate	1000000	Desired Bit Rate in Hz
FixedPlacementEnabled	false	
InterruptOnByteComplete	false	Set Initial Interrupt Source to Enable Interrupt on Byte Transfer Complete
InterruptOnDone	false	Set Initial Interrupt Source to Enable Interrupt on SPI Done
InterruptOnRXEmpty	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Empty
InterruptOnRXFull	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO full
InterruptOnRXNotEmpty	true	Set Initial Interrupt Source to Enable Interrupt on RX Not Empty

Parameter Name	Value	Description
InterruptOnRXOverrun	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO overrun
InterruptOnTXEmpty	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO Empty
InterruptOnTXFull	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO full
InterruptOnTXNotFull	true	Set Initial Interrupt Source to Enable Interrupt on TX FIFO not full
Mode	CPHA = 0, CPOL = 0	Allows for setting the SPI Clock Polarity and Clock Phase from one of the four well known modes
MultiSlaveEnable	false	Allows using of the SPI MISO output enable terminal for multislave mode support
NumberOfDataBits	16	Data Width (3-16 bits)
RxBufferSize	4	RAM size used to store RX Data
ShiftDir	MSB First	Data Shift Direction (MSB First or LSB First)
TxBufferSize	4	RAM size used to store TX Data
UseInternalInterrupt	false	Defines whether internal interrupt is used or not
User Comments		Instance-specific comments.
UseRxInternalInterrupt	false	Defines whether Rx internal interrupt is used or not
UseTxInternalInterrupt	false	Defines whether Tx internal interrupt is used or not

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5LP register map is covered in the PSoC 5LP Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 5LP Technical Reference Manual
  - Low Power Modes chapter in the PSoC 5LP Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 5LP Technical Reference Manual
  - Cache chapter in the System Reference Guide
    - CyFlushCache() API routine