

ECSE 4320/6320 Project A1: Advanced OS and CPU Feature Exploration

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Environment summary (auto-collected; edit README for full details):

uname:

Linux LAPTOP-MKR8JNGQ 6.6.87.2-microsoft-standard-WSL2 #1 SMP PREEMPT_DYNAMIC Thu Jun 5 18:30:46 UTC 2025 x86_64 x86_64 x86_64 GNU/Linux

lscpu (top):

Architecture:	x86_64
CPU op-mode(s):	32-bit, 64-bit
Address sizes:	48 bits physical, 48 bits virtual
Byte Order:	Little Endian
CPU(s):	16
On-line CPU(s) list:	0-15
Vendor ID:	AuthenticAMD
Model name:	AMD Ryzen 7 PRO 5850U with Radeon Graphics
CPU family:	25
Model:	80
Thread(s) per core:	2
Core(s) per socket:	8
Socket(s):	1
Stepping:	0
BogoMIPS:	3792.77
Flags:	fpu vme de pse tsc msr pae mce cx8 apic sep mtrr pge mca cmov pat pse36 clflush mmx fxsr sse sse2 ht syscall nx mmxext fxsr_opt pdpe1gb rdtscp lm constant_tsc rep_good nopl tsc_reliable nonstop_tsc cpuid extd_apicid tsc_known_freq pni pclmulqdq ssse3 fma cx16 sse4_1 sse4_2 movbe popcnt aes xsave avx f16c rrand hypervisor lahf_lm cmp_legacy svm cr8_legacy abm sse4a misalignsse 3dnowprefetch osvw topoext perfctr_core ssbd ibrs ibpb stibp vmmcall fsgsbase bmi1 avx2 smep bmi2 erms invpcid rdseed adx smap clflushopt clwb sha_ni xsaveopt xsavec xgetbv1 xsaves clzero xsaveerptr arat npt nrrip_save tsc_scale vmcb_clean flushbyasid decodeassist pausefilter pfthreshold v_vmsave_vmload umip vaes vpclmulqdq rdpid fsrm
Virtualization:	AMD-V
Hypervisor vendor:	Microsoft
Virtualization type:	full
L1d cache:	256 KiB (8 instances)
L1i cache:	256 KiB (8 instances)
L2 cache:	4 MiB (8 instances)
L3 cache:	16 MiB (1 instance)
NUMA node(s):	1
NUMA node0 CPU(s):	0-15

WSL indicator:

Linux version 6.6.87.2-microsoft-standard-WSL2 (root@439a258ad544) (gcc (GCC) 11.2.0, GNU ld (GNU Binutils) 2.37) #1 SMP PREEMPT_DYNAMIC Thu Jun 5 18:30:46 UTC 2025

perf:

perf version 5.15.189

compiler:

g++ (Ubuntu 11.3.0-1ubuntu1~22.04) 11.3.0

Methodology

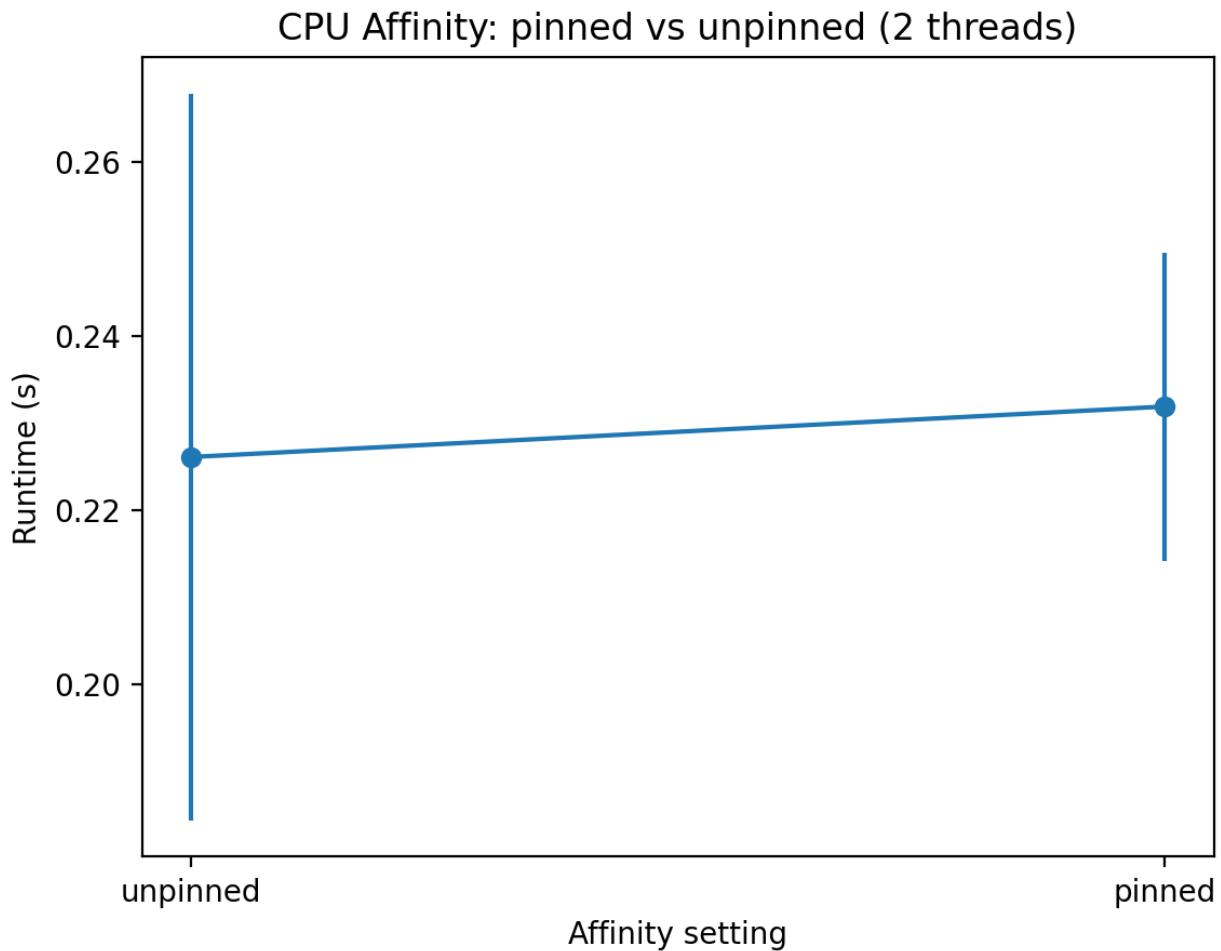
We implemented microbenchmarks targeting four OS/CPU features and executed each configuration multiple times to reduce noise. We report mean and standard deviation for runtime or throughput.

WSL Notes: Under WSL2, some perf hardware events (e.g., LLC-load-misses) may be unavailable. This report records cycles when supported and documents unsupported events as NA. Where CPU affinity is not honored, the benchmark prints a warning.

Raw results CSV (preview)

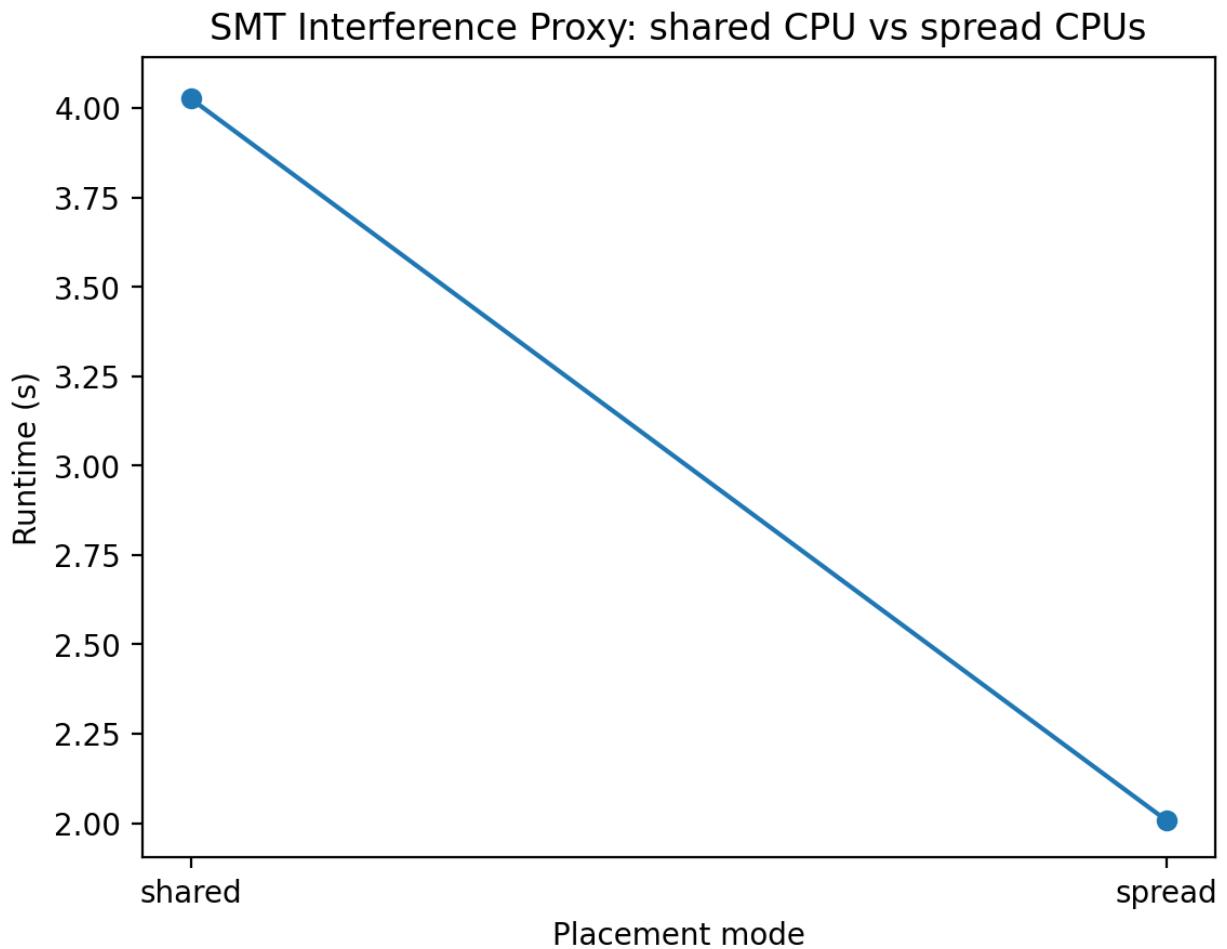
```
experiment,pinned,feature,threads,iters,seconds,seconds_mean,seconds_sd,cycles_mean,cycles_sd,perf_elapsed_mean,perf_elapsed_sd,stderr_note,mode,cpuA,cpuB,stride_elems,thp,mb,reps,touches,touches_per_s,touches_per_s_mean,touches_per_s_sd,pattern,accesses,accesses_per_s,accesses_per_s_mean,accesses_per_s_sd
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/////
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Results: CPU Affinity



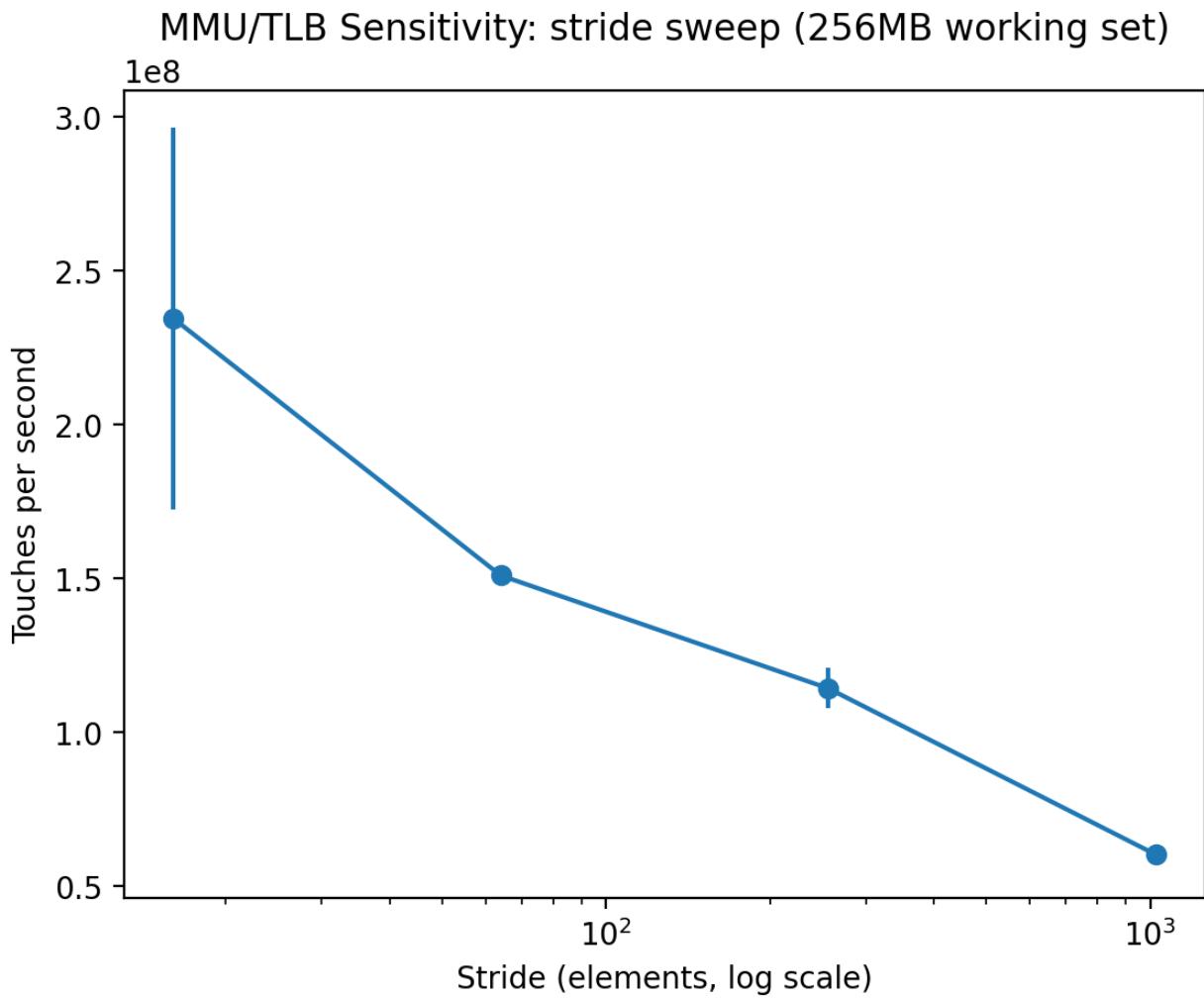
Caption guidance: state the independent variable(s), dependent metric, and the key effect. Tie the trend to OS/CPU mechanisms (contention, scheduling, TLB pressure, prefetch efficiency).

Results: SMT Interference Proxy



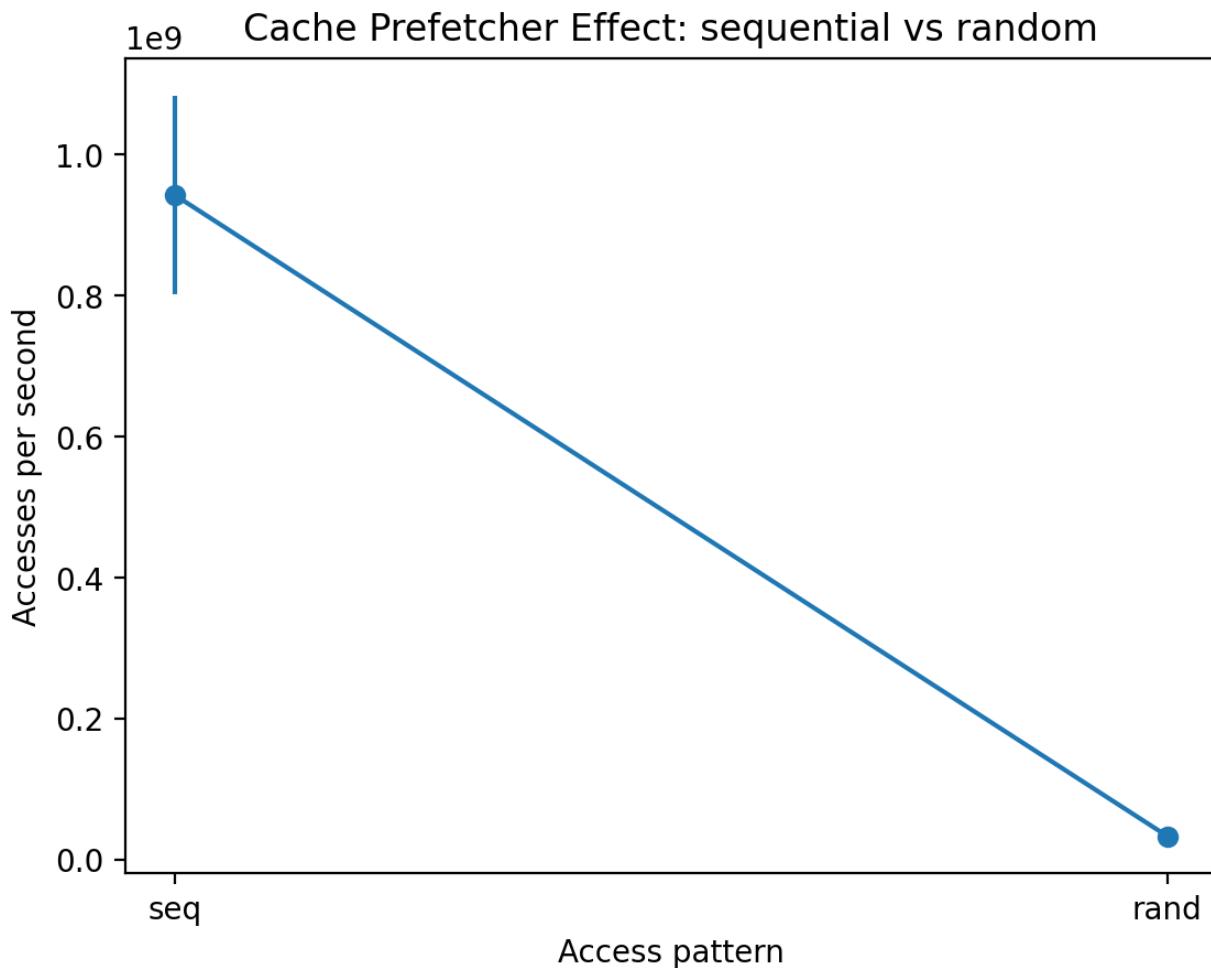
Caption guidance: state the independent variable(s), dependent metric, and the key effect. Tie the trend to OS/CPU mechanisms (contention, scheduling, TLB pressure, prefetch efficiency).

Results: MMU / Stride Sensitivity



Caption guidance: state the independent variable(s), dependent metric, and the key effect. Tie the trend to OS/CPU mechanisms (contention, scheduling, TLB pressure, prefetch efficiency).

Results: Prefetcher Effect



Caption guidance: state the independent variable(s), dependent metric, and the key effect. Tie the trend to OS/CPU mechanisms (contention, scheduling, TLB pressure, prefetch efficiency).