High-performance Video Super-resolution using the Zynq-7000 SoC

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Declaration of Authorship

I, Reich CANLAS, declare that this thesis titled, 'High-performance Video Super-resolution using the Zynq-7000 SoC' and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
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"Thanks to my solid academic training, today I can write hundreds of words on virtually any topic without possessing a shred of information, which is how I got a good job in journalism."

Dave Barry

DE LA SALLE UNIVERSITY

Abstract

Gokongwei College of Engineering

Electronics and Communications Engineering

Master of Science

High-performance Video Super-resolution using the Zynq-7000 SoC

by Reich CANLAS

The Thesis Abstract is written here (and usually kept to just this page). The page is kept centered vertically so can expand into the blank space above the title too...

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Abbreviations

GPU	**G**raphics **P**rocessing **U**nit
CPU	**C**entral **P**rocessing **U**nit
SR	**S**uper-**R**esolution
PSNR	**P**eak **S**ignal-to-**N**oise **Ratio**
SSIM	**S**tructural **S**imilarity **I**ndex **M**easure
FPGA	**F**ield **P**rogrammable **G**ate **A**rray

Chapter 1

INTRODUCTION

1.1 Background of the Study

The search for ever higher screen resolutions led to the advent of ultra high definition television screens and monitors. However, to date, common video sources do not use the full capability of most high-resolution televisions of today.

Super-resolution is the process of rendering or recovering a larger image or video given some low-resolution source (Dong, Loy, & He, 2014). Super-resolution finds its applications in diverse fields of study. Examples include video surveillance, in Caner, a.M. Tekalp, and Heinzelman (2003) and Zhang, Zhang, Shen, and Li (2010), medical imaging in Malczewski and Stasinski (2008), and satellite imaging (cite here). Multi-frame image super-resolution methods use a set of LR images to construct an HR image by exploring the spatial correlations in that set (Cheng, Hwang, Jeng, & Lin, 2013). This kind of SR is applicable in laboratory settings. In other cases, single frame SR is more appropriate. These methods try to extract information from only one HR image, making the task much more difficult than multi-frame.

1.2 Statement of the Problem

In many applications such as super-HD (4K) TV, super resolution has to be performed in real time (Shen, Wu, & Deng, 2014). However, as noted by Ishizaka et al. (2013) "it is several times slower than real-time" to upscale videos using commodity hardware. Besides, power consumption is also an important issue. To integrate super-resolution processing into existing systems, there must not be a drastic increase in power footprint. A number of state-of-the-art methods of SR use GPUs and manycore CPUs, which offer a degree of performance at the expense of electric power. Current solutions also have unstable frame rates (Wu, Xiang, & Lu, 2011). A class of integrated circuits known as FPGAs are demonstrate to have high performance-per-watt ratios.

We are then confronted by the problem of finding a video super-resolution system that uses a fast algorithm to generate high-quality hi-resolution videos from a low-resolution source while maintaining a relatively small power footprint.

1.3 Objectives of the Study

1.3.1 General Objective

This study aims to come up with a new video super-resolution algorithm and implement this for use on an FPGA (field programmable gate array).

1.3.2 Specific Objectives

Specifically, the study aims to tackle the following goals:

- Improve on the state-of-the-art video super-resolution algorithm in terms of PSNR (peak signal-to-noise ratio) and time complexity.

- Determine the FPGA best suited for the purpose of video super-resolution, considering processing resources and power consumption
- Profile the video super-resolution algorithm to determine performance bottlenecks
- Exploit parallelizable steps in the algorithm to further enhance suitability on an FPGA

1.4 Scope and Limitations of the Study

Since previous studies (cite something) have shown that clear upscaling is practical only at a factor of 4, it has been decided that this study should concern itself with x4 upscaling only.

Chapter 2

REVIEW OF RELATED LITERATURE

2.1 Image Super-resolution

Still-image super-resolution (SR) is the reconstruction of a high-resolution (HR) image given one, or a set of, low-resolution (HR) images. Super-resolution began as the problem of image restoration from a noisy signal (Helstrom, 1967). The first known work that directly tackled SR is that of Tsai and Huang (1984). Traditionally, super-resolution of images is performed with several observed LR images. This is done in order to remove artifacts introduced by the low-resolution camera sensor (Yang & Huang, 2010). There is another approach which involves only a single observation or image. The limited set of data severely limits the quality obtainable, thus the SR problem becomes ill-posed (Yang & Huang, 2010).

Super-resolution is necessary in the following fields of interest (Yang & Huang, 2010):

- Surveillance video:
- Satellite imaging:
- Medical imaging: In Malczewski and Stasinski (2008), multi-frame SR is accomplished by taking advantage of small spatial shifts in the LR image set.

- Video upscaling: This is the main premise of the present study, as with the rest of the papers cited in this chapter.

2.1.1 Image Quality Assessment (IQA)

Quantification of quality is a prerequisite in the improvement of the SR algorithm to be developed. Currently, there are two primary measures of output image quality in SR, namely, the Peak Signal-to-Noise Ratio (PSNR) and the Structural Similarity Index Measure (SSIM). The choice of PSNR or SSIM is typically arbitrary, with a few informal arguments favoring one or the other (Farsiu, Robinson, Elad, & Milanfar, 2004). To aid in selection of a suitable metric, an analysis of both image metrics is found in Horé and Ziou (2010). They state that a mathematical relationship exists between the two metrics, thus making it possible to predict the PSNR from the SSIM and vice-versa. They only differ in their sensitivity to image degradations as introduced by noise, compression, and hardware limitations.

A recent addition to the list of metrics is the FSIM (Feature Similarity Index Measure) (Zhang, Zhang, Mou, & Zhang, 2011).

To the present day, super-resolution remains an active area of research. The following sections present various approaches to SR that rely on several different models.

2.1.2 Image Observation Model

Several factors affect the output of a digital system, including finite aperture size and finite sensor size (Yang & Huang, 2010).

2.1.3 Frequency Domain

The first SR paper as authored by Tsai and Huang (1984) describes the SR process in the frequency domain. Their algorithm takes advantage of the shift and aliasing properties of the

continuous and discrete Fourier transforms, given a set of multiple shifted low resolution images. A few extensions have been proposed, such as (Yang & Huang, 2010)

2.1.4 Interpolation-restoration

(Yang, Wright, Huang, & Ma, 2010)

2.1.5 Statistical Methods

Hello (Yang & Huang, 2010)

2.1.6 Set-theoretic Methods

Hello (Yang & Huang, 2010)

2.1.7 Methods Based on Sparse Representations

The relative absence of data in the low resolution patches makes it reasonable to consider the LR patch space as a sparse representation of the HR patch space.

Zeyde, Elad, and Protter (2012) proposed an algorithm that uses the Sparseland model previously developed by Elad and Aharon (2006).

2.1.8 Dictionary Learning Methods

Digital signal data take up too much storage space, but most of this space does not account for the most significant components of the signal it represents. Compression and alternative representations are therefore required to reduce storage size while preserving fidelity. The use

of orthogonal and bi-orthogonal bases in Dictionary learning is the process of training a set of mutually orthogonal basis vectors in order to create a dictionary matrix. This matrix can then model any signal as a combination of its columns, better known as ”atoms”. (citation here)

Wright, Huang, Yang, and Ma (2010) jointly trained a dictionary for low resolution and another for high resolution patches to enforce sparse representation similarity for both patch spaces. Their approach is also robust to noise, as it uses local sparse modeling. Yang, Wang, Lin, Cohen, and Huang (2012) similarly stressed the importance of learning two coupled dictionaries, (observation dictionary and latent dictionary). However, the difference in their methods is that they used a coupled dictionary learning method for single-image SR.

2.1.9 Computational Intelligence Methods

So far, the previous methods mentioned all have solid mathematical foundations. However, it has been found out (citation here) that a great number of real-world problems cannot be modeled into well-posed mathematical problems, including super-resolution. A class of algorithms under ”computational intelligence” rely on mimicking natural systems to model and solve such kinds of problems.

Dong et al. (2014) used a deep convolutional neural network in order to

2.2 Challenges in Image SR

Researchers still struggle with the following challenges, despite years of research.

- Image Registration
- Computation Efficiency
-

2.2.1 Image Registration

Image registration is the process of mapping two images both spatially and with respect to intensity (Brown, 1992). It is a computationally-intensive task (Yang & Huang, 2010)

- Integrating information taken from different sensors
- finding changes in images taken at different times or under different conditions
- Inferring three dimensional information from images in which either the camera or the objects in the scene have moved
- Model-based object recognition

2.2.2 Edge preservation

It is typical in SR algorithms to lose details or edges in the output image/video. SR techniques for edge preservation have therefore been proposed. Vishnukumar, Nair, and Wilscy (2014) uses self-examples.

2.3 Video super-resolution

Video super-resolution is the extension of image SR to moving pictures. An additional temporal dimension can now be factored in the SR process. It can generally be divided into two categories: incremental and simultaneous (Su, Wu, & Zhou, 2011). The former category is faster but less visually consistent to the human eye. Liu and Sun (2014) mentions that video SR is relatively more challenging than image SR which has been studied for decades, due to the presence of an additional temporal dimension.

2.3.1 Mathematical Methods

Liu and Sun (2014) propose a Bayesian video SR system that can simultaneously estimate the motion, blur kernel, and noise level.

2.3.2 Computational Intelligence Methods

As in image SR, video SR is a highly nonlinear task and is amenable to processing via computational intelligence. For example, Cheng et al. (2013) constructed an artificial neural network that uses classifiers for video SR.

2.4 High Performance Computing Platforms

Yang and Huang (2010) suggest that high-performance hardware matters in tackling super-resolution problems. Typically, image SR algorithms are first developed for computer CPUs. Modern CPUs (central processing units) of computers combine high-frequency processors with a degree of parallelism to add more processing power to algorithms. Even so, the CPU is not enough to handle tasks such as SR in real-time. There are several steps in the SR process that may be implemented as parallel tasks. Following are the discussions on GPUs, manycore coprocessors, and FPGAs, three parallel platforms commonly in use today.

2.4.1 Graphics Processing Units

General-purpose computing on Graphics Processing Units GPUs (Graphics Processing Units) have been favored in recent years for this task, as it offers high amounts of parallelism (due to its multiple cores) and compatibility with existing computer systems and programming paradigms. Wu et al. (2011) claims 6x speedup against the same algorithm implemented on a CPU. Shen et al. (2014) used a real-time learning-based SR algorithm based on error feedback.

2.4.2 Manycore Coprocessors

This class of parallel processors are based off CPU architectures but have more cores than the traditional CPU and are meant to run at a lower frequency. A host CPU passes the appropriate parallel instructions to the manycore coprocessor and subsequently fetches the results of the computation. Manycore processors offer more programmability than GPUs simply by the fact that they share the same architecture as the host CPU. The only known product in this category is that of Intel MIC (Many Integrated Core) architecture (Intel, 2014).

Ishizaka et al. (2013) demonstrated a power-efficient real-time SR system that uses a virtual pipeline to improve the performance as well as the utilization of both the manycore and the host processors. Their set-up was able to achieve 31.5 fps, satisfying the real-time requirement. The problem with their set up is the limited adoption of the MIC platform and the power requirement of about 170 W (check the figures).

2.4.3 Field Programmable Gate Arrays (FPGAs)

FPGAs (Field Programmable Gate Arrays) are logic devices that can be reconfigured by a designer on the field after being manufactured. Since at the lowest level, logic circuits are inherently parallel and real-time, FPGAs offer optimization potential that cannot be realized when using instruction-based platforms such as CPUs and GPUs. FPGAs typically run at much lower frequencies than CPUs and GPUs, making them more power efficient. Higher-end FPGAs even offer the ability to be partially dynamically reconfigured, so that even while it is running, parts of the FPGA fabric gets their design altered (Dye, 2012). These factors makes FPGAs suitable for the most computationally-intensive real-time applications while conserving energy.

Sirowy and Forin (2008) investigated the reasons why an FPGA offers high speedups over instruction-based processors such as CPU, manycore, and GPU. Among these are the removal of an instruction fetch step.

2.4.4 Design Considerations and Strategies

Since the SR system of this study is to be integrated into other computing systems, it is imperative to develop an embedded system, one which consumes less space on the motherboard and uses less energy. The more power used, the more heat is generated. According to Anderson, Dykes, and Riedel (2003), failure rates double for every 15 degree Celsius rise in temperature. In this light, for an embedded system, the GPU and CPU are not applicable processors. Mittal (2014) considered using an ”unconventional core” such as an FPGA to realize lower power-consumption in an embedded system. Struyf, Beugher, Uytsel, Kanters, and Goedem (2014)

2.4.4.1 Use in super-resolution applications

The following papers prove the feasibility of an FPGA in SR applications. Angelopoulou, Bouganis, Cheung, and Constantinides (2009) created a real-time video SR system on an FPGA that is robust against noise. It uses the iterative back projection algorithm. However, the system depends on an adaptive image sensor Szydzik, Callico, and Nunez (2011) constructed a high quality SR system on an FPGA. They were able to achieve 2x upscaling at 25 fps while using only less than 37% of FPGA resources of the state-of-the-art algorithm at that time. Bowen and Bouganis (2008) achieved 3x speedup over equivalent software (CPU) implementations.

2.4.4.2 As video processors

Roth (2011) used low-cost FPGA hardware to accomplish real-time video processing tasks such as deinterlacing, alpha blending, and frame buffering.

2.5 Comparison of CPU, GPU and FPGA

Asano, Maruyama, and Yamaguchi (2009) compared the performance of the CPU, GPU and FPGA in image processing applications. They noted that CPUs are consistently lagging behind

the GPU and FPGA, while the GPU is best for ”naive computation methods” in which processing takes place on a per pixel basis.

Fowers, Brown, Cooke, and Stitt (2012) compared the performance and the energy expended by FPGAs, GPUs and multicore CPUs. This paper is significant to the present study since their focus is on sliding-window algorithms, which take the data on a per-block basis instead of per-pixel. This makes computation more efficient.

2.6 Zynq-7000 System-on-a-chip

Chapter 3

CONCEPTUAL FRAMEWORK

3.1 Research Process

3.1.1 Evaluation of state-of-the-art algorithms

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3.1.2 Modifications for speed and quality

3.1.3 FPGA Deployment and Comparative Tests

3.1.4 Exploiting parallelism for FPGAs

3.2 Data Flow

Chapter 4

METHODOLOGY

4.0.1 Evaluation of state-of-the-art algorithms

The state-of-the-art algorithm will first be evaluated as to its speed and output quality. The findings generated will then serve as the baseline for improvement.

4.0.2 Modifications for speed and quality

Successive modifications for speed and output quality will be performed until the improvements are sufficient to guarantee state-of-the-art status. Initially, these measurements will be performed in the CPU. This process is iterative. The criteria are at least +1dB increase in quality and at least 4x speedup.

4.0.3 FPGA Deployment and Comparative Tests

If the criteria are met in the CPU version of the algorithm, the next step is to parallelize using the available FPGA resources. A specialized architecture will be defined

4.0.4 Exploiting parallelism for FPGAs

4.1 Data Flow

4.2 Tools to be Used

The initial algorithm runs will be performed on a computer with an Intel Core i7 3632QM Processor 2.2 GHz, 16GB RAM, NVIDIA GeForce GT 730M 2GB. The FPGA to be used is the Xilinx Zynq-7000 SoC (embedded CPU+FPGA) on a Digilent Zedboard. Using this SoC combines the easy programmability of an embedded CPU with the fine-grained parallelism of an FPGA. The software consists of MATLAB 2015a and Xilinx Vivado Design Suite 2014.2.

Chapter 5

SUMMARY

In summary, the system to be developed is a reading

Appendix A

Gantt Chart

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Appendix B

Proposed Budget

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