Masteral Thesis Proposal

High-performance Video Super-resolution through FPGA

Author:
Reich Canlas

Supervisor:
Engr. Carlo Ochotorena

A thesis submitted in fulfilment of the requirements
for the degree of Master of Science

in

Electronics and Communications Engineering

April 2015

Declaration of Authorship

I, Reich Canlas, declare that this thesis titled, 'High-performance Video Super-resolution through FPGA' and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.
- I have acknowledged all main sources of help.
- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself.

Signed: _____

Date: _____

"Thanks to my solid academic training, today I can write hundreds of words on virtually any topic without possessing a shred of information, which is how I got a good job in journalism."

Dave Barry

DE LA SALLE UNIVERSITY

Abstract

Gokongwei College of Engineering
Electronics and Communications Engineering

Master of Science

High-performance Video Super-resolution through FPGA

by Reich Canlas

The Thesis Abstract is written here (and usually kept to just this page). The page is kept centered vertically so can expand into the blank space above the title too...

Acknowledgements

The acknowledgments and the people to thank go here, don't forget to include your project advisor...

Contents

Declaration of Authorship i

Abstract iii

Acknowledgements iv

Contents v

List of Figures viii

List of Tables ix

Abbreviations x

Physical Constants xi

Symbols xii

1 INTRODUCTION 1
- 1.1 Background of the Study . . . 1
- 1.2 Statement of the Problem . . . 2
- 1.3 Objectives of the Study . . . 2
  - 1.3.1 General Objective . . . 2
  - 1.3.2 Specific Objectives . . . 2
- 1.4 Scope and Limitations of the Study . . . 2

2 REVIEW OF RELATED LITERATURE 3
- 2.1 Image Super-resolution . . . 3
  - 2.1.1 Image Observation Model . . . 3
  - 2.1.2 Frequency Domain . . . 4
  - 2.1.3 Interpolation-restoration . . . 4
  - 2.1.4 Statistical Methods . . . 4
  - 2.1.5 Set-theoretic Methods . . . 4
  - 2.1.6 Methods based on sparsity . . . 4
  - 2.1.7 Dictionary learning methods . . . 4

2.1.8 Computational Intelligence Methods . . . 4
2.2 Challenges in Image SR . . . 5
2.3 Video super-resolution . . . 5
2.3.1 Mathematical Methods . . . 5
2.3.2 Computational Intelligence Methods . . . 5
2.4 Review of High Performance Computing Platforms . . . 6
2.5 Graphics Processing Units . . . 6
2.6 Manycore coprocessors . . . 6
2.7 Field Programmable Gate Arrays (FPGAs) . . . 6
2.7.1 Design Strategies . . . 7
2.7.2 Use in other high performance-per-watt applications . . . 7
2.7.3 As video processors . . . 7

3 CONCEPTUAL FRAMEWORK 8
3.1 Super-resolution phase . . . 8
3.1.1 Algorithmic Testing . . . 8
3.1.2 Computational Intelligence Methods . . . 8
3.2 Video super-resolution . . . 10
3.2.1 Mathematical Methods . . . 10
3.2.2 Computational Intelligence Methods . . . 10
3.3 Field Programmable Gate Arrays (FPGAs) . . . 11
3.3.1 Design Strategies . . . 11
3.3.2 Use in other high performance-per-watt applications . . . 11
3.3.3 As video processors . . . 11

4 METHODOLOGY 12
4.1 Image Super-resolution . . . 12
4.1.1 Mathematical Methods . . . 12
4.1.2 Computational Intelligence Methods . . . 12
4.2 Video super-resolution . . . 13
4.2.1 Mathematical Methods . . . 13
4.2.2 Computational Intelligence Methods . . . 13
4.3 Field Programmable Gate Arrays (FPGAs) . . . 14
4.3.1 Design Strategies . . . 14
4.3.2 Use in other high performance-per-watt applications . . . 14
4.3.3 As video processors . . . 14

5 SUMMARY 15
5.1 Image Super-resolution . . . 15
5.1.1 Mathematical Methods . . . 15
5.1.2 Computational Intelligence Methods . . . 15
5.2 Video super-resolution . . . 16
5.2.1 Mathematical Methods . . . 16
5.2.2 Computational Intelligence Methods . . . 16
5.3 Field Programmable Gate Arrays (FPGAs) . . . 17
5.3.1 Design Strategies . . . 17
5.3.2 Use in other high performance-per-watt applications . . . 17

5.3.3 As video processors 17

A Gantt Chart **18**

B Proposed Budget **19**

References **20**

List of Figures

3.1 Conceptual Framework 9

List of Tables

Abbreviations

LAH **L**ist **A**bbreviations **H**ere

Physical Constants

Speed of Light $c = 2.997\ 924\ 58 \times 10^8\ \mathrm{ms}^{-\mathrm{S}}$ (exact)

Symbols

a	distance	m
P	power	W (Js^{-1})
ω	angular frequency	rads^{-1}

For/Dedicated to/To my...

Chapter 1

INTRODUCTION

1.1 Background of the Study

The advent of ultra high resolution television screens and monitors have been Common video sources do not use the full capability of most high-resolution televisions of today Super-resolution is the process of rendering or recovering a larger image or video given some low-resolution source (Dong, Loy, & He, 2014) Super-resolution finds its applications in diverse fields of study. Examples include video surveillance, in Caner, a.M. Tekalp, and Heinzelman (2003) and Zhang, Zhang, Shen, and Li (2010), medical imaging [3,4], and satellite imaging [5–7], have gained significant interests in consumer electronics, academia, and industries (temporary citation) (Cheng, Hwang, Jeng, & Lin, 2013) Image super-resolution methods that use a set of LR images construct an HR image by exploring the spatial correlations in that set (Cheng et al., 2013). Ishizaka et al. (2013) noted that "high quality SR that can be used for enterprise systems such like broadcasting and video surveillance is very compute intensive. Realtimeness is recognized as important threshold to use SR for a variety of systems. However, for example, it is several times slower than realtime to convert SD to HD by using a commodity server."

Video super-resolution is a difficult task, especially when given severe time constraints (near real-time) Today's state-of-the-art video super-resolution methods run on a GPU (high cost, high wattage) Current solutions also have unstable frame rates. FPGAs are known to have high performance-per-watt ratios.

1.2 Statement of the Problem

We are then confronted by the problem of finding a video super-resolution system that uses a fast algorithm to generate high-quality hi-resolution videos from a low-resolution source while maintaining a relatively small power footprint.

1.3 Objectives of the Study

1.3.1 General Objective

This study aims to come up with a new video super-resolution algorithm and implement this for use on an FPGA (field programmable gate array).

1.3.2 Specific Objectives

Specifically, the study aims on improving on the state-of-the-art video super-resolution algorithm in terms of PSNR (peak signal-to-noise ratio) and processing time Determine the FPGA best suited for the purpose of video super-resolution, considering processing resources and power consumption Profile the video super-resolution algorithm to determine performance bottlenecks Exploit parallelizable steps in the algorithm to further enhance suitability on an FPGA

1.4 Scope and Limitations of the Study

- Near real-time

Since previous studies (cite something) have shown that clear upscaling is practical only at a factor of 4, it has been decided that this study should concern itself with x4 upscaling only.

Chapter 2

REVIEW OF RELATED LITERATURE

2.1 Image Super-resolution

Still-image super-resolution (SR) is the reconstruction of a high-resolution (HR) image given one, or a set of, low-resolution (HR) images. The first known work on this field is that of Tsai and Huang (1984). Traditionally, super-resolution of images is performed with several observed LR images. This is done in order to remove artifacts introduced by the low-resolution camera sensor (Yang & Huang, 2010). There is another approach which involves only a single observation or image. The limited set of data severely limits the quality obtainable, thus the SR problem becomes ill-posed (Yang & Huang, 2010).

Super-resolution is necessary in the following fields of interest (Yang & Huang, 2010):

- Surveillance video:
- Satellite imaging:
- Medical imaging:
- Video upscaling:

To the present day, super-resolution remains an active area of research. The following sections present various approaches to SR that rely on several different models.

2.1.1 Image Observation Model

(Yang & Huang, 2010)

2.1.2 Frequency Domain

Hello (Yang & Huang, 2010)

2.1.3 Interpolation-restoration

Hello (Yang, Wright, Huang, & Ma, 2010)

2.1.4 Statistical Methods

Hello (Yang & Huang, 2010)

2.1.5 Set-theoretic Methods

Hello (Yang & Huang, 2010)

2.1.6 Methods based on sparsity

Hello

2.1.7 Dictionary learning methods

Hello

2.1.8 Computational Intelligence Methods

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

2.2 Challenges in Image SR

Researchers still struggle with the following challenges, despite years of research.

- Image Registration
- Computation Efficiency
-

2.3 Video super-resolution

Video super-resolution is the application of super-resolution to moving pictures. It can generally be divided into two categories: incremental and simultaneous (Su, Wu, & Zhou, 2011). The former category is faster but less visually consistent to the human eye.

2.3.1 Mathematical Methods

Nunc posuere quam at lectus tristique eu ultrices augue venenatis. Vestibulum ante ipsum primis in faucibus orci luctus et ultrices posuere cubilia Curae; Aliquam erat volutpat. Vivamus sodales tortor eget quam adipiscing in vulputate ante ullamcorper. Sed eros ante, lacinia et sollicitudin et, aliquam sit amet augue. In hac habitasse platea dictumst.

2.3.2 Computational Intelligence Methods

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

2.4 Review of High Performance Computing Platforms

Yang and Huang (2010) suggest that high-performance hardware does matter in tackling super-resolution problems. In (insert citation here), something. Modern CPUs (central processing units) of computers combine high-frequency processors with a degree of parallelism to add more processing power to algorithms. Even so, the CPU is not enough to handle tasks such as SR in real-time. There are several steps in the SR process that may be implemented as parallel tasks. Following are the discussions on GPUs, manycore coprocessors, and FPGAs, three parallel platforms commonly in use today.

2.5 Graphics Processing Units

GPUs (Graphics Processing Units) have been favored in recent years for this task, as it offers high amounts of parallelism (due to its multiple cores) and compatibility with existing computer systems and programming paradigms. Wu, Xiang, and Lu (2011) claims 6x speedup against the same algorithm implemented on a CPU. Shen, Wu, and Deng (2014) used a real-time learning-based SR algorithm based on error feedback.

2.6 Manycore coprocessors

This class of parallel processors are based off CPU architectures but have more cores than the traditional CPU and are meant to run at a lower frequency. A host CPU passes the appropriate parallel instructions to the manycore coprocessor and subsequently fetches the results of the computation. Manycore processors offer more programmability than GPUs simply by the fact that they share the same architecture as the host CPU (Ishizaka et al., 2013).

2.7 Field Programmable Gate Arrays (FPGAs)

FPGAs (Field Programmable Gate Arrays), however, can exploit fine-grained parallelism while keeping the power footprint small. Angelopoulou, Bouganis, Cheung, and Constantinides (2009) created a real-time video SR system on an FPGA that is robust against noise. It uses the iterative back projection algorithm.

2.7.1 Design Strategies

Sirowy and Forin (2008) detailed the reason why an FPGA offers high speedups over instruction-based processors such as CPU, manycore, and GPU.

2.7.2 Use in other high performance-per-watt applications

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

2.7.3 As video processors

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

Chapter 3

CONCEPTUAL FRAMEWORK

3.1 Super-resolution phase

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam ultricies lacinia euismod. Nam tempus risus in dolor rhoncus in interdum enim tincidunt. Donec vel nunc neque. In condimentum ullamcorper quam non consequat. Fusce sagittis tempor feugiat. Fusce magna erat, molestie eu convallis ut, tempus sed arcu. Quisque molestie, ante a tincidunt ullamcorper, sapien enim dignissim lacus, in semper nibh erat lobortis purus. Integer dapibus ligula ac risus convallis pellentesque.

3.1.1 Algorithmic Testing

Nunc posuere quam at lectus tristique eu ultrices augue venenatis. Vestibulum ante ipsum primis in faucibus orci luctus et ultrices posuere cubilia Curae; Aliquam erat volutpat. Vivamus sodales tortor eget quam adipiscing in vulputate ante ullamcorper. Sed eros ante, lacinia et sollicitudin et, aliquam sit amet augue. In hac habitasse platea dictumst.

3.1.2 Computational Intelligence Methods

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget

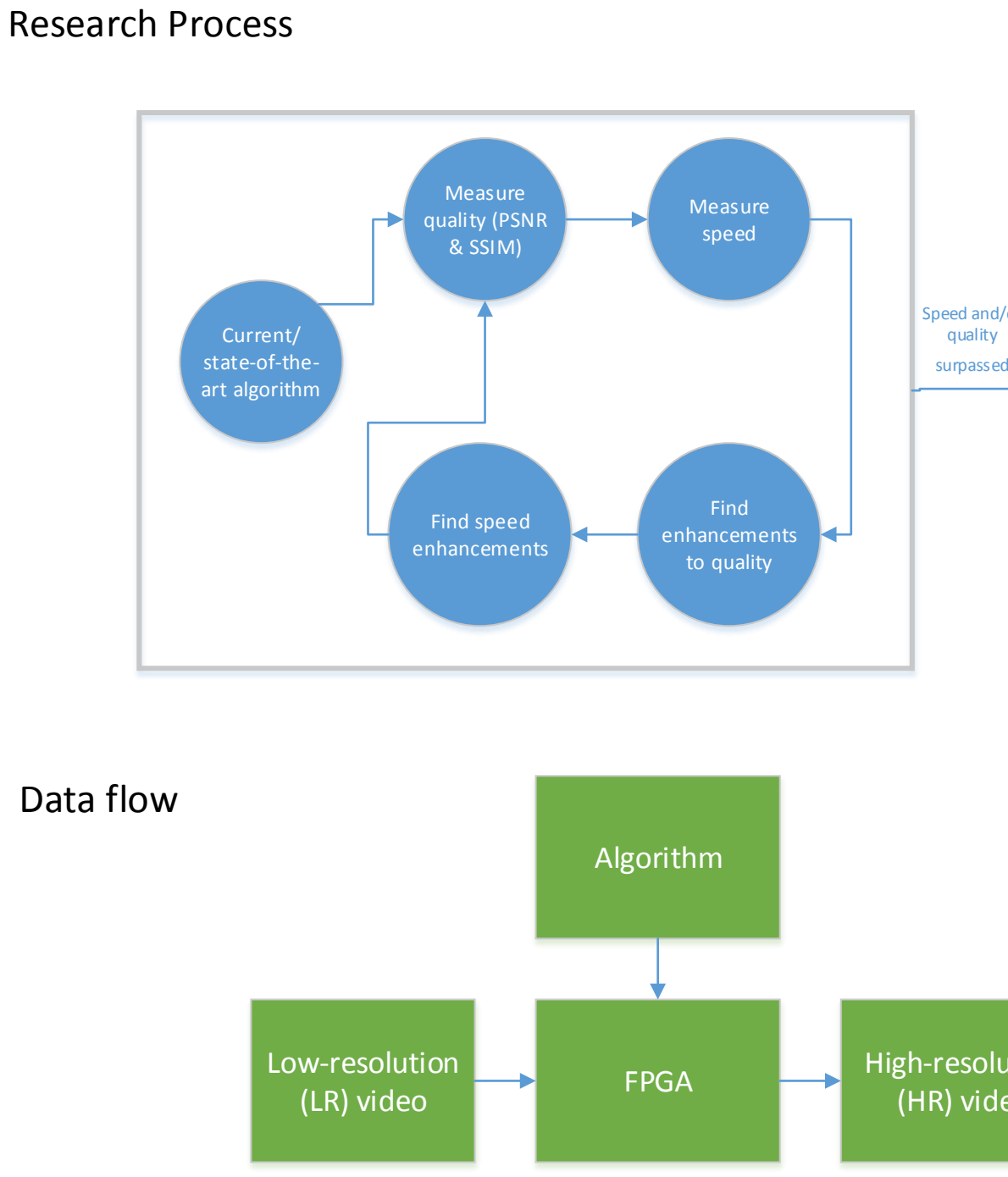

FIGURE 3.1: Conceptual Framework of the Study.

ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

3.2 Video super-resolution

Sed ullamcorper quam eu nisl interdum at interdum enim egestas. Aliquam placerat justo sed lectus lobortis ut porta nisl porttitor. Vestibulum mi dolor, lacinia molestie gravida at, tempus vitae ligula. Donec eget quam sapien, in viverra eros. Donec pellentesque justo a massa fringilla non vestibulum metus vestibulum. Vestibulum in orci quis felis tempor lacinia. Vivamus ornare ultrices facilisis. Ut hendrerit volutpat vulputate. Morbi condimentum venenatis augue, id porta ipsum vulputate in. Curabitur luctus tempus justo. Vestibulum risus lectus, adipiscing nec condimentum quis, condimentum nec nisl. Aliquam dictum sagittis velit sed iaculis. Morbi tristique augue sit amet nulla pulvinar id facilisis ligula mollis. Nam elit libero, tincidunt ut aliquam at, molestie in quam. Aenean rhoncus vehicula hendrerit.

3.2.1 Mathematical Methods

Nunc posuere quam at lectus tristique eu ultrices augue venenatis. Vestibulum ante ipsum primis in faucibus orci luctus et ultrices posuere cubilia Curae; Aliquam erat volutpat. Vivamus sodales tortor eget quam adipiscing in vulputate ante ullamcorper. Sed eros ante, lacinia et sollicitudin et, aliquam sit amet augue. In hac habitasse platea dictumst.

3.2.2 Computational Intelligence Methods

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

3.3 Field Programmable Gate Arrays (FPGAs)

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam ultricies lacinia euismod. Nam tempus risus in dolor rhoncus in interdum enim tincidunt. Donec vel nunc neque. In condimentum ullamcorper quam non consequat. Fusce sagittis tempor feugiat. Fusce magna erat, molestie eu convallis ut, tempus sed arcu. Quisque molestie, ante a tincidunt ullamcorper, sapien enim dignissim lacus, in semper nibh erat lobortis purus. Integer dapibus ligula ac risus convallis pellentesque.

3.3.1 Design Strategies

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

3.3.2 Use in other high performance-per-watt applications

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

3.3.3 As video processors

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

Chapter 4

METHODOLOGY

4.1 Image Super-resolution

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam ultricies lacinia euismod. Nam tempus risus in dolor rhoncus in interdum enim tincidunt. Donec vel nunc neque. In condimentum ullamcorper quam non consequat. Fusce sagittis tempor feugiat. Fusce magna erat, molestie eu convallis ut, tempus sed arcu. Quisque molestie, ante a tincidunt ullamcorper, sapien enim dignissim lacus, in semper nibh erat lobortis purus. Integer dapibus ligula ac risus convallis pellentesque.

4.1.1 Mathematical Methods

Nunc posuere quam at lectus tristique eu ultrices augue venenatis. Vestibulum ante ipsum primis in faucibus orci luctus et ultrices posuere cubilia Curae; Aliquam erat volutpat. Vivamus sodales tortor eget quam adipiscing in vulputate ante ullamcorper. Sed eros ante, lacinia et sollicitudin et, aliquam sit amet augue. In hac habitasse platea dictumst.

4.1.2 Computational Intelligence Methods

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget

ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

4.2 Video super-resolution

Sed ullamcorper quam eu nisl interdum at interdum enim egestas. Aliquam placerat justo sed lectus lobortis ut porta nisl porttitor. Vestibulum mi dolor, lacinia molestie gravida at, tempus vitae ligula. Donec eget quam sapien, in viverra eros. Donec pellentesque justo a massa fringilla non vestibulum metus vestibulum. Vestibulum in orci quis felis tempor lacinia. Vivamus ornare ultrices facilisis. Ut hendrerit volutpat vulputate. Morbi condimentum venenatis augue, id porta ipsum vulputate in. Curabitur luctus tempus justo. Vestibulum risus lectus, adipiscing nec condimentum quis, condimentum nec nisl. Aliquam dictum sagittis velit sed iaculis. Morbi tristique augue sit amet nulla pulvinar id facilisis ligula mollis. Nam elit libero, tincidunt ut aliquam at, molestie in quam. Aenean rhoncus vehicula hendrerit.

4.2.1 Mathematical Methods

Nunc posuere quam at lectus tristique eu ultrices augue venenatis. Vestibulum ante ipsum primis in faucibus orci luctus et ultrices posuere cubilia Curae; Aliquam erat volutpat. Vivamus sodales tortor eget quam adipiscing in vulputate ante ullamcorper. Sed eros ante, lacinia et sollicitudin et, aliquam sit amet augue. In hac habitasse platea dictumst.

4.2.2 Computational Intelligence Methods

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

4.3 Field Programmable Gate Arrays (FPGAs)

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam ultricies lacinia euismod. Nam tempus risus in dolor rhoncus in interdum enim tincidunt. Donec vel nunc neque. In condimentum ullamcorper quam non consequat. Fusce sagittis tempor feugiat. Fusce magna erat, molestie eu convallis ut, tempus sed arcu. Quisque molestie, ante a tincidunt ullamcorper, sapien enim dignissim lacus, in semper nibh erat lobortis purus. Integer dapibus ligula ac risus convallis pellentesque.

4.3.1 Design Strategies

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

4.3.2 Use in other high performance-per-watt applications

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

4.3.3 As video processors

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

Chapter 5

SUMMARY

5.1 Image Super-resolution

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam ultricies lacinia euismod. Nam tempus risus in dolor rhoncus in interdum enim tincidunt. Donec vel nunc neque. In condimentum ullamcorper quam non consequat. Fusce sagittis tempor feugiat. Fusce magna erat, molestie eu convallis ut, tempus sed arcu. Quisque molestie, ante a tincidunt ullamcorper, sapien enim dignissim lacus, in semper nibh erat lobortis purus. Integer dapibus ligula ac risus convallis pellentesque.

5.1.1 Mathematical Methods

Nunc posuere quam at lectus tristique eu ultrices augue venenatis. Vestibulum ante ipsum primis in faucibus orci luctus et ultrices posuere cubilia Curae; Aliquam erat volutpat. Vivamus sodales tortor eget quam adipiscing in vulputate ante ullamcorper. Sed eros ante, lacinia et sollicitudin et, aliquam sit amet augue. In hac habitasse platea dictumst.

5.1.2 Computational Intelligence Methods

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget

ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

5.2 Video super-resolution

Sed ullamcorper quam eu nisl interdum at interdum enim egestas. Aliquam placerat justo sed lectus lobortis ut porta nisl porttitor. Vestibulum mi dolor, lacinia molestie gravida at, tempus vitae ligula. Donec eget quam sapien, in viverra eros. Donec pellentesque justo a massa fringilla non vestibulum metus vestibulum. Vestibulum in orci quis felis tempor lacinia. Vivamus ornare ultrices facilisis. Ut hendrerit volutpat vulputate. Morbi condimentum venenatis augue, id porta ipsum vulputate in. Curabitur luctus tempus justo. Vestibulum risus lectus, adipiscing nec condimentum quis, condimentum nec nisl. Aliquam dictum sagittis velit sed iaculis. Morbi tristique augue sit amet nulla pulvinar id facilisis ligula mollis. Nam elit libero, tincidunt ut aliquam at, molestie in quam. Aenean rhoncus vehicula hendrerit.

5.2.1 Mathematical Methods

Nunc posuere quam at lectus tristique eu ultrices augue venenatis. Vestibulum ante ipsum primis in faucibus orci luctus et ultrices posuere cubilia Curae; Aliquam erat volutpat. Vivamus sodales tortor eget quam adipiscing in vulputate ante ullamcorper. Sed eros ante, lacinia et sollicitudin et, aliquam sit amet augue. In hac habitasse platea dictumst.

5.2.2 Computational Intelligence Methods

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

5.3 Field Programmable Gate Arrays (FPGAs)

Lorem ipsum dolor sit amet, consectetur adipiscing elit. Aliquam ultricies lacinia euismod. Nam tempus risus in dolor rhoncus in interdum enim tincidunt. Donec vel nunc neque. In condimentum ullamcorper quam non consequat. Fusce sagittis tempor feugiat. Fusce magna erat, molestie eu convallis ut, tempus sed arcu. Quisque molestie, ante a tincidunt ullamcorper, sapien enim dignissim lacus, in semper nibh erat lobortis purus. Integer dapibus ligula ac risus convallis pellentesque.

5.3.1 Design Strategies

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

5.3.2 Use in other high performance-per-watt applications

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

5.3.3 As video processors

Morbi rutrum odio eget arcu adipiscing sodales. Aenean et purus a est pulvinar pellentesque. Cras in elit neque, quis varius elit. Phasellus fringilla, nibh eu tempus venenatis, dolor elit posuere quam, quis adipiscing urna leo nec orci. Sed nec nulla auctor odio aliquet consequat. Ut nec nulla in ante ullamcorper aliquam at sed dolor. Phasellus fermentum magna in augue gravida cursus. Cras sed pretium lorem. Pellentesque eget ornare odio. Proin accumsan, massa viverra cursus pharetra, ipsum nisi lobortis velit, a malesuada dolor lorem eu neque.

Appendix A

Gantt Chart

Write your Appendix content here.

Appendix B

Proposed Budget

Write your Appendix content here.

References

Angelopoulou, M. E., Bouganis, C.-S., Cheung, P. Y. K., & Constantinides, G. a. (2009). Robust Real-Time Super-Resolution on FPGA and an Application to Video Enhancement. *ACM Transactions on Reconfigurable Technology and Systems*, *2*(4), 1–29. doi: 10.1145/1575779.1575782

Caner, G., a.M. Tekalp, & Heinzelman, W. (2003). Super resolution recovery for multi-camera surveillance imaging. *2003 International Conference on Multimedia and Expo. ICME '03. Proceedings (Cat. No.03TH8698)*, *1*. doi: 10.1109/ICME.2003.1220866

Cheng, M. H., Hwang, K. S., Jeng, J. H., & Lin, N. W. (2013). Classification-based video super-resolution using artificial neural networks. *Signal Processing*, *93*(9), 2612–2625. Retrieved from http://dx.doi.org/10.1016/j.sigpro.2013.02.013 doi: 10.1016/j.sigpro.2013.02.013

Dong, C., Loy, C. C., & He, K. (2014). Image Super-Resolution Using Deep Convolutional Networks. *arXiv preprint*, 1–14.

Ishizaka, K., Miyamoto, T., Akimoto, S., Iketani, a., Hosomi, T., & Sakai, J. (2013). Power efficient realtime super resolution by virtual pipeline technique on a server with manycore coprocessors. *IEEE Symposium on Low-Power and High-Speed Chips - Proceedings for 2013 COOL Chips XVI*, *2*, 2–4. doi: 10.1109/CoolChips.2013.6547918

Shen, Y., Wu, X., & Deng, X. (2014, December). GPU-aided real-time image/video super resolution based on error feedback. In *2014 ieee visual communications and image processing conference* (pp. 286–290). IEEE. Retrieved from http://ieeexplore.ieee.org/lpdocs/epic03/wrapper.htm?arnumber=7051560 doi: 10.1109/VCIP.2014.7051560

Sirowy, S., & Forin, A. (2008). Where's the Beef ? Why FPGAs Are So Fast. *Microsoft Research*(September).

Su, H., Wu, Y., & Zhou, J. (2011). Adaptive incremental video super-resolution with temporal consistency. *Proceedings - International Conference on Image Processing, ICIP*, 1149–1152. doi: 10.1109/ICIP.2011.6115632

Tsai, R., & Huang, T. S. (1984). Multiframe image restoration and registration. *Advances in computer vision and Image Processing*, *1*(2), 317–339.

Wu, X., Xiang, H., & Lu, P. (2011). A GPU Accelerated Algorithm for Compressive Sensing Based Image Super-Resolution. *2011 Workshop on Digital Media and Digital Content Management*(60633030), 198–202. doi: 10.1109/DMDCM.2011.10

Yang, J., & Huang, T. (2010). Image super-resolution: Historical overview and future challenges. *Super-resolution imaging*. Retrieved from http://books.google.com/books?hl=en&lr=&id=fjTUbMnvOkgC&oi=fnd&pg=PA1&dq=Image+super-resolution:+Historical+overview+and+future+challenges&ots=53GZConOGy&sig=oHgGJVo_57Tv19cxLV_XMtC1OPw

Yang, J., Wright, J., Huang, T., & Ma, Y. (2010). Image Super-Resolution Via Sparse Representation. *IEEE Transactions on Image Processing*, *19*(11), 2861–2873. Retrieved from http://ieeexplore.ieee.org/ielx5/83/5602158/05466111.pdf?tp=&arnumber=5466111&isnumber=5602158$\delimiter"026E30F$nhttp://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=5466111 doi: 10.1109/TIP.2010.2050625

Zhang, L., Zhang, H., Shen, H., & Li, P. (2010). A super-resolution reconstruction algorithm for surveillance images. *Signal Processing*, *90*(3), 848–859. Retrieved from http://dx.doi.org/10.1016/j.sigpro.2009.09.002 doi: 10.1016/j.sigpro.2009.09.002