Cycles Numbers and Test Vectors in Sequential Circuits

Richard Remigoso, Tarek Alzeiback, Kevin Calva

Department of ECE, University of Illinois at Chicago, Chicago, IL
ECE464 - Testing and Reliability of Digital Systems, Fall 2019

Students: rremig2@uic.edu, malzei3@uic.edu, calva2@uic.edu
Professor: wenjing@uic.edu

ABSTRACT
A simulation in technology is an approximate way to expect the operation of a process represents its process over time. In electronics, there are different types of circuits, such as *Combinational Circuits* and *Sequential Circuits*. Combinational circuits are time independent circuits which do not depends upon previous inputs to generate any outputs. In the other hand, Sequential circuits are dependent on clock cycles, which also depends on present as well as past inputs to produce any outputs. Circuit simulation is a very important step in testing process as it mimics the outputs of actual circuits and also detects faults. Simulation speeds up the testing process, which will also assist in giving better results. As more and more complex circuits are developed, finding a more efficient and effective way to test circuits is necessary.

1 INTRODUCTION

In circuit simulation, cycles and test vectors are an integral part of the process. In this report, we will answer the following questions. How to test sequential circuits using simulation? Which parameter will speed up the faults cover? How to higher the chances of covering the faults in the circuit? Does increasing the number of cycles increase the chances of covering the faults or does changing the value of the test vector a better choice? Comparing the results between changing the number of clock cycles and test vectors will give us clues of how to speed-up the Fault Coverage Simulation in the sequential circuits. It could be hypothesized that increasing the number of test vectors would speed up the fault coverage.

2 METHODS AND PROCEDURES

The tests will be done by using sequential circuit benchmarks s27 and s298. Two methods will be applied for this test. First method is applying a test vector to the sequential circuit and monitoring the time needed to cover a fault with the increase of cycles numbers. Second method is applying a test vector to the same sequential benchmark, and increase the test vector value with using a constant cycles number for each test vector. Finally, by comparing the results of the two tests according to the time, different fault converge behaviors can be observed.

2.1 *Circuits, benchmarks, and faults list:*

The two methods should be applied on the same sequential circuit benchmark and the same fault for consistency. Using multiple benchmark sizes will give a better understanding of how circuit simulator would behave with different test vectors. Using only small scale circuits may not be enough, therefore, using different circuit sizes would be optimal for this experiment. Multiple faults should be tested as well.

2.2 *Simulator modification:*

The sequential circuit simulator should be modified, so it will be able to increase the value of the test vector. It should apply a new test vector after finishing a constant number of cycles. Also, the simulator should have a timer to find out which method is faster than the other. The simulator and timer should stop once it detects the fault.

2.2.1 *Increase number of Cycles:*

Increasing number of cycles will be used for the first method. Number of cycles will start from only one cycle, and it will keep increasing until detecting the fault.

2.2.2 *Test Vector value:*

Increasing the value of the test vector will be used for the second method. The value of the test vector will start from one, and it will keep increasing until detecting the fault.

2.2.3 *Timer:*

The timer depends on number of cycles. The timer is the total number of cycle runs to detect the fault coverage. Using the timer will help compare the two methods and find out which method is more efficient.

3 RESULTS

3.1 *Sequential Circuit(s27) Data Tables results:*

The following are data tables of fault coverage for each method. Each table will have 4 lines that indicates which method is used to test the sequential circuit. Several faults has been used for the same circuit.

3.1.1 *The default fault (G0-SA-0):*

Using the default fault and first method, the fault has been detected after the first cycle, and other cycles are not necessary because the fault has been detected. Therefore, method one took 1 cycles to detect the fault according the Timer in Table 1.

For second method, the fault has not been detected after the first cycle. It has been detect at timer 4. Therefore, The first method was faster for this fault.

Method One			
Number of Cycles #	**Timer**	**Test Vector**	**Detection Status**
1	1	5	Detected
2	2	5	Detected
3	3	5	Detected
4	4	5	Detected
5	5	5	Detected

Table 1. The table shows the results of s27 benchmark circuit with variety of number of cycles and constant test vector. The fault is the default fault at input 0.

Method Two			
Number of Cycles #	**Timer**	**Test Vector**	**Detection Status**
2	2	0	Not Detected
2	4	1	Detected
2	6	2	Not Detected
2	8	3	Detected
2	10	4	Not Detected

Table 2. The table shows the results of s27 benchmark circuit with variety of test vectors and constant number of cycles. The fault is the default fault at input 0.

3.1.2 *A fault at input to a DFF (G5-SA-1):*

It seems for stuck at G5, increasing the cycles number did not help in detecting the fault in the circuit. However, when changing the test vector, the fault was detected timer 2.

Method One			
Number of Cycles #	**Timer**	**Test Vector**	**Detection Status**
1	1	5	Not Detected
2	2	5	Not Detected
3	3	5	Not Detected
4	4	5	Not Detected
5	5	5	Not Detected
6	6	5	Not Detected
7	7	5	Not Detected
8	8	5	Not Detected
9	9	5	Not Detected
10	10	5	Not Detected

Table 3. The table shows the results of s27 benchmark circuit with variety of number of cycles and constant test vector. The fault is the default fault at input 5.

Method Two			
Number of Cycles #	**Timer**	**Test Vector**	**Detection Status**
2	2	0	Detected
2	4	1	Not Detected
2	6	2	Detected
2	8	3	Not Detected
2	10	4	Detected

Table 4. The table shows the results of s27 benchmark circuit with variety of test vectors and constant number of cycles. The fault is the default fault at input 5.

3.1.3 *A fault at an output of a gate (G8-SA-0):*

Similar to stuck at 5, the stuck at G8 showed the same behavior. Increasing the cycles number did not help to detect the fault in circuit. Only, when the test vector was changed that the fault was detected timer count 2.

Method One			
Number of Cycles #	**Timer**	**Test Vector**	**Detection Status**
1	1	5	Not Detected
2	2	5	Not Detected
3	3	5	Not Detected
4	4	5	Not Detected
5	5	5	Not Detected
6	6	5	Not Detected
7	7	5	Not Detected
8	8	5	Not Detected
9	9	5	Not Detected
10	10	5	Not Detected

Table 5. The table shows the results of s27 benchmark circuit with variety of number of cycles and constant test vector. The fault is the default fault at input 8.

Method Two			
Number of Cycles #	**Timer**	**Test Vector**	**Detection Status**
2	2	0	Detected
2	4	1	Not Detected
2	6	2	Detected
2	8	3	Not Detected
2	10	4	Detected

Table 6. The table shows the results of s27 benchmark circuit with variety of Test Vectors and constant number of cycles. The fault is the default fault at input 8.

3.2 *Sequential Circuit (s298) Data Tables results:*

The following are data tables of fault coverage for each method. Each table will have 4 lines that indicates which method is used to test the sequential circuit. Several faults has been used for the same circuit.

3.2.1 *The default fault (G0-SA-0):*

It seems for stuck at G0, increasing the cycle number did help to detect the fault in circuit at Timer 4.

For second method, the fault was not detected. Therefore, the first method was faster for this fault.

Method One			
Number of Cycles #	**Timer**	**Test Vector**	**Detection Status**
1	1	5	Not Detected
2	2	5	Not Detected
3	3	5	Not Detected
4	4	5	Detected
5	5	5	Detected
6	6	5	Detected
7	7	5	Detected
8	8	5	Detected
9	9	5	Detected
10	10	5	Detected

Table 7. The table shows the results of S298 benchmark circuit with variety of number of cycles and constant test vector. The fault is the default fault at input 5.

Method Two			
Number of Cycles #	**Timer**	**Test Vector**	**Detection Status**
2	2	0	Not Detected
2	4	1	Not Detected
2	6	2	Not Detected
2	8	3	Not Detected
2	10	4	Not Detected

Table 8. The table shows the results of S298 benchmark circuit with variety of test vectors and constant number of cycles. The fault is the default fault at input 5.

3.3 *Sequential Circuit (s820) Data Tables results:*

The following are data tables of fault coverage for each method. Each table will have 4 lines that indicates which method is used to test the sequential circuit. Several faults has been used for the same circuit. The default fault results has been listed bellow.

3.3.1 *The default fault (G0-SA-0):*

It seems for stuck at G0, increasing the cycle number and increasing the test vector value up to 100 did help to detect the fault in circuit.

Method One			
Number of Cycles #	**Timer**	**Test Vector**	**Detection Status**
1	1	5	Not Detected
2	2	5	Not Detected
3	3	5	Not Detected
4	4	5	Not Detected
5	5	5	Not Detected
6	6	5	Not Detected
7	7	5	Not Detected
8	8	5	Not Detected
9	9	5	Not Detected
100	100	5	Not Detected

Table 9. The table shows the results of S820 benchmark circuit with variety of number of cycles and constant test vector. The fault is the default fault at input 5.

Method Two			
Number of Cycles #	**Timer**	**Test Vector**	**Detection Status**
2	2	0	Not Detected
2	4	1	Not Detected
2	6	2	Not Detected
2	8	3	Not Detected
2	10	4	Not Detected
2	12	5	Not Detected
2	14	6	Not Detected
2	16	7	Not Detected
2	18	8	Not Detected
2	200	100	Not Detected

Table 10. The table shows the results of S820 benchmark circuit with variety of test vectors and constant number of cycles. The fault is the default fault at input 5.

4 DISCUSSION

In the s27 circuit, two faults were used as parameters, *G0-SA-0* and *G5-SA-1*. Based on the data tables, it would seem that neither results supported the hypothesis. For G0-SA-0, method one was the fastest in detecting the fault while method two was the fastest for G5-SA-1. Hence, this trial was inconclusive.

Moving forward to circuit s298 while only applying G0-SA-0, the results were different. Increasing the cycles numbers was faster than increasing the value of test vector. In this case, the fault was detected starting at timer 4. However, the fault was not detected at all using the same number of timer count during method two.

In circuit s820, increasing the maximum number of cycles and test vector did not help in detecting the fault. This may be due to non-linear test vector inputting for method two, and additional cycle number may be needed for method one.

CONCLUSIONS

Based on the circuits that we tested and the overall fault detection status, this experiment proved to be inconclusive. The results were varied and unpredictable. This is most likely due to the results being dependent on the

stuck at fault case, and the current limitation of the sequential simulator. For future work, the simulator can be improved further to accept multiple test vectors, which will be used for each cycles. Not only will this improve method two testing, but also increases the chances of finding fault coverage.

ACKNOWLEDGEMENTS

The authors would like to thank Professor Wenjing Rao for her helpful lectures.

REFERENCES

1. Echo360 Platform | Academic Computing and Communications Center, University of Illinois at Chicago. *https://accc.uic.edu/services/teaching-learning/lecture-capture/echo360-platform/* (accessed November 17)