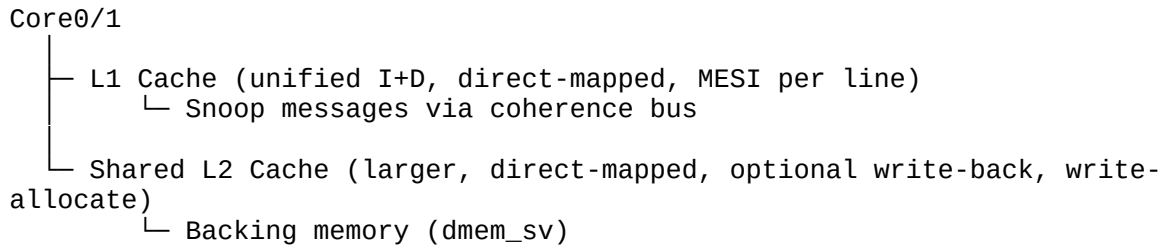


Hierarchy



Features

- MESI coherence:
 - **M**odified, **E**xclusive, **S**hared, **I**nvalid per line.
 - Core writes → invalidate other caches (broadcast via coherence bus).
- Unified L1 cache:
 - Handles both instruction fetch and data access (simplifies MESI implementation).
 - Split I/D can be added later.
- L2 Cache:
 - Larger, write-back, single shared instance.
 - Simple access latency model (MISS_PENALTY cycles).
- Pipeline core:
 - 5 stages (IF, ID, EX, MEM, WB).
 - Forwarding, load-use stall.
 - Branch flush.
 - CSR + exception skeleton.
 - Atomic ops (LL/SC style) using L1 reservation flag.
- Testbench:
 - Two cores, MESI bus.
 - IMEM preload via assembler helper.
 - Self-checking: memory and registers after atomic test program.