RISC-V RV64GC Instruction Set — Quick Reference

Base: RV64 (64-bit integer registers, 32 × x0–x31, 64-bit PC)
Encoding: 32-bit fixed instructions, plus 16-bit compressed (C extension)

Extensions included:

- I – Base integer
- M – Multiply/divide
- A – Atomics (LR/SC, AMOs)
- F – Single-precision floating point
- D – Double-precision floating point
- C – Compressed 16-bit encodings
- Zicsr – CSR access
- Zifencei – Instruction fence

Registers:
Integer: x0–x31 (64-bit), x0 is hardwired zero
Floating point: f0–f31 (IEEE-754, 64-bit, supports 32-bit ops)
CSRs: mstatus, misa, mtvec, mepc, satp, etc.

Memory model:
Load/store architecture, byte-addressable
Alignment: naturally aligned accesses required
Address space: Virtual 39/48-bit (Sv39/Sv48), Physical 36–48-bit typical
Page sizes: 4 KiB base, 2 MiB & 1 GiB superpages

Key instruction groups:
Integer arithmetic/logical: ADD, SUB, SLL, SRL, SRA, AND, OR, XOR, SLT
Immediate: ADDI, ANDI, ORI, XORI, SLTI, LUI, AUIPC
Control: BEQ, BNE, BLT, BGE, JAL, JALR
Load/store: LB, LH, LW, LD, LBU, LHU, LWU, SB, SH, SW, SD
Multiply/divide: MUL, MULH, DIV, REM
Atomics: LR.W/D, SC.W/D, AMOADD.W/D, AMOSWAP, etc.
Floating point: FADD, FSUB, FMUL, FDIV, FSQRT, FSGNJ, FMIN, FMAX, FCVT, FEQ, FLT, FLE
System/CSR: CSRRW, CSRRS, CSRRWI, ECALL, EBREAK, FENCE, FENCE.I
Compressed (C): C.ADDI, C.LW, C.SW, C.J, C.BEQZ, C.BNEZ, etc.

Privileged instructions:
mret, sret (return from trap), wfi (wait for interrupt)

Custom hooks (SoC-specific):
DVFS control: via OpenSBI vendor extension (ecall extid=0x7C595246, YCFR)
Scratchpad SPAD64: memory-mapped window + DMA ioctls
GPGPU chiplet: coherent attach, separate ISA not covered here