Initialization Vreudocode: Twen on dock for for Port & Set direction of Port & as output

Digital Enable & pin 0 - pin 3

Read data from Port & information of Calculate inputes

Corresponding output should be duplayed.

C:\Users\reyes\OneDrive\Desktop\Keil\EE319KwareSpring2020\Lab1_EE319K\main.s

```
;************** main.s *********
    ; Program initially written by: Yerraballi and Valvano
    ; Author: Roberto Reyes
    ; Date Created: 1/15/2018
    ; Last Modified: 2/04/2020
    ; Brief description of the program: Solution to Lab1
    ; The objective of this system is to implement odd-bit counting system
    ; Hardware connections:
9
    ; Output is positive logic, 1 turns on the LED, 0 turns off the LED
10
       Inputs are negative logic, meaning switch not pressed is 1, pressed is 0
11
          PEO is an input
12
          PE1 is an input
         PE2 is an input
1.3
         PE3 is the output
14
    ;
15
    ; Overall goal:
16
        Make the output 1 if there is an odd number of switches pressed,
17
          otherwise make the output 0
18
19
   ; The specific operation of this system
20
         Initialize Port E to make PEO, PE1, PE2 inputs and PE3 an output
        Over and over, read the inputs, calculate the result and set the output
21
22
    ; PE2 PE1 PE0 | PE3
23
    ; 0
            0
                0
                     | 1
                             odd number of 0's
24
    ; 0
            0
                 1
                     | 0
                             even number of 0's
25
    ; 0
                 0
                       0
            1
                             even number of 0's
26
    ; 0
            1
                 1
                        1
                             odd number of 0's
27
    ; 1
            0
                 0
                       0
                             even number of 0's
    ; 1
                       1
28
            0
                             odd number of 0's
                 1
    ; 1
29
           1
                0
                       1
                             odd number of 0's
30
           1
                1
                     | 0
                             even number of 0's
    ;There are 8 valid output values for Port E: 0x01,0x02,0x04,0x07,0x08,0x0B,0x0D, and 0x0E.
33
    ; NOTE: Do not use any conditional branches in your solution.
34
            We want you to think of the solution in terms of logical and shift operations
3.5
36
    GPIO PORTE DATA R EQU 0x400243FC
37
     GPIO PORTE DIR R
                        EQU 0x40024400
38
     GPIO_PORTE_DEN_R
                        EQU 0x4002451C
     SYSCTL RCGCGPIO R EQU 0x400FE608
39
40
41
            THUMB
42
            AREA
                    DATA, ALIGN=2
    ; global variables go here
43
44
           ALIGN
4.5
           AREA
                   |.text|, CODE, READONLY, ALIGN=2
          EXPORT Start
47 Start
48
         ; code to run once that initializes PE3, PE2, PE1, PE0
49
         LDR RO, =SYSCTL RCGCGPIO R
50
         LDR R1, [R0]
51
         ORR R1, #0x10
52
         STR R1, [R0]
53
         NOP
54
         NOP
55
         LDR RO, =GPIO PORTE DIR R
         LDR R1, [R0]
56
         ORR R1, #0x08
57
58
         STR R1, [R0]
         LDR RO, =GPIO_PORTE_DEN_R
59
         LDR R1, [R0]
         ORR R1, #0x0F
         STR R1, [R0]
63
64
         ; code that runs over and over
6.5
         LDR RO, =GPIO_PORTE_DATA_R
66
         LDR R1, [R0]
67
         AND R2, R1, #0x01
68
         AND R3, R1, \#0\times02
69
         LSR R3, #1
70
         AND R4, R1, \#0\times04
71
         LSR R4, #2
72
         EOR R5, R2, R3
```

C:\Users\reyes\OneDrive\Desktop\Keil\EE319KwareSpring2020\Lab1_EE319K\main.s

```
EOR R5, R5, R4
74
         EOR R5, #1
         LSL R5, #3
STR R5, [R0]
75
76
77
78
         В
               loop
79
80
81
                          ; make sure the end of this section is aligned
82
83
            END
                          ; end of file
84
```

TExaS Lab 1 \times Port E Hardware SW2 | SW1 | SW2 | SW2 | SW2 | SW2 | SW2 | SW2 | SW3 | TM4C123 16 MHz PE0 PE3 LED A PE1 •3.3 ≹_ SW3 **▽** PE2 • Port E Registers DATA: 0x08 LOCK: 0x01 PUR: 0x00 DIR: 0x08 PDR: 0x00 CR: 0xFF RCGCGPI0: 0x00000010 DEN: 0x0F Clock enabled Grading Controls Score: 0

Grade

Copy this to EdX:

Number from EdX:

TExaS Lab 1 X Port E Hardware 16 MHz TM4C123 PE0 PE3 ED 🛖 PE1 ▾ PE2 ▼ Port E Registers DATA: 0x04 PUR: 0x00 LOCK: 0x01 DIR: 0x08 PDR: 0x00 CR: 0xFF RCGCGPI0: 0x00000010 DEN: 0x0F Clock enabled Grading Controls Score: 0 Grade Number from EdX:

Copy this to EdX: