Udacity Artificial Intelligence Nanodegree Assignment 2

Review of “Deep Blue” by the IBM Watson Team

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Introduction

This is a review of the paper “Deep Blue” by the IBM Watson Team published in Artificial Intelligence in 2002. The paper describes a brief history of the Deep Blue technology and it covers the new techniques they implemented.

Lineage

Deep Blue had a long history:

ChipTest and Deep Thought: Early efforts started at Carnegie Mellon in the 1980s. They used a single-chip chess move generator and acheived search speeds of 500,000 to 700,000 positions per second.

Deep Thought 2: At the end of the 80s part of the team moved to IBM and made improvements including multi-processing using 24 chess chips, enhanced evaluation hardware, improved search software, and an extended book.

Deep Blue I: This version ran on a 36-node IBM RS/6000 SP with 216 chess chips. It achieved a search speed of 50-100 million positions per second. It still lost to Garry Kasparov in 1996.

Deep Blue II: The version that finally beat Kasparov in 1997 had many improvements including a new chess chip and managed speeds from 100 to 330 million positions per second.

System Overview

Deep Blue was a massively parallel system composed of a 30 node machine with 480 single-chip chess search engines. Each chip had 1Gb of RAM and communicated via a high speed switch.

The Chess Chip

The chess chip divides into three main functions:

Move Generation: This was implemented as an 8x8 array of combinational logic, effectively a silicon chessboard. It generates all possible moves in parallel and selects one to present. This way it can provide a best-first ordering.

Evaluation Function: The chip provided both a fast and a slow evaluation with the fast version used when an approximation was good enough.

Search Control: A number of state machines were used to implement null-window alpha-beta search. The chess chips also supported the use of an external FPGA (Field Programmable Gate Array) to provide access to additional functionality but this was not used.

Software Search

A selective search algorithm was implemented called “dual credit with delayed extensions”. This was based on a number of principles: extended forcing/forced pair moves, forced moves are expectation dependent, fractional extensions, delayed extensions, dual credit, and preserve search envelope.

Hardware Search

A hardware search, implemented on the chess chip, carried out a fixed-depth null-window search. This is a fast but relatively simple search that allows the host processor to do other work. The host polls the chip to determine when the search has completed.

Parallel Search

The hardware hierarchy was one SP processor used to control the other 29 nodes which in turn each controlled 16 chess chips. The early iterations are carried out on the master node and as the search gets deeper the jobs get allocation throughout the system.

Evaluation Function

The chess chip recognized approximately 8000 different “patterns” ranging from a particular piece on a particular square to very complex scenarios such as pawns being semi-transparent to rooks if they are levering (having the possibility of capturing an enemy pawn). Each pattern can be assigned a static or dynamic value - dynamic values can be scaled based on the value and type of other pieces on the board.

Conclusion

The success in 1997 was due to many factors including large search capability, non-uniform search, and a complex evaluation function. As with all systems it was felt improvements were still possible in areas such as parallel search efficiency, the hardware evaluation function, and better pruning mechanisms.