

# TCPWM (QuadDec mode) example project

2.0

#### **Features**

- Project uses TCPWM component with Quadrature Decoder mode configuration
- Indicate capture interrupts on LED

### **General Description**

This example project demonstrates the TCPWM component usage in the Quadrature Decoder mode.

## **Development kit configuration**

This example project is designed to be executed on CY8CKIT-042 from Cypress Semiconductor. A full description of the kit, along with more example programs and ordering information, can be found at http://www.cypress.com/go/cy8ckit-042.

- 1. Connect P2[0] to P0[1].
- 2. Connect the logic low (Gnd) or the logic high (3.3V) signal to P0[0].
- 3. Build the project and program the hex file on to the target device.
- 4. Power cycle the device and observe the results on the LEDs.

The project requires configuration settings changes in order to run on other kits from Cypress Semiconductor. The list of the supported kits is provided in **Table 1**.

In order to switch from CY8CKIT-042 to any other of the supported kit the following steps have to be performed:

1. Change the project's device which corresponds to the available kit (Table 1) with a Device Selector called from the project's context menu.

Table 1. Development Kits vs parts

Development Kit	Device
CY8CKIT-042	CY8C4245AXI-483
CY8CKIT-040	CY8C4014LQI-422
CY8CKIT-042-BLE	CY8C4247LQI-BL483

2. Change assignment of the pin component to physical pin.

In the Workspace Explorer window, double-click the project's design-wide resource file and assign the pins LED\_GREEN, PhiA\_Out accordingly to **Table 2**.

Pin Name	Development Kit			
Pili Naille	CY8CKIT-042	CY8CKIT-040	CY8CKIT-042 BLE	
LED_GREEN	P0[2]	P1[1]	P3[6]	
PhiA_Out	P2[0]	P2[0]	P1[0]	
PhiA_In	P0[1]	P0[1]	P0[1]	
PhiB_In	P0[0]	P0[0]	P0[0]	

# **Project configuration**

The example project consists of the following components: TCPWM, Clock, two digital output pins, two digital input pins, and Interrupt. The TCPWM is used as the Quadrature Decoder mode with the 1x Decoding mode. One of the output pins is used for PhiA signal generation. Another output pin is used to reflect a capture event when interrupts happen. The top design schematic is shown in Figure 1.

#### Parameters used:

- Quadrature Decoder mode
- Encoding mode = 1x
- Interrupt mode = Capture

The TCPWM (Quadrature Decoder mode) datasheet example project

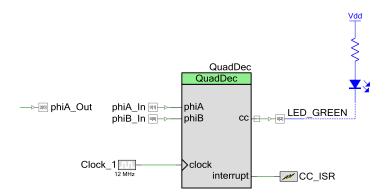


Figure 1. Top design schematic.

The TCPWM component GUI configuration (Figure 2, Figure 3):



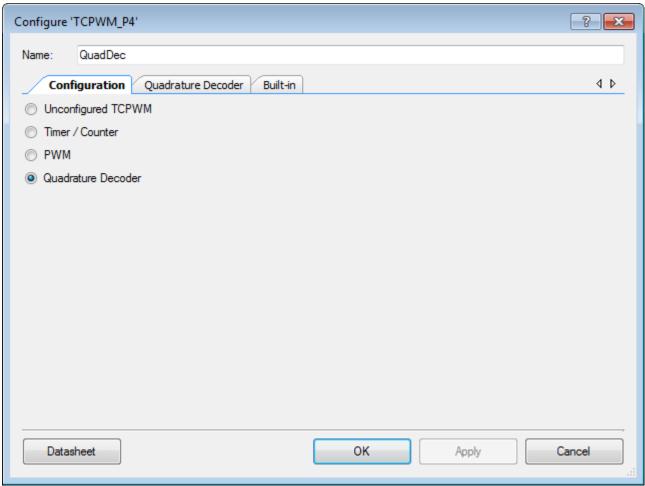


Figure 2. TCPWM Component Configuration Tab



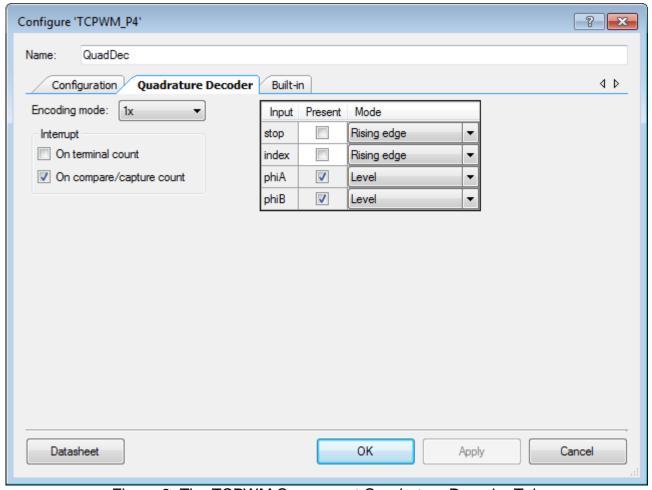


Figure 3. The TCPWM Component Quadrature Decoder Tab

# **Project description**

The counter is initialized with the mid-point counter value (0x8000) on an index event. A positive edge on phiA increments the counter when phiB is 0 and decrements the counter when phiB is 1. In the project, the TCPWM counts from 0x8000u down to 0u or from0x8000 to 0xFFFFu . If the counter reaches the 0xFFFFu value, the interrupt happens, the green color LED blinks for 200ms, and the counter is initialized with the mid-point value (0x8000u).

The index event is generated by the API (QuadDec\_TriggerCommand(QuadDec\_MASK, QuadDec\_CMD\_RELOAD)).

The phiA signal is generated by the PhiAbGeneration function in the main.c file.

If the phiB signal connected to the logic low signal, a simulation is emulated, when the shaft is rotating in the clockwise direction (A leads B). If the phiB signal is connected to the logic high signal, a situation is emulated, when the shaft is rotating in the counter-clockwise direction (B leads A).



#### **Expected results**

The green color LED is blinking when the counter value is captured (0xFFFF).

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