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Marcos Antônio de Oliveira Campos Filho

COMPARISON OF DIGITAL DEMODULATION ALGORITHMS FOR LVDT SENSORS IN CIRCUITS WITH LIGHTNING PROTECTION

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COMPARISON OF DIGITAL DEMODULATION ALGORITHMS FOR LVDT SENSORS IN CIRCUITS WITH LIGHTNING PROTECTION

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Para Bianca, Victor, Rosane e Marcos.

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"I was born not knowing and have had only a little time to change that here and there"
— Richard Feynman

Resumo

A implementação de Sistemas de Controle digitais pode trazer muitas vantagens para os fabricantes de aeronaves, dentre eles melhoria de confiabilidade, uma vez que parte dos circuitos analógicos são substituídos por software, redução de custos através da reutilização de hardware e maior tolerância a fatores ambientais como temperatura e ruído elétrico.

Um modelo para acquisição digital de posição em superfícies de controle primárias numa aeronave é apresentado, composto por um Transformador Diferencial Linear Variável (LVDT, em inglês) como elemento sensor de deslocamento, um filtro passivo para proteção contra transientes provenientes de descargas elétricas, um conversor Analógico/ Digital e um sistema de demodulação digital. Uma vez integrado ao modelo de atuador eletro-hidráulico desenvolvido em (BALLESTEROS, 2015), o modelo serve como plataforma para análise de desempenho de algorítmos de demodulação digital, o objetivo final deste trabalho.

Duas estratégias, o Detector de Pico, baseado na amplitude instantânea do sinal e o *Oversampling/Averaging*, baseado no valor médio do sinal durante um determinado período foram comparadas. Ambos os algorítmos permitiram o fechamento da malha de controle e o posicionamento correto da superfície, com o Detector de Pico produzindo uma resposta ligeiramente mais rápida enquanto o *Oversampling/Averaging* sendo mais robusto em relação ao ruído e tendo um erro de estado estacionário menor. Esse trabalho realiza uma implementação e comparação de tais algorítmos digitais de demodulação para obter posição a partir de sensores LVDT aplicado ao servoposicionamento de um atuador eletro-hidráulico.

Abstract

The implementation of digital Control Systems can bring several advantages to aircraft manufacturers including improvement in reliability, since parts of analog circuitry would be replaced by software, reduced costs by hardware reusing and increased tolerance to environmental conditions such as temperature and electrical noise.

A model for a digital position acquisition system for aircraft primary control surfaces is presented, comprised by a Linear Variable Differential Transformer (LVDT) as displacement sensing element, a protective passive filter for transients caused by lightning strikes, an Analog-to-Digital converter and a digital demodulation system. Once integrated with the electro-hydraulic actuator model developed in (BALLESTEROS, 2015), the model serves as platform to analyse the performance of digital demodulation algorithms, the main objective of this work.

Two strategies, the Peak Detector, based on the instant amplitude of the signal and the Oversampling/Averaging, based on the mean value of the signal over a period of time were compared. Both algorithms allowed closing the control loop and correctly positioning the surface, with Peak Detector producing a slightly faster response while Oversampling/Averaging being more robust to noise and having smaller steady state error. This work performs an implementation and comparison of such digital demodulation algorithms to retrieve positioning from LVDTs applied to servo-positioning of an electro-hydraulic actuator.

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List of Abbreviations and Acronyms

AC	Alternating Current
ADC	Analog-to-Digital Converter
CLAW	Controw Law
CPU	Central Processing Unit
DAC	Digital-to-Analog Converter
DAE	Differential Algebraic Equation
DC	Direct Current
DNL	Differential Nonlinearity
EHSV	Electrohydraulic Servovalve
EMF	Electromotive Force
ENOB	Effective Number of Bits
FS	Full-scale
FSR	Full-scale Range
GSPS	Giga-Samples Per Second
INL	Integral Nonlinearity
kSPS	kilo-Samples per Second
LSB	Least Significant Bit
LUT	Lookup Table
LVDT	Linear Variable Differential Transformer
MSPS	Mega-Samples Per Second
NMOS	N-type Metal Oxide Semiconductor
P	Proportional
PD	Proportional-Differential
PI	Proportional-Integral
PID	Proportional-Integral-Differential
PMOS	P-type Metal Oxide Semiconductor
RMS	Root Mean Square
RTCA	Radio Technical Commission for Aeronautics
SAR	Successive Approximation Register
SFDR	Spurious-free Dynamic Range

SINAD	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
THD	Total Harmonic Distortion
ZS	Zero-scale

List of Symbols

V_a	Voltage on secondary A
V_b	Voltage on secondary B
R_x	Resistance of element x
L_x	Self-inductance of element x
M_{ap}	Mutual inductance from primary to secondary A
M_{bp}	Mutual inductance from primary to secondary B
V_{map}	Induced voltage on secondary A
V_{mbp}	Induced voltage on secondary B
V_{mabp}	Induced voltage on primary
i_a	Current on secondary A
i_b	Current on secondary B
i_p	Current on primary
k	Coupling coefficient
r	Linear Variable Differential Transformer voltage ratio
n	Number of bits for an Analog-to-Digital Converter
T_s	Sampling period
V_{f_k}	k-th harmonic amplitude
R	Horn radius
L	Actuator length in neutral position
C	Distance from non-moveable surface and control surface's anchorage point
S	Actuator stroke
θ	Control surface angular position
Φ	Magnetic flux
T_{w_k}	Duration of the window for channel k in seconds
N_{cycles_k}	Duration of the window for channel k in simulation cycles
MST	Simulation time step
Z_{x_t}	Zero crossing threshold

Contents

1 Introduction

Only 65 years separate the first controlled, powered and sustained heavier-than-air human flight from the first digital computer controlled flight. After English engineer George Cayley figured out the mechanisms of lift generation in the early years of 1800, it became possible for his sucessors to experiment and develop technologies, with understanding of the physics involved. The first aircrafts were built to be highly inherently stable, as it was thought to be a desirable trait, but there are two main problems with excess of stability: the first one is making the aircraft too dificult to control and change flight conditions; the second is the strong responses to wind perturbations when the aircraft tries returning to equilibrium (TOMAYKO, 2000).

It became clear with further experimentation in the following years that a less stable aircraft was necessary, instead of pursuing a way to mantain static stability. The new paradigm of using the pilot to close the loop, forming a dynamically stable system would permit the use of automatic control in the future. As the years passed and technology advanced, faster and larger aircrafts were created and the new systems were presenting faster dynamics or requiring too much strength to be operated, easily exceeding the capabilities of human pilots. In response, hydraulic systems emerged to extend pilot powers, feedback systems allowed more complex forms of control, and togheter with other innovations, they paved the way for the actively controlled aircrafts.

The use of computers to actively control aircrafts unlocked the potential to countless applications, allowing completely unstable stealth planes to fly, landing with zero visibility and automatic compensation for changes in flight conditions such as variable wing geometry and load drop, among others. To accomplish these, the computer must rely on a wide range of sensors, responsible to feed the necessary data, keeping it aware of current conditions.

Which such complexity and safety concerns, the design process is no easy task. There are many variables and conditions that must be tested to ensure proper functioning on the diverse operating scenarios. The use of computer simulations greatly reduces the developing and testing time, helping to predict how the system behavior is affected by varying parameters, including failure situations and even allowing hardware-in-the-loop

tests, where the real hardware is used, such as in the Iron Bird (AIRBUS, 2015).

1.1 Motivation and Objective

Understanding the advantages and limitations of digital algorithms may allow Flight Control Systems to move towards a digital implementation, bringing advantages including reduction of weight and volume, since parts of the system would be replaced by software, reduced costs by hardware reusing, and increased tolerance to environmental conditions such as temperature and electrical noise.

The main objective of this work is to evaluate the performance of two digital algorithms, Peak Detector and Oversampling/Averaging, to demodulate the output of a Linear Variable Differential Transformer (LVDT), utilized as positioning sensor on an electro-hydraulic actuator.

To met this objective, a model capable of representing the dynamics and relevant non-linearities of each element of the position control loop will be created. The actuator position acquisition system, composed of an LVDT, a signal conditioner and analog-to-digital converters will then be integrated to the electro-hydraulic actuator model developed in (BALLESTEROS, 2015) and the composite model will serve as platform to analyse both demodulation algorithms under the following aspects:

1. Steady state error for a step input;
2. Effect of number of sampled points per cycle;
3. Tolerance to noise on input.

1.2 Bibliographic review

(NYCE, 2003) presents in detail the operation of several types of linear position sensors used in industry, their performance specifications and applications. The topics about the Linear Variable Differential Transformer also cover signal conditioning and analog demodulation.

(DIAS, 2015) presents an electrical model of an LVDT sensor which was used to simulate and design a signal conditioning circuit and synchronous analog demodulation scheme.

(RADIO TECHNICAL COMMISSION FOR AERONAUTICS, 2010) defines standard environmental test conditions and procedures for airborne equipment (DO-160). The purpose of

these tests is to provide a controlled (laboratory) means of assuring the performance characteristics of airborne equipment in environmental conditions similar of those which may be encountered in airborne operation of the equipment. Specifically, Section 22 (Lightning Induced Transient Susceptibility) provides the specific guidelines for testing the resilience of an equipment against indirect lightning effects.

(MEASUREMENTE COMPUTING, 2004), (TEXAS INSTRUMENTS, 1995), (MAXIM INTEGRATED, 2002) and (NATIONAL SEMICONDUCTORS, 2003) present in details the inner workings of analog-to-digital converters (ADCs), covering the modern architectures with their advantages and limitations, the non-idealities inherent to these devices and how they are mitigated, in addition to pratical aspects of real-world applications.

(CONSTANTINO, 2010) develops a high fidelity model representative up to high frequencies of a Flight Control System with hydraulic actuation on active-active mode, comprised of an EHSV, hydraulic actuator, a position loop and the control surface. The step input response and frequency response were shown to be close to a real system response up to high frequencies and the behavior of an oscillatory mal-function scenario was studied, showing the expected level of structure load, as well as its fatigue life consumption.

(BALLESTEROS, 2015) develops a primary actuator classic sizing methodology, which is validated using an actuator model based on (CONSTANTINO, 2010). The performance for different classical controllers (P, PI, PD, and PID), in addition to modern control approaches is evaluated. The modern controllers presented good performance and enhanced the actuator's dynamic stiffness especially for frequencies above 10 Hz, allowing a piston area reduction of one seal size. It was also presented the feasibility to design an optimized flight control actuator, taking credit of a modern control approach that would reduce hydraulic consumption, and the actuator's weight and size, bringing benefits to the aircraft performance.

(ASTROM; WITTENMARK, 2011) provides a broad overview of theory and practical aspects discrete-time systems, covering the mathematical foundation, sampling theory, design and analysis of digital controllers.

1.3 Organization

In Chapter 1, the introduction for this work is presented. Chapter 2 provides theoretical background for the positioning sensor and data acquisition techniques including filtering, sampling and analog to digital conversion. In Chapter 3, the process of model synthesis and validation is presented. Chapter 4 covers the implementation and comparison of two different digital demodulation techniques. Finally, Chapter 5 presents the conclusions and future work.

2 Theoretical Background

This chapter provides a brief theory review about the subjects addressed in this work. More details are provided on the indicated references.

2.1 Linear Variable Differential Transformer

2.1.1 Overview

The Linear Variable Differential Transformer (LVDT) is a position transducer that is contactless (i.e. no physical connection between the moving and the stationary parts), absolute reading (indicates the position with respect to a constant reference) and has essentially infinite resolution (NYCE, 2003). It is comprised of three coils within which a magnetically permeable core moves (figure 2.1) to provide variable magnetic coupling between the primary coil and the secondary coils CH_A and CH_B (figure 2.2).

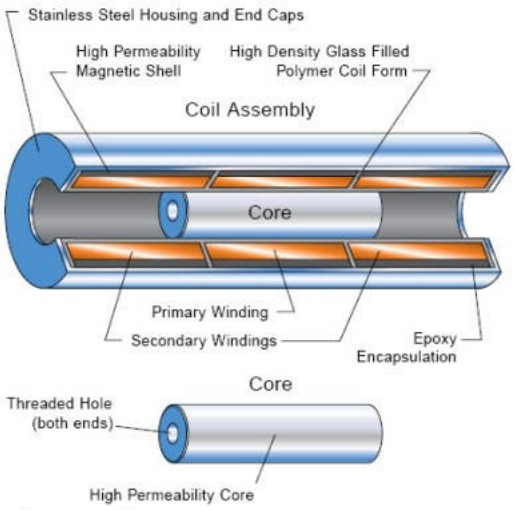

FIGURE 2.1 – LVDT cutaway - Source: (TE CONNECTIVITY, 2016) (modified)

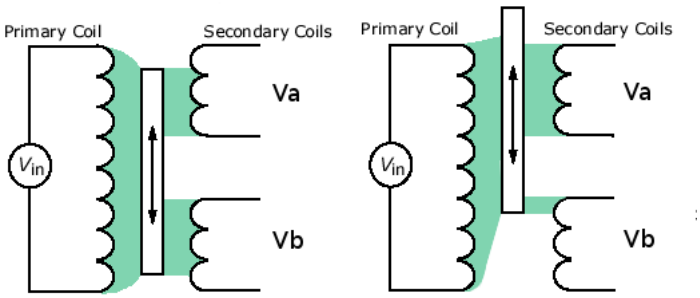

FIGURE 2.2 – Variable magnetic coupling - Source: (EFUNDA INC, 2016) (modified)

The core is connected to the exterior by rod made of non-magnetic material and moves within the bore of the LVDT without touching the internal walls. As the core moves, the induced voltages across the secondaries varies linearly, increasing on one channel and decreasing on another. These voltages are proportional to the input voltage on the primary and the LVDT sensitivity, usually given in $[(mV/V)/mm]$ or milivolts per volts of excitation, per milimeter. A wide variety of measurement ranges are available, typically from $\pm 100\mu m$ to $\pm 25cm$ (ZUMBAHLEN, 2016).

Other relevant metrological characteristics of the LVDT are:

(a) Excellent repeatability, i.e. the ability to reproduce the same output for repeated trials of exactly the same input, due to very low hysteresis. This is the only irreducible and uncorrectable source of static error and the limiting factor on measurement using sensors (MACROSENSORS, 2016).

(b) Low nonlinearity, as pratical sensors can be constructed with nonlinearities of less than 0.2% from best straight line (least squares) (figure 2.3), which can be reduced even further with signal post processing (NYCE, 2003).

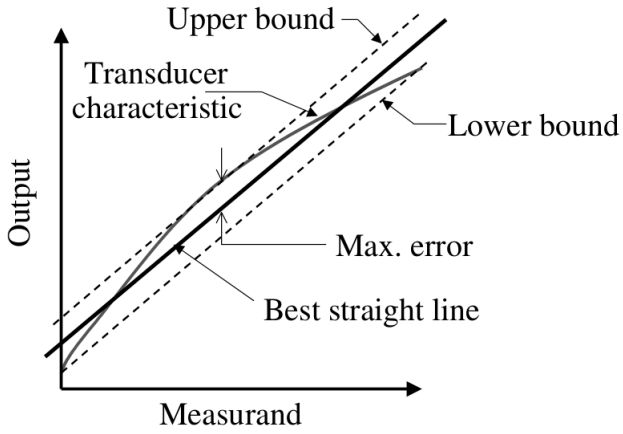

FIGURE 2.3 – Best Straight Line Nonlinearity - Source: (NYCE, 2003)

2.1.2 Electrical model

An equivalent circuit for the LVDT is presented in figure 2.4, similar to one used by (DIAS, 2015). To obtain the equation for the primary winding, an excitation voltage source is connected to the primary (figure 2.5).

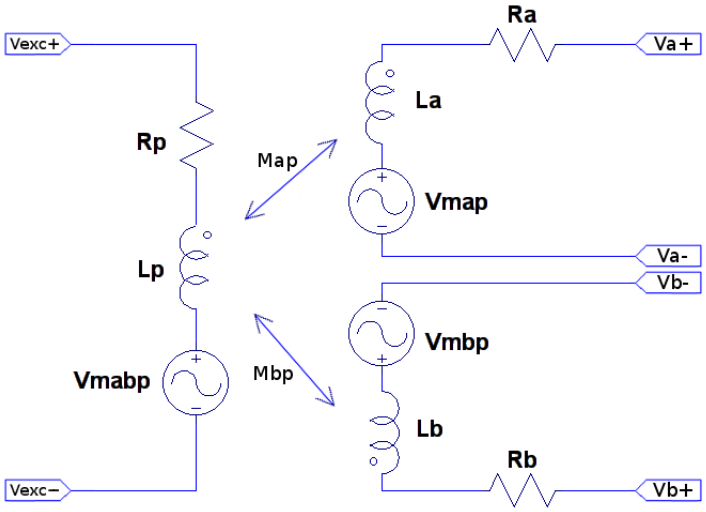

FIGURE 2.4 – LVDT equivalent circuit

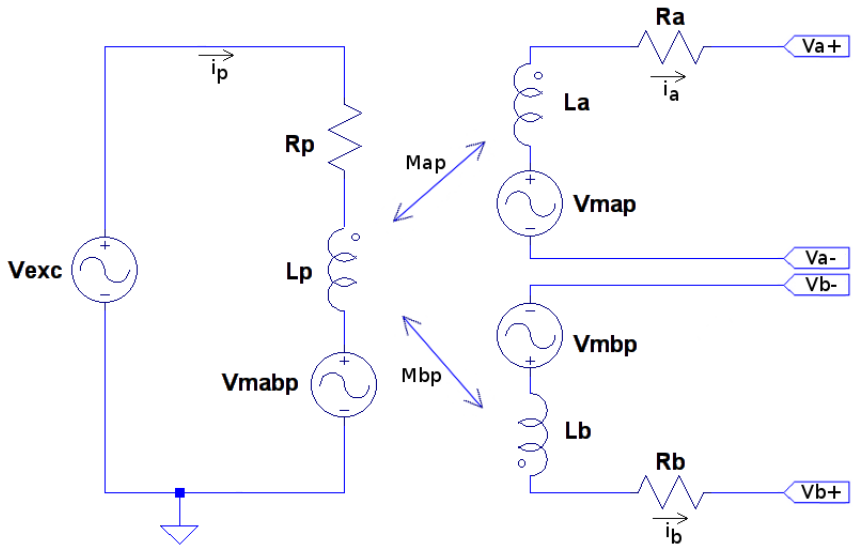

FIGURE 2.5 – LVDT equivalent circuit with excitation voltage

The voltage on primary is given by equation 2.1,

$$V_{exc} = R_p i_p + L_p \frac{di_p}{dt} + V_{mabp} \tag{2.1}$$

where the values L_p and R_p are the primary self-inductance and resistance, respectively, i_p is the current on primary and V_{mabp} (equation 2.2) is the sum of the voltages induced by the currents i_a and i_b circulating on each secondary coil. The mutual inductances M_{ap} and M_{bp} between the primary coil and each secondary are given by equation 2.3 (ELECTRONICS TUTORIALS, 2016).

$$V_{mabp} = M_{ap} \frac{di_a}{dt} + M_{bp} \frac{di_b}{dt} \tag{2.2}$$

$$\begin{aligned} M_{ap} &= k_a \sqrt{L_a L_p} \\ M_{bp} &= k_b \sqrt{L_b L_p} \end{aligned} \tag{2.3}$$

The values k_a and k_b are called *coupling coefficients*, meaning the amount of inductive coupling that exists between the coils and is expressed as a fractional number between 0 and 1, where 0 indicates no inductive coupling, and 1 indicating full or maximum inductive coupling.

The voltages induced on each secondary are also determined by the mutual inductance

and represented by the voltage sources V_{map} and V_{mbp} in figure 2.4. They are given by:

$$\begin{aligned} V_{map} &= M_{ap}\frac{di_p}{dt} \\ V_{mbp} &= M_{bp}\frac{di_p}{dt} \end{aligned} \tag{2.4}$$

Using equation 2.4, the voltages on each secondary are given by equations 2.5, 2.6 and 2.7. The values L_x and R_x are the self-inductance and resistance of each coil indicated by x, respectively.

$$\begin{aligned} V_a &= V_{a_+} - V_{a_-} \\ V_b &= V_{b_+} - V_{b_-} \end{aligned} \tag{2.5}$$

$$V_{map} = L_a\frac{di_a}{dt} + R_a i_a + V_a \tag{2.6}$$

$$V_{mbp} = L_b\frac{di_b}{dt} + R_b i_b + V_b \tag{2.7}$$

For simulation purposes, the open wiring at each secondary is replaced by a high value resistive load R_{METER_x}, where the voltage will be measured across (figure 2.6). Equation 2.6 becomes 2.8 and equation 2.7 becomes 2.9.

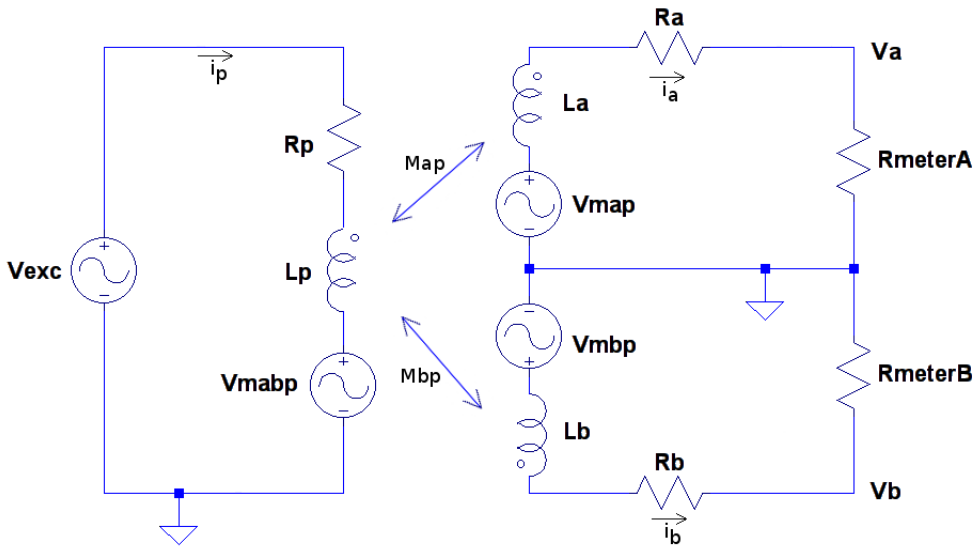

FIGURE 2.6 – LVDT equivalent circuit with excitation voltage and measurement resistors

$$V_{map} = L_a \frac{di_a}{dt} + R_a i_a + R_{METER_a} i_a \tag{2.8}$$

$$V_{mbp} = L_b \frac{di_b}{dt} + R_b i_b + R_{METER_b} i_b \tag{2.9}$$

The model presented in figure 2.6 uses the concept of voltage sources in series with the coils, which is useful to determine values for the components. Despite LVDTs being widely used in the industry the information presented on the majority of public datasheets was scarce and incomplete regarding electrical parameters.

More important than the actual values of the components per se is the behaviour of the model regarding the relation between excitation and output voltages, phases and frequency response. To find suitable values for the simulation, the following procedure was used in conjunction with typical values collected from multiple sources ((TE CONNECTIVITY, 2017), (ALTHEN, 2017), (ACTIVE SENSORS, 2017)) and summarized on table 2.1.

TABLE 2.1 – Typical values for LVDT electrical parameters

Parameter	Value
Minimum impedance on primary ($Z_{p_{min}}$)	650Ω
Total maximum impedance on secondaries ($Z_{s_{max}}$)	2000Ω
Maximum current on primary ($i_{p_{max}}$)	$7mA_{RMS}$
Maximum phase on output	15.00°

1. Obtain the excitation voltage and frequency from datasheet;

$$V_{exc} = 7V_{RMS} \text{ @ } 3000Hz \tag{2.10}$$

2. Select values for primary self-inductance L_p and resistance R_p so that the primary impedance Z_p on excitation frequency is above $Z_{p_{min}}$ and primary current is below $i_{p_{max}}$.

$$\begin{aligned} L_p &= 80mH \\ R_p &= 200\Omega \end{aligned} \tag{2.11}$$

$$
\begin{aligned}
Z_p &= R_p + X_{L_p} \\
Z_p &= R_p + (2\pi f_{exc} L_p)j \\
Z_p &= 200 + (2\pi * 3000 * 80 * 10^{-3})j \\
Z_p &= 200 + 1507.96j\Omega \\
Z_p &= 1521.17\underline{/82.45^\circ}
\end{aligned}
\tag{2.12}
$$

For the current on primary i_p:

$$
\begin{aligned}
i_p &= \frac{V_{exc}}{Z_p} \\
i_p &= \frac{7\underline{/0^\circ}}{1521.17\underline{/82.45^\circ}} \\
i_p &= 4.60\underline{/-82.44^\circ}\ mA
\end{aligned}
\tag{2.13}
$$

3. Using equation 2.4, the result obtained in equation 2.13 and the desired output for the LVDT (figure 2.7), calculate the mutual inductance necessary to achieve the output voltages when the LVDT is retracted and extended. A large value in the order of $M\Omega$ is used for R_{METER_x} (FLUKE CORPORATION, 2013), so $V_{map} \approx V_a$ and $V_{mbp} \approx V_b$.

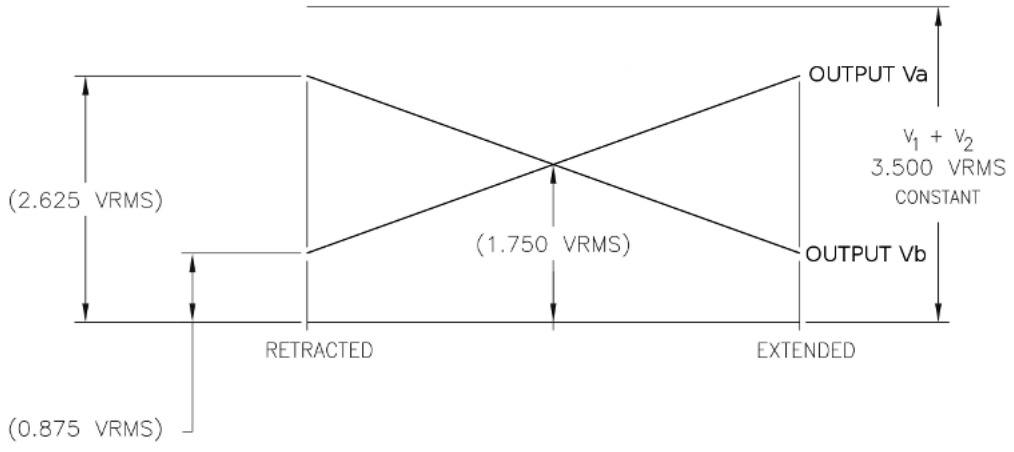

FIGURE 2.7 – LVDT output

$$
\begin{aligned}
i_p &= 4.60\sqrt{2} * sin(2\pi * 3000 * t - 82.44^\circ)\ mA \\
\frac{di_p}{dt} &= 4.60\sqrt{2} * 2\pi * 3000 * cos(2\pi * 3000 * t - 82.44^\circ)\ \frac{mA}{s}
\end{aligned}
\tag{2.14}
$$

$$\begin{aligned} V_{ret} &= M_{ret}\frac{di_p}{dt} \\ 0.875\sqrt{2} &= M_{ret}\frac{di_p}{dt} \\ M_{ret} &= 10.09\ mH \end{aligned} \tag{2.15}$$

$$\begin{aligned} V_{ext} &= M_{ext}\frac{di_p}{dt} \\ 2.625\sqrt{2} &= M_{ext}\frac{di_p}{dt} \\ M_{ext} &= 30.27\ mH \end{aligned} \tag{2.16}$$

4. Select values for secondary self-inductance L_x greater than the maximum mutual inductance and resistance R_x so that the total secondary impedance Z_s on excitation frequency is below $Z_{s_{max}}$, where x is channel a or channel b.

$$\begin{aligned} L_x &= 40mH \\ R_x &= 150\Omega \end{aligned} \tag{2.17}$$

$$\begin{aligned} Z_x &= R_x + X_{L_x} \\ Z_x &= R_x + (2\pi f_{exc} L_x)j \\ Z_x &= 150 + (2\pi * 3000 * 40 * 10^{-3})j \\ Z_x &= 150 + 753.98j\Omega \\ Z_x &= 768.76\underline{/78.75^\circ} \\ Z_{a+b} &= 1537.52\underline{/78.75^\circ} \end{aligned} \tag{2.18}$$

5. Verify that coupling coefficients fall between 0 and 1;

$$\begin{aligned} M &= \sqrt{L_p L_x} \\ M &= \sqrt{80mH * 40mH} \\ M &= 56.57mH \end{aligned} \tag{2.19}$$

$$k_{ret} = \frac{M_{ret}}{M}$$
$$k_{ret} = 0.178 \tag{2.20}$$

$$k_{ext} = \frac{M_{ext}}{M}$$
$$k_{ext} = 0.535 \tag{2.21}$$

The final LVDT parameters are summarized on table 2.2.

TABLE 2.2 – LVDT parameters

Parameter	Value
Excitation voltage (V_{exc})	$7V_{RMS}$
Excitation frequency (f_{exc})	$3000Hz$
Primary self-inductance (L_p)	$80mH$
Primary resistance (R_p)	200Ω
Secondary A self-inductance (L_a)	$40mH$
Secondary A resistance (R_a)	150Ω
Secondary B self-inductance (L_b)	$40mH$
Secondary B resistance (R_b)	150Ω

Varying the coupling coefficients linearly with core position allows the output to behave according to figure 2.7. This model was tested using LTspice XVII, a SPICE simulator of electronic circuits produced by semiconductor manufacturer Linear Technology (LTC). LTspice provided a quick and easy way to evaluate the behaviour of the model before a more complex implementation was done on Simulink. A slightly different model (figure 2.8) was built without the voltage sources in series, since SPICE provides a directive to set the mutual inductance between inductors (LINEAR TECHNOLOGY, 2014). A value of $10M\Omega$ was used for R_{METER}, obtained from the input resistence of a typical multimeter (FLUKE CORPORATION, 2005). To validate the model against the datasheet, it was tested with LVDT fully extended and with LVDT at null position.

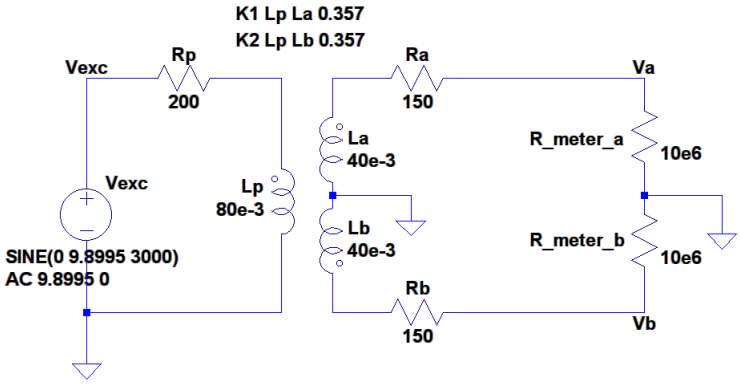

FIGURE 2.8 – SPICE LVDT model

TABLE 2.3 – Simulation parameters - LVDT fully extended

Parameter	Value
Coupling between primary and secondary A (k_a)	0.535
Coupling between primary and secondary B (k_b)	0.178
Resistive load (R_{METER_x})	$10M\Omega$
Stop time	$30ms$
Maximum timestep	$10^{-7}s$

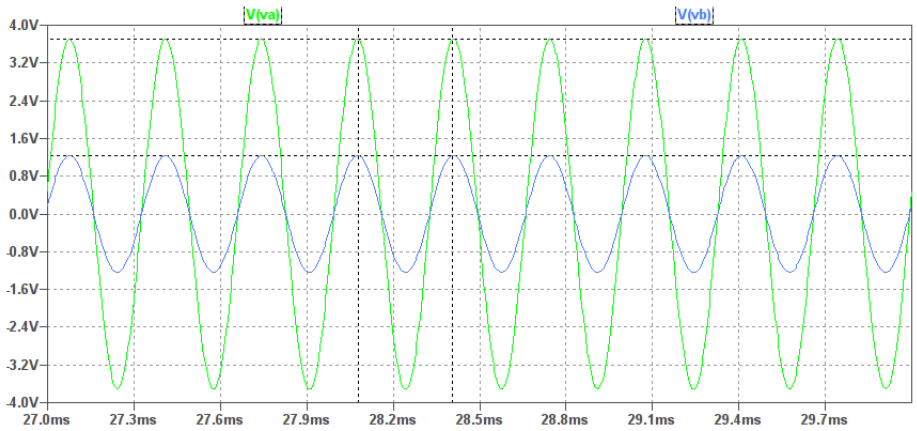

FIGURE 2.9 – LVDT waveform output (fully extended)

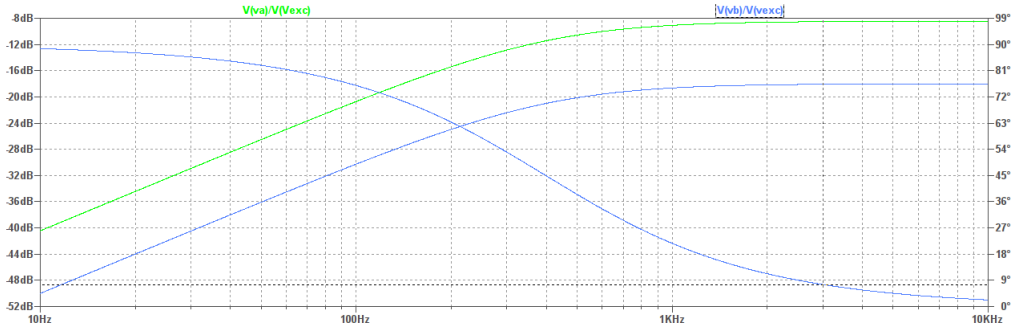

FIGURE 2.10 – LVDT magnitude-phase output (fully extended)

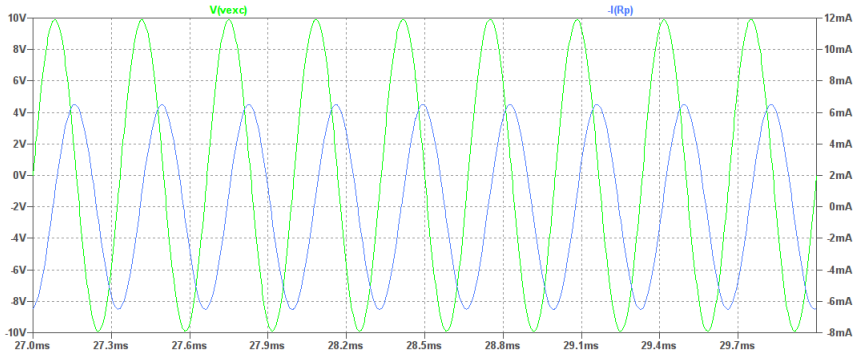

FIGURE 2.11 – LVDT primary current (fully extended)

Due to a SPICE convention, current on figure 2.11 is plotted with inverted signal.

TABLE 2.4 – Simulation results - LVDT fully extended

Parameter	Value	Expected value
Channel A voltage (V_a)	$2.625V_{RMS}$	$2.625V_{RMS}$
Channel A phase	$7.55°$	$< 15.00°$
Channel B voltage (V_b)	$0.873V_{RMS}$	$0.875V_{RMS}$
Channel B phase	$7.55°$	$< 15.00°$
Current on primary (i_p)	$4.601mA_{RMS}$	$< 7mA_{RMS}$

When LVDT is at null, both secondaries have the same coupling factor (equation 2.22) since the variation is linear.

$$\begin{aligned} k_{null} &= \frac{k_{min} + k_{max}}{2} \\ k_{null} &= \frac{0.178 + 0.535}{2} \\ k_{null} &= 0.357 \end{aligned} \tag{2.22}$$

TABLE 2.5 – Simulation parameters - LVDT at null

Parameter	Value
Coupling between primary and secondary A (k_a)	0.357
Coupling between primary and secondary B (k_b)	0.357
Resistive load (R_{METER_x})	$10M\Omega$
Stop time	$30ms$
Maximum timestep	$10^{-7}s$

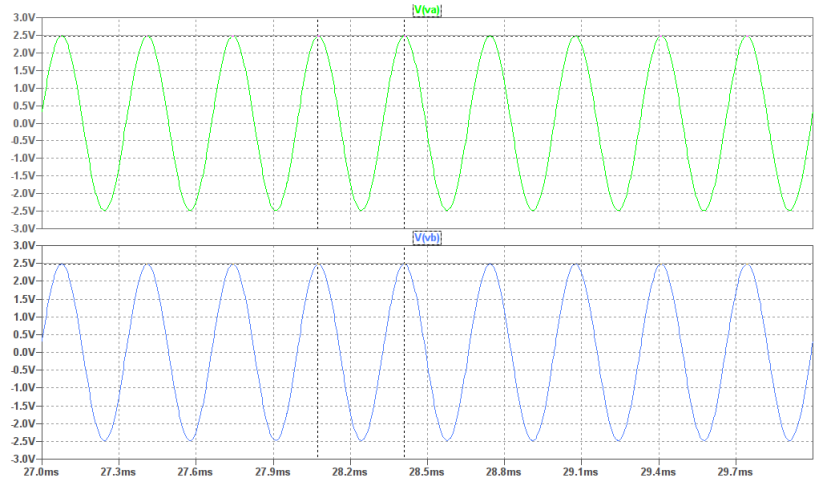

FIGURE 2.12 – LVDT waveform output (at null)

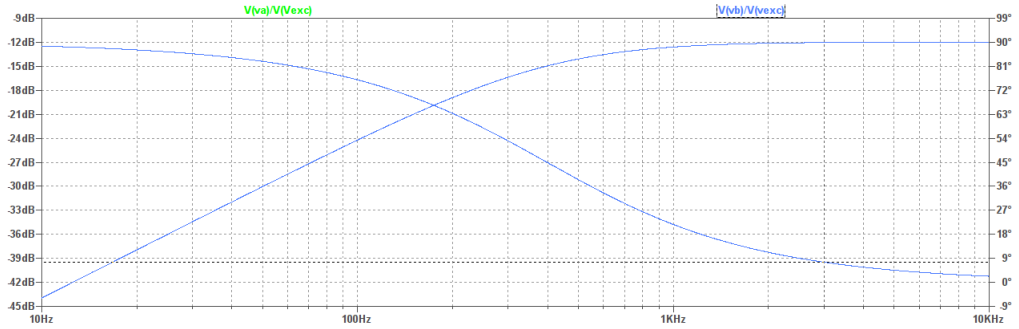

FIGURE 2.13 – LVDT magnitude-phase output (at null)

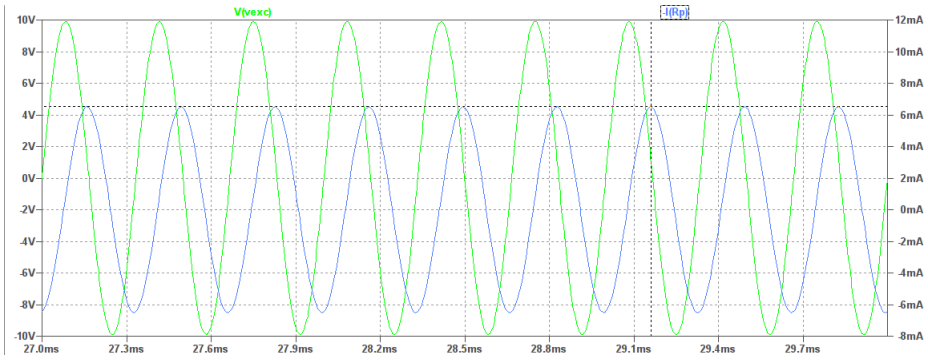

FIGURE 2.14 – LVDT primary current (at null)

Due to a SPICE convention, current on figure 2.14 is plotted with inverted signal.

TABLE 2.6 – Simulation results - LVDT at null

Parameter	Value	Expected value
Channel A voltage (V_a)	$1.752V_{RMS}$	$1.750V_{RMS}$
Channel A phase	7.55°	$< 15.00°$
Channel B voltage (V_b)	$1.752V_{RMS}$	$1.750V_{RMS}$
Channel B phase	7.55°	$< 15.00°$
Current on primary (i_p)	$4.601mA_{RMS}$	$< 7mA_{RMS}$

The electrical model behaved as expected and produced the correct values. On chapter 3 it will be reimplemented as a Simscape model to support time-variant mutual inductance coefficients, so it can be integrated with the rest of the models.

2.1.3 Analog demodulation

LVDTs are available with either four, five or six wires (figure 2.15). In the four wires model the secondaries are internally connected in series but wound in opposite directions, causing the signals on each secondary to be 180° out of phase. This configuration is called phase-sensitive, where the phase of the output signal determines direction and its magnitude, distance, and requires a synchronous demodulator in order to compare the excitation signal with the output signal and determine the correct position of the core. Interfacing with this type of LVDT is out of the scope of this work, but it is covered in detail in (DIAS, 2015).

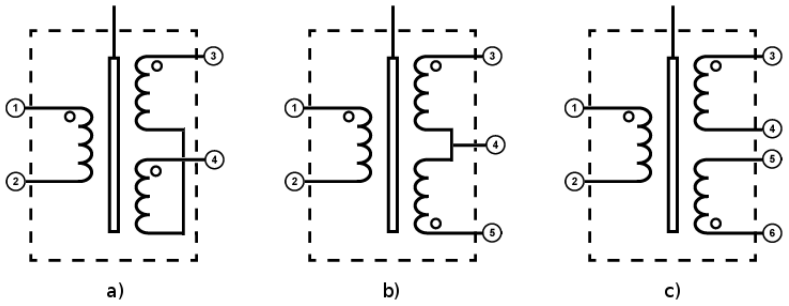

FIGURE 2.15 – Different wirings for commercially available LVDTs

The five and six wires models, in the other hand, allows one to known the magnitudes of each secondary individually. Assuming the sum of the voltages on the secondaries are practically constant over a given linear range of operation, it is possible to use 2.23 to determine the core position.

$$r = \frac{V_a - V_b}{V_a + V_b} \tag{2.23}$$

Consider that the LVDT operates only in the linear region and normalized core position varies from -1 (fully retracted) to $+1$ (fully extended). When fully extended, the voltage amplitude observed on secondary A is V_{max} and on secondary B is V_{min} and when fully retracted, the opposite. Since the amplitudes vary linearly with core position, it is possible to use the scale on figure 2.16.

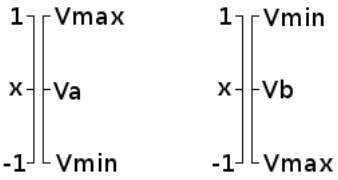

FIGURE 2.16 – Voltage variation according to core position

The voltages on each channel in function of core position x are given by:

$$\begin{aligned} \frac{V_{max} - V_a}{V_{max} - V_{min}} &= \frac{1 - x}{1 - (-1)} \\ 2V_{max} - 2V_a &= (V_{max} - V_{min}) - x(V_{max} - V_{min}) \\ V_a(x) &= \frac{(V_{max} - V_{min})x + (V_{max} + V_{min})}{2} \end{aligned} \tag{2.24}$$

$$\begin{aligned} \frac{V_b - V_{max}}{V_{max} - V_{min}} &= \frac{x - (-1)}{-1 - 1} \\ -2V_b + 2V_{max} &= (V_{max} - V_{min}) + x(V_{max} - V_{min}) \\ V_b(x) &= \frac{-(V_{max} - V_{min})x + (V_{max} + V_{min})}{2} \end{aligned} \tag{2.25}$$

This way, the sum of voltages V_a and V_b is constant in the linear region (equation 2.26).

$$\begin{aligned} V_a(x) + V_b(x) &= \frac{(V_{max} - V_{min})x + (V_{max} + V_{min})}{2} + \frac{-(V_{max} - V_{min})x + (V_{max} + V_{min})}{2} \\ V_a(x) + V_b(x) &= \frac{(V_{max} - V_{min})x}{2} - \frac{(V_{max} - V_{min})x}{2} + 2\frac{(V_{max} + V_{min})}{2} \\ V_a(x) + V_b(x) &= 2\frac{(V_{max} + V_{min})}{2} \\ V_a(x) + V_b(x) &= V_{max} + V_{min} \end{aligned} \tag{2.26}$$

The difference between V_a and V_b is given by:

$$\begin{aligned} V_a(x) - V_b(x) &= \frac{(V_{max} - V_{min})x + (V_{max} + V_{min})}{2} - \frac{-(V_{max} - V_{min})x + (V_{max} + V_{min})}{2} \\ V_a(x) - V_b(x) &= \frac{(V_{max} - V_{min})x}{2} + \frac{(V_{max} - V_{min})x}{2} \\ V_a(x) - V_b(x) &= (V_{max} - V_{min})x \end{aligned} \tag{2.27}$$

and the ratio r in function of x is given by:

$$\begin{aligned} r(x) &= \frac{V_{max} - V_{min}}{V_{max} + V_{min}}x \\ r(x) &= r_{max}x \end{aligned} \tag{2.28}$$

where r_{max} is the maximum absolute ratio. The ratio varies from $-r$ for fully retracted to $+r$ for fully extended (figure 2.17). This method has the advantage of being independent of primary excitation level, thus not affected by loading and temperature drift problems and common ratios are 0.3, 0.4 and 0.5 (PI RESEARCH, 1999).

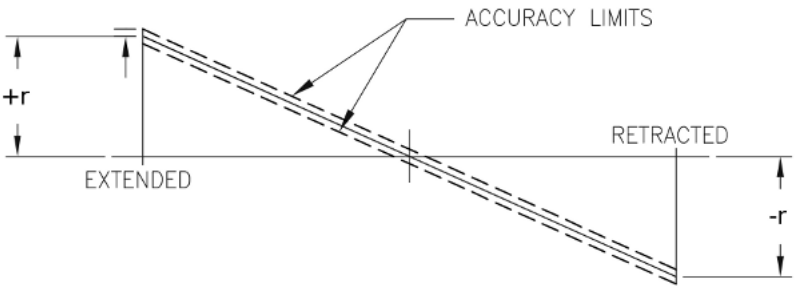

FIGURE 2.17 – Variation of the ratio r according to core position

To perform the ratiometric demodulation, an analog circuit, such as in figure 2.18, would first rectify both waves, then calculate the sum and difference of the signals and finally determine the ratio between the difference and the sum. This analog implementation would need a series of operational amplifiers to perform the functions depicted in figure 2.18, where each one would contribute in error stack up, heat dissipation and failure rate increase.

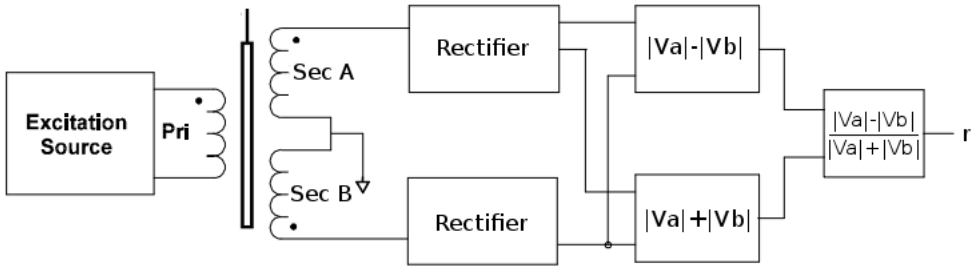

FIGURE 2.18 – Analog asynchronous LVDT demodulation

In order to reduce components and save board space, electronic manufacturers developed analog demodulators in monolithic integrated circuits such as the Analog Devices AD598 (ANALOG DEVICES, 2016) but they also require external passive components for filtering and correct matching the LVDT output. In Aerospace industry safety requirements drives levels of redundancy into the design, often requiring dissimilar implementation and independent control and monitor for safety critical functions (CRANE AEROSPACE & ELECTRONICS, 2015). In such scenario, both solutions could coexist providing different means for interfacing with the LVDT. Some of the advantages of the digital approach are reduced component count, saving space on circuit board and the ease to switch algorithms without redesigning the hardware in case the need arises.

2.2 Lightning susceptibility

Inside the aircraft, innumerous sensitive components are performing critical functions from navigation to engine control. These components have to keep working under environmental stress conditions such as lightning. Aircraft manufacturers refer to RTCA/DO-160 Section 22 (Lightning Induced Transient Susceptibility) as minimum requirements to design and test airborne equipment. This document presents standardized current waveforms considered to be adequate for the demonstration of compliance for the protection of an aircraft and its systems against the lightning environment.

Before the use of composite materials were common, most parts of the airframe were made of metal. If a lightning strike occurred, the current would travel outside the fuselage, exit the surface and continue to ground. The metallic airframe behaved as a Faraday cage reducing current coupling on the internal wiring of the aircraft and greatly reducing the risk of damage on sensitive components. Composite materials are largely employed nowadays (figure 2.19) and being poor current conductors, the increased impedance of the outer skin as a path for the lightning increases the possibility of higher voltages and currents coupling directly onto wiring and equipment (IN COMPLIANCE, 2010).

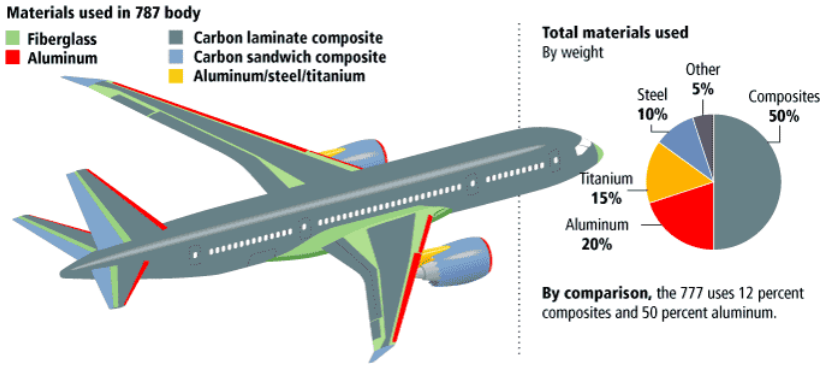

FIGURE 2.19 – A pictorial representation of the materials used to construct the Boeing 787 Dreamliner - Source: (MODERN AIRLINERS, 2015)

DO160 defines five test power levels varying from 1 (lowest) to 5 (highest), based on the installation characteristics for the equipment within the aircraft (table 2.7), and three main methods of injecting a discharge:

- **Pin Injection**, used to directly inject the waveform into component inputs;
- **Cable Bundle Induction**, uses a coupling transformer to inductively couple the waveform onto the cable bundle;
- **Ground Injection**, used to directly inject the waveform into the ground plane of the component.

TABLE 2.7 – DO160 Section 22 Test Power Levels

Level 1	Equipment and wiring are installed in a well protected environment
Level 2	Equipment and wiring are in a partially protected environment
Level 3	Equipment and wiring are in a moderate electromagnetic environment
Level 4 and 5	Equipment and wiring are in severe electromagnetic environments

A typical configuration is given by the controller installed in a well protected environment such as the electronic and equipment bay, and the sensor in a moderate to severe environment. The actuator is installed in a non-pressurized region and its sensor interfaces and cabling passes through non-metallic (composite) regions. For this configururation, a pin injection test comprised of waveforms 3 and 4 (figure 2.20) at power level 3 is indicated to verify the controller's susceptibility.

Operational amplifiers and analog-to-digital converters have limited operating voltage/current ranges, which can by several times smaller than the ones induced by lightning phenomena. For example, ADS8638 absolute maximum input is about $33V$ (TEXAS INSTRUMENTS, 2017) while waveform 3 at power level 3 presents a peak voltage of about

$600V$ (RADIO TECHNICAL COMMISSION FOR AERONAUTICS, 2010)). For this reason, a passive low pass filter (figure 2.21) was designed to atenuate the waveforms so the maximum output lies below $10V$. The varistor provides a very low resistance path to the ground when input voltage is above a determined level and the zener clamp on the output restrics the voltage to about $\pm V_z$ (zener breakdown voltage). The SPICE model for varistor and technical details were obtained from (VISHAY, 2017).

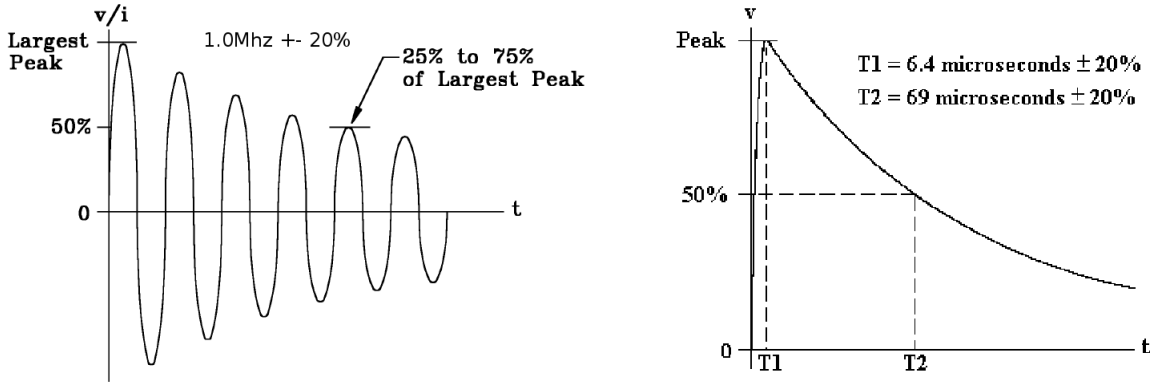

FIGURE 2.20 – Waveforms 3 and 4 - Source: (RADIO TECHNICAL COMMISSION FOR AERONAUTICS, 2010)

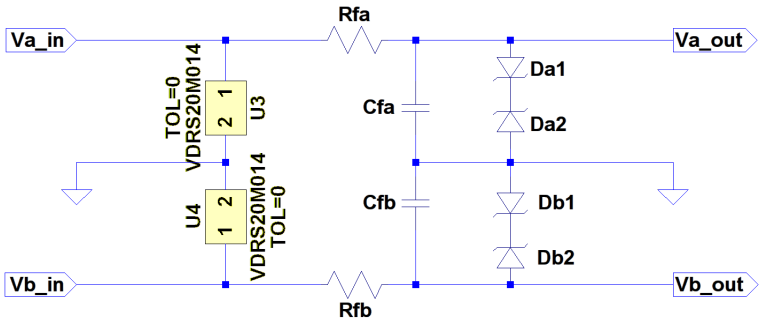

FIGURE 2.21 – Complete transient filter

The circuit on figure 2.22 was used to evaluate the filter response to waveform 3 (figure 2.23) and waveform 4 (figure 2.24).

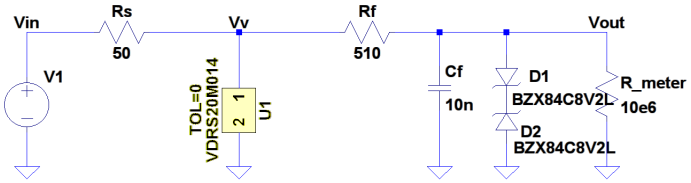

FIGURE 2.22 – Complete filter test circuit for one channel

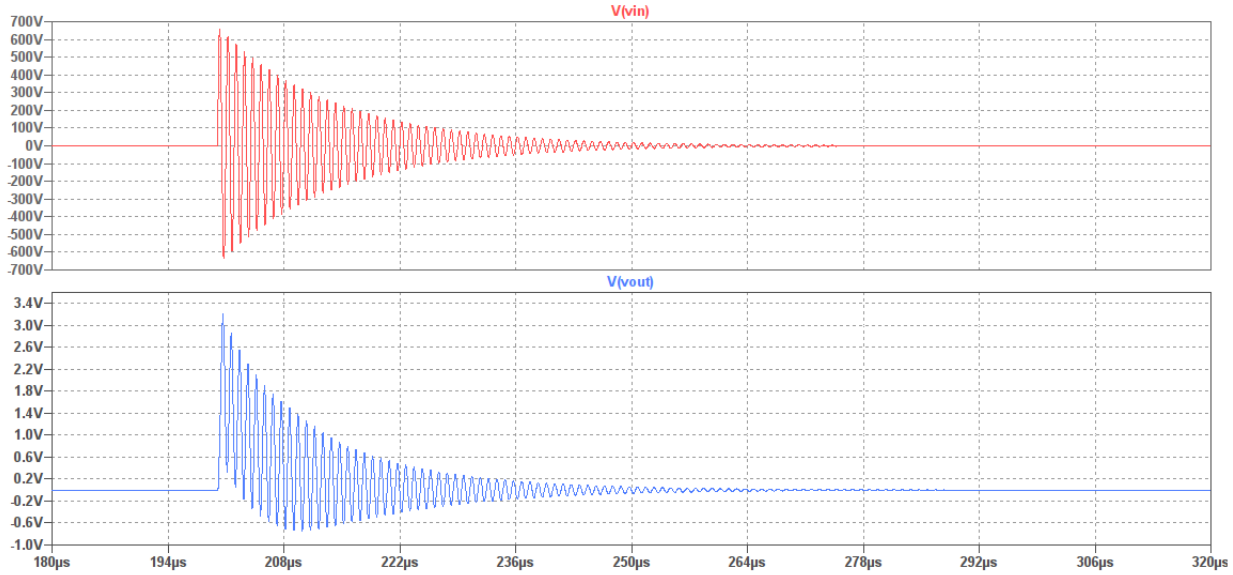

FIGURE 2.23 – Waveform 3 voltage input and filter output

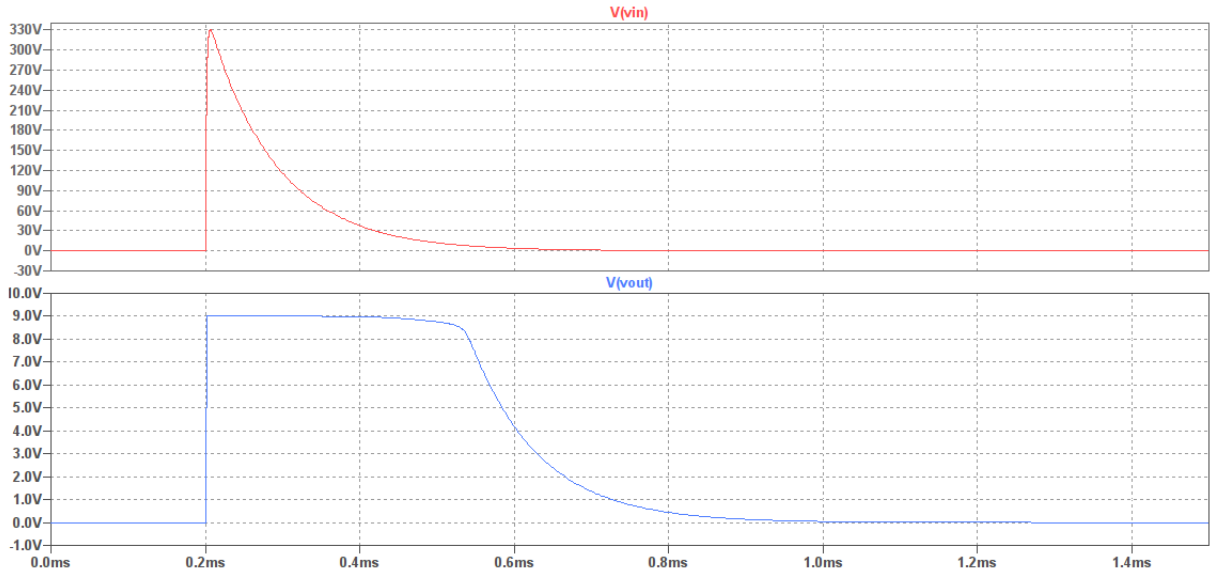

FIGURE 2.24 – Waveform 4 voltage input and filter output

Detecting and handling these transients in the controller is out of the scope of this work and to speed up the simulation the transient filter implemented on chapter 3 is simplified, comprised only by the RC filter part (figure 2.25). For this reason, the cut-off frequency of the RC filter was chosen so the magnitude and phase of the simplfied filter approximate the complete filter (figure 2.27) around $3kHz$. The filter parameters are summarized in tables 2.8 and 2.9. The final values for channel A on a fully extended LVDT are show on figure 2.26 and summarized on table 2.10.

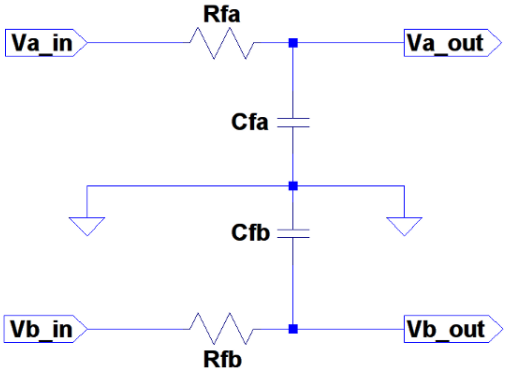

FIGURE 2.25 – Simplified transient filter

TABLE 2.8 – RC Low pass filter parameters - I

Parameter	Value
R_f	510Ω
C_f	$10nF$
Calculated cut-off frequency	$30000.00Hz$
Real cut-off frequency	$31206.85Hz$

TABLE 2.9 – RC Low pass filter parameters - II

Parameter	Unfiltered	Complete filter	Simplified filter
Magnitude @$3kHz$	$-8.519dB$	$-4.549dB$	$-7.717dB$
Phase @$3kHz$	$7.554°$	$-11.37°$	$-0.66°$

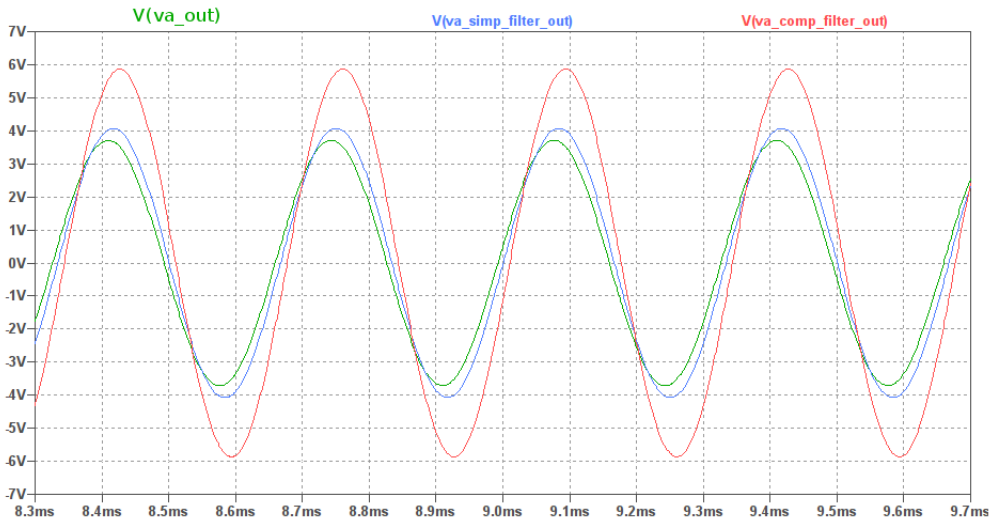

FIGURE 2.26 – Unfiltered LVDT (green); simplified filter (blue) and complete filter (red) response

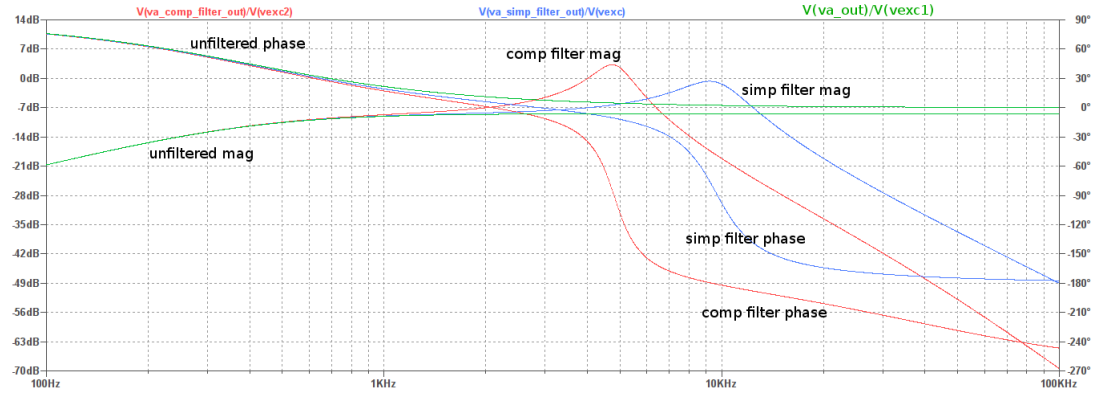

FIGURE 2.27 – Unfiltered LVDT (green); simplified filter (blue) and complete filter (red) response

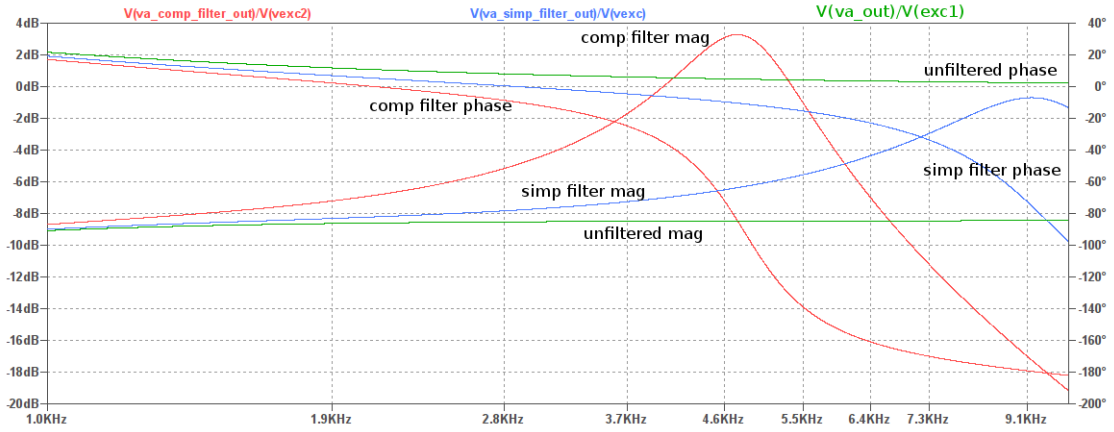

FIGURE 2.28 – Unfiltered LVDT (green); simplified filter (blue) and complete filter (red) response (zoomed in)

TABLE 2.10 – LVDT output (fully extended)

Parameter	Unfiltered output	Complete filter	Simple filter
Channel A voltage (V_a)	$2.625V_{RMS}$	$4.146V_{RMS}$	$2.879V_{RMS}$
Channel B voltage (V_b)	$0.873V_{RMS}$	$1.380V_{RMS}$	$0.958V_{RMS}$

2.3 Analog-to-Digital Conversion

Analog-to-Digital converters (ADCs) are mixed-signal devices used to convert a continuous signal from the physical world into a limited number of digital output codes, readable by a computer. Figure 2.29 shows an ideal ADC, comprised of a sample-and-hold (S/H) device, which takes a continuously varying analog signal and holds its value at a constant level for a specified period of time, and a quantizer, which effectively produces

the digital output code. The sample-and-hold device is triggered at sampling frequency f_s.

The digital output is an approximation of the analog input, and how close it is to the real value depends in part on the ADC resolution, defined by the number of bits n in the ADC. There are 2^n quantization levels on a $n-$bits ADC, and every time instant kT_s, where T_s is the sampling period (inverse of f_s, the sampling frequency) and k is a positive integer, the analog input $x(t)$ is quantized in time and amplitude to produce a output $X[k]$ (figure 2.30) in the range $[0, 2^n - 1]$.

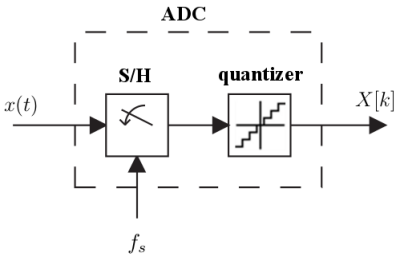

FIGURE 2.29 – An ideal ADC

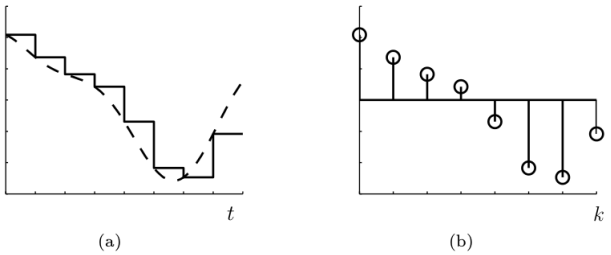

FIGURE 2.30 – The operation of an ideal S/H device (left). The value of the input signal x(t) (dashed) at the sampling instant is held until the next sampling instant, producing a piecewise constant output signal (solid). The output signal can be represented with a discrete-time signal X[k] (right) - Source: (LUNDIN, 2005) (modified)

Consider an ideal $3-$bits ADC whose input varies between $0V$ and $10V$. There are 8 possible output codes, from 0 to 7 (figure 2.31). However, since the first (zero) step and the last step are only one half of a full width, the full-scale range (FSR) is divided into $2^n - 1$ step widths, hence, 1 $LSB = 1.429V$. The quantization error in this case is specified to be no more than half of the least significant bit (LSB). For a $3-$bit ADC, the error is $\pm 0.714V$ or 7.14%

$$LSB = \frac{FSR}{2^n - 1} \tag{2.29}$$

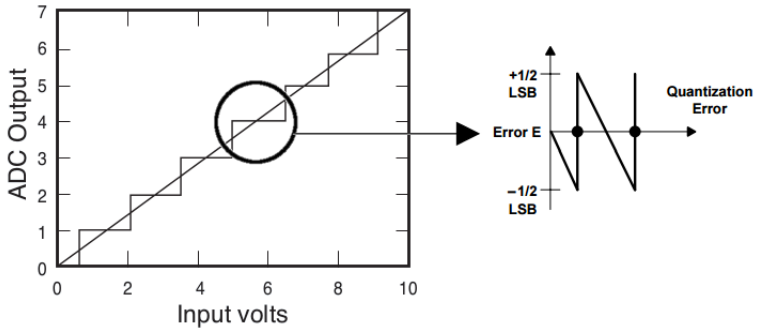

FIGURE 2.31 – Ideal ADC output and quantization error

2.3.1 Non-linearities of ADCs

Real ADCs, however, are non-linear non-ideal devices as a result of being comprised of non-linear circuits. These non-idealities impose constraints to the operation of ADCs in real-world systems. It is crucial to understand how they affect the response of a device and how to mitigate these effects. Although there are diverse architectures for commecially available ADCs each one with specific non-ideal behaviours, in general, the non-idealities can be divided in two main categories: static and dynamic. Static errors affect the accuracy when the ADC is converting static (DC) signals and be completely described by just four terms (TEXAS INSTRUMENTS, 1995):

1. **Offset error** - The difference between the nominal and actual offset points, i.e. the midstep value when the digital output is zero (figure 2.32a). This error affects all codes by the same amount and can be compensated by calibration;

2. **Gain error** - The difference between the nominal and actual gain points after the offset error has been corrected. The gain point is the midstep value when the digital output is full scale (figure 2.32b). This error represents a difference in the slope of the actual and ideal transfer functions and can be compensated by calibration;

3. **Differential non-linearity (DNL)** - The difference between an actual step width and the ideal value of 1 LSB (figure 2.33a). If the step width is exactly 1 LSB, then the DNL is zero. If the DNL exceeds 1 LSB, there is a possibility that there can be missing codes i.e. one or more of the possible 2^n binary codes are never output. DNL errors cannot be directly compensated by calibration (MAXIM INTEGRATED, 2002);

4. **Integral non-linearity (INL)** - The deviation of the values on the actual transfer function from a straight line, usually between the end points of the transfer function once the gain and offset errors have been corrected (figure 2.33b). The deviations are measured at the transitions from one step to the next. The name derives from

the fact that the summation of the differential nonlinearities from the bottom up to a particular step, determines the value of the integral nonlinearity at that step. INL errors cannot be directly compensated by calibration (MAXIM INTEGRATED, 2002);

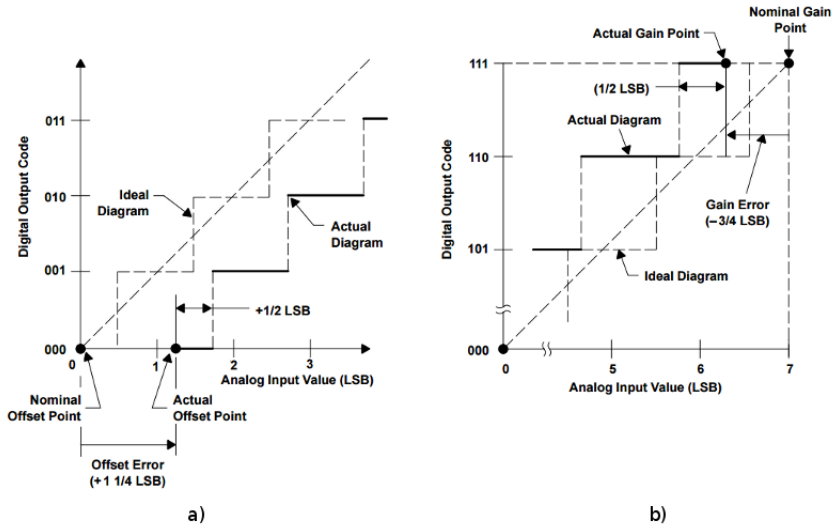

FIGURE 2.32 – a) Offset error and b) Gain error - Source: (TEXAS INSTRUMENTS, 1995) (modified)

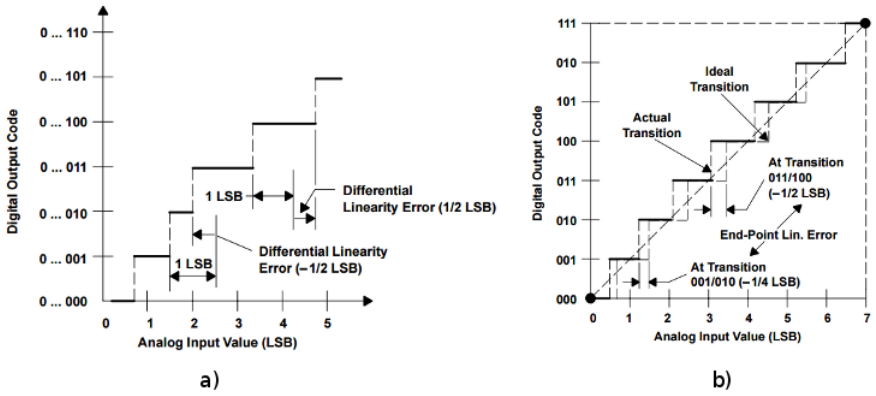

FIGURE 2.33 – a) DNL and b) INL - Source: (TEXAS INSTRUMENTS, 1995) (modified)

Dynamic non-linearities, in the other hand, affect the accuracy of the ADC when it is converting dynamic (AC) signals, and are expressed by:

1. **Signal-to-Noise ratio (SNR)** - The ratio of the output signal amplitude to the output noise level, not including harmonics or DC components. A signal level of $1V_{RMS}$ and a noise level of $100\mu V_{RMS}$ yields an SNR of 10^4 or $80dB$ (figure 2.34). SNR usually degrades as frequency increases because the accuracy of the comparators within the ADC degrades at higher input slew rates. The theoretical maximum

signal-to-noise ratio for an ADC with a full-scale sine-wave input derives from quantization noise and is about $6.02n+1.76dB$, where n is the number of bits (NATIONAL SEMICONDUCTORS, 2003).

2. **Total harmonic distortion (THD)** - The ratio of the RMS total of a given number harmonic components to the RMS value of the output signal (equation 2.30). V_{f1} is the fundamental amplitude while V_{fk} is the $k-$th harmonic amplitude. This parameter gives an indication of a circuit's linearity in terms of its effect on the harmonic content of a signal (figure 2.35).

$$THD = \sqrt{\frac{V_{f2}^2 + V_{f3}^2 + \cdots + V_{fn}^2}{V_{f1}}} \tag{2.30}$$

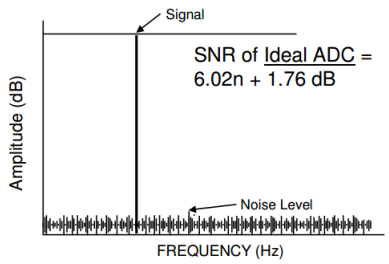

FIGURE 2.34 – Spectral content of an input signal - Source: (NATIONAL SEMICONDUCTORS, 2003) (modified)

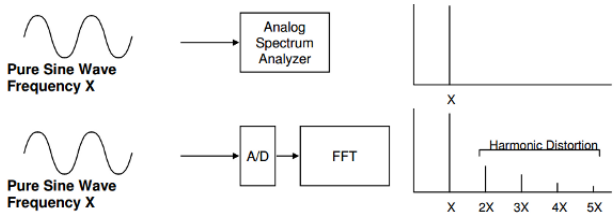

FIGURE 2.35 – Harmonics on a sampled signal - Source: (NATIONAL SEMICONDUCTORS, 2003) (modified)

3. **Signal-to-Noise-and-Distortion ratio (SINAD)** - The combination of the SNR and the THD specifications, defined as the RMS value of the output signal to the RMS value of all of the other spectral components below half sampling frequency, including harmonics but excluding DC components. Because it compares all undesired frequency components with the input frequency, it is an overall measure of ADC dynamic performance. Current ADCs performance in respect to THD is very good, practically unchanged by input level, causing SINAD to be dominated by SNR (NATIONAL SEMICONDUCTORS, 2003).

4. **Effective number of bits (ENOB)** - The alternate form for SINAD, meaning the ADC performance as if it were a theoretically perfect converter with a resolution of ENOB (e.g. an ENOB of 10.5 bits means that ADC performs, as far as SINAD is concerned, as if it were an ideal 10.5−bit ADC). Expression for ENOB is given by equation 2.31.

$$ENOB = \frac{SINAD - 1.76}{6.02} \tag{2.31}$$

5. **Spurious-free dynamic range (SFDR)** - The difference between the value of the desired output signal and the value of the highest amplitude output frequency that is not present in the input (figure 2.36).

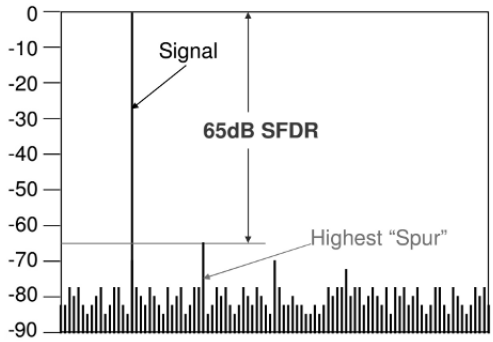

FIGURE 2.36 – Spurious free dynamic range - Source: (NATIONAL SEMICONDUCTORS, 2003) (modified)

2.3.2 Types of Analog-to-Digital Converters

This section gives a brief description of three common ADC architecures: the flash (pipelined), the successive approximation (SAR) and the sigma-delta ($\Sigma - \Delta$) converters. Most ADC applications can be classified into four broad market segments:

(a) Data acquisition;

(b) Precision industrial measurement;

(c) Voiceband and audio;

(d) "High speed" (sampling rates above about $5MSPS$).

In figure 2.37, the x-axis represents the typical sampling rate in a given application and the y-axis the typical resolution. It is possible to see a clear trade-off between speed and resolution and how each architecture relates to a market segment.

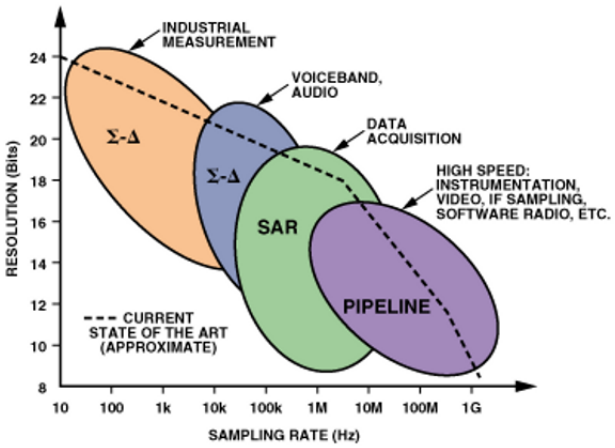

FIGURE 2.37 – ADC architectures, applications, resolution, and sampling rates - Source: (KESTER, 2005)

The Flash converter gets its name from the fact that it performs the conversion in one clock cycle. An ADC with b bits of resolution uses $2^b - 1$ comparators, a resistence ladder and an encoder (figure 2.38). The extremities of the resistence ladder define the range in which the ADC operates and the transition levels. The input voltage is compared simultaneously with all possible levels producing an output that is "thermometer-encoded" (i.e. encoded in unary) and finally, the encoder maps the output of the comparators to a $b-$bit word.

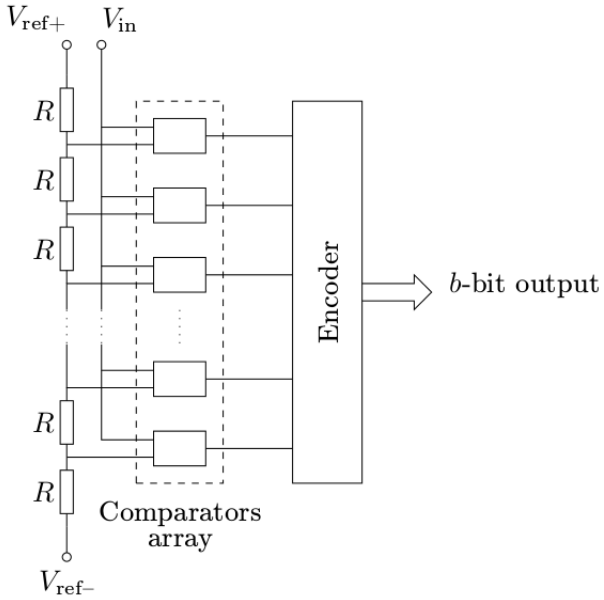

FIGURE 2.38 – Flash ADC architecture - Source: (LUNDIN, 2005)

These converters can operate in very high rates with low resolution (e.g. Analog Devices HMCAD5831, a $3 - bit$, 26 $GSPS$ flash converter (ANALOG DEVICES, 2017b)). The major drawback is that the number of comparators grows exponentially with the

number of desired bits, increasing chip area and power consumption. To increase the resolution, it is possible to use multiple low resolution converters in a pipeline (figure 2.39). Each stage produces a digital value which is fed to a digital-to-analog converter and a residue is computed. This residue is amplified and drives the next stage. The conversion time is longer than for a fully parallel flash but high sample rates are still possible (e.g. the Analog Devices AD9625, a $12-bit$, 2.6 $GSPS$ pipelined flash converter (ANALOG DEVICES, 2017a)). Correction logic is often used due to the recursive structure of a pipelined converter, which may cause repetitive error patterns and shifted regions on the transfer function (LUNDIN, 2005).

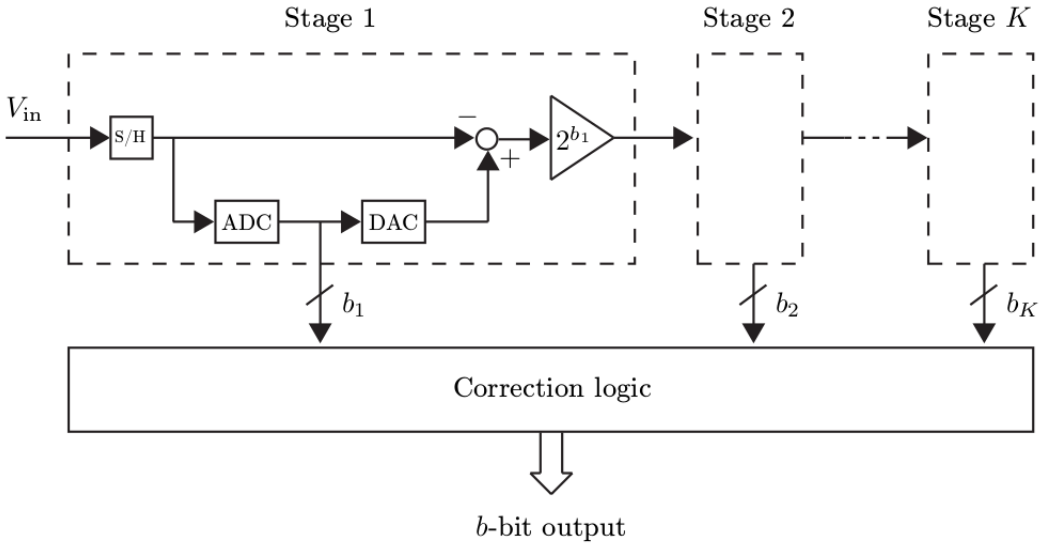

FIGURE 2.39 – Pipelined Flash ADC architecture - Source: (LUNDIN, 2005)

The Successive Approximation Register (SAR) ADC is one of the most popular architecture for data-acquisition applications in the industry (KESTER, 2005). The basic architecture is shown on figure 2.40. When conversion starts, the input is connected to a sample and hold device. A digital-to-analog converter with b bits is initialized with the mid value (only most significant bit set) and on every clock cycle the output is compared to the input voltage: if the DAC voltage is greater than the input the current bit is reset, else, the current bit is kept (figure 2.41). This process is repeated until the least significant bit is tested, taking b clock cycles to complete the conversion.

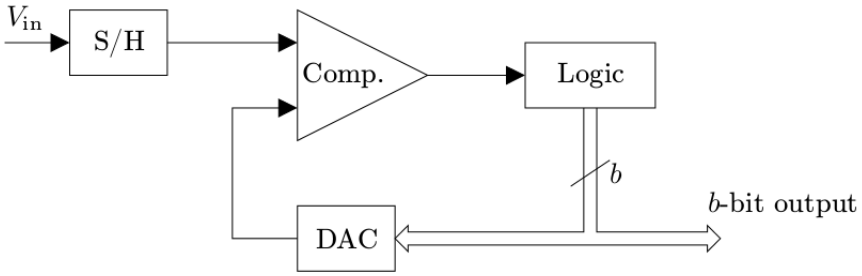

FIGURE 2.40 – SAR ADC architecture - Source: (LUNDIN, 2005)

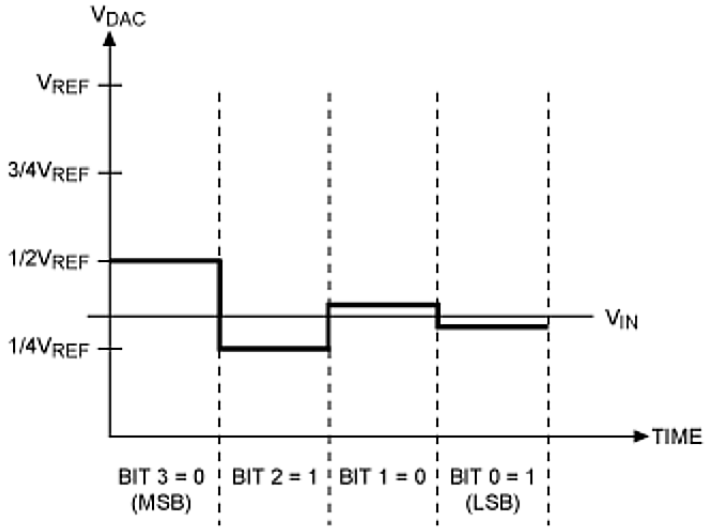

FIGURE 2.41 – SAR ADC architecture - Source: (MAXIM INTEGRATED, 2001)

The Sigma-Delta converter consist of an oversampling modulator followed by a digital/decimation filter that together produce a high-resolution data-stream output (figure 2.42). The modulator is responsible for digitizing the analog input signal and pushes noise at lower frequencies up to higher frequencies (noise shaping). This way, this type of converter is well-suited for low-frequency, high-accuracy measurements (TEXAS INSTRUMENTS, 2011).

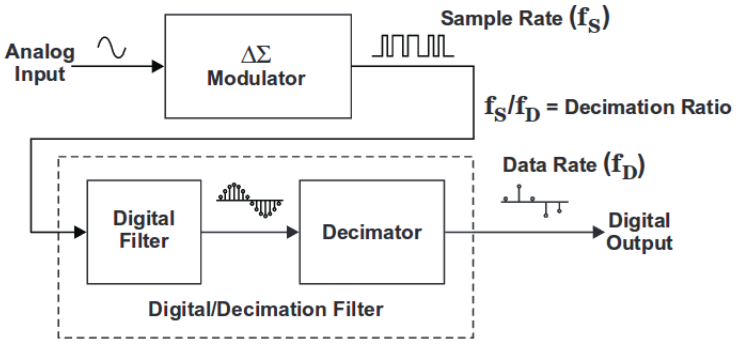

FIGURE 2.42 – Sigma-Delta ADC architecture - Source: (TEXAS INSTRUMENTS, 2011)

2.3.3 Multiplexing

An ideal data acquisition system uses a single ADC for each measurement channel, capturing all data in parallel. This approach has some problems such as increasing the number of components on the board (thus, increasing heat dissipation, cost, weight and reducing board space) and underutilizing the ADC to capture limited bandwidth signals. Using a multiplexer, however, it's possible to switch among the inputs of multiple channels that drive a single ADC (figure 2.43), substantially reducing the cost of a system. This approach is used in so-called sampled-data systems and a multiplexer was integrated in the ADC model develped in this work.

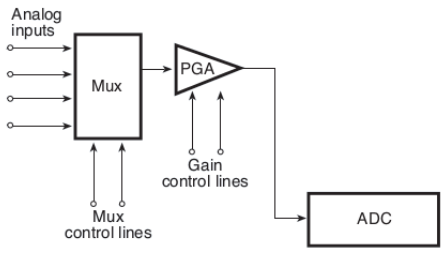

FIGURE 2.43 – The multiplexer switches between multiple input channels to feed a single ADC - Source: (MEASUREMENTE COMPUTING, 2004) (modified)

A multiplexer is an array of solid-state switches with non-idealities of its own, some of them described below:

1. **ON Resistance** - A quality analog switch can have an ON resistance of 10Ω to 100Ω, and an analog multiplexer can be 100Ω to 2500Ω per channel (MEASUREMENTE COMPUTING, 2004). The ON resistance adds directly to the signal source impedance and can affect the system's measurement accuracy if not compensated, for example, increasing settling time.

2. **Charge injection** - Is a level change caused by stray capacitance associated with the NMOS and PMOS transistors that make up the analog switch, manifesting as a spike in the output. This glitch produces measurement errors and altough a compensating circuit can minimize its effects, keeping the source impedance as low as possible is the most effective way to prevent this phenomena.

3. **Channel-to-channel cross talk** - Is when the voltage applied to any one channel affects the accuracy of the reading in another channel, usually caused when one signal has magnitude and frequency relatively high to another. High frequency multiplexing also increases cross talk effects.

3 Model Construction

This chapter presents the implementation of the building blocks of signal acquisition system using the Simulink environment.

3.1 Linear Variable Differential Transformer

This section presents the implementation of an 6-wire LVDT linear model using Simscape, a library to model physical systems within the Simulink environment. The custom behavioral model is described by a system of differential algebraic equations (DAEs) and was built using Simscape language (MATHWORKS, 2016). The Simscape language extends the modeling environment by using constructs specific to physical modeling such as unit handling, definition of physical domains (e.g. electrical, mechanical, among others) and a solver more capable of solving DAEs better than the Simulink algebraic loop solver (POPINCHALK, 2009).

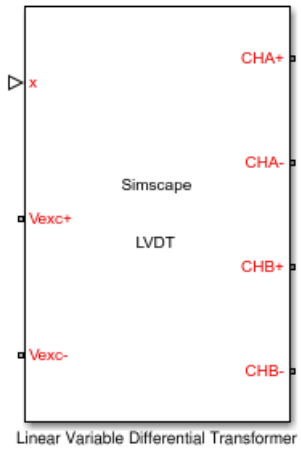

FIGURE 3.1 – Custom 6-wire LVDT on Simscape

The model takes as input the normalized position x, varying from -1 for fully retracted to $+1$ to fully extended. The values for self-inductances and resistances for each coil and

the minimum and maximum coupling coefficients are passed as parameters to the model (figure 3.2).

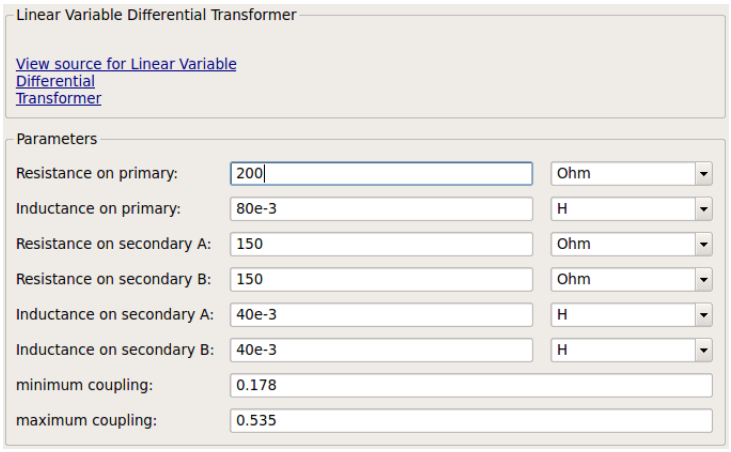

FIGURE 3.2 – LVDT parameters

Despite the usefulness of the SPICE model for static analysis, the coupling coefficients between the primary and each secondary cannot be varied while simulation is running and must be defined *a priori*. The equations presented in Section 2.1.2 must be modified to account for time-varying coupling between coils.

Consider two coils in the configuration shown in figure 3.3. Both coils have length L and radius R. Coil 1 has N_1 windings and coil 2 has N_2.

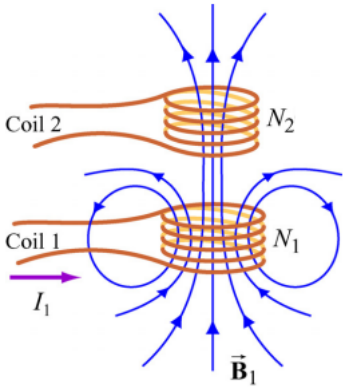

FIGURE 3.3 – Coupled coils - Source (KNUTESON *et al.*, 2005)

When a current I_1 circulates through coil 1 a magnetic flux Φ_1 passes through coil 1, given by:

$$\Phi_1 = \mu_0 \frac{N_1 I_1}{L} \pi R^2 \tag{3.1}$$

where μ_0 is the permeability of free space. Since the two coils are close to each other, *some* of the magnetic field lines through coil 1 will also pass through coil 2. The magnetic

flux through one turn of coil 2 due to I_1 is given by:

$$\begin{aligned} \Phi_{21} &= k(t)\Phi_1 \\ \Phi_{21} &= k(t)\mu_0 \frac{N_1 I_1}{L}\pi R^2 \end{aligned} \tag{3.2}$$

where $k(t)$ is the *coupling coefficient*, as explained on Section 2.1.2, but as a function of time.

By varying I_1 with time, by Faraday's Law, there will be an induced EMF V associated with the changing magnetic flux Φ_{21} in coil 2:

$$V = N_2 \frac{d\Phi_{21}}{dt} \tag{3.3}$$

Differentiating equation 3.2 gives:

$$\frac{d\Phi_{21}}{dt} = \frac{dk(t)}{dt}\mu_0 \frac{N_1}{L}\pi R^2 I_1 + k(t)\mu_0 \frac{N_1}{L}\pi R^2 \frac{dI_1}{dt} \tag{3.4}$$

If the coupling coefficient is constant ($\frac{dk(t)}{dt} = 0$), equation 3.4 reduces to:

$$\frac{d\Phi_{21}}{dt} = k\mu_0 \frac{N_1}{L}\pi R^2 \frac{dI_1}{dt} \tag{3.5}$$

and the the proportionality constant between V and $\frac{dI_1}{dt}$ is called the mutual inductance M (KNUTESON *et al.*, 2005). Replacing equation 3.5 in 3.3 gives:

$$\begin{aligned} V &= N_2 \frac{d\Phi_{21}}{dt} \\ V &= N_2 \left(k\mu_0 \frac{N_1}{L}\frac{dI_1}{dt}\pi R^2 \right) \\ V &= kN_1N_2 \frac{\mu_0 \pi R^2}{L}\frac{dI_1}{dt} \end{aligned} \tag{3.6}$$

Thus,

$$M = k\mu_0 \frac{N_1 N_2}{L}\pi R^2 \tag{3.7}$$

But for an LVDT, the coupling coefficient indeed varies with time, so:

$$\begin{aligned} V &= N_2 \frac{d\Phi_{21}}{dt} \\ V &= N_2 \left(\frac{dk(t)}{dt} \mu_0 \frac{N_1}{L} \pi R^2 I_1 + k(t) \mu_0 \frac{N_1}{L} \pi R^2 \frac{dI_1}{dt} \right) \\ V &= \frac{dk(t)}{dt} \mu_0 \frac{N_1 N_2}{L} \pi R^2 I_1 + k(t) \mu_0 \frac{N_1 N_2}{L} \pi R^2 \frac{dI_1}{dt} \end{aligned} \tag{3.8}$$

Since,

$$M(t) = k(t) \mu_0 \frac{N_1 N_2}{L} \pi R^2 \tag{3.9}$$

then

$$\frac{dM(t)}{dt} = \frac{dk(t)}{dt} \mu_0 \frac{N_1 N_2}{L} \pi R^2 \tag{3.10}$$

Using equations 3.9 and 3.10 to simplify equation 3.8:

$$V = \frac{dM(t)}{dt} I_1 + M(t) \frac{dI_1}{dt} \tag{3.11}$$

The self-inductances of coil 1 and coil 2 are given by:

$$L_1 = \mu_0 \frac{N_1^2 \pi R^2}{L} \tag{3.12}$$

$$L_2 = \mu_0 \frac{N_2^2 \pi R^2}{L} \tag{3.13}$$

Equations 3.12 and 3.13 can be rewritten as:

$$N_1 = \sqrt{\frac{L L_1}{\mu_0 \pi R^2}} \tag{3.14}$$

$$N_2 = \sqrt{\frac{L L_2}{\mu_0 \pi R^2}} \tag{3.15}$$

Replacing equations 3.14 and 3.15 in 3.7 gives the following expression for the mutual

inductance M:

$$\begin{aligned} M &= k\sqrt{\frac{LL_1}{\mu_0\pi R^2}}\sqrt{\frac{LL_2}{\mu_0\pi R^2}}\frac{\mu_0\pi R^2}{L} \\ M &= k\sqrt{L_1L_2}\frac{L}{\mu_0\pi R^2}\frac{\mu_0\pi R^2}{L} \\ M &= k\sqrt{L_1L_2} \end{aligned} \tag{3.16}$$

In Section 2.1.2, the minimum (K_{min}) and maximum (K_{max}) coupling coefficients were empirically obtained from the SPICE simulation. When the LVDT is totally retracted, the coupling coefficient for channel a (k_a) is K_{min} and for channel b (k_b) is K_{max} and when totally extended, the opposite. To obtain the coupling coefficients for each channel in function of core position x, the following scale can be used:

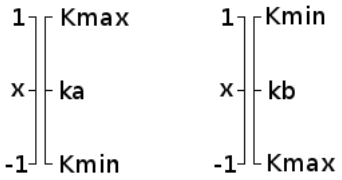

FIGURE 3.4 – Coupling coefficient variation according to core position

$$\begin{aligned} \frac{K_{max}-k_a}{K_{max}-K_{min}} &= \frac{1-x}{1-(-1)} \\ 2K_{max}-2k_a &= (K_{max}-K_{min})-x(K_{max}-K_{min}) \\ k_a(x) &= \frac{K_{max}-K_{min}}{2}x+\frac{K_{max}+K_{min}}{2} \end{aligned} \tag{3.17}$$

$$\begin{aligned} \frac{k_b-K_{max}}{K_{max}-K_{min}} &= \frac{x-(-1)}{-1-1} \\ -2k_b+2K_{max} &= (K_{max}-K_{min})+x(K_{max}-K_{min}) \\ k_b(x) &= \frac{-(K_{max}-K_{min})}{2}x+\frac{K_{max}+K_{min}}{2} \end{aligned} \tag{3.18}$$

Since the core position varies with time:

$$\begin{aligned} k_a(t) &= \frac{K_{max} - K_{min}}{2} x(t) + \frac{K_{max} + K_{min}}{2} \\ k_b(t) &= \frac{-(K_{max} - K_{min})}{2} x(t) + \frac{K_{max} + K_{min}}{2} \end{aligned} \tag{3.19}$$

Using equations 3.16 and 3.19, the mutual inductances for each secondary to primary are given by:

$$\begin{aligned} M_{ap}(t) &= k_a(t)\sqrt{L_p L_a} \\ M_{bp}(t) &= k_b(t)\sqrt{L_p L_b} \end{aligned} \tag{3.20}$$

Differentiating equations 3.20 gives:

$$\begin{aligned} \frac{dM_{ap}(t)}{dt} &= \frac{K_{max} - K_{min}}{2}\sqrt{L_p L_a}\frac{dx(t)}{dt} \\ \frac{dM_{bp}(t)}{dt} &= \frac{-(K_{max} - K_{min})}{2}\sqrt{L_p L_b}\frac{dx(t)}{dt} \end{aligned} \tag{3.21}$$

Equations 3.11, 3.20 and 3.21 will be used in the following procedure to build the Simscape model.

A Simscape language equation consists of two expressions connected with the == operator (MATHWORKS, 2016). Unlike the regular assignment operator (=), the == operator specifies continuous mathematical equality between the two expressions. In this way, the model implements the circuit on figure 3.5 and the converted expressions are shown below.

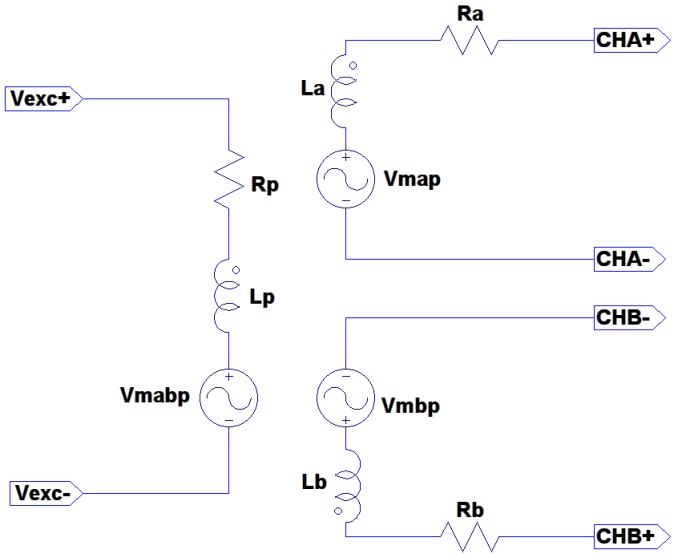

FIGURE 3.5 – LVDT internal circuit

For the primary, equation 3.22 for fixed coupling coefficients turns into Simscape expression 3.23, where vp is the voltage across terminals $Vexc+$ and $Vexc-$.

$$V_{exc} = R_p i_p + L_p \frac{di_p}{dt} + M_{ap} \frac{di_a}{dt} + M_{bp} \frac{di_b}{dt} \tag{3.22}$$

$$vp == R_p i_p + L_p \frac{di_p}{dt} + \left(M_{ap} \frac{di_a}{dt} + i_a \frac{dM_{ap}}{dt} \right) + \left(M_{bp} \frac{di_b}{dt} + i_b \frac{dM_{bp}}{dt} \right) \tag{3.23}$$

For the secondaries, va is the voltage across terminals $CHA+$ and $CHA-$ and vb is the voltage across terminals $CHB+$ and $CHB-$ (expression 3.24).

$$\begin{aligned} va &== R_a i_a + L_a \frac{di_a}{dt} + \left(M_{ap} \frac{di_p}{dt} + i_p \frac{dM_{ap}}{dt} \right) \\ vb &== R_b i_b + L_b \frac{di_b}{dt} + \left(M_{bp} \frac{di_p}{dt} + i_p \frac{dM_{bp}}{dt} \right) \end{aligned} \tag{3.24}$$

A simple test model that was built to verify the implementation is shown in figure 3.6 and the results are shown in figures 3.7 and 3.8.

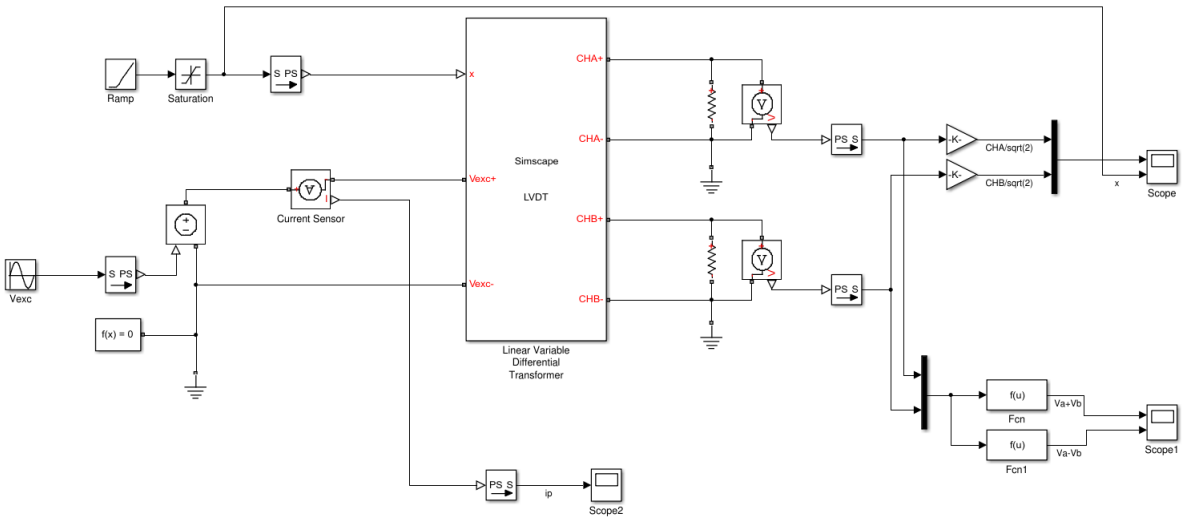

FIGURE 3.6 – LVDT test model

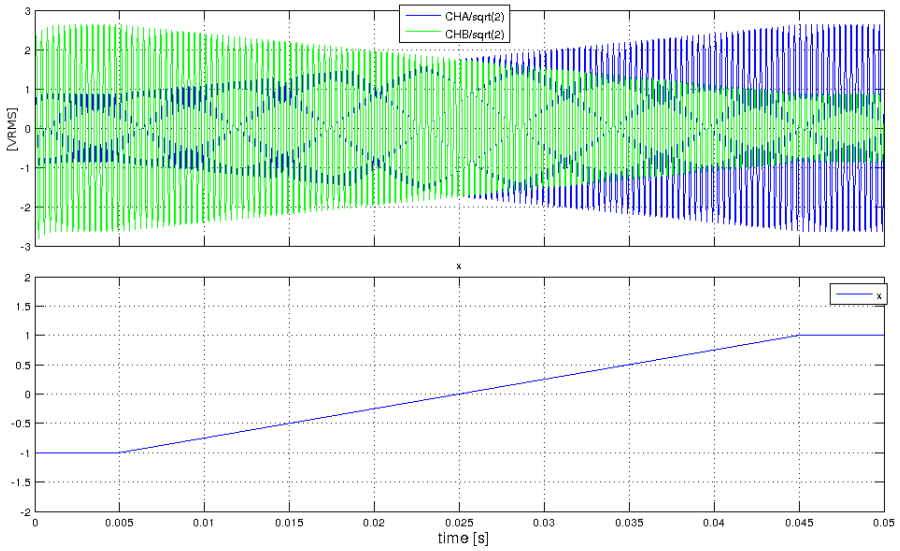

FIGURE 3.7 – Channels output and position

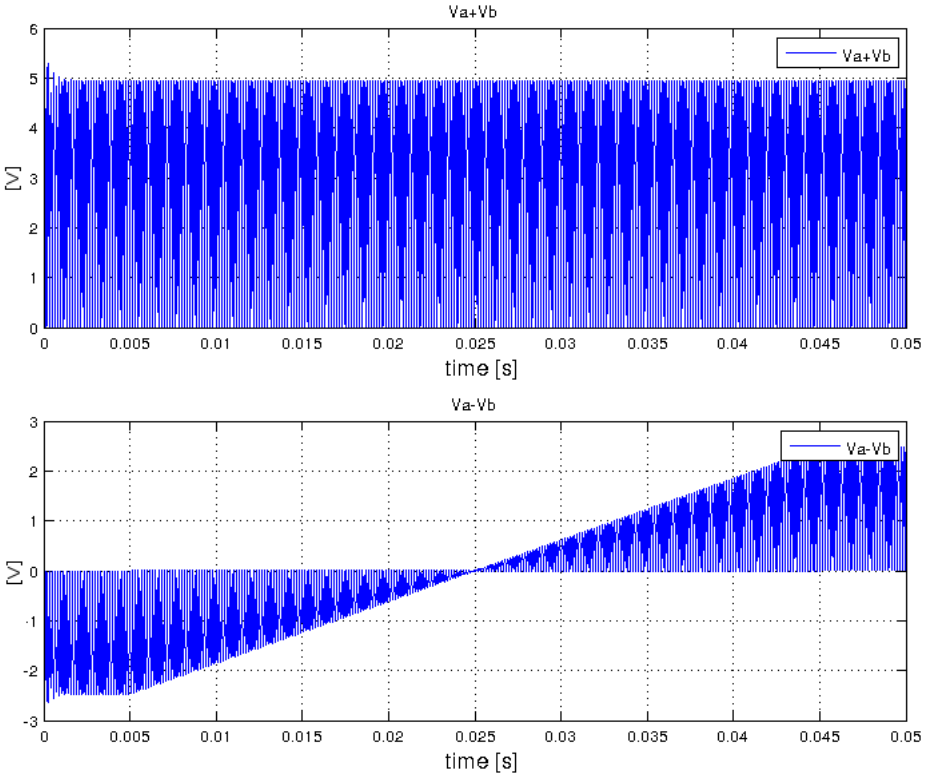

FIGURE 3.8 – Sum and difference of channels A and B

3.2 Signal Conditioner

The signal conditioner is responsible for matching the voltage range of the filter output to the ADC input. With this block it is possible do adjust a voltage offset and apply a voltage gain. In addition, the operational amplifier serves as a high impedance load for the filter and a low impedance source for the ADC. This section details the modeling of such circuit on Simulink environment.

3.2.1 Input Filter

The filter designed on Section 2.2 was then implemented on Simulink environment using Simscape default blocks (figure 3.9).

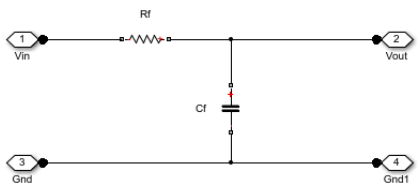

FIGURE 3.9 – Transient Filter A/B (Simscape model)

The output of the filter with an LVDT connected on the input (figure 3.10) is shown on figure 3.11.

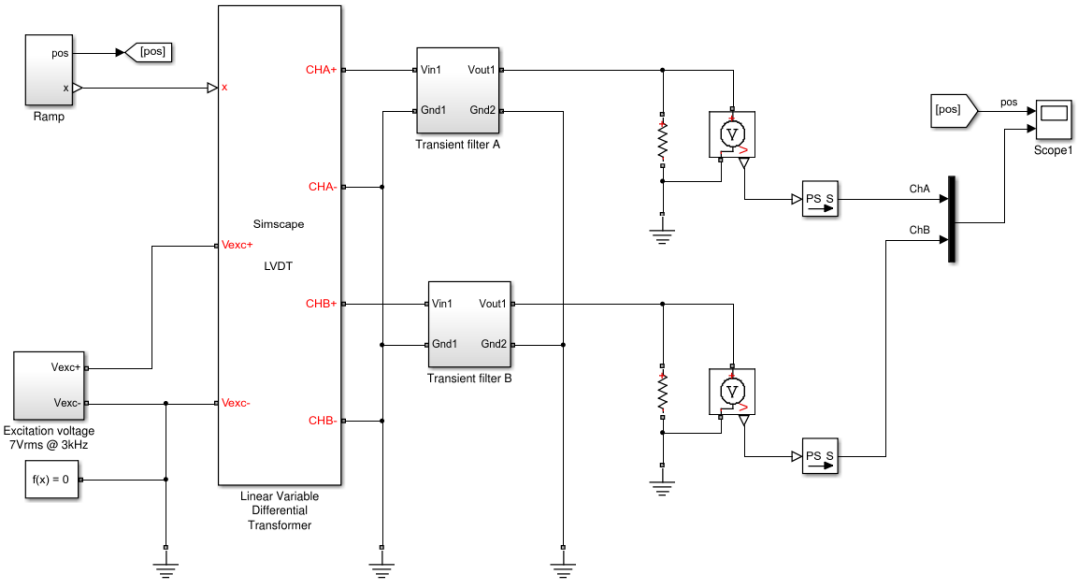

FIGURE 3.10 – LVDT and filter test model

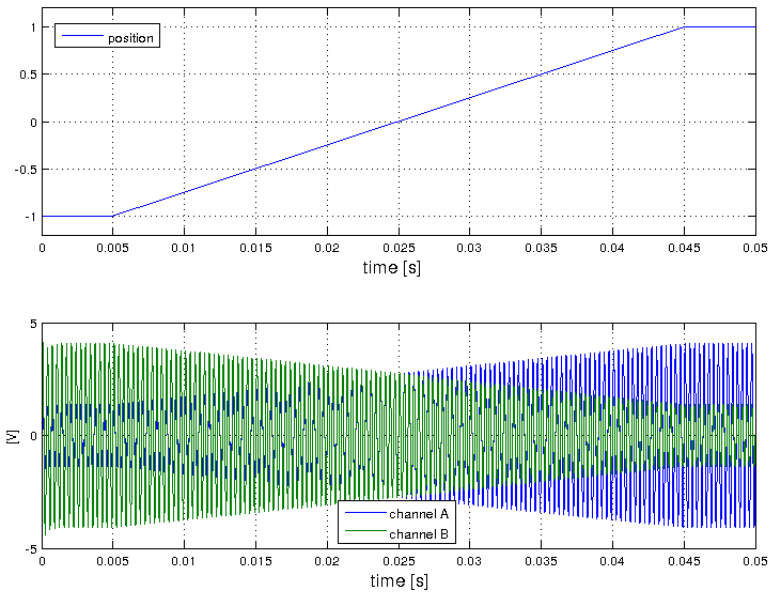

FIGURE 3.11 – LVDT and filter test model output

3.2.2 Range Conversion

After the signals from both channels are properly filtered and band-limited, it is necessary to convert the range of the signal excursion to match the input of the analog-to-digital

converter. This step also makes possible to balance the attenuation caused by the previous filtering stage. (TEXAS INSTRUMENTS, 2002) provides guiding to design a circuit (figure 3.12) capable of adding gain and DC offset to a signal, based on the desired input and output ranges, described on the steps below.

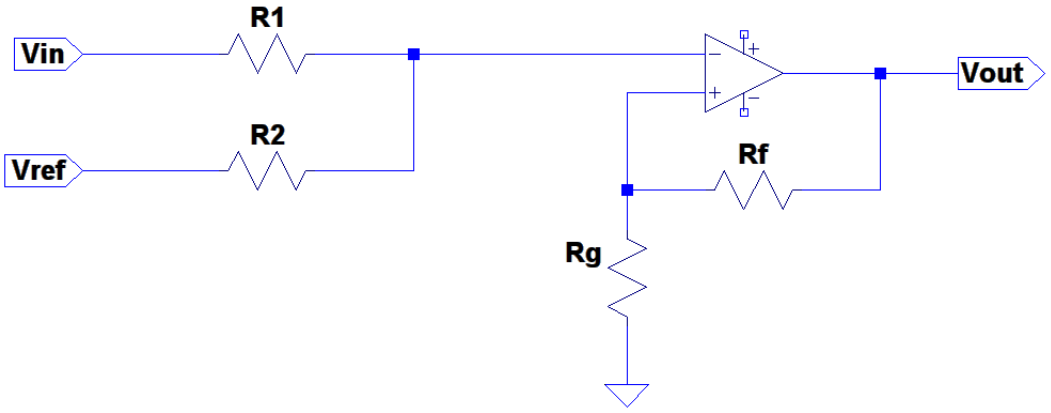

FIGURE 3.12 – Gain and DC offset circuit

1. Determine the zero-scale input voltage $V_{in_{ZS}}$ and the full-scale input voltage $V_{in_{FS}}$. From the model output (figure 3.11), the input voltage is in the range $\pm 4.5V$;

2. Determine the zero-scale output voltage $V_{out_{ZS}}$ and the full-scale output voltage $V_{out_{FS}}$. From the ADC specification on Section 3.3, $0V$ and $10V$, respectively. A slightly smaller range will be used to not saturate ADC input;

3. Select a stable voltage reference V_{ref};

TABLE 3.1 – Gain and Offset circuit parameters - I

Parameter	Value
$V_{in_{ZS}}$	$-4.500V$
$V_{in_{FS}}$	$4.500V$
$V_{out_{ZS}}$	$0.100V$
$V_{out_{FS}}$	$9.900V$
V_{ref}	$5.000V$

4. Calculate the gain m of the stage;

$$\begin{aligned} m &= \frac{V_{out_{FS}} - V_{out_{ZS}}}{V_{in_{FS}} - V_{in_{ZS}}} \\ m &= \frac{9.900 - 0.100}{4.500 - (-4.500)} \\ m &= 1.089 \end{aligned} \tag{3.25}$$

5. Calculate the offset b of the stage;

$$\begin{aligned} b &= V_{out_{ZS}} - mV_{in_{ZS}} \\ b &= 0 - 1.089(-4.500) \\ b &= 4.901 \end{aligned} \tag{3.26}$$

6. Select R_1 and R_f (may be suggested by op-amp datasheet);

7. Calculate R_2 and R_g. The values were approximated to nearest commercial value available;

$$\begin{aligned} R_2 &= \frac{V_{ref} R_1 m}{b} \\ R_2 &= \frac{5.000 * 357k\Omega * 1.089}{4.901} \\ R_2 &= 396.63k\Omega \\ R_{2_c} &= 392k\Omega \end{aligned} \tag{3.27}$$

$$\begin{aligned} R_g &= \frac{R_2 R_f}{m(R_1 + R_2) - R_2} \\ R_g &= \frac{392k\Omega * 7.680k\Omega}{1.089(357k\Omega + 392k\Omega) - 392k\Omega} \\ R_g &= 7.11k\Omega \\ R_{g_c} &= 7.15k\Omega \end{aligned} \tag{3.28}$$

TABLE 3.2 – Gain and Offset circuit parameters - II

Parameter	Value
R_1	$357k\Omega$
R_2	$392k\Omega$
R_f	$7.68k\Omega$
R_g	$7.15k\Omega$

The parameters for the operational amplifier used in the simulation are shown on table 3.3 and the performance of the range conversion circuit (figure 3.13) with commercial resistors is shown on figure 3.14 and summarized on table 3.4.

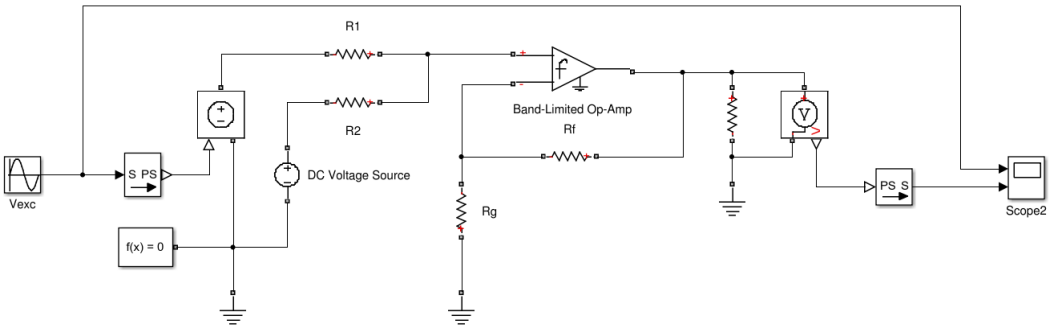

FIGURE 3.13 – Gain and DC offset circuit test model

TABLE 3.3 – Operational amplifier parameters

Parameter	Value
Gain (A)	10^4
Input resistance (R_{in})	$1M\Omega$
Output resistance (R_{out})	100Ω
Minimum output (V_{min})	$-12V$
Maximum output (V_{max})	$12V$
Maximum slew rate ($\dot{V}$)	$10V/us$
Bandwidth (BW)	$100kHz$
Initial output voltage (V_0)	0.000

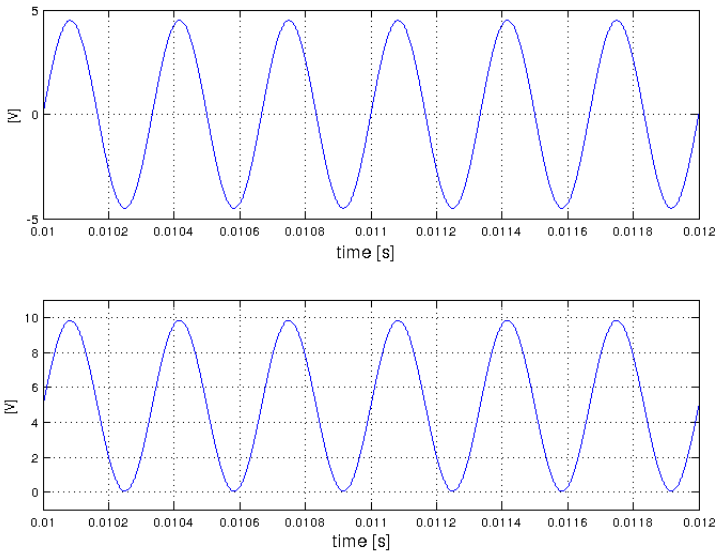

FIGURE 3.14 – Gain and DC offset circuit output

TABLE 3.4 – Gain and Offset circuit output

Parameter	Value
$V_{in_{ZS}}$	$-4.500V$
$V_{in_{FS}}$	$4.500V$
$V_{out_{ZS}}$	$0.000V$
$V_{out_{FS}}$	$9.825V$

A model composed by the LVDT, the transient filter and the range conversion circuit is shown in figure 3.15 and the output for a ramp position input is shown in figure 3.16. The final values are summarized on table 3.5.

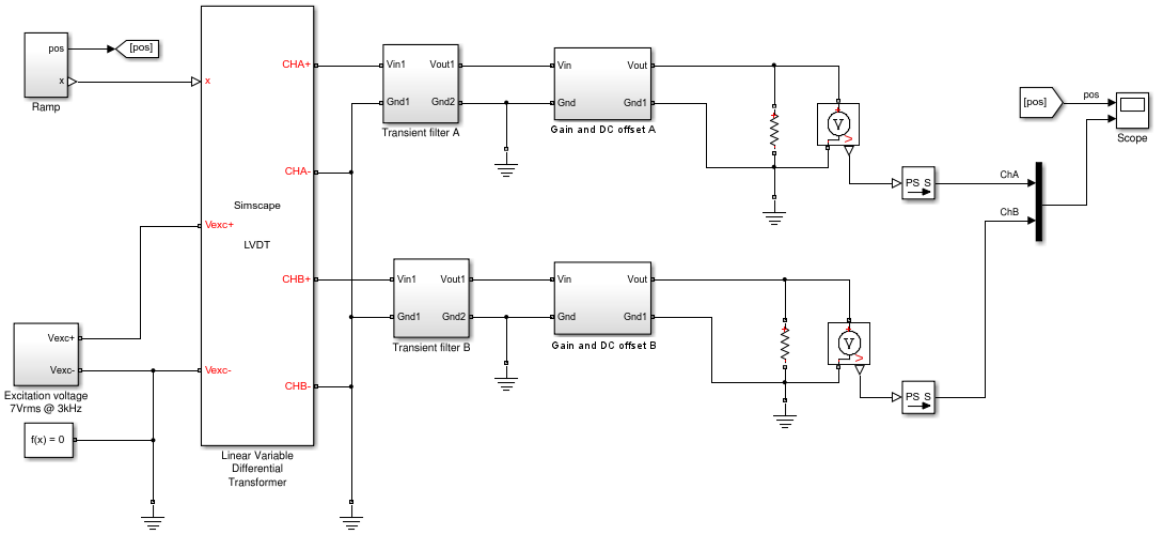

FIGURE 3.15 – LVDT and conditioning circuit test model

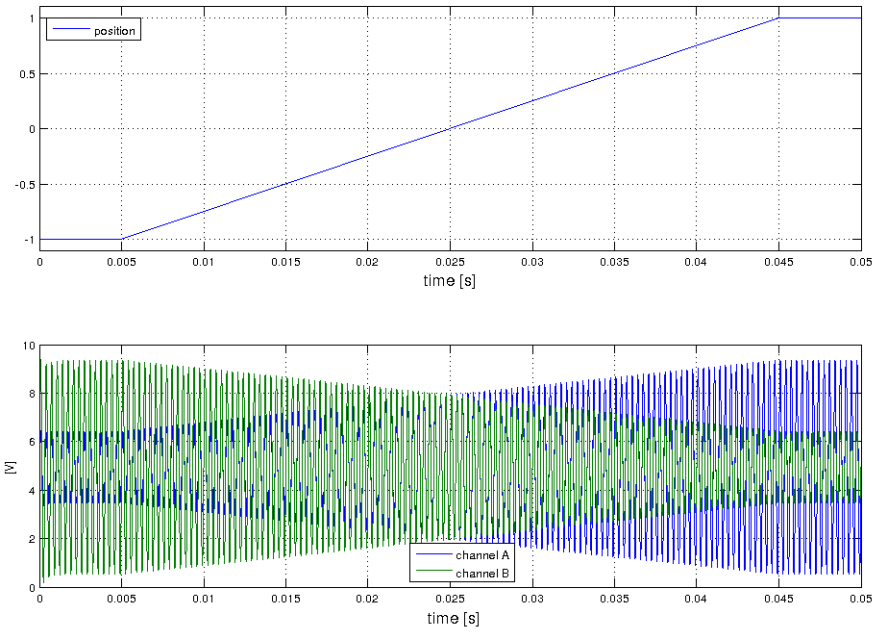

FIGURE 3.16 – LVDT and conditioning circuit model output

TABLE 3.5 – Conditioning circuit model output

Parameter	Value
Minimum signal output	$0.0199V$
Maximum signal output	$9.4006V$
ADC range utilization	93.8%

3.3 Analog-to-Digital Converter

This section presents the behavioral model of a Successive Approximation Register (SAR) ADC which performance parameters were based on the Texas Instruments ADS8638, a 12-bit SAR ADC capable of measuring 8 time-multiplexed channels in multiple selectable ranges up to $\pm 10V$ at $1MSPS$ (mega samples per second). This device provides a sample-and-hold front-end with no latency in conversions and no missing codes (TEXAS INSTRUMENTS, 2017). The ADS8638 performance parameters are summarized on table 3.6.

TABLE 3.6 – ADS8638 performance parameters

Parameter	Value
Resolution	12 $Bits$
Sample rate	$1MSPS$
Selected input range	$[0, 10]V$
Integral non-linearity (INL)	$-0.9/+0.9$ LSB
Differential non-linearity	$-0.5/+0.9$ LSB
Offset error	$-0.8/+0.8$ LSB
Gain error	$-2.0/+2.0$ LSB
Noise	0.33 LSB
Channel crosstalk	$-110dB$
Total harmonic distortion (@$1kHz$)	$-81dB$
Signal-to-noise ratio (@$1kHz$)	$71.8dB$
Signal-to-noise and distortion ratio (@$1kHz$)	$71.3dB$
Spurious-free dynamic range (@$1kHz$)	$-83dB$
Full-power bandwidth (@$-3dB$)	$1MHz$

3.3.1 Input stage

The input stage of the ADC was modelled as a voltage meter across a large value resistor ($1M\Omega$) for each input, as shown on figure 3.17. The reason for this is that the settling time of the ADS8638 is in the order of $250ns$ for sources with small impedance ($< 200\Omega$) such as the range converter circuit, which is slightly above the simulation timestep ($100ns$). In addition, it is also reasonable to assume that the output of the multiplexer is connected to a buffer (figure 3.18) with input resistance many times larger than the ON resistance of each channel (R_{ON}) (ANALOG DEVICES, 2008).

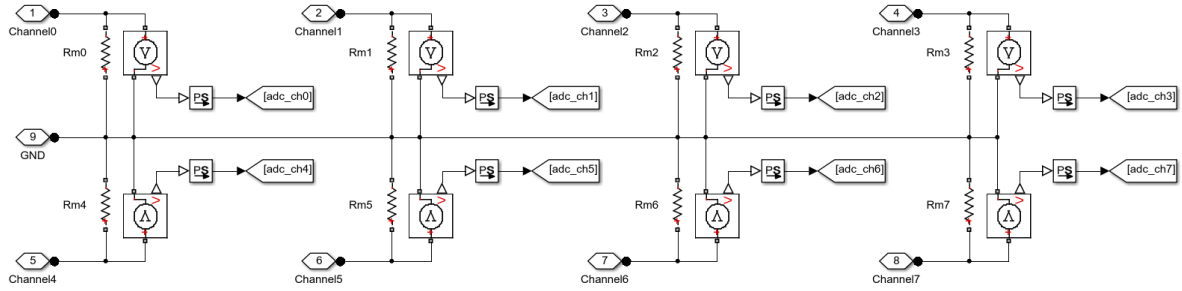

FIGURE 3.17 – ADC input stage

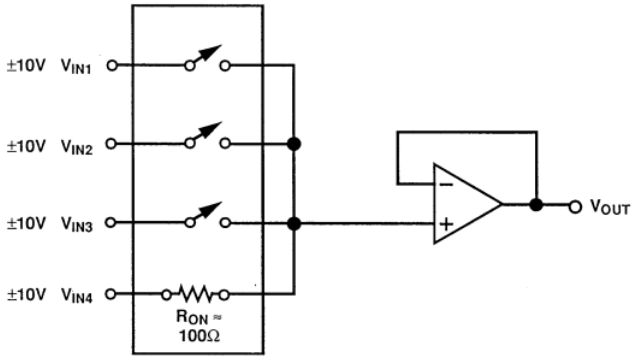

FIGURE 3.18 – Minimizing the influence of R_{ON} - Source: (ANALOG DEVICES, 2008)

3.3.2 Channel crosstalk and channel selection

The crosstalk observed on channel 0 while it is permanently selected and a full-scale $2kHz$ sine wave is applied on channel 1 with all other channels grounded is $-110dB$ (TEXAS INSTRUMENTS, 2017). This value is converted to a gain (CT_g) and a square matrix with order equal to the number of channels is built as shown in 3.29. In order to simplify the implementation, it is considered that the crosstalk is the same for each pair of channels.

$$CT_M = \begin{bmatrix} 1 & CT_{g_{0,1}} & \cdots & CT_{g_{0,n-1}} \\ CT_{g_{1,0}} & 1 & \cdots & CT_{g_{1,n-1}} \\ \vdots & \vdots & \ddots & \vdots \\ CT_{g_{n-1,0}} & CT_{g_{n-1,1}} & \cdots & 1 \end{bmatrix} \tag{3.29}$$

The crosstalk gain matrix CT_M is multiplied (3.30) by the vector comprised of the signals from the input stage resulting in 3.31. The resulting vector is fed to a multiport

switch that selects the desired channel. The implementation is shown on figure 3.19.

$$\begin{bmatrix} \hat{V}_{Ch_0} \\ \hat{V}_{Ch_1} \\ \vdots \\ \hat{V}_{Ch_{n-1}} \end{bmatrix} = \begin{bmatrix} 1 & CT_g & \cdots & CT_g \\ CT_g & 1 & \cdots & CT_g \\ \vdots & \vdots & \ddots & \vdots \\ CT_g & CT_g & \cdots & 1 \end{bmatrix} \begin{bmatrix} V_{Ch_0} \\ V_{Ch_1} \\ \vdots \\ V_{Ch_{n-1}} \end{bmatrix} \tag{3.30}$$

$$\begin{aligned} \hat{V}_{Ch_0} &= V_{Ch_0} + CT_g V_{Ch_1} + \cdots + CT_g V_{Ch_{n-1}} \\ \hat{V}_{Ch_1} &= CT_g V_{Ch_0} + V_{Ch_1} + \cdots + CT_g V_{Ch_{n-1}} \\ &\cdots \\ \hat{V}_{Ch_{n-1}} &= CT_g V_{Ch_0} + CT_g V_{Ch_1} + \cdots + V_{Ch_{n-1}} \end{aligned} \tag{3.31}$$

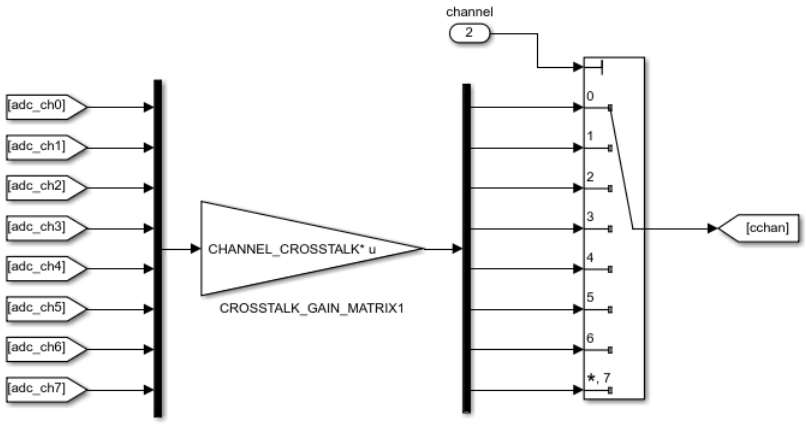

FIGURE 3.19 – Crosstalk injection and channel selection

3.3.3 Harmonic distortion

Since the ADC model in this work does not implement a electric circuit, harmonic distortion must be artificially created. The scheme is similar to one used in (TAHERI; MOHAMMADI, 2014), consisting in taking the input signal and applying a non linear function. The harmonics are created according to 3.32 and a gain for each signal is adjusted to approximate the desired THD. The implementation is shown on figure 3.20.

$$\begin{aligned} sin^2(\omega t) &= \frac{1}{2}(1 - cos(2\omega t)) \\ sin^3(\omega t) &= \frac{1}{4}(3sin(\omega t) - sin(3\omega t)) \\ sin^4(\omega t) &= \frac{1}{8}(-4cos(2\omega t) + cos(4\omega t) + 3) \end{aligned} \tag{3.32}$$

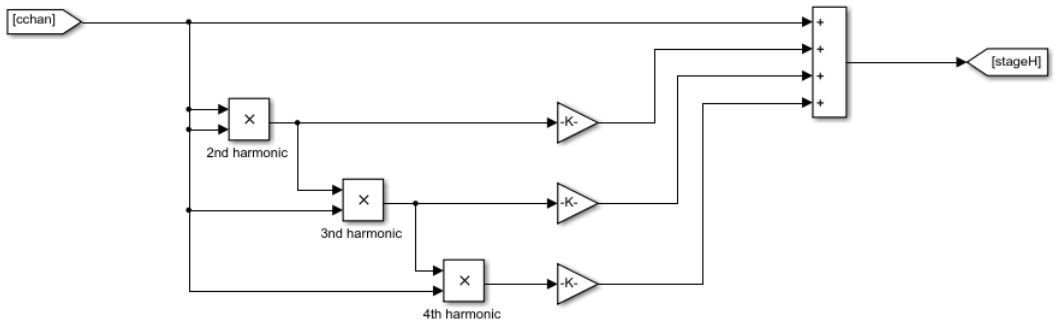

FIGURE 3.20 – Harmonic distortion

3.3.4 Gain, offset and internal noise

The final stage before quantization inserts the gain error, the offset error and adds the internal noise, modelled as a Band-Limited White Noise block. All quantities are specified in LSB units and the implementation is straightforward, shown in figure 3.21.

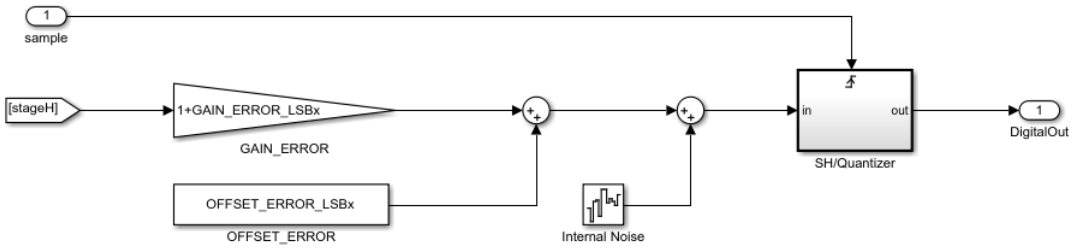

FIGURE 3.21 – Gain and offset errors and internal noise

3.3.5 Quantizer

The quantizer block is responsible for converting the input signal with all the previous non-linearities into the actual digital code. Recalling from section 2.3.1, an ideal quantizer has code widths of uniform size while this is not true for a real quantizer (figure 3.22). The strategy adopted in this work uses a lookup table (LUT) block with interpolation disabled, i.e., the voltage read in sampling instant kT_s is rounded to the nearest code. The model allows the selection of three types of quantizer, the Simulink built-in ideal quantizer, an ideal LUT-based quantizer and a LUT-based quantizer with non-ideal code sizes (figure 3.23).

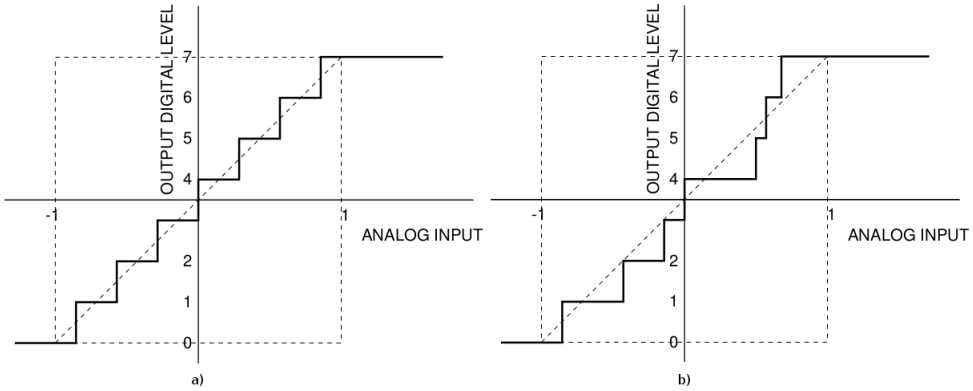

FIGURE 3.22 – An ideal 3-bit quantizer (a) and 3-bit quantizer with non-uniform code bins (b) - Source: (LUNDIN, 2005)

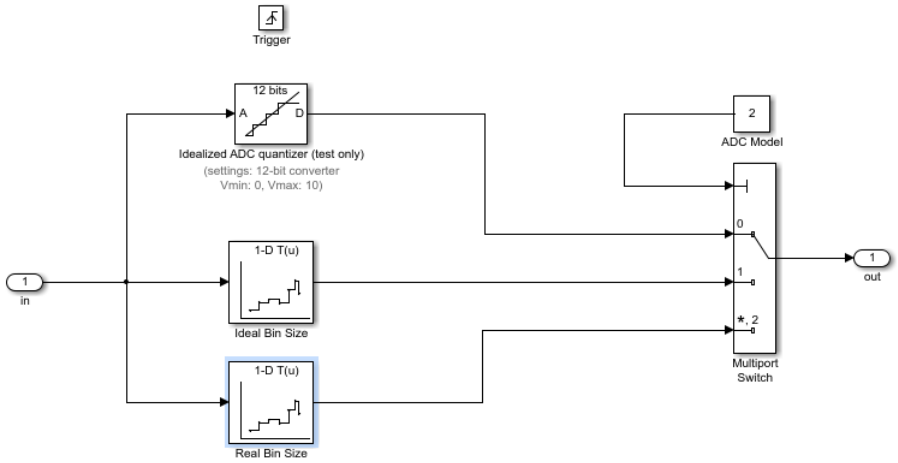

FIGURE 3.23 – The quantizer model on ADC

In the case of a SAR ADC, the comparator and the feedback DAC are the most significative error sources affecting code transition levels (MICHAELI *et al.*, 2006), caused by inaccuracies of the weight values for each bit b_i for $i = 1, 2, \ldots, N$, where N is ADC resolution. The error model proposed by (MICHAELI; SALIGA, 2014) uses measurements of a real device to determine the weight of each bit. INL and DNL differs from device to device and since we are interested on a general behavior, a simplification was made so all bits have the same weight.

To generate the periodic behavior on INL, the INL vector is initialized with a sine function with low frequency (equation 3.33). The function is evaluated for $k = 1 : 2^N - 1$. A weight value W_0 can be used and in this case $W_0 = 1$. For N steps, a sine with double the frequency of the previous one is added to the INL vector (equation 3.34). It is possible to see the evolution of INL vector in figure 3.24 considering $W_n = 1$ for all n and noting

that the final values are not scaled yet.

$$INL_0 = W_0 * sin\left(2\pi\frac{k}{2^N - 1}\right) \tag{3.33}$$

$$INL = \sum_{n=1}^{N-1}\left(INL_{n-1} + W_n * sin\left(2^{n+1}\pi\frac{k}{2^N - 1}\right)\right) \tag{3.34}$$

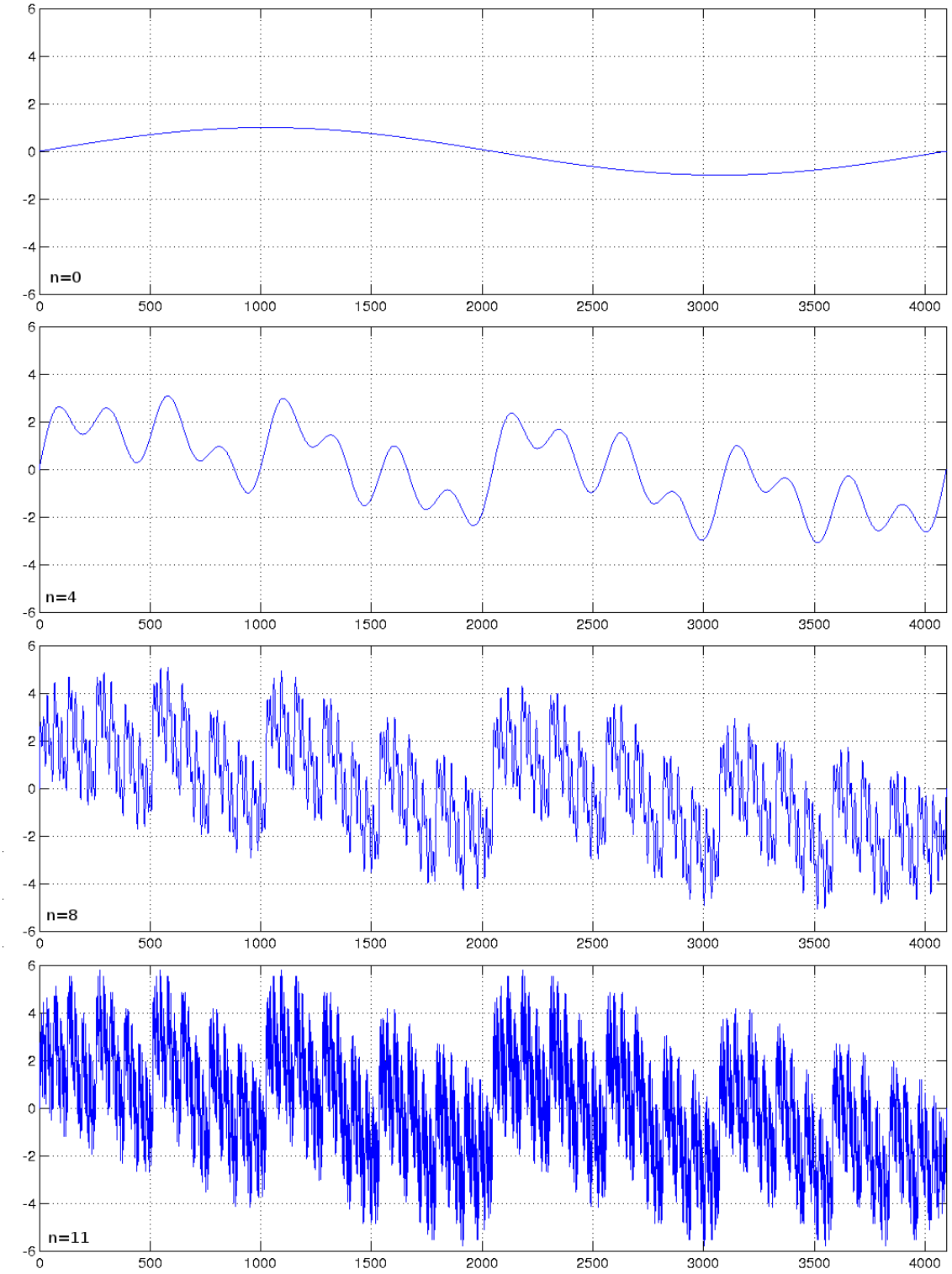

FIGURE 3.24 – Artificially generated INL before adjusting for minimum and maximum values

After this step, the obtained vector is normalized, a small amount of noise is added to it and it is then scaled to comply with minimum and maximum values from datasheet. Since INL is found by computing the cumulative sum of DNL (equation 3.35), to obtain

DNL the opposite operation was used (equation 3.36).

$$INL_k = \sum_{i=1}^{k-1} DNL_i \tag{3.35}$$

$$DNL_k = INL_{k+1} - INL_k \tag{3.36}$$

The obtained DNL and INL values are shown on figure 3.25 and the values from ADS8638 datasheet are show on figure 3.26. It is possible to see that the generated values fall in the range considered typical by the manufacturer. Figure 3.27 shows a zoomed view on the real transition levels around $5V$. In addition:

1. $|DNL|$ is always below 1, guaranteeing that no code is missing;
2. It is possible to see the periodic behavior of INL on both simulated and real cases, as described by (MICHAELI; SALIGA, 2014).

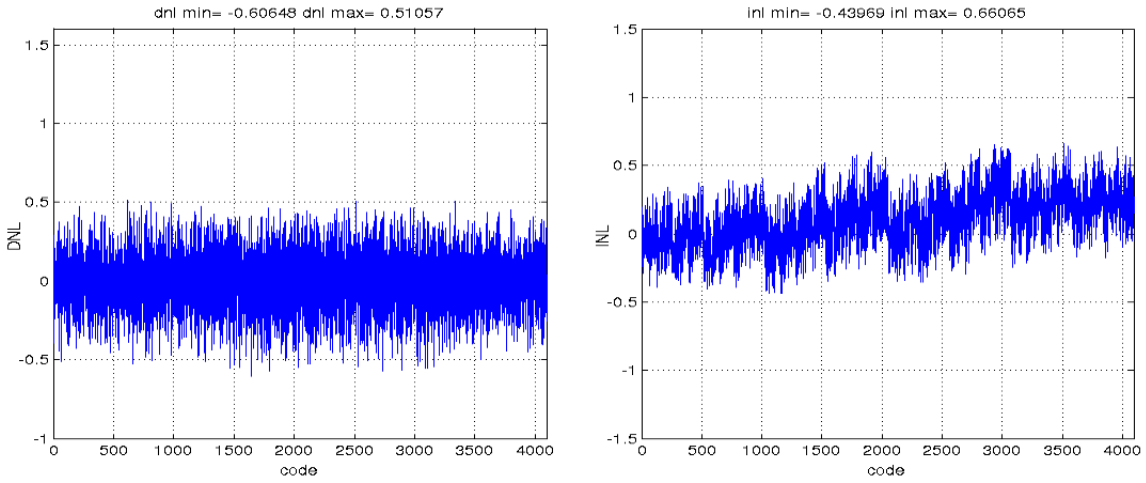

FIGURE 3.25 – Generated DNL and INL values

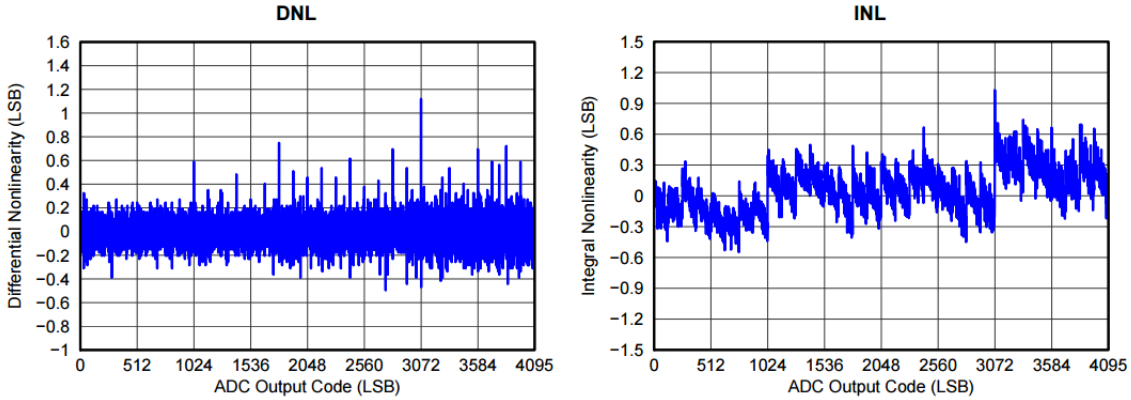

FIGURE 3.26 – Real DNL and INL values for ADS8638- Source: (TEXAS INSTRUMENTS, 2017)

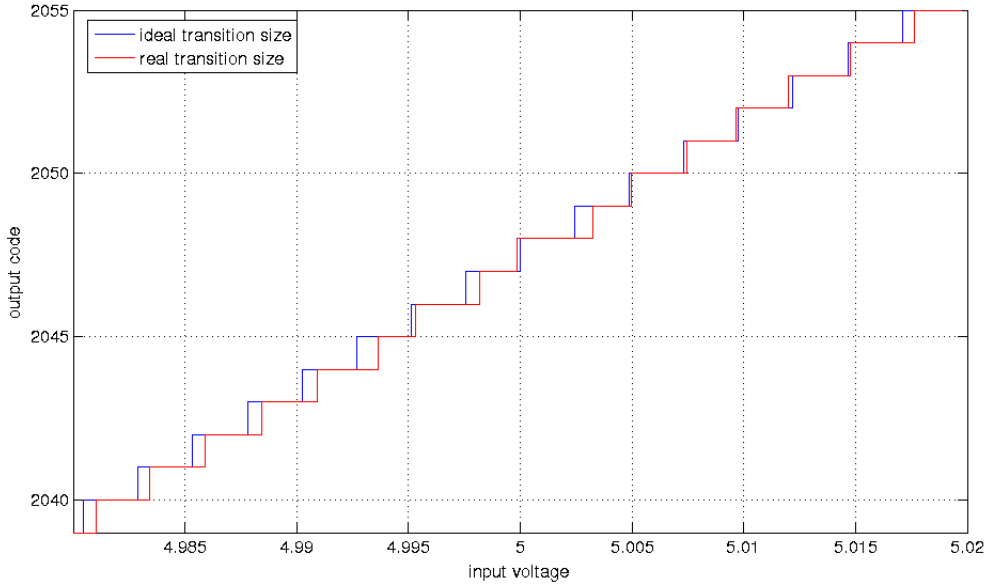

FIGURE 3.27 – Real and ideal transition levels

In order to demonstrate the ADC performance, the model on figure 3.28) was used. The channel 0 was permanently selected and fed with a signal given by 3.37.

$$y(t) = 5 + 4.9 * sin(2\pi 3000t) \tag{3.37}$$

The ADC input parameters are shown on table 3.7, results are shown on figures 3.28 to 3.31 and the final parameters for the model are summarized on table 3.8.

TABLE 3.7 – ADC input parameters

Parameter	Value
Gain error	2 LSB
Offset error	-0.8 LSB
Internal noise	0.33 LSB
Channel crosstalk gain (CT_g)	$3.1623 * 10^{-5}$
2nd harmonic gain	$7.8773 * 10^{-8}$
3rd harmonic gain	$-2.5298 * 10^{-6}$
4th harmonic gain	$-8.5044 * 10^{-10}$

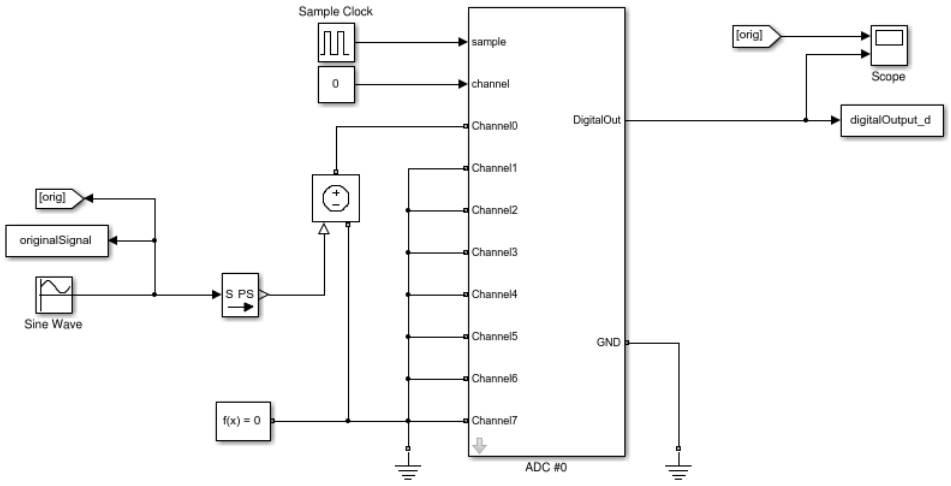

FIGURE 3.28 – ADC evaluation model

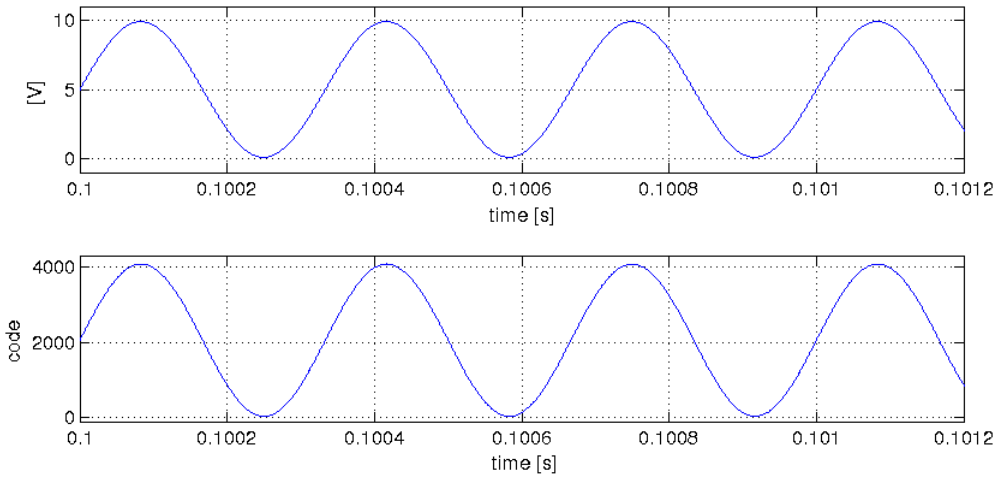

FIGURE 3.29 – Input signal and ADC output

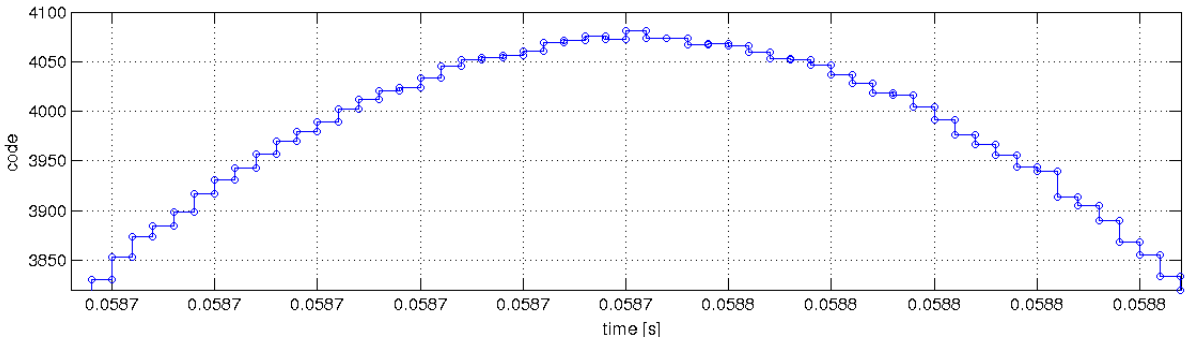

FIGURE 3.30 – ADC output (zoomed in)

In figure 3.31, it is possible to see the DC offset applied on the wave at $0Hz$. The peak value at $3kHz$ is the input signal and the smaller peaks are the harmonics.

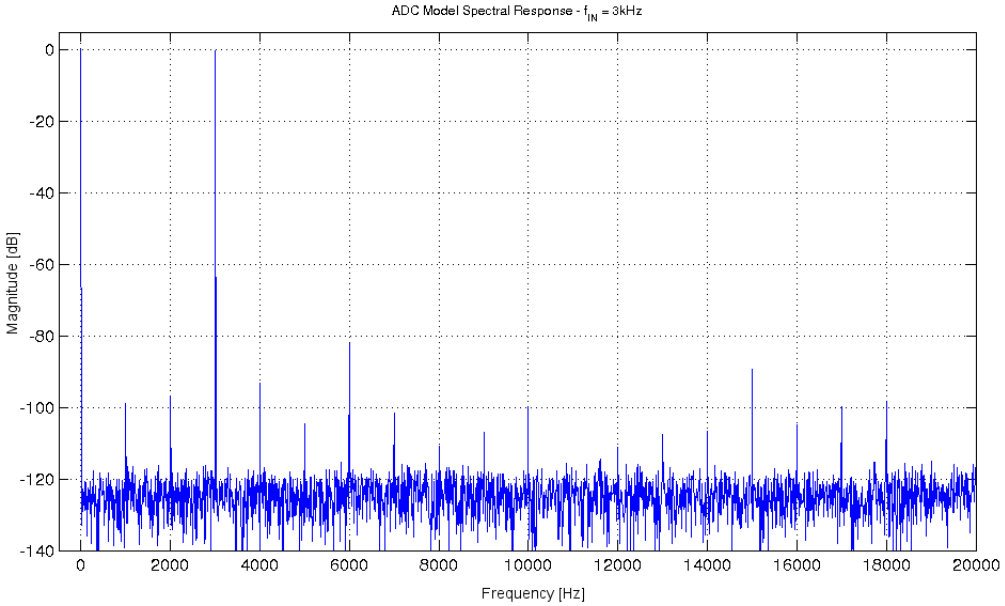

FIGURE 3.31 – ADC model spectral response - $f_{IN} = 3kHz$

TABLE 3.8 – Final ADC performance parameters

Parameter	Datasheet value	Model value
Signal-to-Noise ratio (SNR)	$71.8dB$	$72.2dB$
Total harmonic distortion (THD)	$-81dB$	$-81.05dB$
Signal-to-Noise-and-Distortion ratio (SINAD)	$71.3dB$	$71.6dB$
Spurious-free dynamic range (SFDR)	$-83dB$	$-82dB$
Effective number of bits (ENOB)	11.55	11.61

3.4 ADC Controller

The ADC controller (figure 3.32) is responsible for selecting the appropriate channels according to a scheduling table constructed using 3.38.

$$N_{cyles_k} = \frac{T_{w_k}}{MST} \tag{3.38}$$

where T_{w_k} is the duration of the window for channel k in seconds and MST is the simulation timestep.

On initialization and every time a channel k is selected, an internal counter is loaded with N_{cyles_k}. Each simulation step decrements the counter until the value is zero, triggering an increment the channel selector. When the last channel is finished and channel 0 is selected again, a flag is set indicating the data is ready for processing. This organization was chosen to facilitate the integration with the discrete control law used by (BALLESTEROS, 2015), which will be presented in details on Section 3.5. For now, it is sufficient to say that the update rate of the actuator control law ($CLAW_{rate}$) is $500Hz$.

It is worth noting that the sum of all windows times must be equal to $2ms$ or $\frac{1}{CLAW_{rate}}$. It is possible to use one controller per ADC but to facilitate the implementation and speed up the simulation, the same scheduling table is used for the two ADCs on the final model, to be presented on Section 3.5.

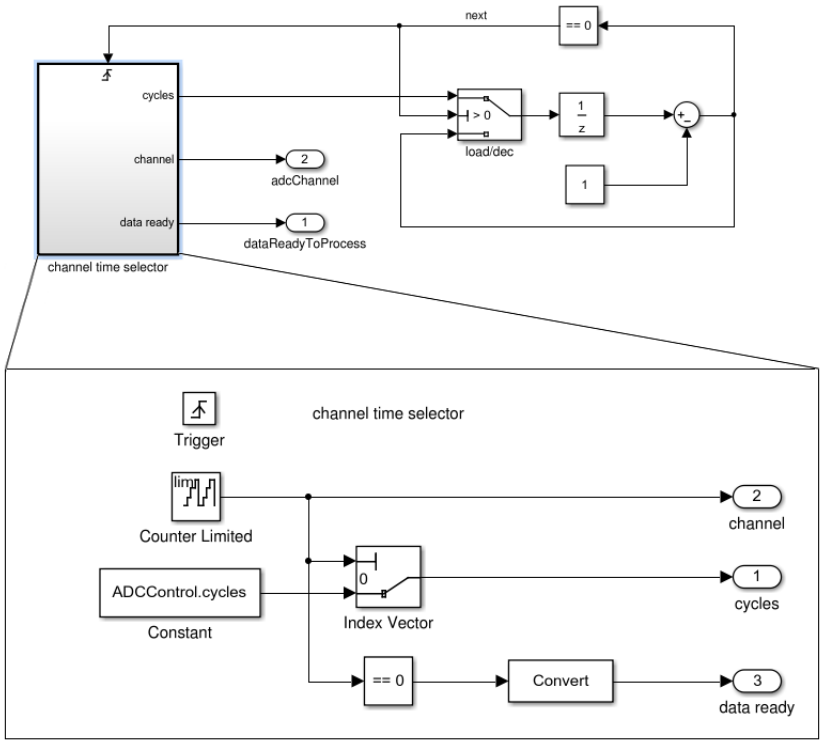

FIGURE 3.32 – ADC controller model

For demonstration, consider that $MST = 10^{-7}s$, channel 0 is selected for $1.2ms$ and the remaining $0.8ms$ is divided between 7 dummy tasks. The controller output is shown on figure 3.33.

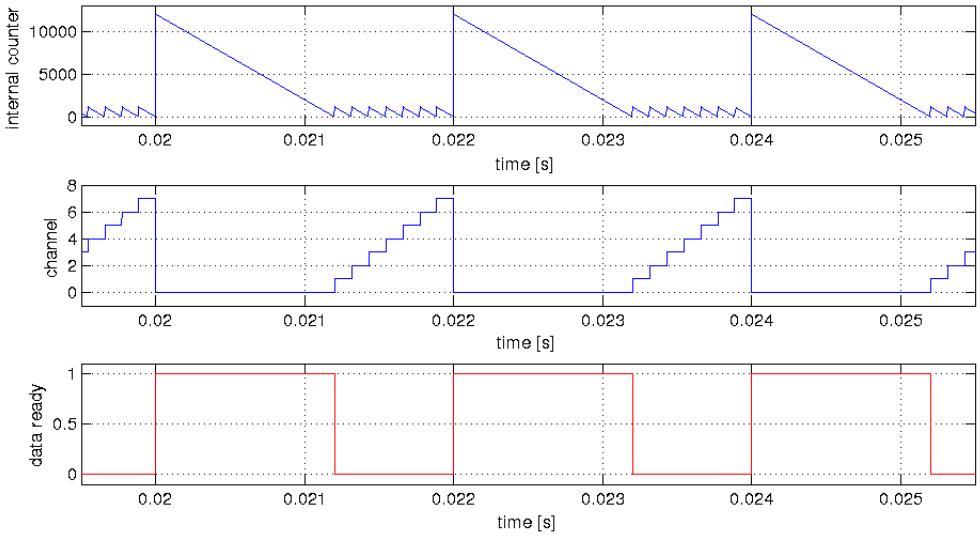

FIGURE 3.33 – ADC controller output

3.4.1 Demodulation algorithm

The final block on the demodulator system (figure 3.34) houses the digital demodulation algorithms and the support code that allows selection of the proper algorithm. It is a MATLAB Function block with the following inputs:

1. The digital output for each ADC on the system;
2. The current channel being sampled;
3. The “data ready” signal;
4. The sampling clock;
5. The algorithm to be used for demodulation.

The block outputs the computed position value in inches, as used by the control law.

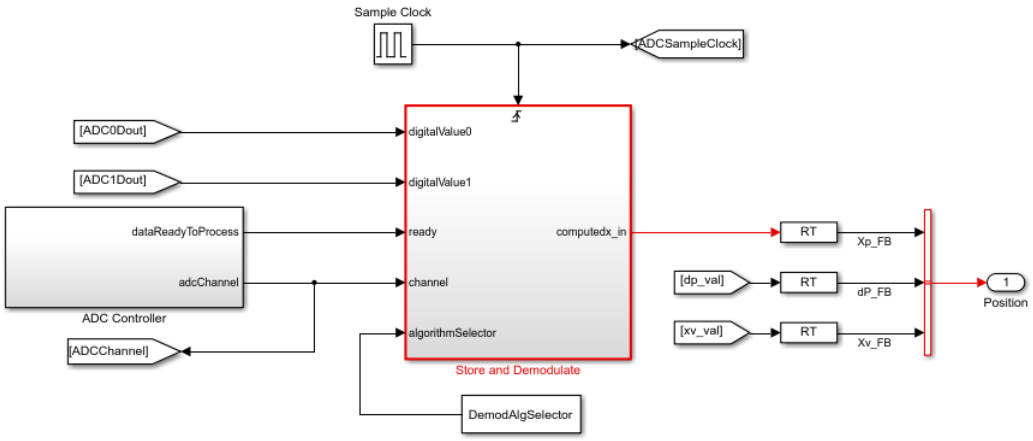

FIGURE 3.34 – Digital demodulator block

Each time the ADCs are sampled, the digital value is stored on memory. The block verifies if the data is ready for processing, calling the appropriate algorithm. Real implementations do not need to store the entire frame before processing, but from a practical point of view it makes no difference if the computed position is ready by the end of the $2ms$ window.

The complete signal acquisition path and demodulation system can be seen on figure 3.35.

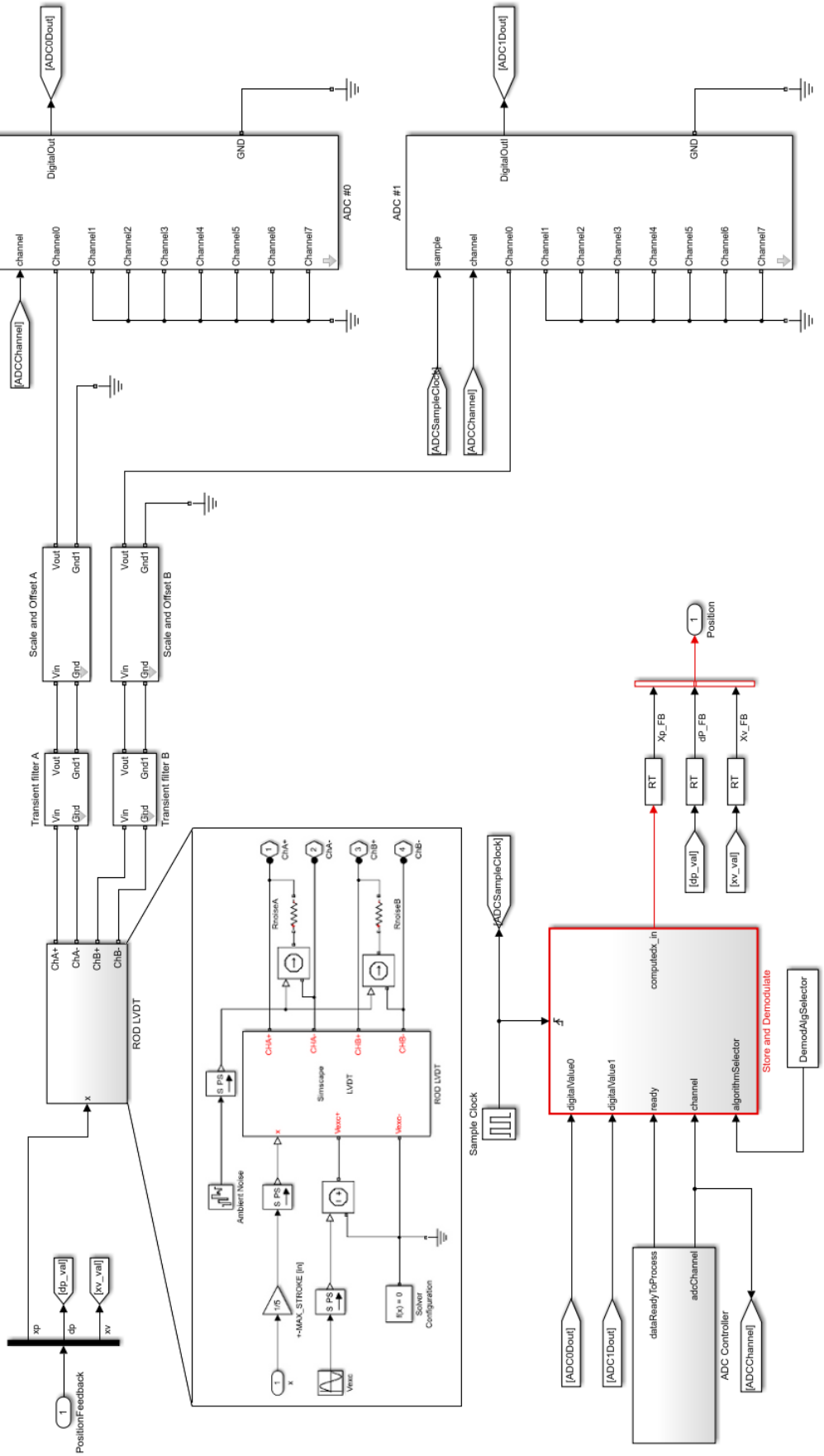

FIGURE 3.35 – Complete signal acquisition path and demodulation system

3.5 Model Integration

This section describes the integration of the signal acquisition and demodulation model developed in this work with the electro-hydraulic actuator model developed by (BALLESTEROS, 2015). The complete system in shown on figure 3.36. It is comprised of three main blocks:

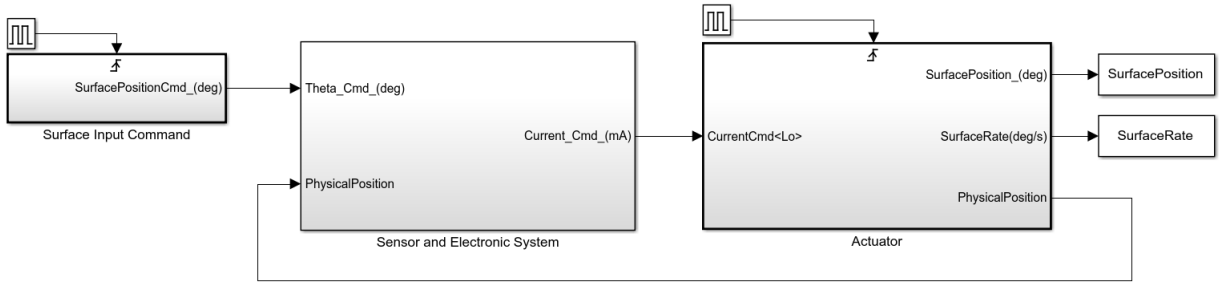

FIGURE 3.36 – Integrated models

1. **Surface Input Command** - This subsystem provides the surface command in degrees. It was developed by (BALLESTEROS, 2015) and modified to update at the same rate as the control law ($500Hz$). In this work, only the step command will be used to investigate the steady state error;

2. **Sensor and Electronic System** - This subsystem houses the models developed in this work (LVDT, transient filter, voltage range converter, analog-to-digital converter and signal demodulator) in addition to the digital controller developed by (BALLESTEROS, 2015). It takes as input the surface command and the real physical positions provided by the actuator model, producing a current command which drives the actuator. The modification allows simple switching between the orignal (in white) and the developed acquisition system (in blue, figure 3.37);

3. **Actuator** - The electro-hydraulic actuator model developed by (BALLESTEROS, 2015). It is comprised by the hydraulic system, the actuator with valves dynamics and surface kinematics (figure 3.38). This model takes as input the actuation current and produces the actual position of the piston rod, the EHSV spool displacement and pressure difference on piston chambers, in addition to surface position in degrees and rate in degrees per second. Because the timestep required to simulate the electrical parts is much smaller that the hydraulic ones, this model was modified to run with a different timestep than the rest of the simulation. Details of the modification are provided on Section 3.5.1.

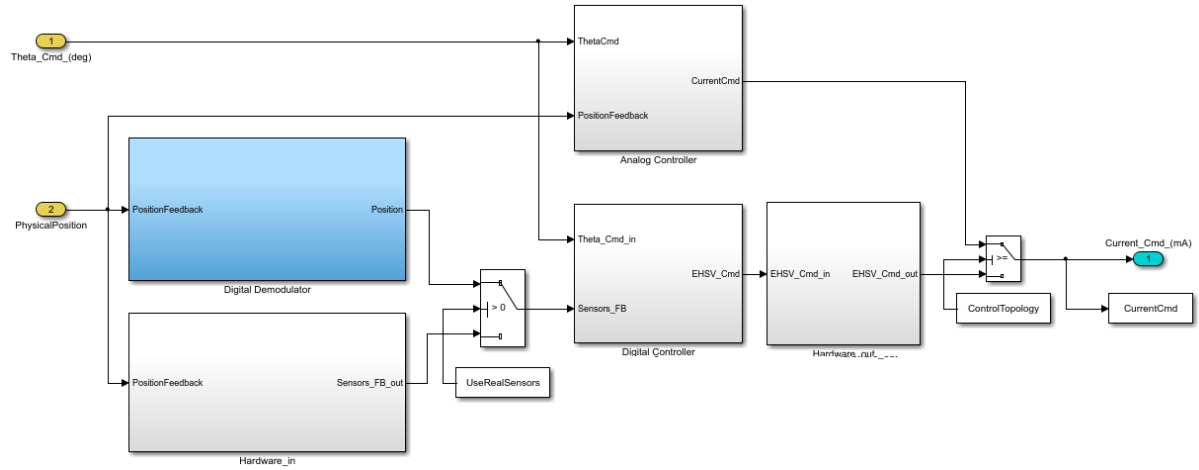

FIGURE 3.37 – Sensor and Electronic System

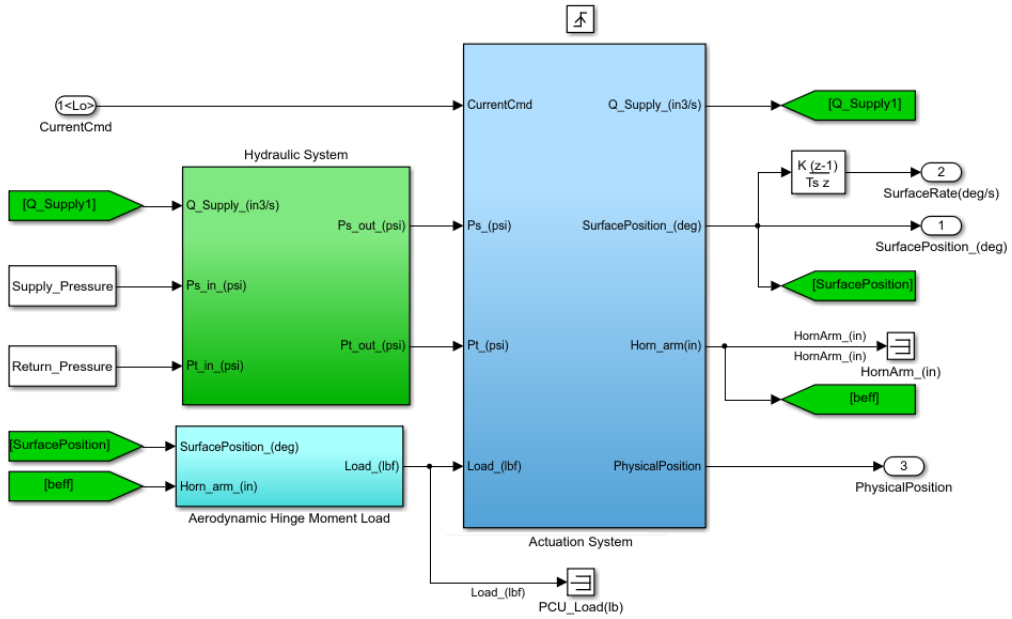

FIGURE 3.38 – Electro-hydraulic Actuator

3.5.1 Electro-hydraulic Actuator

To be able to execute in a different timestep from the rest of the model, the actuator was discretized in the following manner:

1. All the integrator blocks were replaced by discrete integrators (figure 3.39) with unitary gain and sample time equal to "−1", i.e. inherited from from the clock driving the actuator model to update. In practice, this value would be $10^{-5}s$, the same timestep used by (BALLESTEROS, 2015);

2. All transfer functions were discretized using the command "c2d" in MATLAB with

a sample time of $10^{-5}s$ and using the bilinear (Tustin) approximation (ASTROM; WITTENMARK, 2011);

3. Unity delays were inserted to break algebraic loops when necessary.

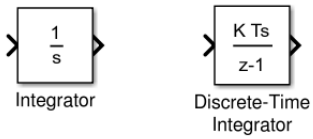

FIGURE 3.39 – Continuous and discrete time integrators

The bilinear approximation relates the $s-$domain with the $z-$domain with equation 3.39, where T_s is the discrete system sample time. Figure 3.40 shows the original model and figure 3.41 illustrates items (2) and (3). The continuous transfer functions and their discrete equivalents are shown on equations 3.40 to 3.43, using $T_s = 10^{-5}$.

$$s = \frac{2}{T_s}\frac{z-1}{z+1} \tag{3.39}$$

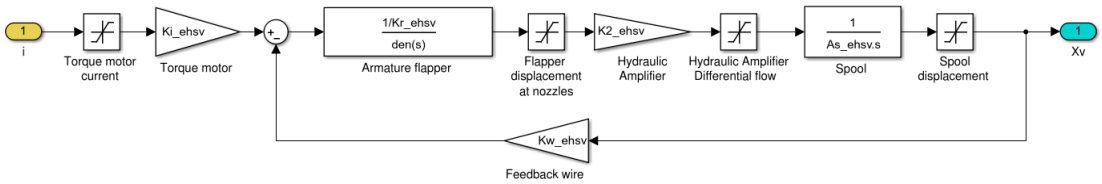

FIGURE 3.40 – EHSV 1st Stage - Continuous model - Source: (BALLESTEROS, 2015)

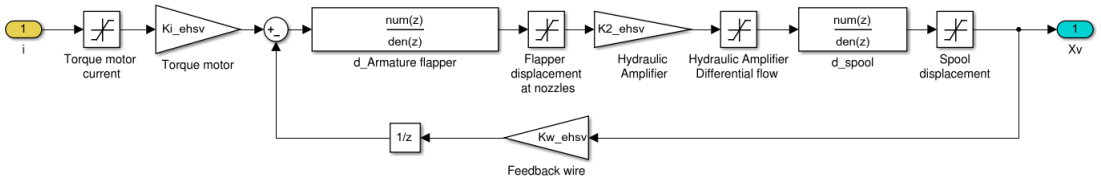

FIGURE 3.41 – EHSV 1st Stage - Discrete model

$$ArmatureFlapper(s) = \frac{0.01075}{4.731 * 10^{-8}s^2 + 0.000172s + 1} \tag{3.40}$$

$$ArmatureFlapper_d(z) = \frac{5.577 * 10^{-6}z^2 + 1.115 * 10^{-5}z + 5.577 * 10^{-6}}{z^2 - 1.962z + 0.9643} \tag{3.41}$$

$$Spool(s) = \frac{1}{0.026s} \tag{3.42}$$

$$Spool_d(z) = \frac{0.0001923z + 0.0001923}{z - 1} \tag{3.43}$$

The step response from the original model versus the discretized model is shown on figures 3.42 and 3.43. Both models used the same controller and the sensor model created by (BALLESTEROS, 2015).

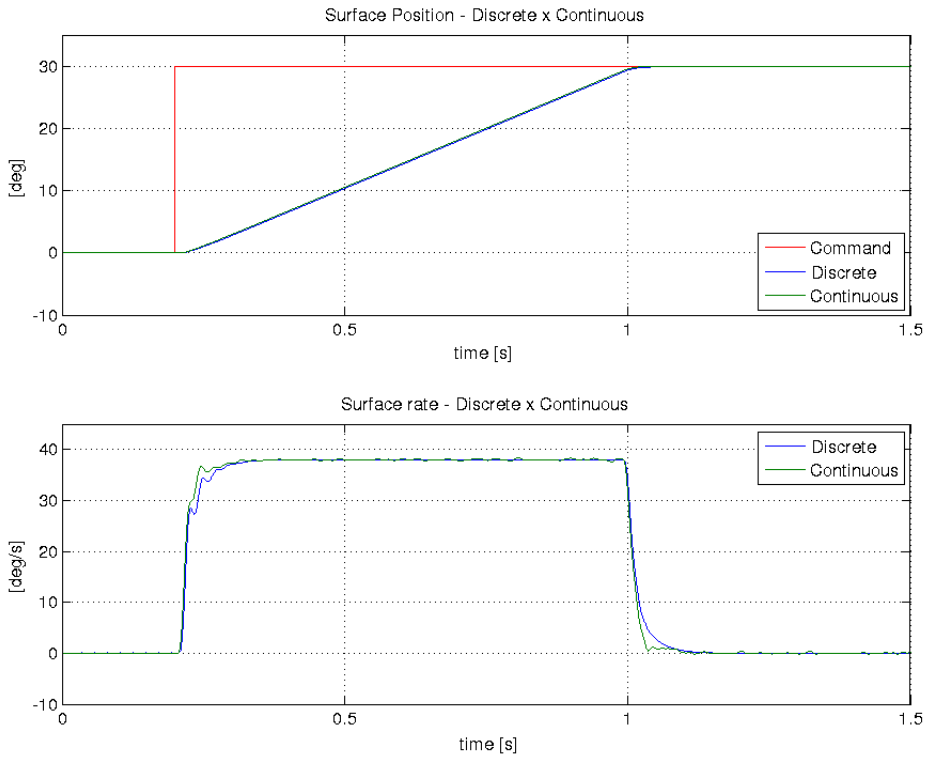

FIGURE 3.42 – Surface position and rate for discrete and continuous model

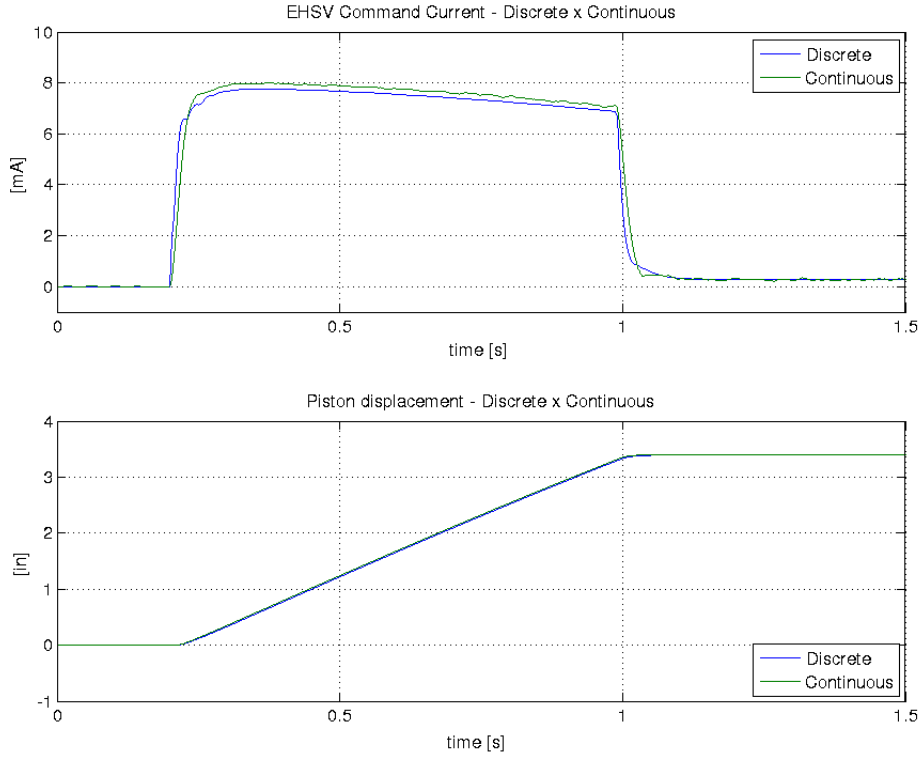

FIGURE 3.43 – EHSV command current and piston displacement for discrete and continuous model

3.5.2 Digital Controller

The controller used in this work is a classic, digital PID built and tuned in (BALLESTEROS, 2015). A discrete PID controller can be described by equation 3.44 in z-domain, where T_s is the controller sample time, $U(z)$ is the action command, $E(z)$ is the error signal computed from the difference between the surface input command and the actual surface position and K_p, K_i and K_d correspond to proportional, integral and derivative gain respectively (ASTROM; WITTENMARK, 2011).

$$U(z) = \left(K_p + K_i \frac{T_s}{2} \frac{z+1}{z-1} + K_d \frac{2}{T_s} \frac{z-1}{z+1} \right) E(z) \tag{3.44}$$

The controller implemented by (BALLESTEROS, 2015) differs slightly from the classical formulation in two aspects: firstly, by using a high-pass filter to implement the derivative term (equation 3.45) since an unfiltered approach would give a very large amplification of measurement noise (ASTROM; WITTENMARK, 2011). The value N is the filter coefficient.

$$U(z) = \left(K_p + K_i \frac{T_s}{2} \frac{z+1}{z-1} + K_d \frac{N}{1 + N \frac{T_s}{2} \frac{z+1}{z-1}} \right) E(z) \tag{3.45}$$

The second aspect is the anti-windup mechanism used to prevent the integrators windup, a situation in a PID feedback controller where a large change in setpoint occurs and the integral terms accumulates a significant error during the rise (windup), thus overshooting and continuing to increase as this accumulated error is unwound. The adopted mechanism decreases the integral term when the control variable surpass the actuator limits. The final model is shown on figure 3.44.

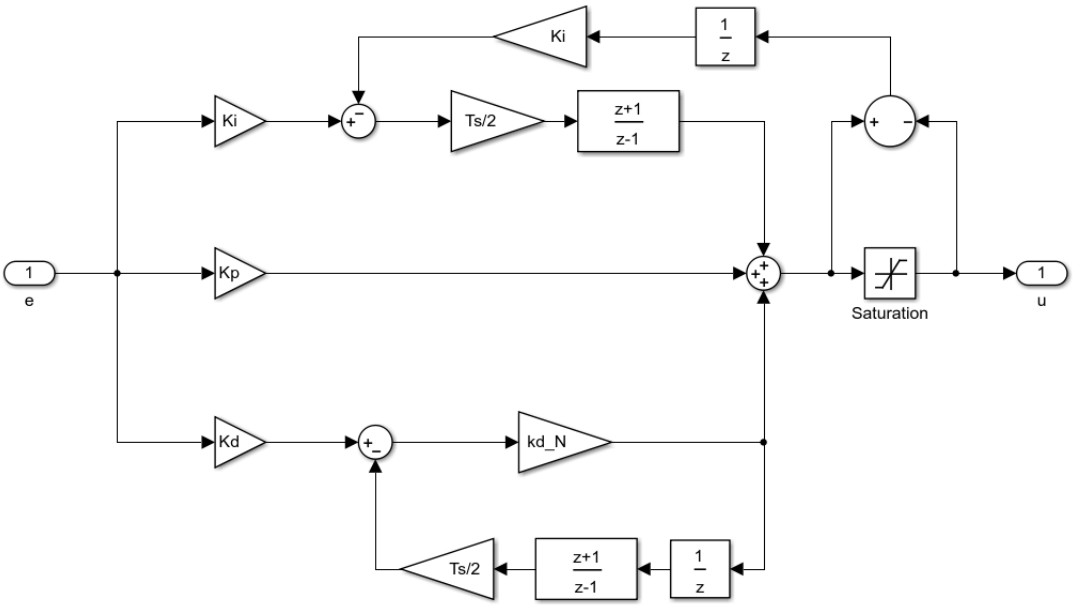

FIGURE 3.44 – Discrete PID controller - Source: (BALLESTEROS, 2015)

Four different PID controllers were implemented by (BALLESTEROS, 2015) and the values selected on table 3.9 yielded the smallest settling time ($651ms$) and steady state error (0.12%) with no overshoot. This controller will be used in all experiments on Chapter 4, so any steady state error can be attributed to the readings received by the controller.

TABLE 3.9 – PID Controller Parameters

Parameter	Value
Proportional gain (K_p)	60
Integral gain (K_i)	10^{-6}
Derivative gain (K_d)	0.5
Filter coefficient (N)	100
Sample time (T_s)	$2ms$

4 Demodulation Algorithms

This chapter presents the implementation and evaluation of two different digital demodulation algorithms, the Peak Detector and Oversampling and Averaging.

4.1 Initial considerations

To correctly demodulate the signal and compute the position in software, some quantities must be known and some considerations must be made. Firstly, an LVDT of adequate range must be selected. From (BALLESTEROS, 2015), the excursion of the piston rod is $\pm 3.74in$ or about $\pm 95mm$. For an LVDT with stroke range of $\pm 4in$ ($101.6mm$) this would be about 94% of the excursion leaving a small mechanical tolerance. Thus, an LVDT with stroke range equal to $\pm 5in$ ($127mm$) is selected and the rod excursion is 74.8%.

Another important parameters are the electrical output of the LVDT and the full displacement ratio. In order to use the ratiometric demodulation (equation 4.1), an LVDT with 5 or 6 wires must be used, so the voltage on each coil can be obtained individually. Recalling from Section 2.1.2, the model LVDT output is shown on figure 4.1 with a ratio of 0.5 (equation 4.2).

$$r = \frac{V_a - V_b}{V_a + V_b} \tag{4.1}$$

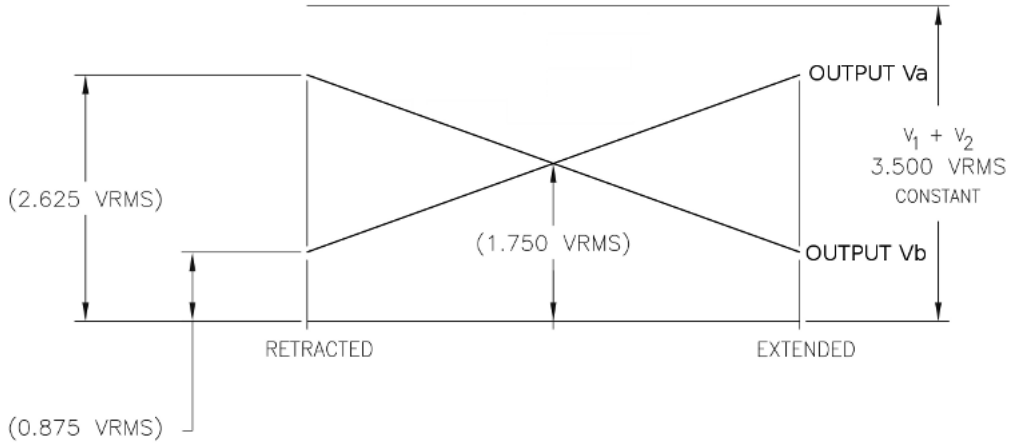

FIGURE 4.1 – LVDT output

$$
\begin{aligned}
r &= \frac{V_a - V_b}{V_a + V_b} \\
r &= \frac{2.625 - 0.875}{2.625 + 0.875} \\
r &= \frac{1.750}{3.500} \\
r &= 0.5
\end{aligned}
\tag{4.2}
$$

Table 4.1 summarizes the values expected to be seen on each step of the signal acquisition path.

TABLE 4.1 – Electrical ranges on the signal acquisition path

Parameter	Value
LVDT output	$[1.237, 3.712]\ V$
Filter output	$[1.355, 4.072]\ V$
Range converter full output	$[0.000, 9.825]\ V$
Range converter output for maximum filter output	$[3.433, 6.392]\ V$
Range converter output for minimum filter output	$[0.467, 9.357]\ V$

4.1.1 Actuator kinematics

Although the variable being acquired is the piston rod position, the controlled one is the surface deflection, against which the performance of the algorithms will be evaluated. The rod position is expressed in inches while the surface deflection is expressed in degrees. The actuator is usually attached to a fixed structure and to a control surface, the movable structure, as shown on figure 4.2). By convention, L is the actuator length, known as

pin-to-pin distance, R is the horn radius and C is the distance between the anchorage point in the non-moveable surface and the anchorage point in the control surface, defining the RLC triangle (figures 4.3 and 4.4) (BALLESTEROS, 2015).

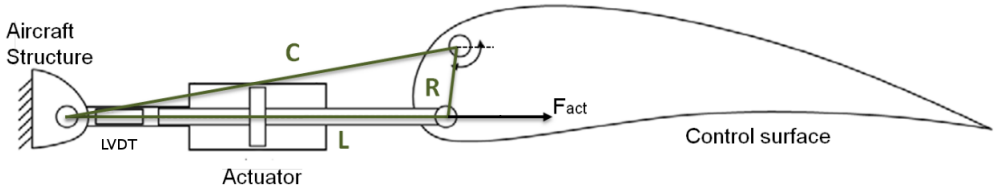

FIGURE 4.2 – Actuator, LVDT, surface and RLC triangle - Source: (BALLESTEROS, 2015) (modified)

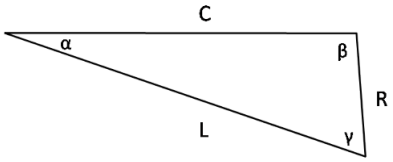

FIGURE 4.3 – RLC triangle for an actuator in neutral position - Source: (BALLESTEROS, 2015) (modified)

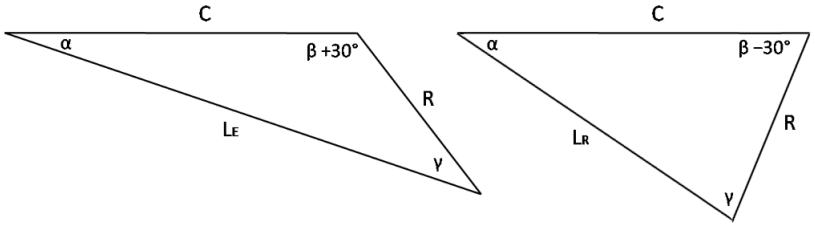

FIGURE 4.4 – RLC triangle for an actuator in extended and retracted positions - Source: (BALLESTEROS, 2015) (modified)

Using the law of cosines, the relations between the triangle sidees to the internal angles can be obtained:

$$L^2 = R^2 + C^2 - 2RCcos(\beta) \tag{4.3}$$

Considering L_0 and β_0 the length and angle for actuator in neutral position, x_p the current piston rod displacement and θ_s the surface deflection:

$$cos(\beta_0) = \frac{R^2 + C^2 - L_0^2}{2RC} \tag{4.4}$$

$$cos(\beta_0 + \theta_s) = \frac{R^2 + C^2 - (L_0 + x_p)^2}{2RC} \tag{4.5}$$

The relation between piston displacement and surface deflection can be summarized by equation 4.6.

$$\theta_s = arccos\left(\frac{R^2 + C^2 - (L_0 + x_p)^2}{2RC}\right) - \beta_0 \tag{4.6}$$

The parameters obtained from(BALLESTEROS, 2015) are summarized on table 4.2.

TABLE 4.2 – Actuator installation parameters

Parameter	Value
R	6.81 *in*
L_0	19.88 *in*
C	20.85 *in*
β_0	72.40°
Deflection range	±30.00°
Deflection range (mechanical)	±33.29°

4.2 Peak Detector

To obtain the peak value, the following procedure is used. Consider that the input vectors $\hat{V}_a$ and $\hat{V}_b$ contain only channel 0 data, i.e. the data read from the ADCs are already separated into channels (figure 4.5).

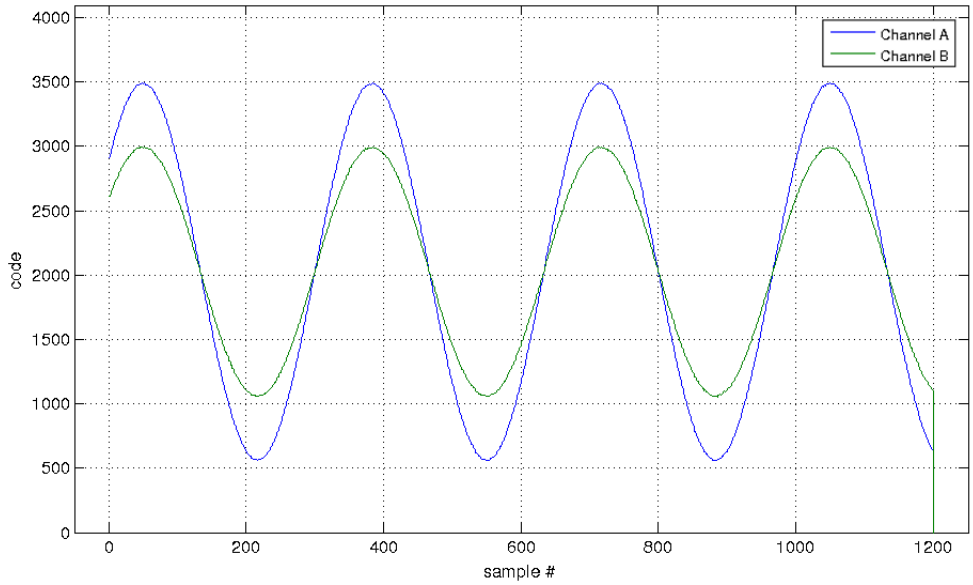

FIGURE 4.5 – Sampled data before processing

1. From the range converter output on table 4.3, the offset value V_{off} is obtained (4.7).

This is the mid value of the range converter circuit, produced when the input crosses zero. The digital value V_{off_d} correspondent is 2012.

$$V_{out} = 1.0917 * V_{in} + 4.9125 \tag{4.7}$$

TABLE 4.3 – Gain and Offset circuit output

Parameter	Value
$V_{in_{ZS}}$	$-4.500V$
$V_{in_{FS}}$	$4.500V$
$V_{out_{ZS}}$	$0.000V$
$V_{out_{FS}}$	$9.825V$

2. The digital offset value is subtracted from both vectors and the absolute value is taken, effectively rectifying the signal (figure 4.6). The red line is the zero crossing threshold used on next step.

$$\begin{aligned} \hat{V}_{a_{rec}} &= abs(\hat{V}_a - V_{off_d}) \\ \hat{V}_{b_{rec}} &= abs(\hat{V}_b - V_{off_d}) \end{aligned} \tag{4.8}$$

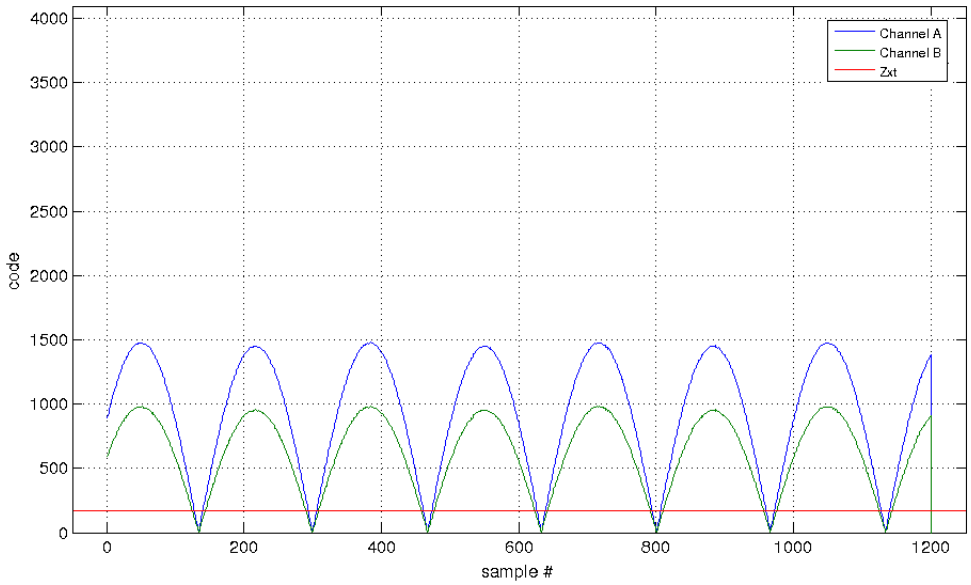

FIGURE 4.6 – Rectified signal

3. The resulting vectors are swept and the algorithm on figure 4.7 is applied to obtain the mean peak value, where Z_{x_t} is the zero crossing threshold and Z_c is the counted

number of samples below the threshold. Both values and the sufficient number of samples below Z_c to consider a zero crossing were empirically determined. Other relevant variables are "peak", a vector containing the peaks for each half wave, "cycle" is the current half wave being examined and "testing for maximum value" is a flag indicating that the rectified signal has crossed zero and is increasing. It is clear from figure 4.8 the need to discard the rightmost peak, preventing incomplete half waves to interfere with result.

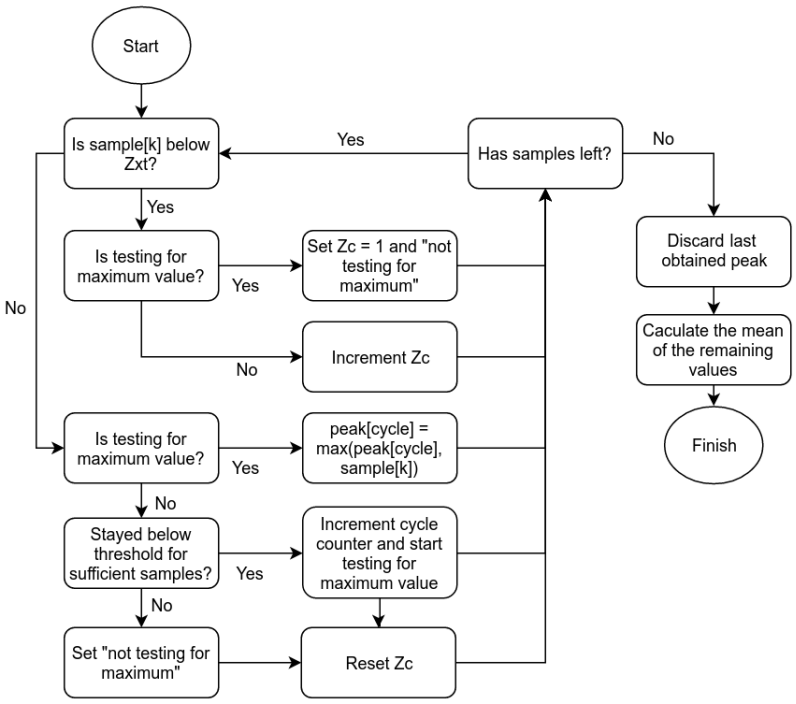

FIGURE 4.7 – Peak detection algorithm

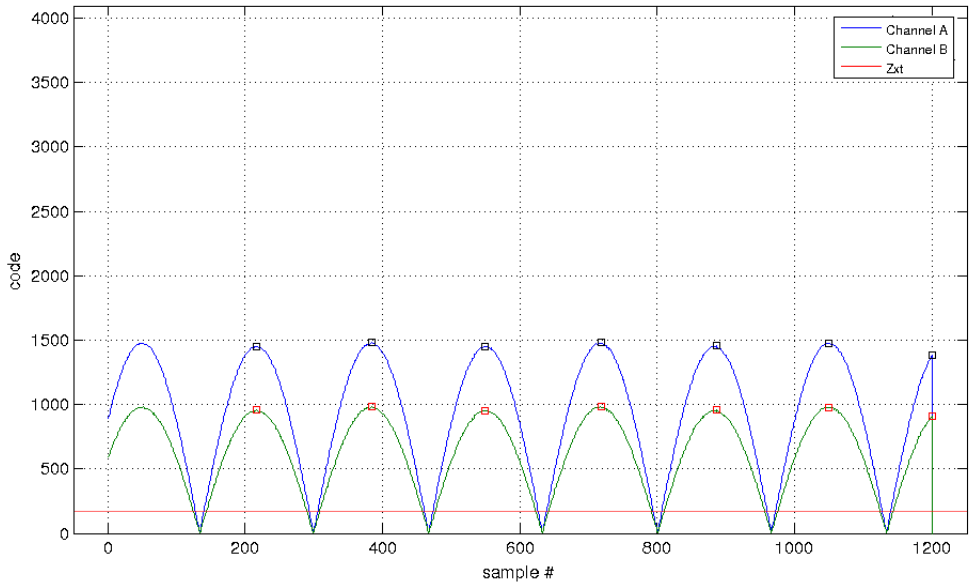

FIGURE 4.8 – Detected peaks

4. The peak values for $\hat{V}_{a_{rec}}$ and $\hat{V}_{b_{rec}}$ are applied on equation 4.1 to obtain the current ratio $r_{computed}$. For a maximum stroke (S_{max}) of $5in$, the maximum ratio (r_{max}) would be 0.5. The position in inches in obtained from expression 4.9.

$$X_{p_{computed}} = \frac{r_{computed}}{r_{max}} S_{max} \tag{4.9}$$

4.3 Oversampling and Averaging

Oversampling and averaging can be used to increase measurement resolution, without using a high resolution ADC. The technique improves the SNR (when white noise is concerned) and resolution at the cost of increased CPU utilization and lower throughput. Recalling Section 2.2, a low pass filter with cutoff frequency of $30kHz$ was used. The required sampling frequency (f_s) according to the Nyquist theorem is at least twice this value. To increase the effective number of bits (ENOB) the signal should be oversampled with a new sampling frequency f_{os} (SILICON LABORATORIES, 2003):

$$f_{os} = 4^w f_s \tag{4.10}$$

where w is the number of additional bits of resolution desired. Sampling the input signal with an $1MSPS$ ADC would increase the resolution in about 2 bits, according to equation 4.11. This way, 4^w points are collected, summed and averaged to produce one data point

with increased resolution.

$$\begin{aligned} w &= log_4\left(\frac{f_{os}}{f_s}\right) \\ w &= log_4\left(\frac{10^6}{60\times 10^3}\right) \\ w &= 2.03 \end{aligned} \tag{4.11}$$

In this algorithm, we use the average value of the signal to compute ratio between the difference and sum of the voltages because it is less expensive computationally. Calculating the RMS value would require one multiplication per sample per channel and one radiciation per computed position point per channel. The average value of a discrete signal $U[k]$ is given by:

$$U_{AVG} = \frac{1}{N}\sum_{i=1}^{N} abs(U[i]) \tag{4.12}$$

where $abs(x)$ is the absolute value of x. To obtain the position, the following procedure is used. Consider that the input vectors $\hat{V_a}$ and $\hat{V_b}$ contain only channel 0 data, i.e. the data read from the ADCs are already separated into channels (figure 4.5).

1. Similarly to peak detector algorithm, the signal is rectified by subtracting the offset inserted by the range converter and the absolute value is taken.

$$\begin{aligned} \hat{V}_{a_{rec}} &= abs(\hat{V_a} - V_{off_d}) \\ \hat{V}_{b_{rec}} &= abs(\hat{V_b} - V_{off_d}) \end{aligned} \tag{4.13}$$

2. The first and the last zero crossings are obtained from the sampled signal (figure 4.9), delimiting a integer number of half-cycles. The points between the zero crossings are applied on equation 4.12 and the average value for each channel is obtained.

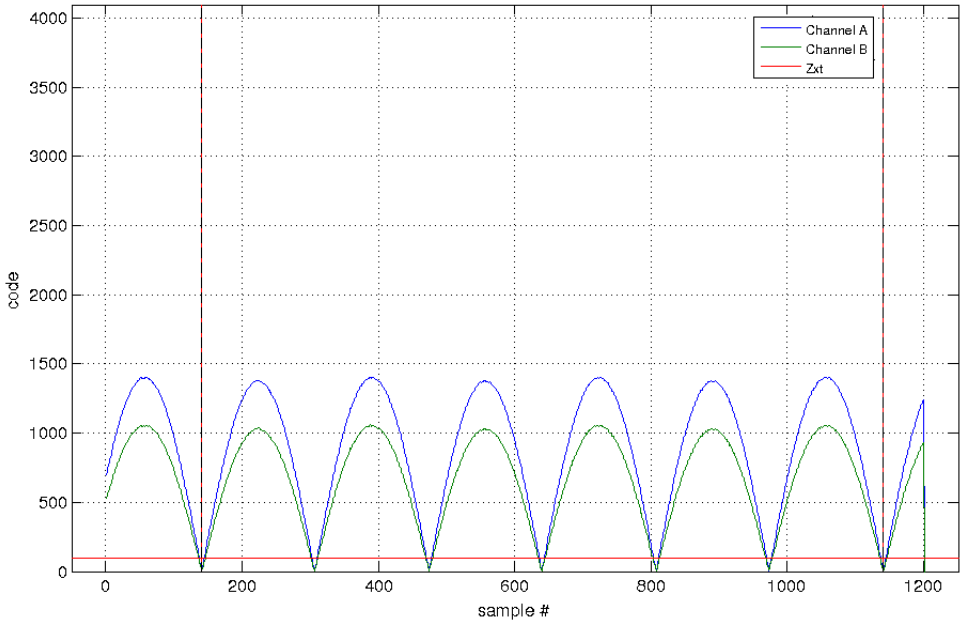

FIGURE 4.9 – First and last zero crossings

3. The average values for $\hat{V}_{a_{rec}}$ and $\hat{V}_{b_{rec}}$ are applied on equation 4.1 to obtain the current ratio $r_{computed}$. For a maximum stroke (S_{max}) of $5in$, the maximum ratio (r_{max}) would be 0.5. The position in inches in obtained from expression 4.14.

$$X_{p_{computed}} = \frac{r_{computed}}{r_{max}} S_{max} \tag{4.14}$$

4.4 Experiments

In this section, the previously implemented algorithms will be tested regarding the following aspects.

1. Steady state error for a step input;
2. Effect of number of sampled points per cycle;
3. Tolerance to noise on input.

For the following tests in this section, the PID controller was used with the following parameters:

TABLE 4.4 – PID Controller Parameters

Parameter	Value
Proportional gain (K_p)	60
Integral gain (K_i)	10^{-6}
Derivative gain (K_d)	0.5
Filter coefficient (N)	100
Sample time (T_s)	$2ms$

4.4.1 Steady state error

The main goal of this section is to verify the steady state error for a step input of 30° for each algorithm in the absence of external influence. In this tests, no noise was inserted on the signal path besides the internal noise from the ADC. The gain and offset errors, correctable via calibration, are set to zero. The results are shown on figures 4.10 and 4.11 and are summarized on table 4.5.

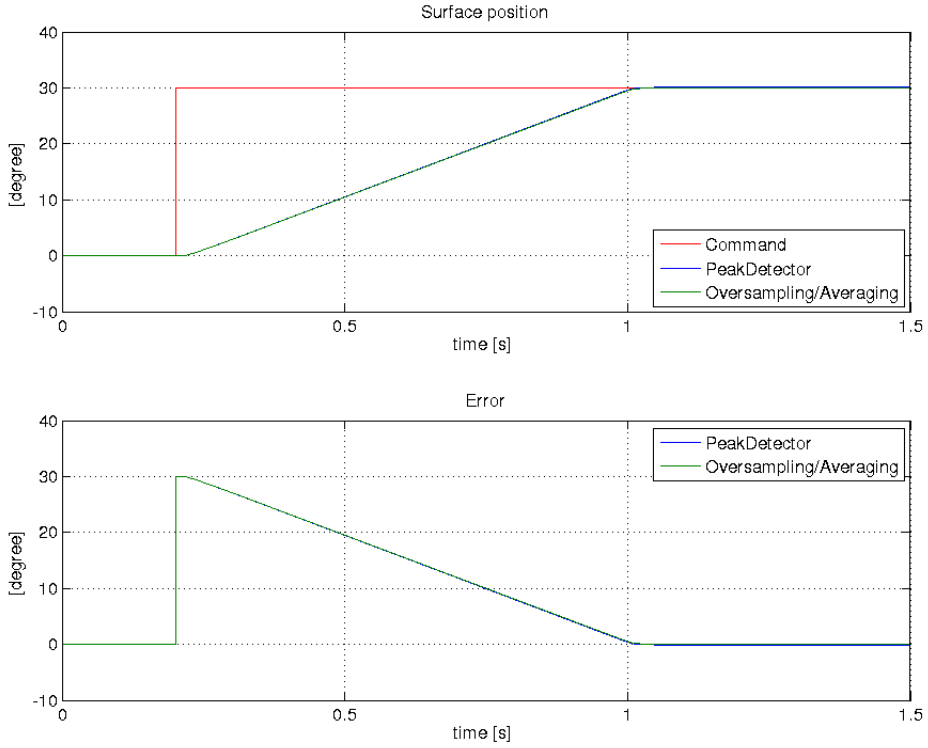

FIGURE 4.10 – Step response for both algorithms in the absence of external error

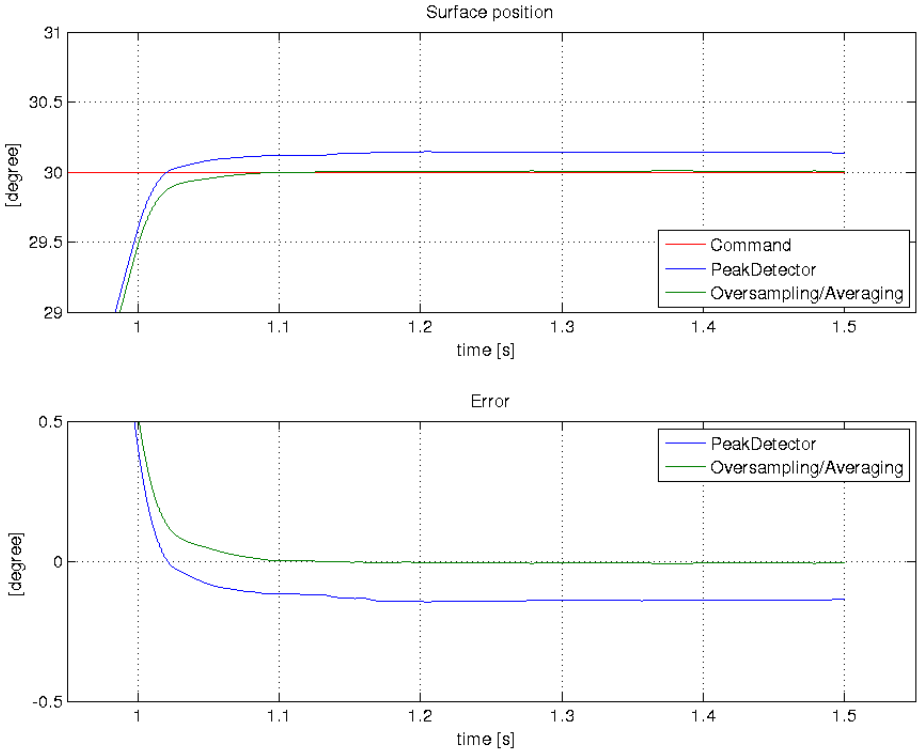

FIGURE 4.11 – Step response for both algorithms in the absence of external error (zoom)

TABLE 4.5 – Step input response

Parameter	Requirement	Peak Detector	Oversampling/Averaging
Steady state value	30°	30.14°	30.01°
Steady state error	$< 1\%$	0.456%	0.020%
Settling time (1%)	-	0.802	0.806

It is possible to see that Oversampling/Averaging has an advantage regarding the steady state error while the Peak Detector is faster. Oversampling/Averaging uses all sampled points within a valid range (i.e, complete half-waves between known zero-crossings) to extract a measure of magnitude from the signal. This works as a filter, producing a smoother measure and ratio at the cost of a small delay being introduced. The Peak Detector in the other hand looks only to the maximum values of the half-waves, responding faster but being more susceptible to noise.

4.4.2 Effect of number of sampled points per cycle

The main goal of this section is to characterize the influence the number of sampled points on each half wave in the step response of the system. Effectively, changing the

number of the points is equivalent to sample at a lower frequency. To verify this effects, a point will be taken every given number of points N before processing, as described by table 4.6 (column "Rule" specifies this quantity as $1/N$). The effect of the reduced number of points on the shape of the signal is shown on figure 4.12.

TABLE 4.6 – Number of used points

Rule	Number of points	Effective sampling frequency	Additional bits (w)
1/1	166	1000 $kSPS$ (default)	2.03
1/2	83	500 $kSPS$	1.53
1/4	41	250 $kSPS$	1.03
1/8	20	125 $kSPS$	0.53

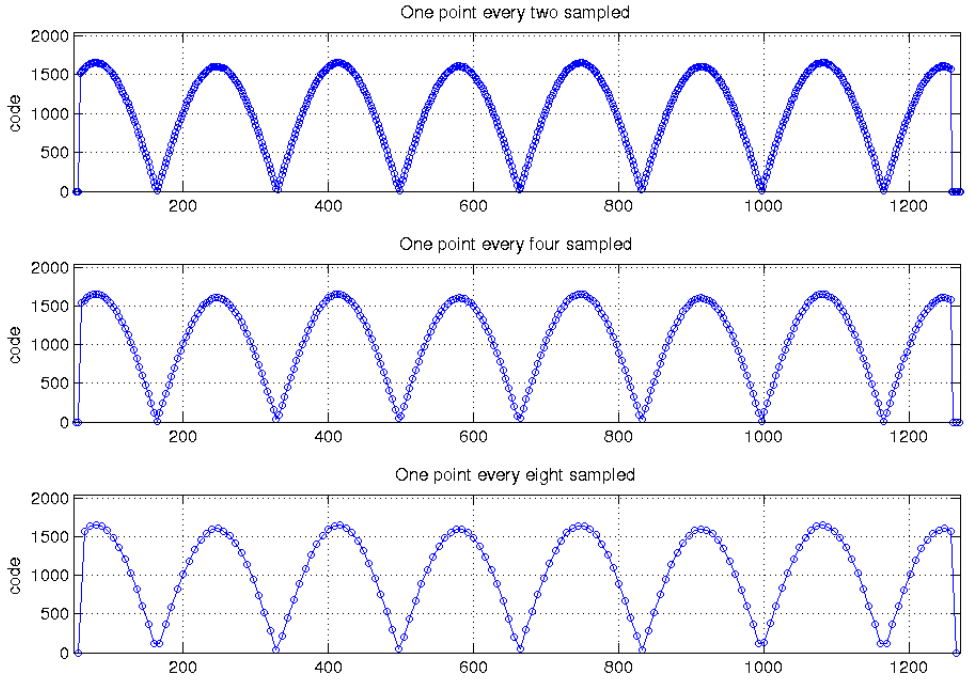

FIGURE 4.12 – Effect of reduced number of points on the shape of the signal

In these tests, a small quantity of white noise, about $60mV_{RMS}$ (figure 4.13), was added to the signal between the LVDT and the first filter. This was done via a controlled current source in series with a resistor connected on each channel, as shown on figure 4.14. The gain and offset errors are set to the worst case, 2 LSB and 0.8 LSB respectively. The results are shown on figures 4.15 to 4.22 and are summarized on tables 4.7 to 4.8 and figures 4.23 and 4.24.

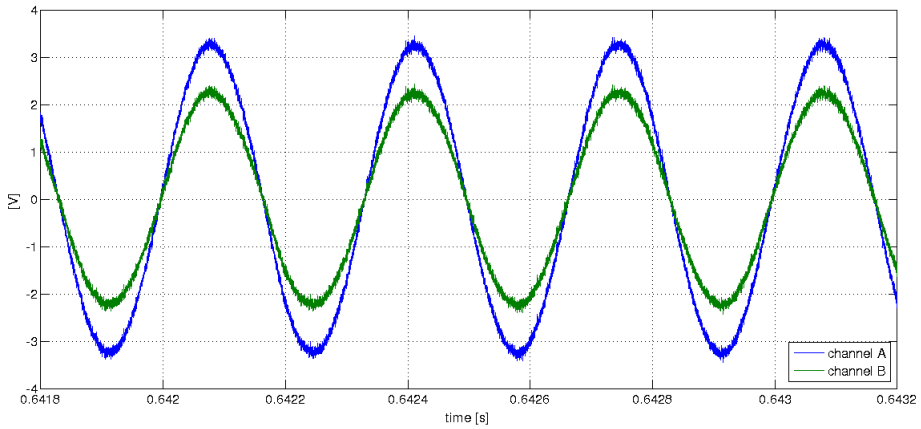

FIGURE 4.13 – Noise on signal from channels A and B

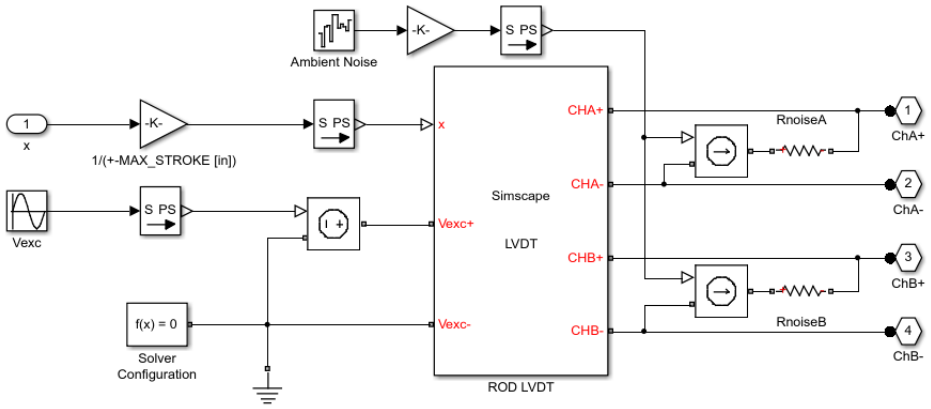

FIGURE 4.14 – LVDT model with noise injection circuit on the output of each channel

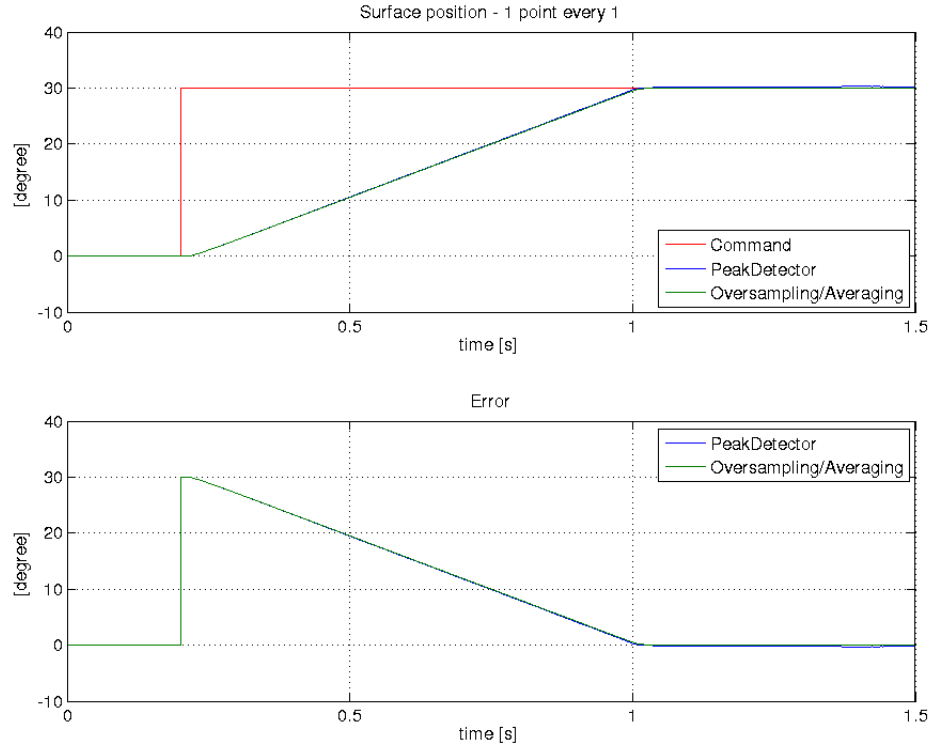

FIGURE 4.15 – Step response for both algorithms using all samples

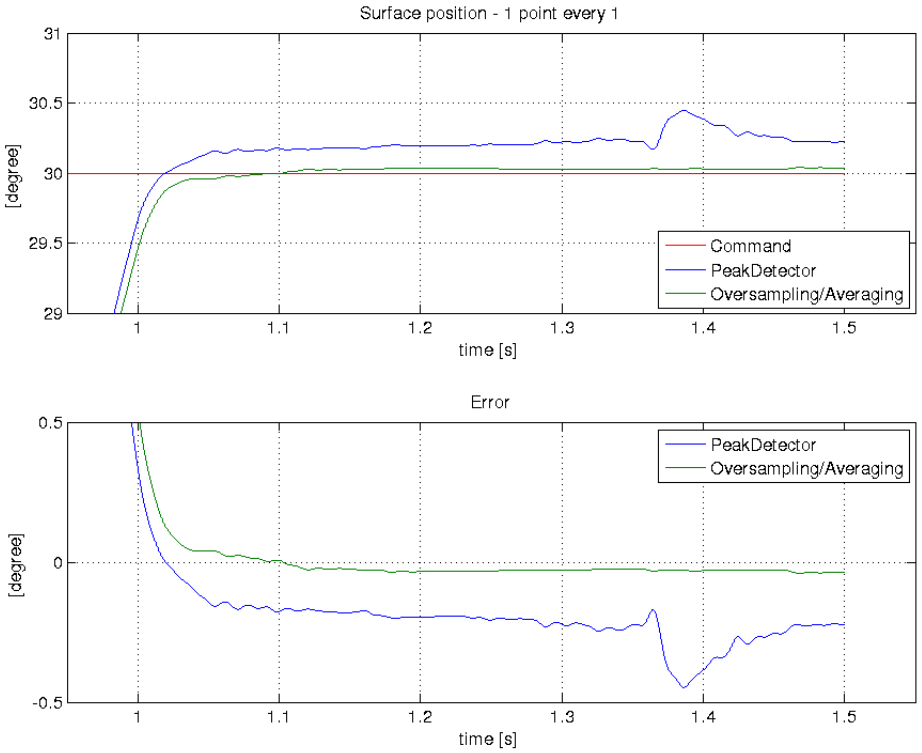

FIGURE 4.16 – Step response for both algorithms using all samples (zoom)

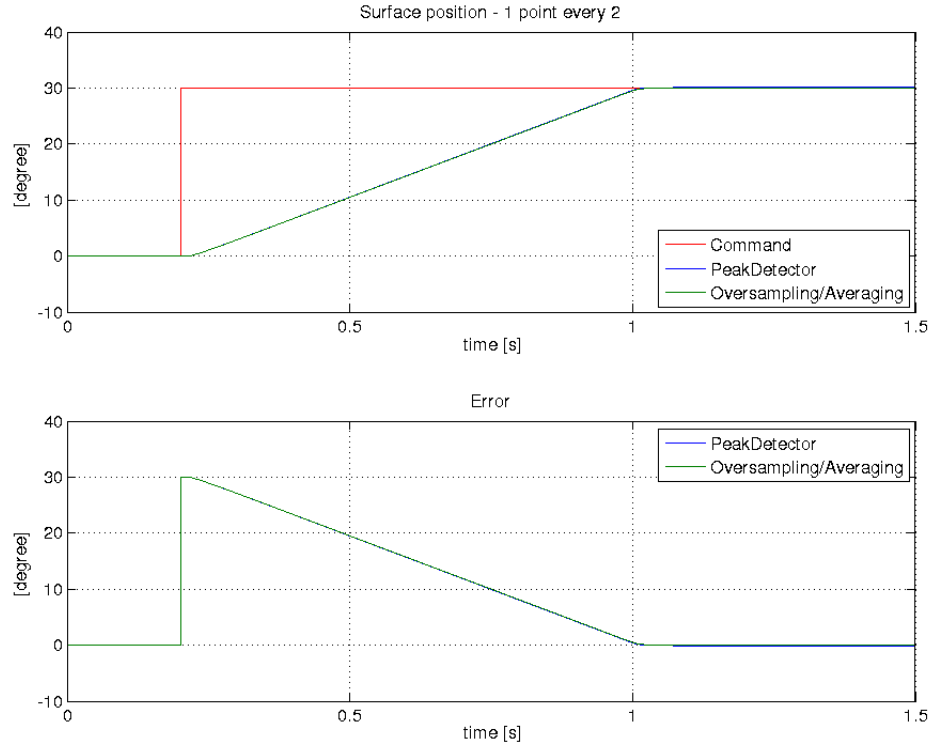

FIGURE 4.17 – Step response for both algorithms using 1 sample every 2

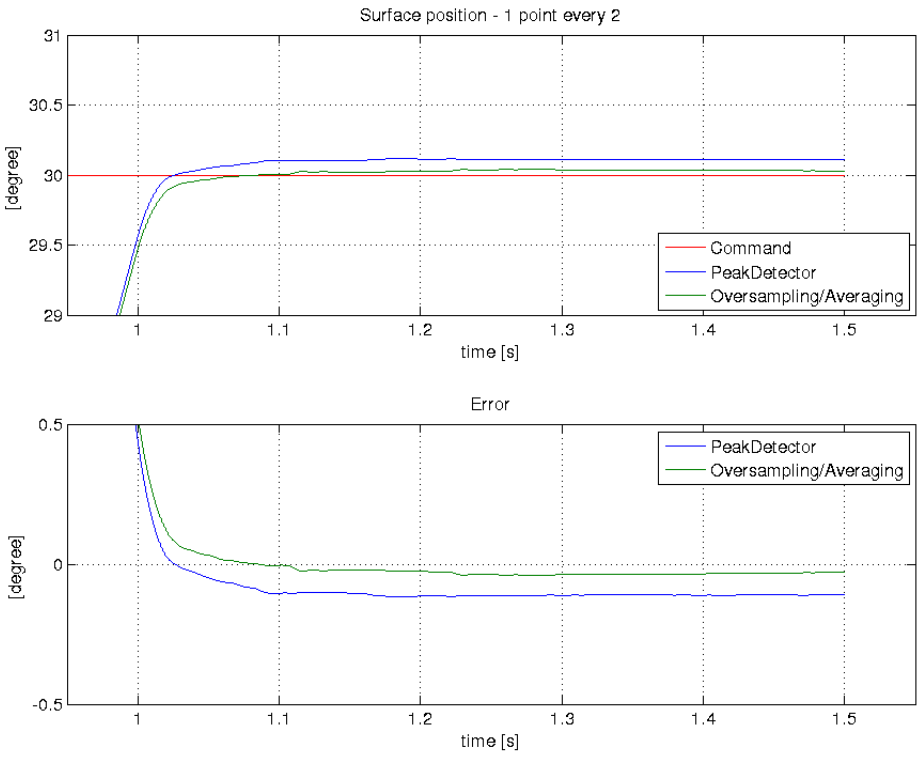

FIGURE 4.18 – Step response for both algorithms using 1 sample every 2 (zoom)

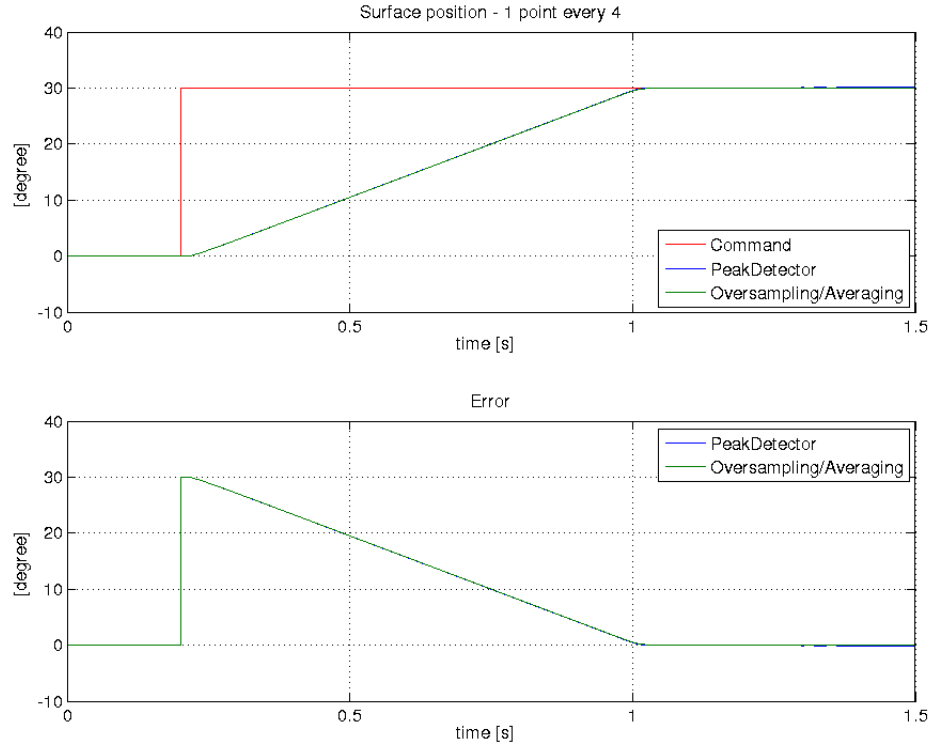

FIGURE 4.19 – Step response for both algorithms using 1 sample every 4

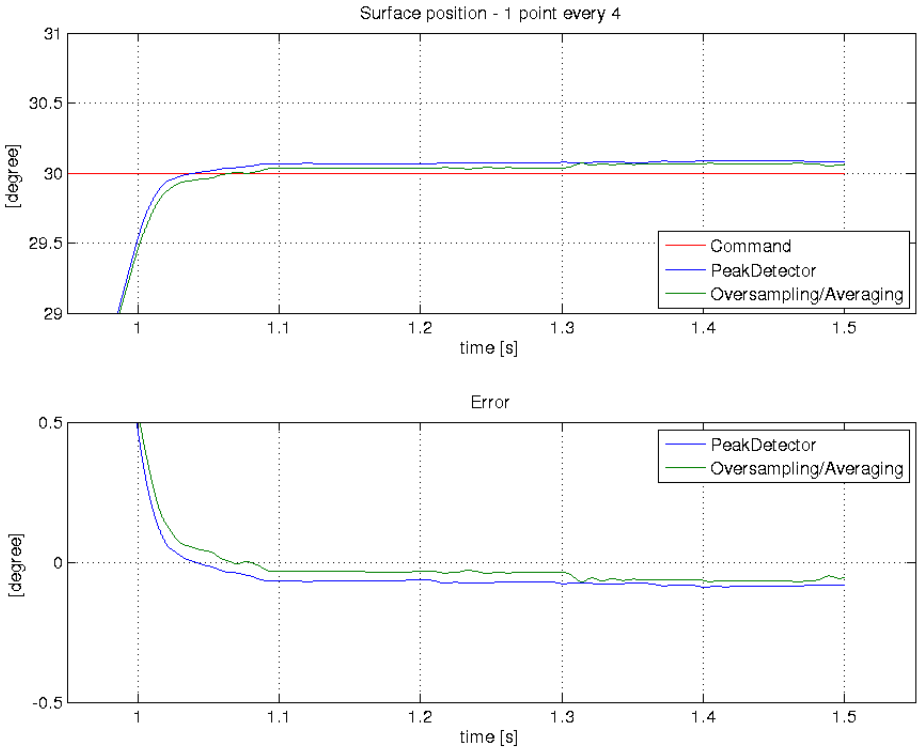

FIGURE 4.20 – Step response for both algorithms using 1 sample every 4 (zoom)

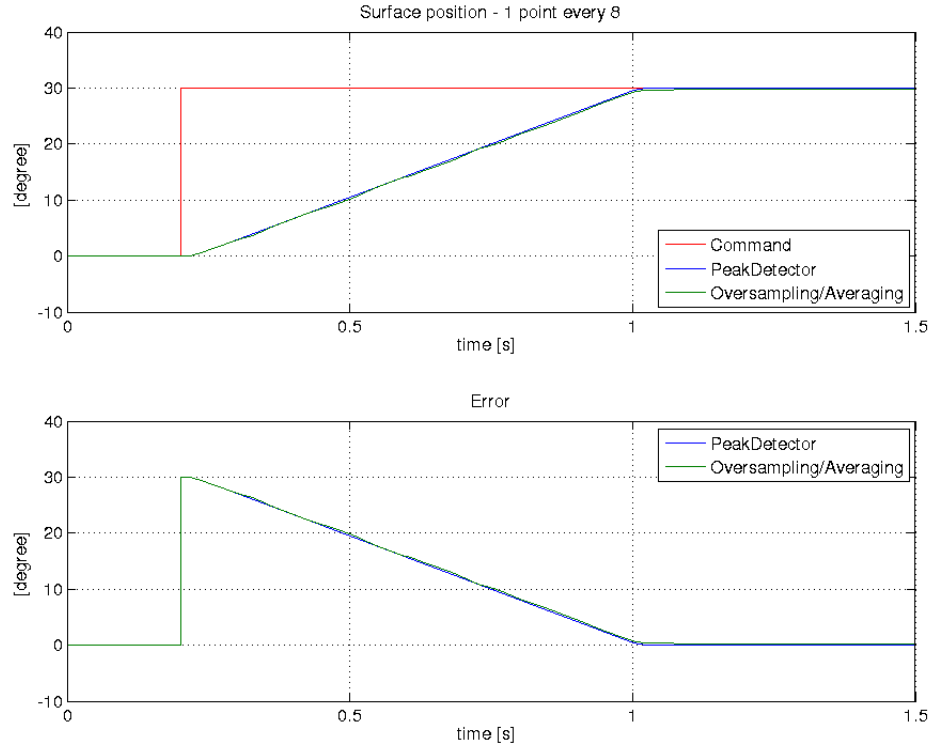

FIGURE 4.21 – Step response for both algorithms using 1 sample every 8

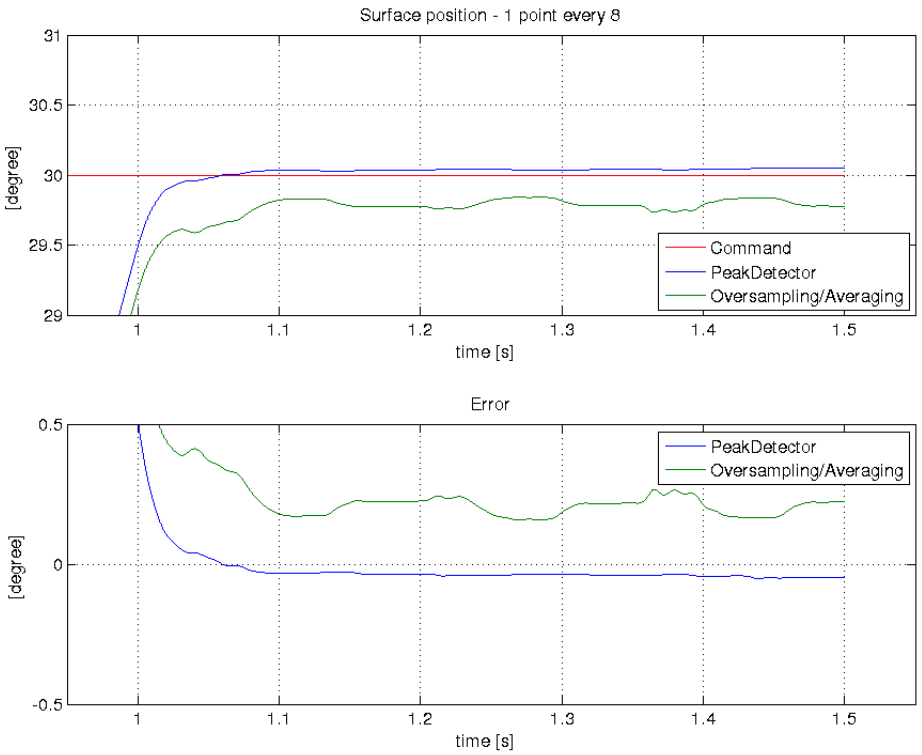

FIGURE 4.22 – Step response for both algorithms using 1 sample every 8

The settling time on tables 4.7 and 4.8 refers to the amount of time since the moment the step command is applied ($0.202s$) to when the response has settled, i.e. when the absolute error $|y(t) - y_{final}|$ becomes smaller than 1% of its peak value. This parameter was extracted using the command "stepinfo" in MATLAB.

TABLE 4.7 – Step input response - Peak Detector

Parameter	Requirement	Number of samples per half-cycle			
		166	83	41	20
Steady state value	30°	30.22°	30.11°	30.08°	30.05°
Steady state error	$< 1\%$	0.745%	0.365%	0.274%	0.156%
Settling time (1%)	-	$1.218s$	$0.802s$	$0.804s$	$0.805s$

TABLE 4.8 – Step input response - Oversampling/Averaging

Parameter	Requirement	Number of samples per half-cycle			
		166	83	41	20
Steady state value	30°	30.04°	30.03°	30.06°	29.78°
Steady state error	$< 1\%$	0.123%	0.096%	0.184%	−0.739%
Settling time (1%)	-	$0.807s$	$0.806s$	$0.808s$	$0.873s$

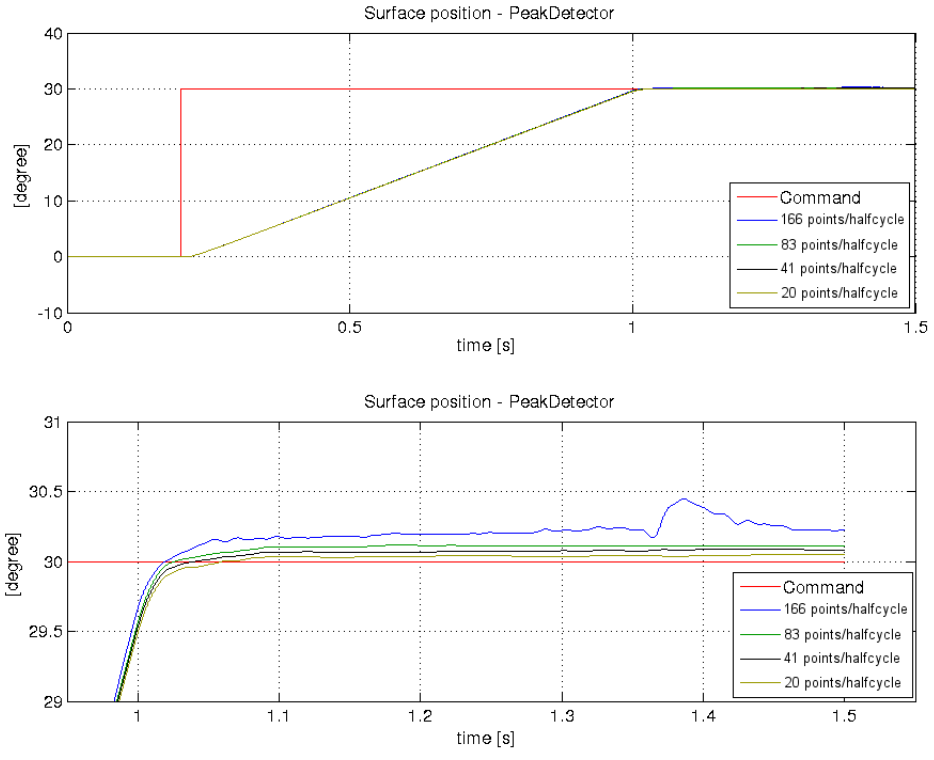

FIGURE 4.23 – Effect of the number of samples on the Peak Detector algorithm

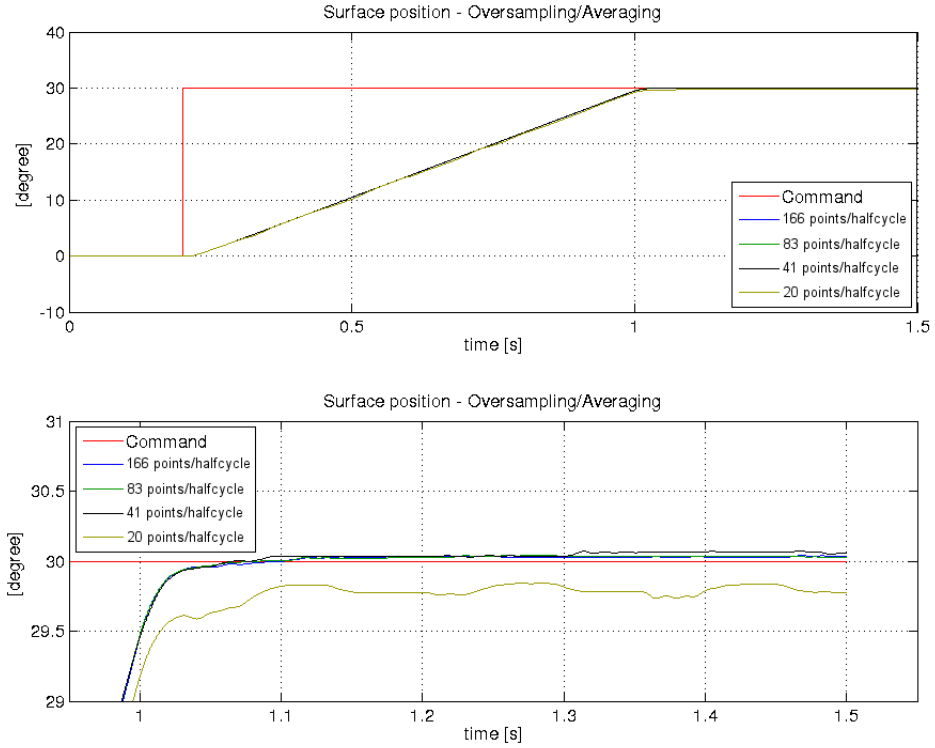

FIGURE 4.24 – Effect of the number of samples on the Oversampling/Averaging algorithm

The Peak Detector performed better than Oversampling/Averaging when the number of samples is reduced. In a low noise scenario such as this test, the decimation effectively smoothed the signal (figure 4.25) giving an advantage to the Peak Detector - despite the reduced number of points, from figure 4.12 it is possible to see that the point concentration near the peak is still sufficient to represent the amplitude of the signal. When the noise level is increased, Oversampling/Averaging performance stays approximately the same while Peak Detector performance severely degrades (figure 4.26 and table 4.9). Figure 4.28 summarizes the effect of number of sampled points per cycle on steady state error.

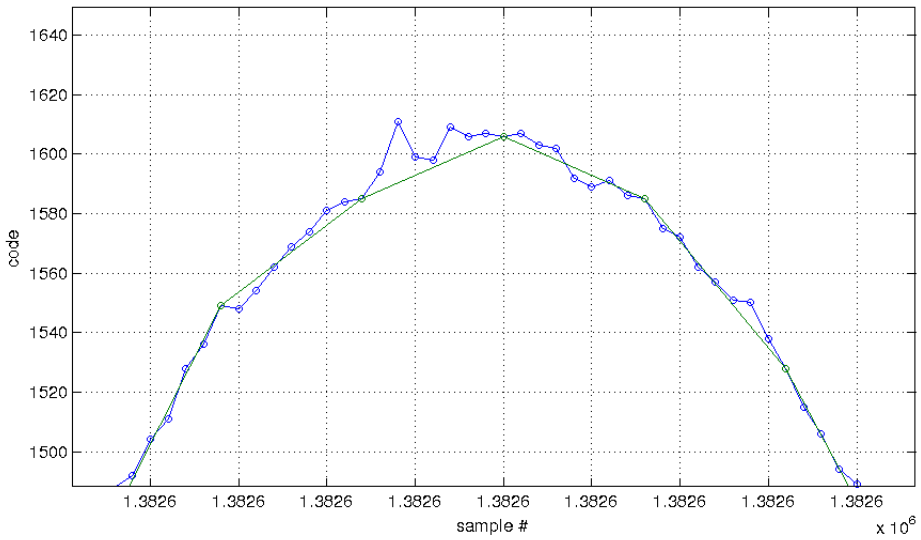

FIGURE 4.25 – Smoothed signal

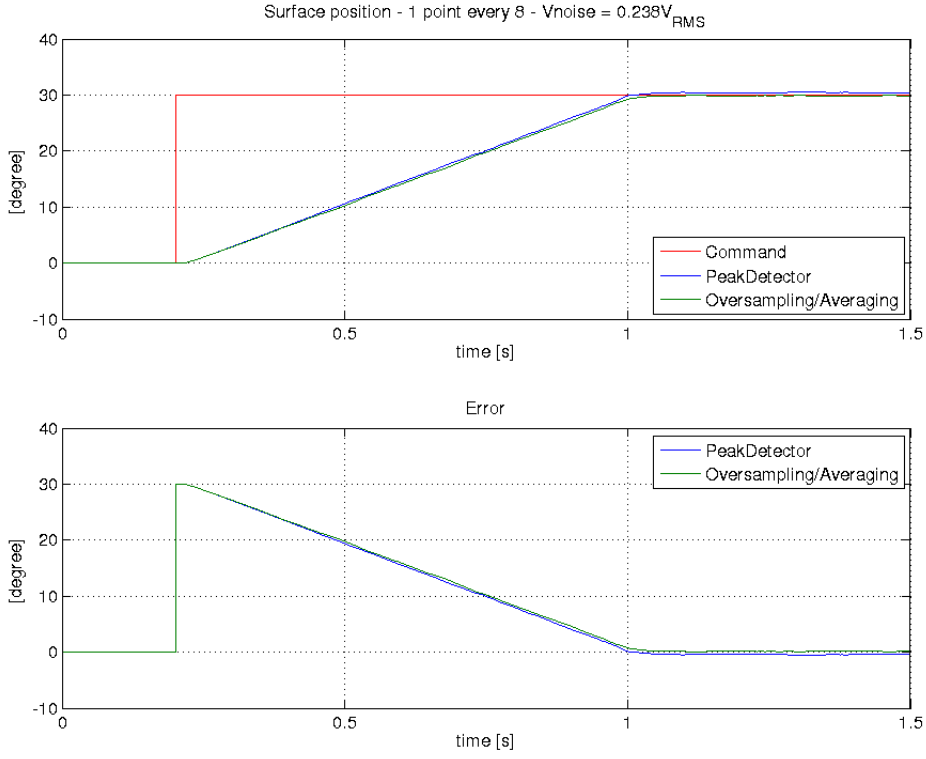

FIGURE 4.26 – Step response for both algorithms using 1 sample every 8 with increased noise level

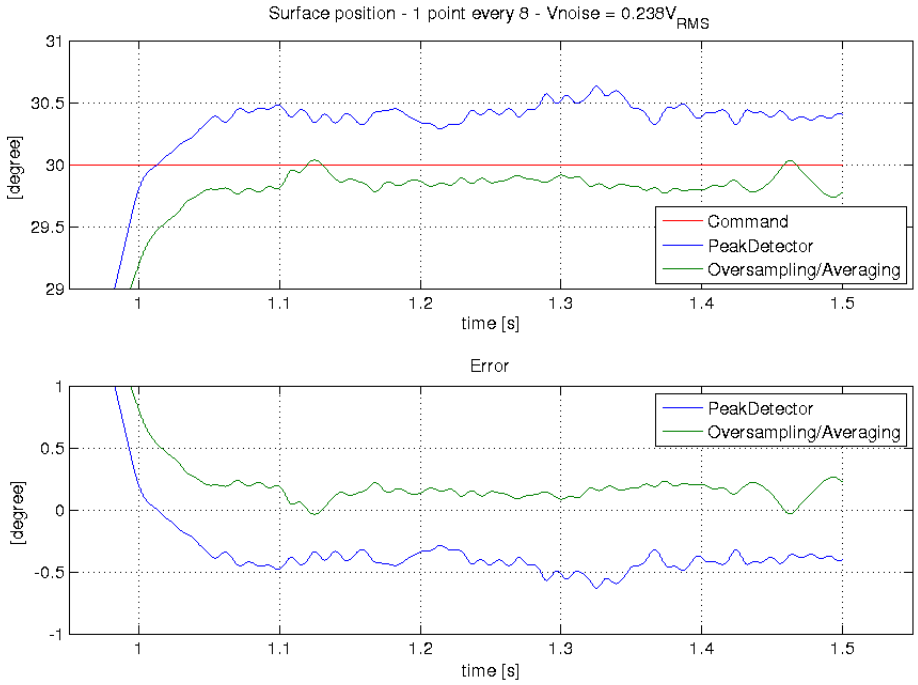

FIGURE 4.27 – Step response for both algorithms using 1 sample every 8 with increased noise level (zoom)

TABLE 4.9 – Step input response for both algorithms - 1 sample every 8 - $V_{noise} = 0.238V_{RMS}$

Parameter	Requirement	Peak Detector	Oversampling/Averaging
Steady state value	30°	30.40°	29.78°
Steady state error	$< 1\%$	1.349%	-0.748%
Settling time (1%)	-	$0.832s$	N/A

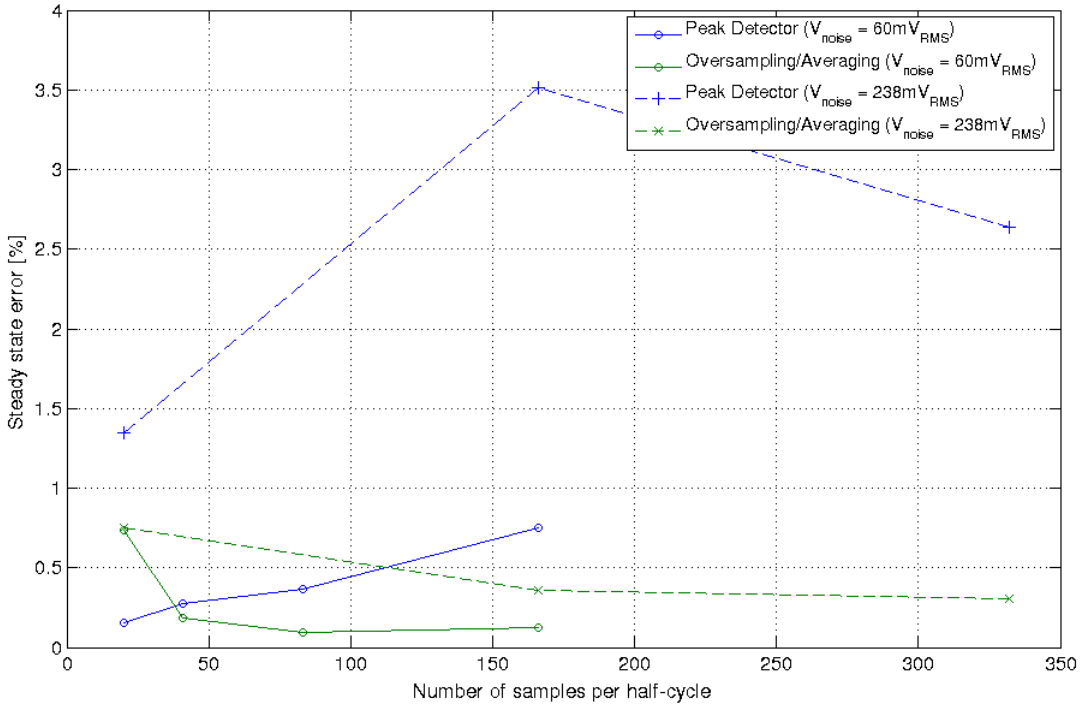

FIGURE 4.28 – Effect of number of sampled points per cycle on steady state error

4.4.3 Tolerance to noise on input

The following tests are intended to verify the tolerance of both algorithms to a noisy input. The same white noise signal is injected into both channels through independent current sources on each channel. The results are shown in figures 4.29 to 4.36 and are summarized on tables 4.10 and 4.11.

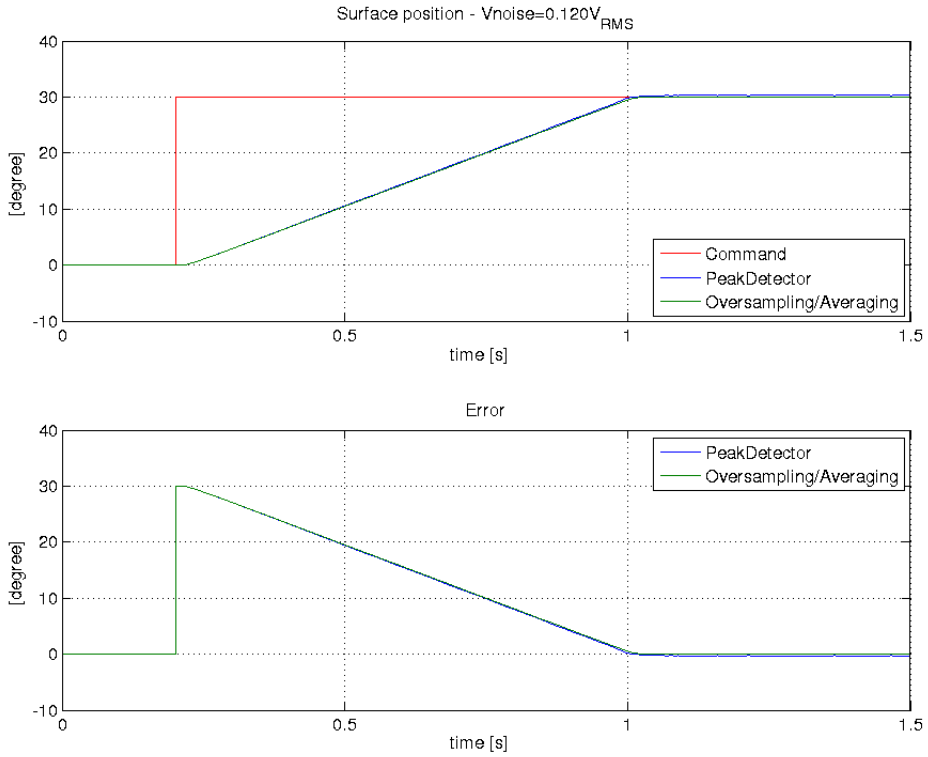

FIGURE 4.29 – Step response for both algorithms with $V_{noise} = 120mV_{RMS}$

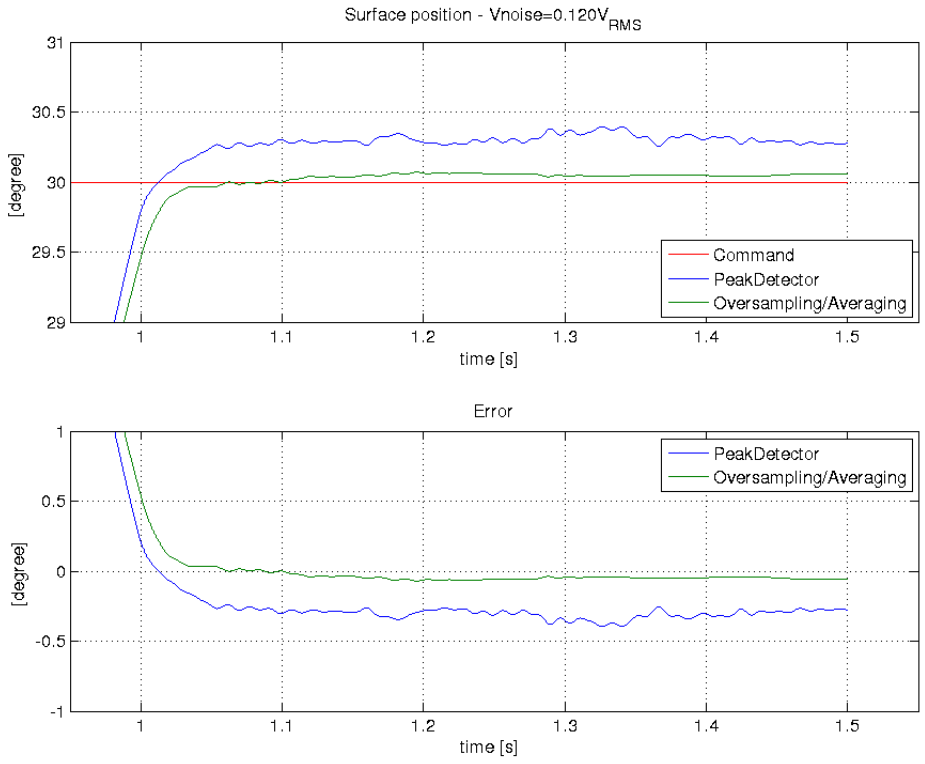

FIGURE 4.30 – Step response for both algorithms with $V_{noise} = 120mV_{RMS}$ (zoom)

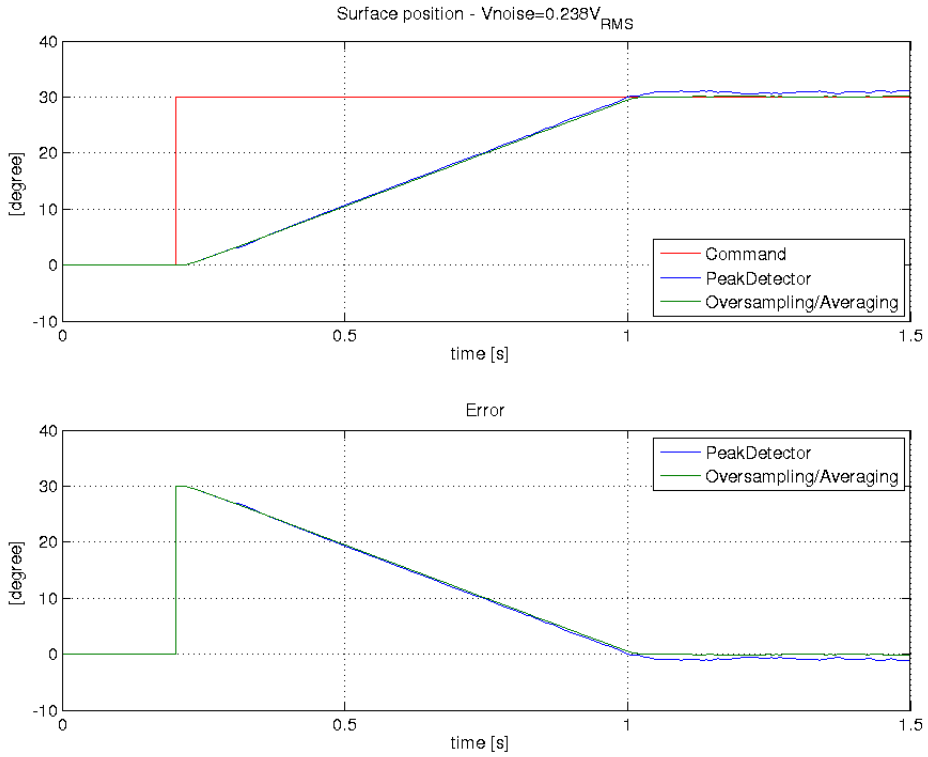

FIGURE 4.31 – Step response for both algorithms with $V_{noise} = 238mV_{RMS}$

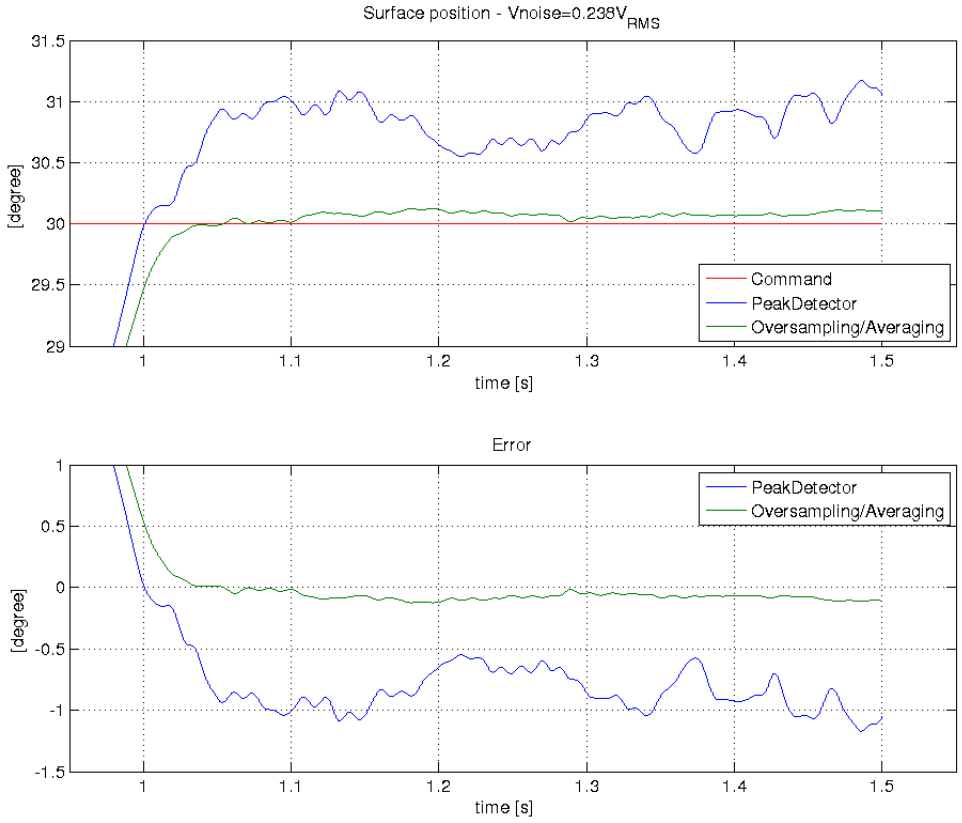

FIGURE 4.32 – Step response for both algorithms with $V_{noise} = 238mV_{RMS}$ (zoom)

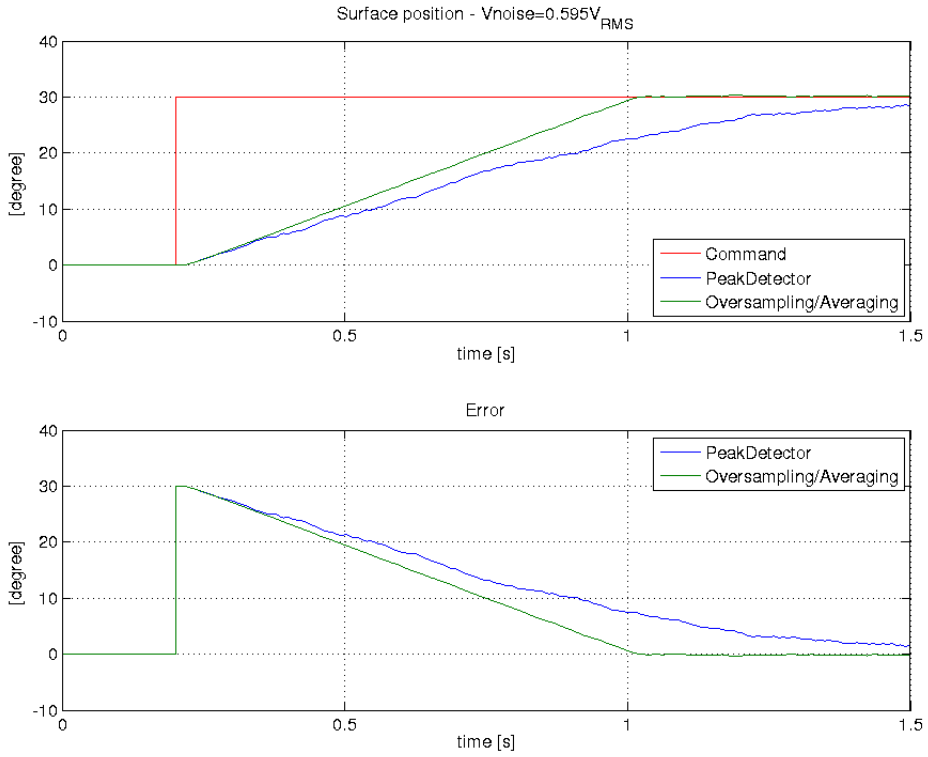

FIGURE 4.33 – Step response for both algorithms with $V_{noise} = 595mV_{RMS}$

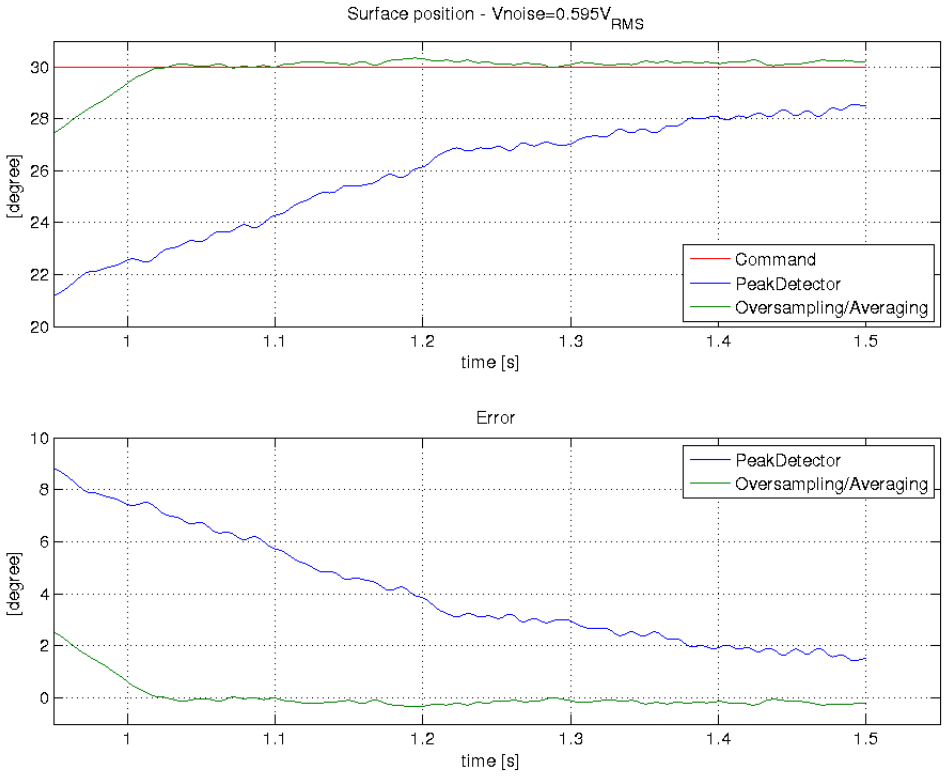

FIGURE 4.34 – Step response for both algorithms with $V_{noise} = 595mV_{RMS}$ (zoom)

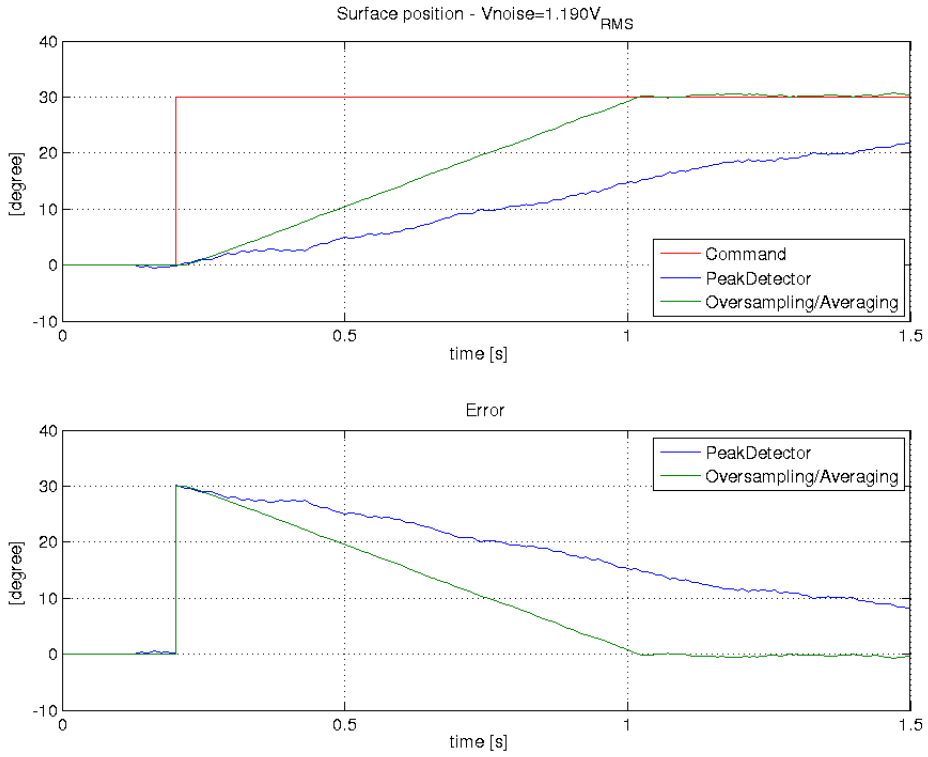

FIGURE 4.35 – Step response for both algorithms with $V_{noise} = 1.120V_{RMS}$

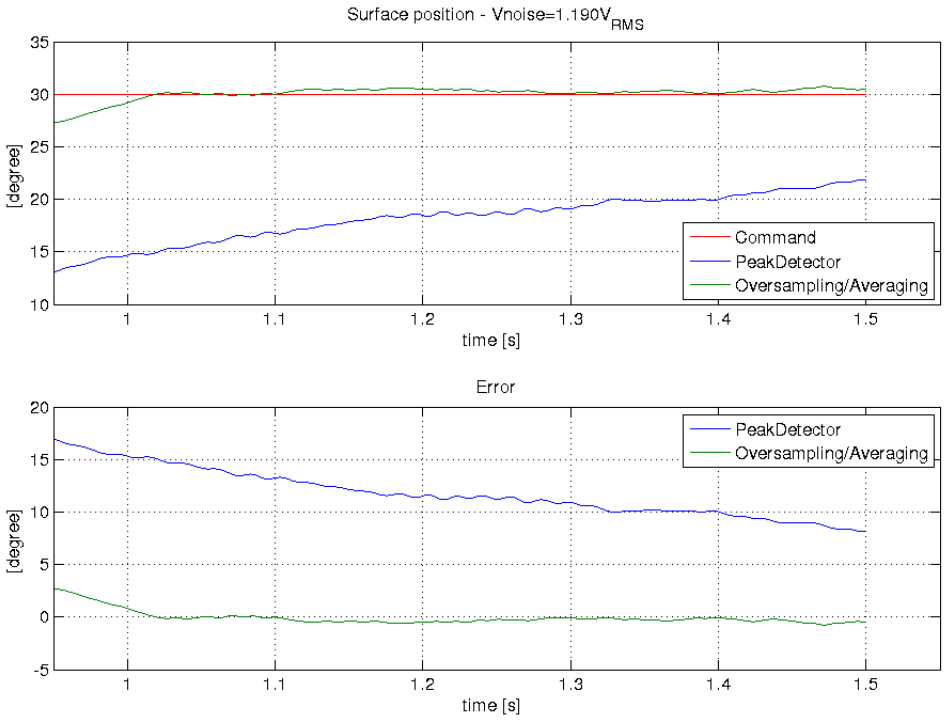

FIGURE 4.36 – Step response for both algorithms with $V_{noise} = 1.120V_{RMS}$ (zoom)

The settling time on tables 4.10 and 4.11 refers to the amount of time since the

moment the step command is applied ($0.202s$) to when the response has settled, i.e. when the absolute error $|y(t)-y_{final}|$ becomes smaller than 1% of its peak value. This parameter was extracted using the command "stepinfo" in MATLAB.

TABLE 4.10 – Step input response - Peak Detector

Parameter	Requirement	V_{noise}			
		$120mV_{RMS}$	$238mV_{RMS}$	$595mV_{RMS}$	$1.120V_{RMS}$
Steady state value	30°	30.28°	31.05°	28.50°	21.83°
Steady state error	$< 1\%$	0.924%	3.514%	-5.018%	-27.238%
Settling time (1%)	-	$1.233s$	–	–	–

TABLE 4.11 – Step input response - Oversampling/Averaging

Parameter	Requirement	V_{noise}			
		$120mV_{RMS}$	$238mV_{RMS}$	$595mV_{RMS}$	$1.120V_{RMS}$
Steady state value	30°	30.06°	30.11°	30.22°	30.46°
Steady state error	$< 1\%$	0.188%	0.357%	0.736%	1.547%
Settling time (1%)	-	$0.806s$	$0.807s$	$1.001s$	–

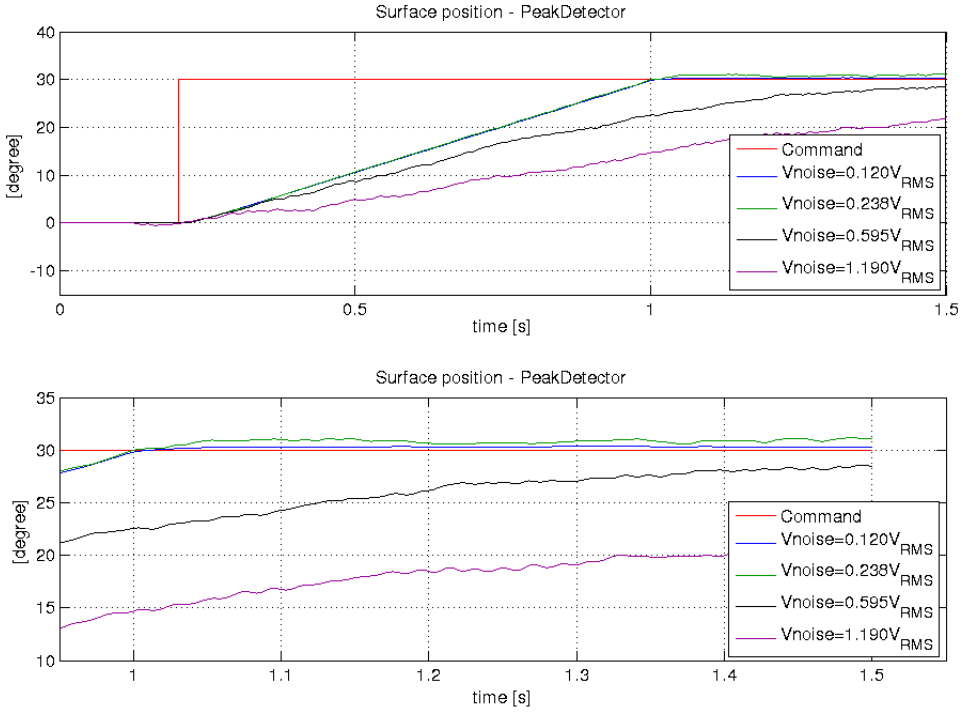

FIGURE 4.37 – Effect of input noise on the Peak Detector algorithm

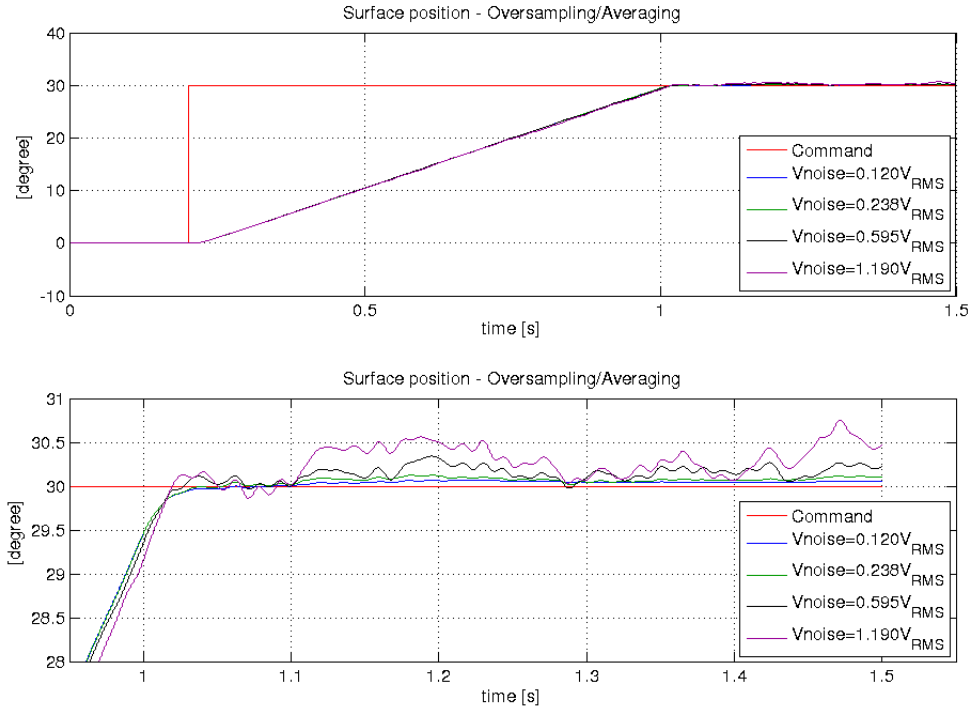

FIGURE 4.38 – Effect of input noise on the Oversampling/Averaging algorithm

For $V_{noise} = 238mV_{RMS}$, the Peak Detector steady state error exceeds 1° in some moments, already making it unsuitable for controling the surface position. At $V_{noise} = 595mV_{RMS}$ and above the response from Peak Detector is completely degraded. The Oversampling/Averaging algorithm can still retrieve the position but an error is added by taking the absolute value of the noise, which accumulates and may become significative for a large number of points. Figure 4.39 summarizes the effect of electrical noise on steady state error.

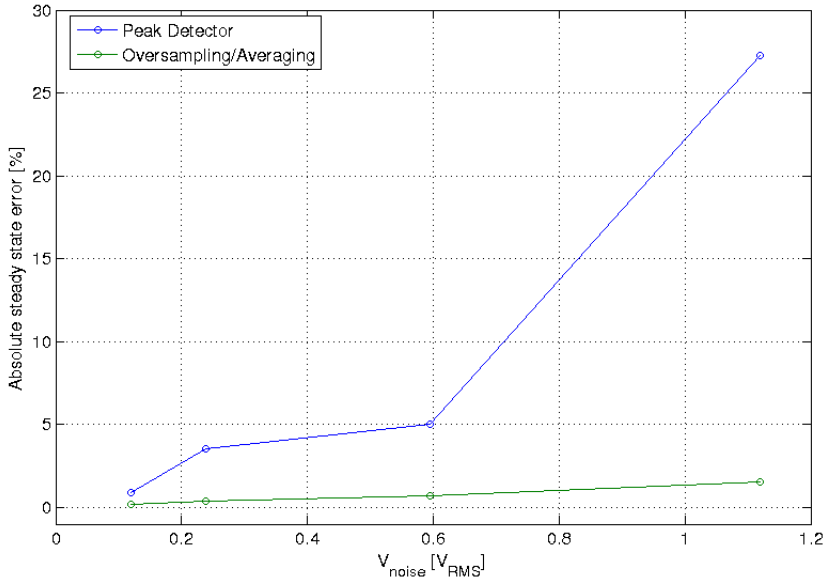

FIGURE 4.39 – Effect of electrical noise on steady state error

5 Conclusion

The position acquisition system was modelled taking into account the dynamics and relevant non-linearities of each part: the linear variable differential transformer, the signal conditioning circuitry, the analog-to-digital converter and the demodulation algorithms. The model was successfully integrated to the electro-hydraulic actuator model developed by (BALLESTEROS, 2015) and was possible to close the control loop with the position provided by both demodulation strategies, the Peak Detector and Oversampling and Averaging.

The constructed model is easily adaptable to other types of LVDTs by adjusting the electrical parameters such as impedance on the coils and coupling factor or extending the Simscape model equations. The signal conditioning was designed using commercially available component values and can be reconfigured through mask parameters. The analog-to-digital converter allows the variation of static and diverse dynamic performance parameters from data presented on component datasheet through a set of scripts. The digital demodulator block is highly versatile, supporting the coexistence of multiple algorithms and a scheme to select the correct output.

In order to evaluate the performance of the demodulation algorithms regarding steady state error, an experiment was set up minimizing the external error sources (no noise on LVDT, null gain and offset errors on ADC) and was observed that the Peak Detector responded faster, reaching the setpoint first but also presented a steady state error larger than the Oversampling/Averaging.

Another study was performed, varying the number of samples fed to the algorithms. In this study, a low noise environment caused the Peak Detector performance to improve when the number of points was reduced, since this was effectively smoothing the signal. The performance of Oversampling/Averaging degraded with reduction of the number of points reaching a steady state error greater than Peak Detector when using only 1/8 of points. Once the noise was increased Oversampling/Averaging outperformed the Peak Detector, suggesting a higher susceptibility to noise on the latter.

Finally, the tolerance to electrical noise was analysed by injecting different noise levels between the LVDT and the input filter. The results confirmed that Oversam-

pling/Averaging is more robust, being capable of resolving the rod position even with noise levels as high as $0.6V_{RMS}$ without violating the steady state error requirement of 1% of full scale. At noise levels as low as $0.120V_{RMS}$ the Peak Detector produced a steady state error of 0.924%, almost reaching the limit above mentioned.

In conclusion, for Oversampling/Averaging, is not advantageous to use more than 150 sample points per half-cycle with a $3kHz$ carrier. The Peak Detector can be utilized in applications where positioning tolerance is more flexible or for monitoring purposes. Concerning performance, the Peak Detector is advantageous to save computational resources. The Peak Detector can also be utilized to mitigate design errors by means of a dissimilar implementation in high integrity systems, preventing implementation errors to cause harmful behaviour in the system.

5.1 Future Works

In this section, some future work suggestions are presented, aiming to expand the capabilities of the current simulation model.

The first suggestion arises from the nature of the algorithms presented in this work - performing a comparison between digital and analog demodulators based on half-wave and full-wave rectifiers. In addition, analyse the performance of the demodulators separately, in an open loop scenario.

An approach to increase the robustness of the model is to include a digital filter on the output of the demodulator to cut off frequencies above half the control law update rate, preventing aliasing inside the control law. This would certainly improve the quality of the response but would also introduce another source of delay and would be interesting to perform an analysis of the effects.

In Appendix A, it was demonstrated the adverse effect of a short-to-ground failure on the demodulation algorithm, which may lead to catastrophic results if it goes unnoticed. One possible improvement is implementing monitors on the channels to detect electrical failures such as short-to-ground and open wiring, making safety analysis possible. The circuits models should be modified to allow detection, mitigation and passivation of these events.

On the subject of safety analysis, it would be interesting to implement the full transient filter and perform the pin injection tests on the model to verify how it would affect the demodulated value in the presence of a system monitor to detect and mitigate any spurious commands from this scenario.

The components on the circuits were selected from commercially available values and

exact ones were used. Real components present variations in a given tolerance range caused by manufacturing processes, temperature variations, ageing, among others factors. It would be interesting to characterize the operational amplifiers and passive components according to their tolerances to enable a full stack up analysis of error introduced by these elements and their effect on the actuator steady state error.

It also would be interesting to extract the electrical parameteres from a real LVDT and compare the model output with of the real sensor.

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Appendix A - General Topics

A.1 Effects of electrical failure on demodulation

During the implementation and validation of the demodulation algorithms it was observed a scenario where the zero crossings were incorrectly detected producing an invalid value for a channel. This led to a questioning about real scenarios where electrical failures that may lead to loss of signal on one or both channels.

In figure A.1 it is demonstrated the ill effects of a failure where one LVDT channel is shorted to ground, delimited by red line at $0.75s$. The algorithm used was Oversampling/Averaging - without the signal, after the retification the computed mean for the channel is slightly above zero, causing the ratio (equation A.1) to become approximately -1.0, greater in modulus than the maximum expected ratio of 0.5. The computed position is then saturated at the minimum value for the piston displacement and the surface is commanded until reaching the mechanical stop.

$$r = \frac{V_a - V_b}{V_a + V_b} \tag{A.1}$$

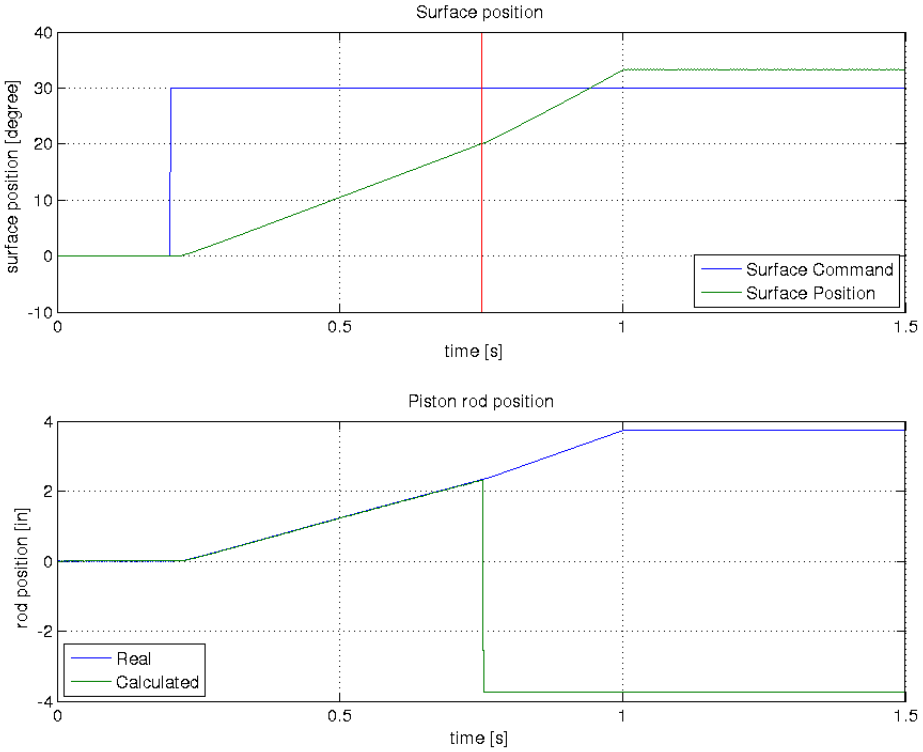

FIGURE A.1 – Surface hardover due to short-to-ground failure

To implement proper monitoring of such events the signal conditioning circuits must be modified to prevent voltage floating in case of a open wiring failure and an algorithm to detect abnormal signal conditions must be included on the digital demodulator. The algorithm must take into account multiple variables when deciding the course of action during these events such as presence of redundand systems, phase of flight, among others. The design of such system is out of scope of this work but is suggested as future work.

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11. RESUMO:

The implementation of digital Control Systems can bring several advantages to aircraft manufacturers including improvement in reliability, since parts of analog circuitry would be replaced by software, reduced costs by hardware reusing and increased tolerance to environmental conditions such as temperature and electrical noise. A model for a digital position acquisition system for aircraft primary control surfaces is presented, comprised by a Linear Variable Differential Transformer (LVDT) as displacement sensing element, a protective passive filter for transients caused by lightning strikes, an Analog-to-Digital converter and a digital demodulation system. Once integrated with the electro-hydraulic actuator model developed in (BALLESTEROS, 2015), the model serves as platform to analyse the performance of digital demodulation algorithms, the main objective of this work.
Two strategies, the Peak Detector, based on the instant amplitude of the signal and the Oversampling/Averaging, based on the mean value of the signal over a period of time were compared. Both algorithms allowed closing the control loop and correctly positioning the surface, with Peak Detector producing a slightly faster response while Oversampling/Averaging being more robust to noise and having smaller steady state error. This work performs an implementation and comparison of such digital demodulation algorithms to retrieve positioning from LVDTs applied to servo-positioning of an electro-hydraulic actuator.

12. GRAU DE SIGILO:

( ) **OSTENSIVO** (**X**) **RESERVADO** ( ) **CONFIDENCIAL** ( ) **SECRETO**